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(54) **Title:** A METHOD AND A MIRRORED SERIAL INTERFACE (MSI) FOR TRANSFERRING DATA

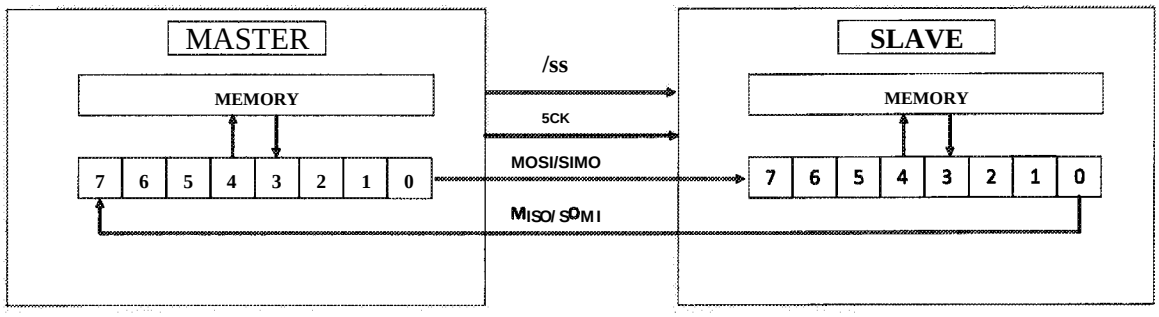

Fig. l

(57) **Abstract:** The present disclosure relates to a mirrored serial interface (MSI) for accessing peripherals through four wire serial interface. More particularly, the present disclosure is related to serial peripheral protocol with looped back mechanism in which contents of source data line are looped back onto the destination line and compared at every clock edge to ensure data sanity and to assert presence of slave and master device during and between cycles.

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A METHOD AND A MIRRORED SERIAL INTERFACE (MSI) FOR TRANSFERRING DATA

FIELD OF THE INVENTION

The present disclosure relates to a method and a mirrored serial interface (MSI) for transferring data with loopback mechanism through four wire serial interface. More particularly, the present disclosure is related to mirrored serial interface (MSI) with loopback mechanism in which contents of source data line is looped back onto the destination line and compared at every clock edge to ensure data sanity and to assert presence of slave and master device during and between cycles.

BACKGROUND OF THE INVENTION

The serial peripheral interface (SPI) protocol is related to the serial communication between a master device and a slave device. Slave device may in turn cater to its own independent peripherals.

SPI bus is a synchronous serial data link standard that operates in full duplex mode with a single master device and one or more slave devices. Its implementation uses four signal lines for data and control i.e. SCLK, MOSI, MISO and SS, wherein SCLK refers to serial clock (output from master); MOSI or SIMO refers to master output-slave input (output from master); MISO or SOMI refers to master input-slave output (output from slave) and SS refers to slave select (active low, output from master). The shift register of master and slave are connected in a ring formation as shown in figure **1.**

In a conventional SPI protocol, data frame or data transfer cycle is initiated by the master by asserting the SS line low and enabling the clock for the selected slave. The shift register of master and slave are connected in a ring formation. Hence, the master is writing the data and reading from it at the same time. This process continues until all the data bits are transferred to and from master and slave. It is for the controllers of the master and slave to decide if the data is meaningful or not.

However, the conventional SPI protocol suffers from the following disadvantages:-

- SPI does not have an acknowledgement mechanism to confirm receipt of data. Data sanity is not ensured. Slave may receive inverted bits due to timing violations, channel noise or temperature changes.
- SPI master has no knowledge of whether a slave even exists, until complete transaction is executed. Master may continue to send data without even knowing if it is being received correctly.
- SPI also offers no flow control (no handshaking signals or acknowledgement) like REQ and ACK to tell whether slave has completed transacting with any slow peripheral it is serving. There is no mechanism to tell when slave is ready to transmit data during read cycle, in case of slower access at the secondary end of slave.

US 2006/0143348 relates to a system, method, and apparatus for interchip communication between an extended serial peripheral interface (EPSI) master chip having clocking capability and an EPSI slave chip. The method comprises the master chip selecting a slave chip, the master clocking data into the slave chip from the master chip and at the same time clocking data from the slave chip into the master chip, and processing the clocked in data to negotiate further data transfer between the master chip and the slave chip. Selection of a slave chip by the master chip may also take place in response to an interrupt received by the master chip from the slave chip, with the master then clocking data in both directions to negotiate further data transfer between the master chip and the slave chip. However, this prior art document does not provide any provision for error detection and physical layer and it uses two general purpose lines for flow control.

US20020133662 related to the serial peripheral interface and high performance buffering scheme. An improved high performance buffering scheme is provided with a serial peripheral interface (SPI) to enable microcontroller-based products and other components and devices to achieve a higher serial transmit and receive data rate. The SPI comprises a single buffer having a high data rate, for example, at least the throughput of double buffer schemes, but without the increased size in logic area. To facilitate the throughput of data, the SPI single buffer can be configured with a queuing arrangement. The queuing arrangement for the SPI single buffer can comprise any queuing configuration, such as, for example, a circular queuing arrangement or a linear queuing arrangement. Through operation of the queuing arrangement, the SPI can be configured to provide for the receiving of new data in a register at substantially the same time

that stored data can be transmitted to another device, thus the SPI can realize a high data rate. The queuing arrangement is configured in a FIFO buffer having a pointer and counter arrangement. In addition the buffering scheme can provide a high data rate without requiring frequent CPU polling or high interrupt overhead wherein the buffering scheme is configured with an interrupt configuration for identifying when data is ready for transmitting or for reading by the CPU. However, this prior art document does not provide any provision for error detection and aims to increase data rate over the serial link.

US6529979 relates to method and apparatus for a high-speed serial communications bus protocol with positive acknowledgement. There is two-wire serial bus consisting of an address line and a data line that connects a plurality of satellites in a daisy-chain fashion to a central source where address packet is modified by clearing the stop bit of the address packet to provide a positive acknowledgment of a receipt of the address packet back to the central source of the transaction. However, this prior art document does not ensure data sanity and does not provide provision for data flow control and physical layer.

US5260933 provides acknowledgement protocol for serial data network with out-of-order delivery. The data frames transmitted by the initiator node to the recipient node include frame serial number or sequence count information; Acknowledgment frames, transmitted by the recipient node to indicate delivery of the data frame or packet, include matching serial number or sequence count information; acknowledgement is received for each data frame transmission. However, this prior art document does not ensure data sanity and does not provide provision for error detection and it uses two general purpose lines for flow control.

OBJECT OF THE INVENTION

An object of the present disclosure is to ensure data sanity implementing a loop back mechanism i.e. data latched by the slave flip flop at the MISO line is looped back to the master at every clock edge for detecting instantaneous communication errors.

Another object of the present disclosure is to ascertain the presence / absence of slave and master by a looped back mechanism on the MISO and MOSI lines even in the absence of any accessing cycles.

Another object of the present disclosure is to provide flow control support to cater slow peripherals.

Yet another object of the present disclosure is to confirm the receipt of data by the destination to the source using acknowledgement mechanism.

SUMMARY OF THE INVENTION

An aspect of the present disclosure is to provide a method of transmitting data via a mirrored serial interface, the method comprising:

a master device receiving address, data and read/write command from a master host, loading address and read/write first in master shift register, shifting it to a slave device via MOSI line, simultaneously receiving mirrored address bits via MISO line to check for data sanity;

the slave device after successful transmission of address information fetching data from a slave host;

if the read instruction received, the slave device sending data to the master device via MISO line, simultaneously receiving mirrored data bits via MOSI line to check for data sanity;

if the write instruction received, the slave receiving the data from the master device and sharing it with the slave host for further processing, the master device again checking the mirrored data bits via the MISO line;

the master device and the slave device switching between data from shift register and acknowledgement from a slave controller or a master controller via multiplexers, and

the presence and absence of the master device or the slave device being detected through internal pull ups when transaction not being in progress.

An embodiment of the present disclosure provides loopback mechanism on the MISO and MOSI lines determines presence or absence of the master device and slave device in absence of a slave select signal.

An embodiment of the present disclosure provides the method steps for checking the data sanity comprise:-

looping back the content of source data line onto destination data line; and

comparing the content at every clock edge by a source device controller.

Another embodiment of the present disclosure provides that either of the master device or the slave device is a source depending on whether it is a read or a write transaction.

Another embodiment of the present disclosure provides that the source device sends a flag to destination after transferring every burst of data bits indicating data sanity for each transfer.

Still another embodiment of the present disclosure provides transfer of a burst of data bits includes an address transfer phase and a data transfer phase.

Still another embodiment of the present disclosure provides the address bits flow from master device to slave device and data bits flow in either direction.

Another embodiment of the present disclosure provides the slave device generates an acknowledgement signal to indicate its readiness for the next cycle.

Another embodiment of the present disclosure provides that flag and acknowledgement is a single bit in band signals asserted on the MOSI and MISO lines and is either high or low.

Still another embodiment of the present disclosure provides that the method is implemented by using four signal lines including MOSI, MISO, SCLK, SS for data and control.

Another embodiment of the present disclosure provides that in absence of slave select signal a) the master drives logic 0 on MOSI line, b) the slave, in loopback mode, loops back the contents of MOSI line to MISO line at every clock edge; and c) controller of master samples the contents of MISO at every clock edge, if the master senses logic 1 on its MISO line input, it indicates absence of slave device.

Another embodiment of the present disclosure provides that slave drives logic 0 on the MOSI line indicating valid data transfer and logic 1 for one clock indicating invalid data transfer.

Another aspect of the present disclosure provides a mirrored Serial interface comprising

a master device and at least one slave device;

the master device and each of the at least one slave device connected to one another with four signal lines, a serial clock line (SCLK), a master-in-slave-out (MISO) line and a master-out-slave-in (MOSI) line, and a slave select (SS) line for selecting a slave device in a multi-slave configuration;

the master device configured for transmitting data to and receiving data from at least on slave peripheral device, said master peripheral interface device comprising a serial clock generator to generate clock for synchronizing data movement in and out of the device through MOSI and MISO lines, a shift register comprising a group of flip-flops for shifting data into internal storage elements and shifting data out at the serial-out, a memory element and a controller for controlling function of the master device; and

the at least one slave device comprising a shift register comprising a group of flip- flops for shifting data into internal storage elements and shifting data out at the serial-out, a memory element, and a controller for controlling function of the slave device, Characterized in that

the master device and the at least one slave device have multiplexers to switch between data from shift register and acknowledgement from any of the controller,

the master device has an internal pull up at the MISO line and each of the at least one slave device has an internal pull up at the MOSI line to detect presence and absence of master device or slave device when transaction is not in progress, and

the data latched by the slave flip-flop at the MISO line is configured to be looped back to the master at every clock edge for reporting communication errors.

These and other features, aspects and advantages of the present subject matter will become better understood with reference to the following description and appended claims. This summary is provided to introduce a selection of concepts in a simplified form. This summary is not intended to be used to limit the scope of the claimed subject matter.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 illustrates the structure of conventional SPI protocol;

Figure 2 shows the fundamental building blocks of Mirrored Serial Interface (MSI);

Figures 3, 4 & 5 are showing flowcharts of the control mechanism of Master Controller;

Figures 6 & 7 are showing flowcharts of the control mechanism of Slave Controller.

DETAILED DESCRIPTION OF THE INVENTION

The present disclosure relates to a method and a mirrored serial interface (MSI) for transferring data with loopback mechanism through four wire serial interface namely SCLK, SS, MOSI and MISO wherein four wire interface is improved to introduce mechanisms like flow control, acknowledgement, data sanity checks and latency of device served by slave. The present disclosure provides flexible serial protocol with fault resilience as main feature desirable for accessing peripherals with mission critical importance. The protocol is defined for a single / multiple slave devices.

In the present disclosure contents of source data line is looped back onto the destination line and compared at every clock edge to ensure data sanity and assert presence of slave and master

device during and between cycles. Herein source refers to the controller which is sending the data and can be either master or slave based on whether it is a read or a write transaction. The signals used in the Mirrored serial interface (MSI) protocol are same as conventional SPI. As mentioned above, in the protocol of present invention, data sanity is checked at every clock edge using loopback mechanism i.e. data latched by the destination flip flop at the MOSI / MISO line is loop backed to the source at every clock edge to check for any communication errors.

After every burst of information (address / data) transfer, the source sends an acknowledgement to destination indicating data sanity for that particular transfer. In case, there is a violation both the master and slave controllers are in sync, and can take appropriate action. Burst of information transfer is an address phase or data phase. Address always flows from master to slave. Data flows in either direction based on whether it is a read or a write transaction. Acknowledgement signal generated by a slave is to indicate its readiness for the next cycle. This mechanism caters to any latency on the part of slow peripherals being served by the slave. The presence / absence of slave and master is ascertained by a loopback mechanism on the MISO and MOSI lines in the absence of any cycle, i.e. in the absence of slave select. Cycle termination or presence of data in case of read cycle is initiated by the slave to cater for any latency on the part of slow peripherals being served by the slave.

Both flag and acknowledgment is single bit in band signals asserted on the MISO or MOSI and can be high or low.

The present disclosure has the following advanced features in comparison to conventional SPI:

- Data sanity is checked at every clock edge implementing mirroring at the terminating end i.e. data latched by the slave flip flop at the MISO line is looped backed to the master at every clock edge for detecting instantaneous communication errors. The controllers have info about data sanity at every clock edge. Therefore, no need for any error calculation check such as CRC.
- After every burst of information (address / data) transfer, the source or destination sends an acknowledgement to destination indicating data sanity for that particular transfer. In case, there is a violation, both the master and slave controllers are in sync, and can take appropriate action.
- The presence / absence of slave and master can be ascertained by a looped back mechanism on the MISO and MOSI lines even in the absence of any accessing cycles.

- Data transmission can be done at both edges for enhance data rate.
- Cycle termination for host processor is automatically initiated by the master to cater slaves of different latencies.

Referring to figure-1, which shows a conventional serial peripheral interface protocol. Its implementation uses four signal lines for data and control i.e. SCLK, MOSI, MISO and SS. The shift register of master and slave are connected in a ring formation. In conventional SPI, the master sends a query to slave through MOSI. Simultaneously, slave responds to the previous query on the MISO line because of the ring formation mentioned above. Essentially, because of ring formation there is bidirectional flow of data but without any error checking. Master and slave controller in SPI do not sense the data lines. They only load and unload data from shift registers, align clock polarity, phases, configure clock frequency and present it for further processing.

Referring to figure-2, which shows the implementation of mirrored serial interface (MSI) according to embodiment of the present disclosure. The mirrored serial interface (MSI) have the presence of physical layer mirroring where data is sent back after the first bit is latched by the slave shift register. As per present disclosure, there is a master device and a number of slave devices, however in figure 2, one master device and one slave device have been shown.

To achieve the mirroring i.e. to implement the loopback mechanism the following hardware building blocks and interconnects are used in the mirrored serial interface (MSI) protocol:-

1) Presence of mux [113] and [114] to switch between data from shift registers and acknowledgment from master / slave controller.

2) Internal pull ups [107] and [108] on MOSI line in slave and MISO line in master respectively to detect presence and absence of slave when transaction is not in progress.

3) Data from Slave MSB and master MSB is sent to master controller. Similarly, data from slave LSB and master LSB is sent to slave controller.

4) Master and slave controller in mirrored serial interface (MSI) senses the data lines at every clock edge to compare the contents.

Figure 2 shows the fundamental building blocks of Mirrored Serial Interface (MSI).

1) MASTER AND SLAVE SHIFT REGISTER [101] and [115]: These register shift data between master and slave modules under the control of their respective controllers. They are connected to respective MUX ([113] and [114]) send data to the destination end.

Also, they are connected to respective controllers to enable comparison of looped back data at every clock edge.

2) MASTER CONTEOLLER [103]: Master controller manages data transfer flow between master and slave. It is responsible for loading and unloading of contents to and from shift register. It also compares the transmitted and looped back data at every clock edge on the MOSI line. It generates acknowledgment signal based after processing the information burst and steers the control of MUX [113]. Master controller also receives the in-band acknowledgment from the slave indicating successful previous information burst. It receives address, data, read/write command indication from MASTER HOST [116] and communicates if the cycle was successful or unsuccessful back to the HOST.

3) SLAVE CONTROLLER [112]: Slave controller manages data flow between master and slave. It loads and unloads contents to and from shift register. It also compares the transmitted and looped back data at every clock edge on the MISO line. It generates acknowledgment signal. It generates acknowledgment signal based after processing the information burst and steers the control of MUX [114]. Slave controller also receives the in-band acknowledgment from the master indicating successful previous information burst. It sends address, data, read/write command indication from SLAVE HOST [117] for further processing.

The protocol between master and slave based on the algorithm running in their respective controllers as mentioned in Figure 3 - 8 is as follows:-

In the absence of any slave select signal master drives logic 0 on the MOSI line. Slave on the contrary is in loopback mode, i.e. it loops the contents MOSI line back to the MISO line at every clock edge. Controller of master samples the contents of MISO at every clock edge. In the absence of slave device, i.e. its power failure or reset condition, MISO line is in tri state. As a result, master sense logic 1 on its MISO input because of its internal pull up indicating the absence of slave device. Similarly in the absence of master device, i.e. its power failure of reset condition, MOSI line is in tri state. Hence, the slave senses logic 1 on its MOSI input because of internal pull up indicating absence of master device.

Referring to figures 3, 4 and 5, showing flowcharts of control mechanism of Master Controller [103].

First burst of information transfer is the address phase. Host for master loads address along with

read / write bit in the universal shift register [101]. Address length is 8 bits and 1 bit for read/ write making a total of 9 bits. R/$\overline{W}$(Read/ Write bar) shall be logic '1' for read transaction and logic '0' for write transaction. The transaction between master and slave shall begin with assertion of slave select as in the case of SPI. All this information is transmitted on the MOSI line. Also, it sends back on the MISO line as the output of flip-flop [102] receiving the first bit on MOSI line. This is done to verify address sanity by the master. Comparison logic in the master controller [103] asserts the validity by comparing the data looped back from the slave [102] with the data looped back internally [104] on a particular clock edge.

Master keeps the clock enabled after first burst of address transfer. There is a wait state equivalent to 1 clock cycle during which master checks the sanity of the address transfer. Correspondingly, slave extract address along with the R/$\overline{W}$bit. On the next clock, master send an acknowledgement on MOSI line by driving logic 0 for 1 clock cycle indicating successful address transfer. In case the transfer was corrupt, logic 1 shall be sent for 1 clock cycle. Controller FSM's of both master and slave aborts the cycle in this case. Address and R/$\overline{W}$ bit from slave universal shift register are unloaded by the slave controller into the host.

If it is a write cycle, Master sends data on the MOSI line which is looped back on the MISO line by the slave as in the case of address transfer to ensure data sanity during the transfer. There is again a wait state of one clock during which master checks sanity of data transfer. An acknowledgement signal in the form of logic 0 is sent by the master to the slave to indicate valid transfer and logic 1 for one clock otherwise on the next clock. Cycle is aborted by both master and slave in case data transfer was corrupt. In case of valid data transfer, controller unloads the data from the universal shift register into the host. Since the address and data are now available to the host for processing, controller interrupts the host to retrieve the contents from register for further processing.

This is a wait phase for the master while the slave is busy processing the instruction. During this phase, Master continues to drive logic 0 on the MOSI line. Slave continues to loopback the contents MOSI line on the MISO line till it has not finished its transaction with the peripheral. In case, slave undergoes reset/power failure during this phase, loopback mechanism breaks because there is logic '1' on the master because of internal pull up and master can abort the cycle by de-asserting slave select. There shall also be a pre-configured timeout counter in the master controller to ensure the wait phase does not extend beyond a particular delay in case the host is in

hung state. After the slave host finishes the processing it sends an ACK to slave controller. Slave shall then generate a pulse equal to one clock width on MISO line to indicate completion of transaction. Master waits for one more clock after receiving ACK to ensure it MISO goes low indicating a successful acknowledgment. Master then asserts DTACK (Data acknowledgement) to the Master Host indicating successful cycle. Master Host then de-asserts Slave select and terminates the cycle. In case, it is a read cycle, Slave controller shall interrupt the host to unload the address from universal shift register. Host then begins its independent read cycle on another register / peripheral device.

Referring to figures 6 & 7, showing flowcharts of the control mechanism of Slave Controller.

Master continues to drive logic 0 on the MOSI line. Slave continues to loopback the contents of MOSI line on the MISO line till it has not finished its transaction with the peripheral. In case, slave undergoes reset/power failure during this phase, loopback mechanism breaks because there will be logic '1' on the master because of internal pull up and master can abort the cycle. There is also a pre-configured timeout counter in the master controller to ensure the wait phase does not extend beyond a particular delay in case the host is in hung state. After the slave host finishes the processing it sends an ACK to slave controller.

Slave then generate a pulse equal to one clock width on MISO line to indicate availability of data in its shift register. Master waits for one more clock after receiving ACK to ensure it MISO goes low indicating a successful acknowledgment. Master then reads the data from the slave which is looped back on the MOSI line [109]. Comparison logic in the slave controller [112] shall assert the validity by comparing the data looped back from the master [101] with the data looped back internally [11 1] on a particular clock edge.

Slave drives logic 0 on the MISO line indicating valid data transfer and logic 1 for one clock indicating invalid/corrupt data transfer. Master de-asserts slave select to terminate cycle if data transfer was valid. In case of invalid data transfer, cycle is terminated.

ADVANTAGES OF THE INVENTION

- Ensure data sanity;
- Ensure presence / absence of master and slave;
- Provide flow control to cater slow peripheral devices;
- Provide acknowledgement on receipt of data;

WE CLAIM

1. A method of transmitting data via a mirrored serial interface, the method comprising:

a master device receiving address, data and read/write command from a master host, loading address and read/write first in master shift register, shifting it to a slave device via MOSI line, simultaneously receiving mirrored address bits via MISO line to check for data sanity;

the slave device after successful transmission of address information fetching data from a slave host;

if the read instruction received, the slave device sending data to the master device via MISO line, simultaneously receiving mirrored data bits via MOSI line to check for data sanity;

if the write instruction received, the slave receiving the data from the master device and sharing it with the slave host for further processing, the master device again checking the mirrored data bits via the MISO line;

the master device and the slave device switching between data from shift register and acknowledgement from a slave controller or a master controller via multiplexers, and

the presence and absence of the master device or the slave device being detected through internal pull ups when transaction not being in progress.

2. The method as claimed in claim 1, wherein loopback mechanism on the MISO and MOSI lines determines presence or absence of the master device and slave device in absence of a slave select signal.

3. The method as claimed in claim 1, wherein method steps for checking the data sanity comprise:-

looping back the content of source data line onto destination data line; and

comparing the content at every clock edge by a source device controller.

4. The method as claimed in claim 1 or 3, wherein either of the master device or the slave device is a source depending on whether it is a read or a write transaction.

5. The method as claimed in claim 1 or 3, wherein source device sends a flag to destination after transferring every burst of data bits indicating data sanity for each transfer.

6. The method as claimed in claim 5, wherein transfer of a burst of data bits includes an address transfer phase and a data transfer phase.
7. The method as claimed in claim 6, wherein the address bits flow from master device to slave device and data bits flow in either direction.
8. The method as claimed in claim 7, wherein the slave device generates an acknowledgement signal to indicate its readiness for the next cycle.
9. The method as claimed in any one of the claim 1, 5 or 8, wherein flag and acknowledgement is a single bit in band signals asserted on the MOSI and MISO lines and is either high or low.
10. The method as claimed in claim 1, wherein the method is implemented by using four signal lines including MOSI, MISO, SCLK, SS for data and control.
11. The method as claimed in claim 1, wherein in absence of slave select signal a) the master drives logic 0 on MOSI line, b) the slave, in loopback mode, loops back the contents of MOSI line to MISO line at every clock edge; and c) controller of master samples the contents of MISO at every clock edge, if the master senses logic 1 on its MISO line input, it indicates absence of slave device.
12. The method as claimed in claim 1, wherein slave drives logic 0 on the MOSI line indicating valid data transfer and logic 1 for one clock indicating invalid data transfer.
13. A mirrored Serial interface comprising

a master device and at least one slave device;

the master device and each of the at least one slave device connected to one another with four signal lines, a serial clock line (SCLK), a master-in-slave-out (MISO) line and a master-out-slave-in (MOSI) line, and a slave select (SS) line for selecting a slave device in a multi-slave configuration;

the master device configured for transmitting data to and receiving data from at least on slave peripheral device, said master peripheral interface device comprising a serial clock generator to generate clock for synchronizing data movement in and out of the device through MOSI and MISO lines, a shift register comprising a group of flip-flops for shifting data into internal storage elements and shifting data out at the serial-out, a memory element and a controller for controlling function of the master device; and

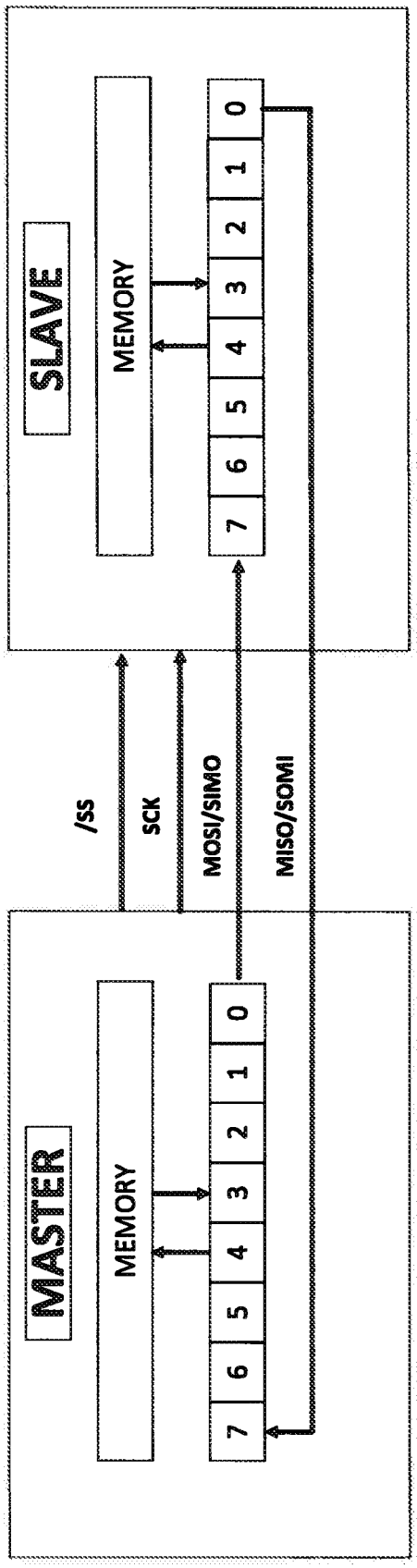
the at least one slave device comprising a shift register comprising a group of flip-flops for shifting data into internal storage elements and shifting data out at the serial-out, a memory element, and a controller for controlling function of the slave device,

Characterized in that

the master device and the slave device have multiplexers to switch between data from shift register and acknowledgement from any of the controller,

the master device has an internal pull up at the MISO line and each of the slave device has an internal pull up at the MOSI line to detect presence and absence of master device or slave device when transaction is not in progress, and

the data latched by the slave flip-flop at the MISO line is configured to be looped back to the master at every clock edge for reporting communication errors.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1
0

Fig.1

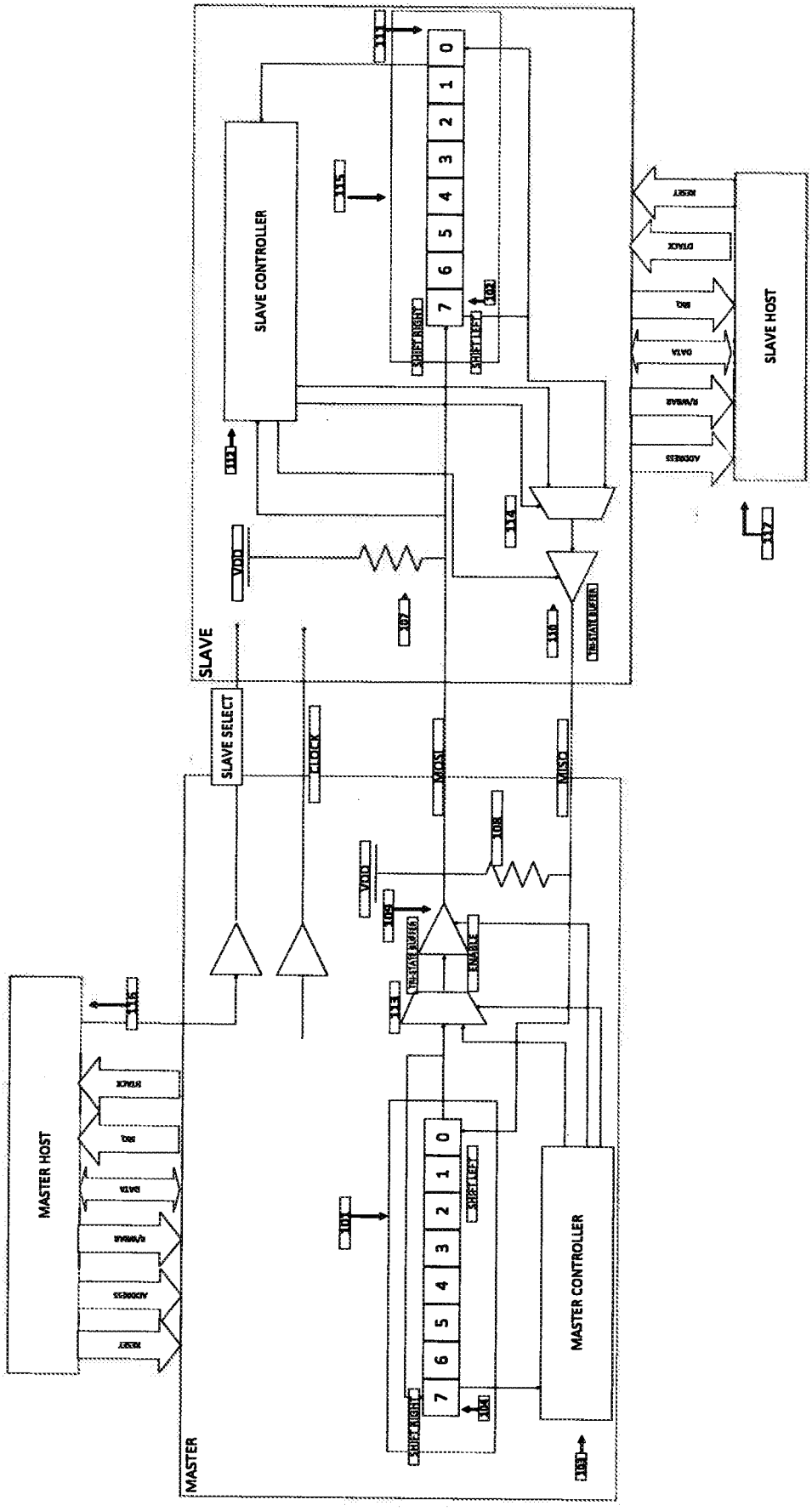
SLAVE
SLAVE CONTROLLER
SLAVE HOST
SLAVE SELECT
CLOCK
MOSI
MISO
MASTER
MASTER HOST
MASTER CONTROLLER
VDD
TRI-STATE BUFFER
ENABLE
SHIFT RIGHT
SHIFT LEFT
RESET
DTACK
REQ
DATA
R/WBAR
ADDRESS

Fig.2

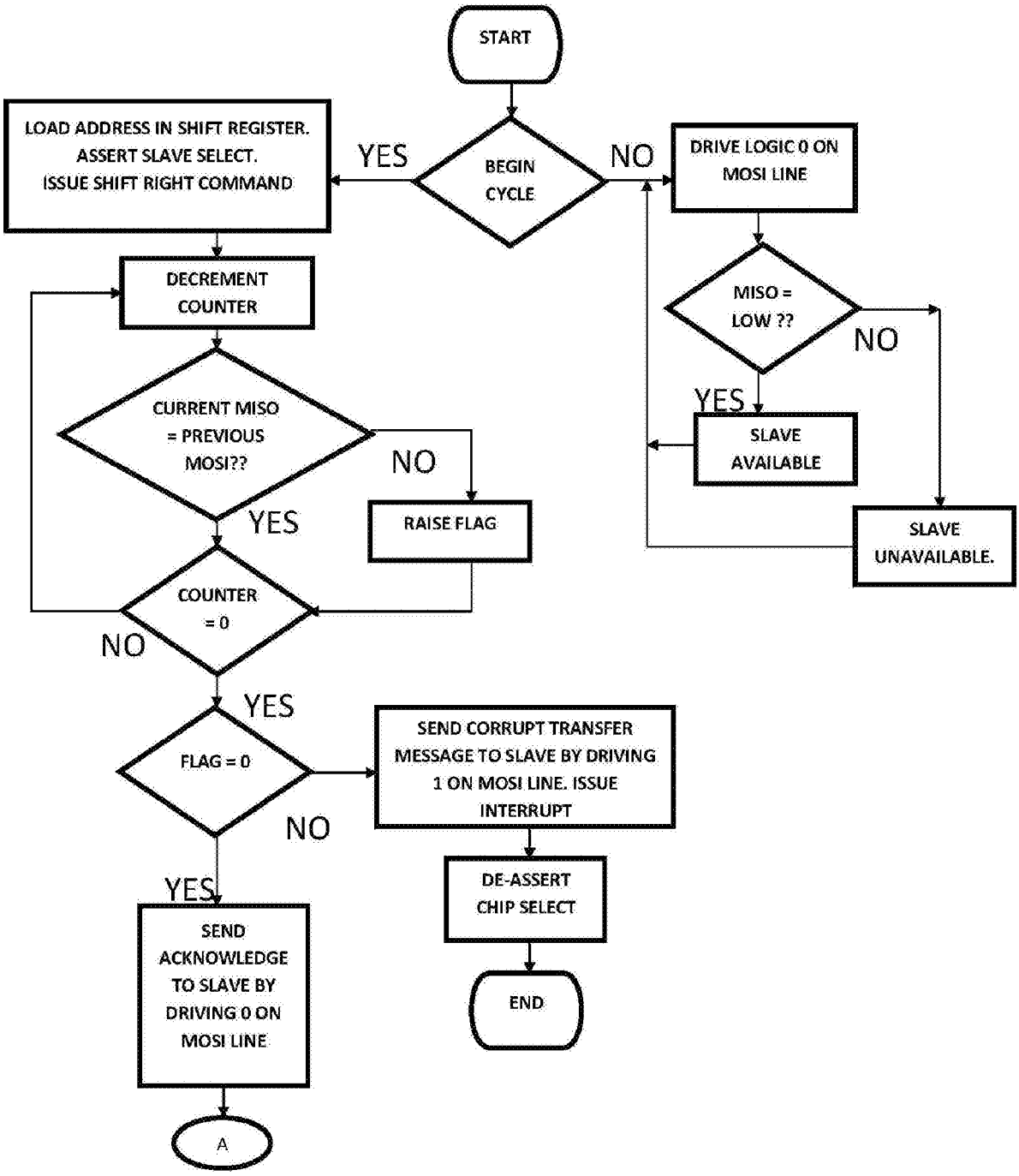
START
BEGIN CYCLE
YES
NO
LOAD ADDRESS IN SHIFT REGISTER. ASSERT SLAVE SELECT. ISSUE SHIFT RIGHT COMMAND
DRIVE LOGIC 0 ON MOSI LINE
DECREMENT COUNTER
MISO = LOW ??
NO
YES
SLAVE AVAILABLE
SLAVE UNAVAILABLE.
CURRENT MISO = PREVIOUS MOSI??
NO
YES
RAISE FLAG
COUNTER = 0
NO
YES
FLAG = 0
NO
YES
SEND CORRUPT TRANSFER MESSAGE TO SLAVE BY DRIVING 1 ON MOSI LINE. ISSUE INTERRUPT
DE-ASSERT CHIP SELECT
END
SEND ACKNOWLEDGE TO SLAVE BY DRIVING 0 ON MOSI LINE
A

Fig. 3

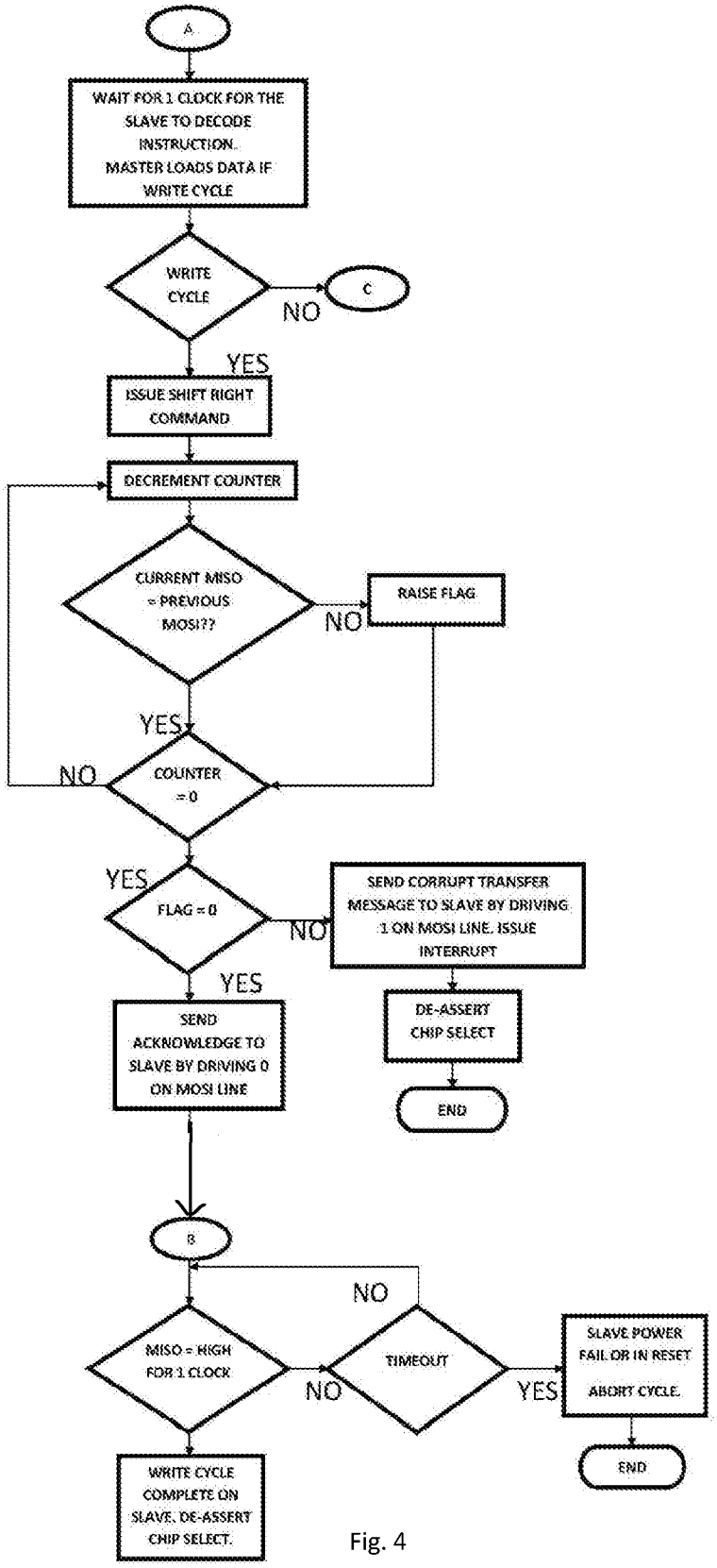
A
WAIT FOR 1 CLOCK FOR THE SLAVE TO DECODE INSTRUCTION. MASTER LOADS DATA IF WRITE CYCLE
WRITE CYCLE
NO
C
YES
ISSUE SHIFT RIGHT COMMAND
DECREMENT COUNTER
CURRENT MISO = PREVIOUS MOSI??
NO
RAISE FLAG
YES
NO
COUNTER = 0
YES
FLAG = 0
NO
SEND CORRUPT TRANSFER MESSAGE TO SLAVE BY DRIVING 1 ON MOSI LINE. ISSUE INTERRUPT
DE-ASSERT CHIP SELECT
END
YES
SEND ACKNOWLEDGE TO SLAVE BY DRIVING 0 ON MOSI LINE
B
NO
MISO = HIGH FOR 1 CLOCK
NO
TIMEOUT
YES
SLAVE POWER FAIL OR IN RESET ABORT CYCLE.
END
WRITE CYCLE COMPLETE ON SLAVE. DE-ASSERT CHIP SELECT.

Fig. 4

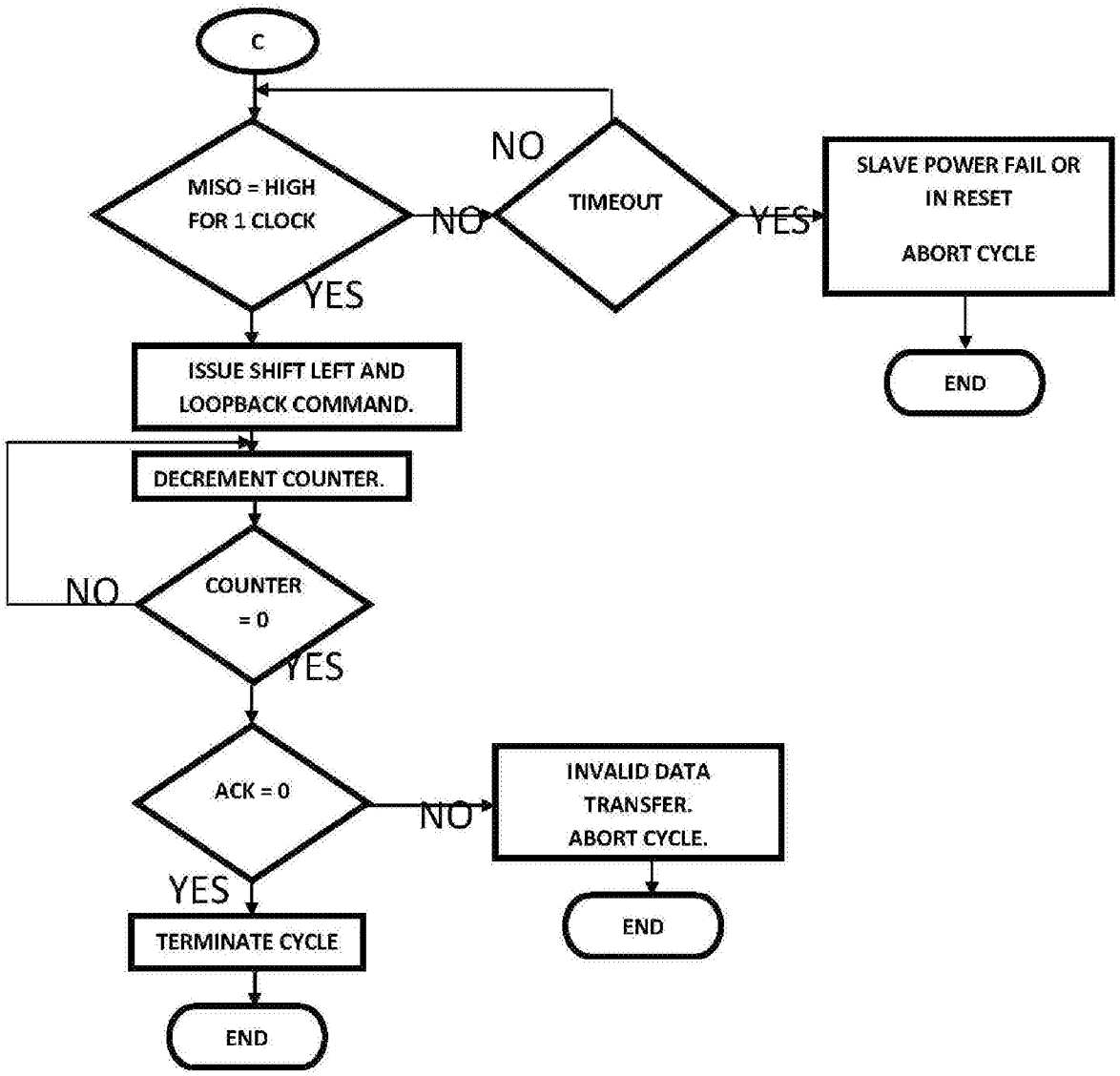
C
MISO = HIGH FOR 1 CLOCK
NO
TIMEOUT
YES
SLAVE POWER FAIL OR IN RESET
ABORT CYCLE
END
NO
YES
ISSUE SHIFT LEFT AND LOOPBACK COMMAND.
DECREMENT COUNTER.
NO
COUNTER = 0
YES
ACK = 0
NO
INVALID DATA TRANSFER. ABORT CYCLE.
END
YES
TERMINATE CYCLE
END

Fig. 5

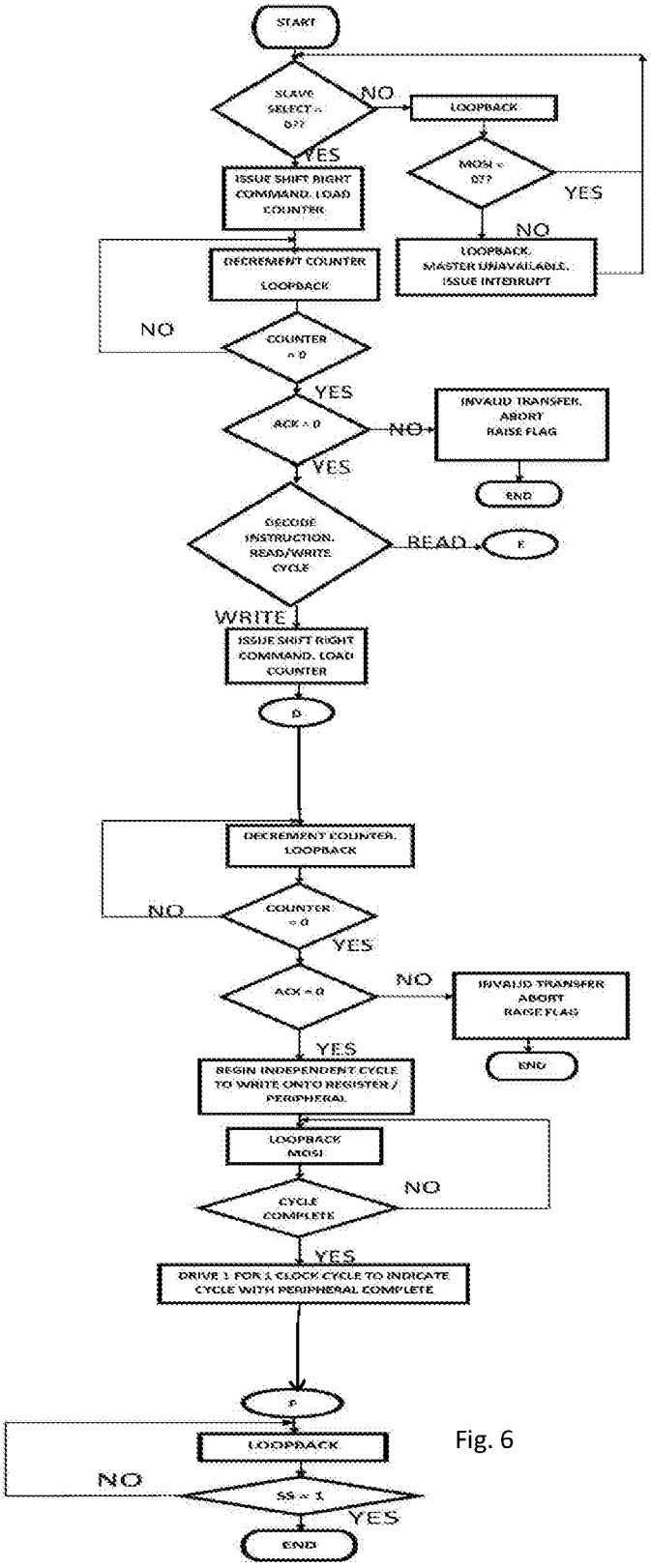
START
SLAVE SELECT = 0??
NO
LOOPBACK
YES
MOSI = 0??
YES
NO
ISSUE SHIFT RIGHT COMMAND, LOAD COUNTER
LOOPBACK, MASTER UNAVAILABLE, ISSUE INTERRUPT
DECREMENT COUNTER
LOOPBACK
NO
COUNTER = 0
YES
ACK = 0
NO
INVALID TRANSFER, ABORT RAISE FLAG
END
YES
DECODE INSTRUCTION, READ/WRITE CYCLE
READ
F
WRITE
ISSUE SHIFT RIGHT COMMAND, LOAD COUNTER
D
DECREMENT COUNTER, LOOPBACK
NO
COUNTER = 0
YES
ACK = 0
NO
INVALID TRANSFER ABORT RAISE FLAG
END
YES
BEGIN INDEPENDENT CYCLE TO WRITE ONTO REGISTER / PERIPHERAL
LOOPBACK MOSI
CYCLE COMPLETE
NO
YES
DRIVE 1 FOR 1 CLOCK CYCLE TO INDICATE CYCLE WITH PERIPHERAL COMPLETE
F
LOOPBACK
NO
SS = 1
YES
END

Fig. 6

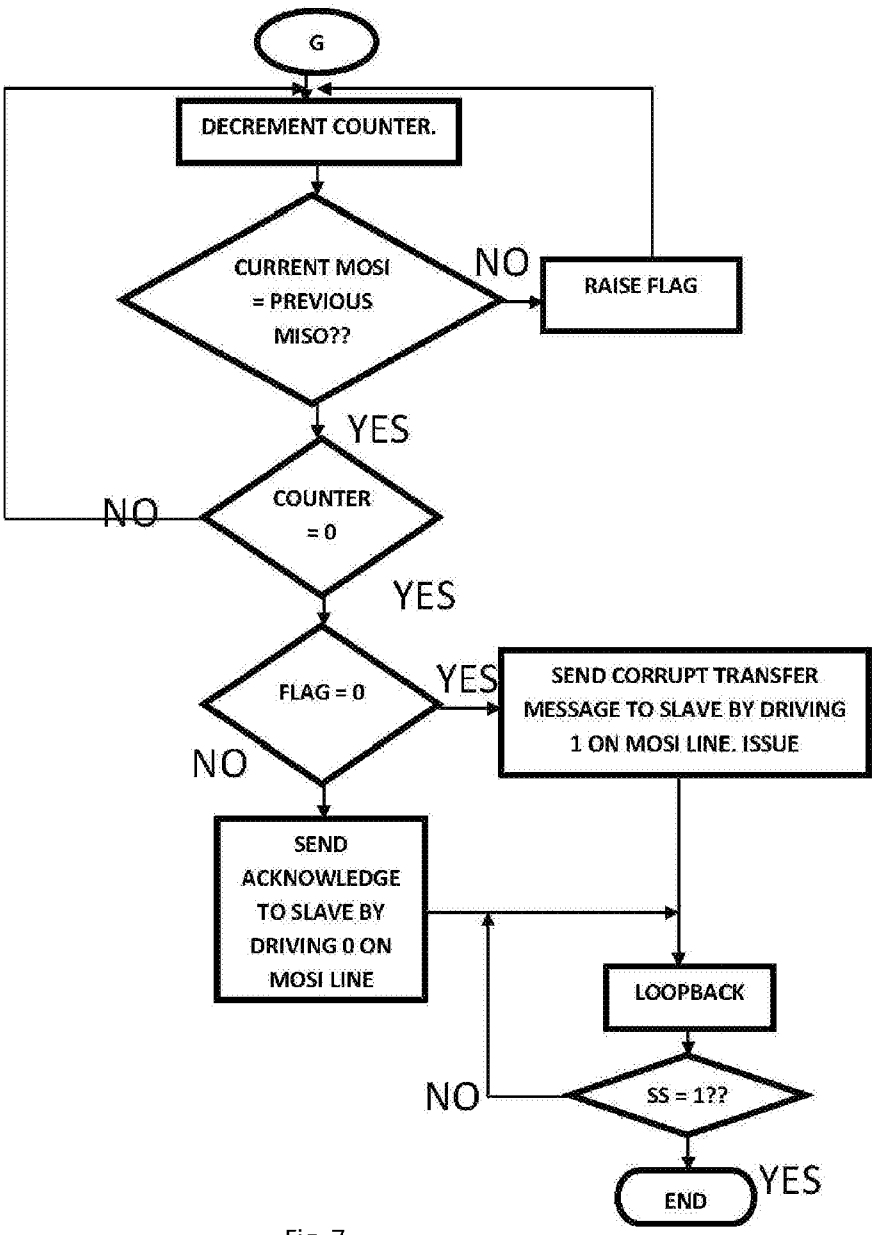
G
DECREMENT COUNTER.
CURRENT MOSI = PREVIOUS MISO??
NO
RAISE FLAG
YES
COUNTER = 0
NO
YES
FLAG = 0
YES
SEND CORRUPT TRANSFER MESSAGE TO SLAVE BY DRIVING 1 ON MOSI LINE. ISSUE
NO
SEND ACKNOWLEDGE TO SLAVE BY DRIVING 0 ON MOSI LINE
LOOPBACK
SS = 1??
NO
END
YES

Fig. 7

INTERNATIONAL SEARCH REPORT

International application No.
PCT/IN 17/50179

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - G06F 13/00 (2017.01), H03M 13/00 (2017.01)
CPC - G06F13/4291, G06F13/4217, H04L29/06, G06F13/385,

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
See Search History Document

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
See Search History Document

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
See Search History Document

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2008/0183928 A1 (DEVILA et al.), 31 July 2008 (31.07.2008), entire document, especially Abstract; Para [0027], [0029], [0031]-[0034], [0049], [0055], [0114]-[0119]	1-8 and 10-12
Y	US 2005/0163277 A1 (Georgakos et al.), 28 July 2005 (28.07.2005), entire document, especially Abstract; Para [0026], [0028], [0043]-[0045]	1-8 and 10-12
Y	US 2004/0101133 A1 (Le et al.), 27 May 2004 (27.05.2004), entire document, especially Abstract; Para [0002], [0020]-[0023]	1-8 and 10-12
A	US 5,828,592 A (Tran et al.), 27 October 1998 (27.10.1998), entire document	1-8 and 10-12
A	US 20120072628 A1 (Crockett et al.), 22 March 2012 (22.03.2012), entire document	1-8 and 10-12

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
11 October 2017	30 OCT 2017

Name and mailing address of the ISA/US	Authorized officer:
Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-8300	Lee W. Young PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

INTERNATIONAL SEARCH REPORT

International application No.
PCT/IN 17/50179

Box No. I I Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely.

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☒ Claims Nos.: 9
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. Ill Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

This application contains the following inventions or groups of inventions which are not so linked as to- form a single general inventive concept under PCT Rule 13.1 . In order for all inventions to be examined, the appropriate additional examination fees must be paid.

Group I - Claims 1-8 and 10-12 are directed to a method of transmitting data via a mirrored serial interface.

Group II - Claim 13 is directed to a mirrored Serial interface.

— (See Continuation in Supplemental Box) —

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:
1-8 and 10-12

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

Continuation of:
Box III. Observations where unity of invention is lacking

The inventions listed as Groups I-II do not relate to a single general inventive concept under PCT Rule 13.1 because, under PCT Rule 13.2, they lack the same or corresponding special technical features for the following reasons:

Special Technical Features:

The invention of Group I included the features of a master device receiving address, data and read/write command from a master host, loading address and read/write first in master shift register, shifting it to a slave device via MOSI line, simultaneously receiving mirrored address bits via MISO line to check for data sanity; the slave device after successful transmission of address information fetching data from a slave host; if the read instruction received, the slave device sending data to the master device via MISO line, simultaneously receiving mirrored data bits via MOSI line to check for data sanity; if the write instruction received, the slave receiving the data from the master device and sharing it with the slave host for further processing, the master device again checking the mirrored data bits via the MISO line, not required by Group II.

The invention of Group II included the features of the master device and each of the at least one slave device connected to one another with four signal lines, a serial clock line (SCLK), and a slave select (SS) line for selecting a slave device in a multi-slave configuration; master peripheral interface device comprising a serial clock generator to generate clock for synchronizing data movement in and out of the device through MOSI and MISO lines, a shift register comprising a group of flip-flops for shifting data into internal storage elements and shifting data out at the serial-out, a memory element and a controller for controlling function of the master device; and the at least one slave device comprising a shift register comprising a group of flipflops for shifting data into internal storage elements and shifting data out at the serial-out, a memory element, and a controller for controlling function of the slave device, not required by Group I.

Common Technical Features

Groups I-II share the technical features of a master device and at least one slave device; the master device configured for transmitting data to and receiving data from at least on slave peripheral device; a master-in-slave-out (MISO) line; a master-out-slave-in (MOSD line; the master device and the slave device switching between data from shift register and acknowledgement from a slave controller or a master controller via multiplexers, and the presence and absence of the master device or the slave device being detected through internal pull ups when transaction not being In progress.

However, the shared technical features does not represent a contribution over prior art as being obvious over US 5,828,592 A to Tran et al. (hereinafter 'Tran'), 27 October 1998 (27.10.1998) in view of US 2004/0101 133 A 1 to Le et al. (hereinafter 'Le'), 27 May 2004 (27.05.2014).

Tran teaches a master device and at least one slave device (col 3, In 23-45 - the master device); the master device configured for transmitting data to and receiving data from at least on slave peripheral device (col 3, In 23-45; col 6, In 5-40 - the master device (microcontroller) and is used to synchronize Ad data transfers in and out of the device through the Master Out Slave In (MOSI) and Master In Slave Out (MISO) terminals); a master-in-slave-out (MISO) line (col 4, In 23-45 - The MISO terminal is the serial output of the integrated circuit 10. This output goes into a high-impedance state if the integrated circuit 10 is not selected.); a master-out-slave-in (MOSI) line (col 4, In 23-45 - The MOSI pin is a serial input to the SPI 14. The master device (microcontroller 15) places data on the MOSI line one-half cycle before the SCLK clock edge); the master device and the slave device switching between data from shift register and acknowledgement from a slave controller or a master controller via multiplexers (col 5, In 50 to col 6, In 55 - Instead of reading cell by cell serially by multiplexing the shift registers, a group of cells, for example 100 cells, are read in parallel in the source follower mode, A fast serial shift is executed to shift out all the logic signals, instead of analog signals, into a digital output pad, bypassing the output analog path. The speed is limited by the shift register and the output digital pad for every 100 cells; a shift register, which is part of the column driver, is used as a cyclic binary shifter to enable the provision of one memory output at a time, along the column drivers, beginning from the first column to the 100th column; A 12:1 mux is used to multiplex 12 columns to one column driver; The clocking of the shift register SR is derived from an oscillator on the integrated circuit 10. The output at output terminal DIGOUT is then multiplexed to a digital output through the HSARYD signal).
Le teaches the presence and absence of the master device or the slave device being detected through internal pull ups when transaction not being in progress (Para [0002], [0020]-[0023] - method and apparatus for detecting the presence or absence of devices connected to communications networks; voltage comparator is used as a presence detector, the comparator can compare the low-frequency voltage to a number of different reference voltages, so that if different values of pull-down resistors are used in peripheral devices for each type of device, the detection scheme can be used to detect not only the presence of hardware, but also the type of hardware).

As the common features were known in the art at the time of the invention, this cannot be considered a common technical feature that would otherwise unify the groups. Therefore, Groups I-II lack unity under PCT Rule 13.