

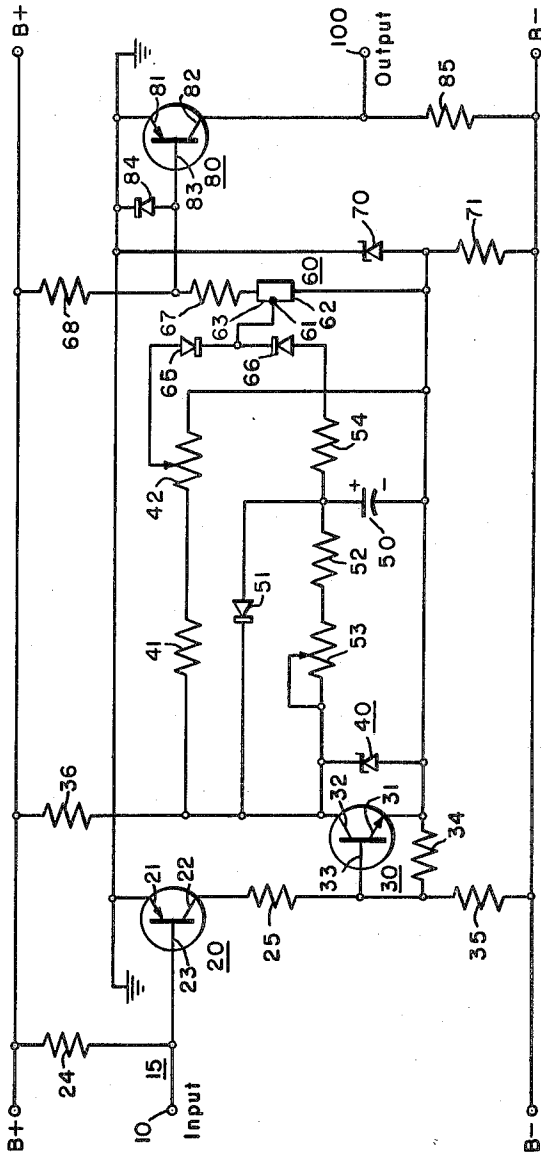
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TIMING CIRCUIT

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WITNESSES

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TIMING CIRCUIT

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This invention relates to timing circuits in general and in particular to static timing circuits.

It is an object of this invention to provide an improved static timing circuit.

It is another object of this invention to provide an improved static timing circuit which is accurate, very reliable and easily adjustable over a considerable timing range.

It is still another object of this invention to provide an improved static timing circuit which is temperature and voltage compensated.

Further objects of this invention will become apparent from the following description when taken in conjunction with the accompanying drawing. In said drawing, for illustrative purposes only, there is shown a preferred embodiment of the invention.

The drawing is a schematic diagram of a static, semiconductor timing circuit which is temperature and voltage compensated, illustrating the teachings of this invention.

In general, the apparatus illustrated in the drawing comprises input means 15 having terminal means 10 and input transistor means 20, intermediate transistor means 30, double base diode means 60, voltage compensating means 40 and 70, and output transistor means 80.

The input transistor means 20 comprises an emitter electrode 21, a collector electrode 22 and a base electrode 23. The emitter electrode 21 is connected to a common conductor or ground. The collector electrode 22 is connected through a resistance 25 and a resistance 35 to a negative or B— bias supply. The base electrode 23 is connected to the input terminal 10 and to a positive or B+ bias supply through a current limiting resistor 24.

The intermediate transistor means 30 comprises an emitter electrode 31, a collector electrode 32, and a base electrode 33. The emitter electrode 31 is connected through a resistor 34 and the resistor 35 to the B— supply. The emitter electrode 31 is connected to the base electrode 33 through the resistor 34. The collector electrode 32 is connected through a current limiting resistor 36 to the B+ supply. The base electrode 33 is connected through the resistor 25 to the collector electrode 22 of the input transistor 20.

The voltage compensating or constant voltage means 40 comprises a semiconductor diode connected across the collector 32-emitter 31 circuit of the intermediate transistor 30. The semiconductor diode 40 is connected to utilize its Zener type breakdown effect to maintain a constant voltage across the diode 40 in spite of normal bias supply variation in a reverse direction. A capacitive means 50 is connected through a current limiting resistor 52 and a potentiometer 53 across the collector 32-emitter 31 circuit of the transistor 30. A rectifying means 51 is connected in shunt across the resistor 52 and the potentiometer 53.

The double base diode or unijunction transistor means 60 comprises an emitter electrode 61, a first base elec-

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trode 62 and a second base electrode 63. The capacitor 50 is connected through a resistor 54 and a rectifier 66 across the emitter 61-first base electrode 62 circuit of the double base diode 60. The emitter electrode 61 of the double base diode 60 is connected through a rectifying means 65, a potentiometer 42, a resistor 41 and the resistor 36 to the B+ supply. This applies a constant voltage from the diode 40 to the emitter 61-first base 62 circuit of the double base diode 60. The second base electrode 63 is connected through a resistor 67 and a resistor 68 to the B+ supply. The first base electrode 62 is connected through a resistor 71 to the B— supply. A semiconductor diode 70, similar or identical to the semiconductor diode 40, is connected between common or ground through a resistor 71 to the B— supply. The semiconductor diode 70 functions in the same fashion as the semiconductor diode 40 by means of a Zener type breakdown to hold a constant voltage across the diode 70 in a reverse direction.

The output transistor 80 comprises an emitter electrode 81, a collector electrode 82 and a base electrode 83. The emitter electrode 81 is connected to ground. The collector electrode 82 is connected through the output terminal 100 and a resistor 85 to the B— supply. The base electrode 83 is connected through the resistor 67 to the second base electrode 63 of the double base diode 60. The base electrode 83 is also connected through a rectifying means 84 to ground.

The transistor means 20, 30 and 80 utilized in the preferred embodiment of this invention are, as illustrated, of the three electrode type commonly used for switching purposes. That is the direct-current voltage to be switched is connected to two of said three electrodes. In response to a bias voltage of the proper polarity and magnitude, applied between the third and one of said two electrodes, conduction is allowed in the said two electrode circuits. Although P-N-P or N-P-N types are illustrated, N-P-N and P-N-P types, respectively, may be used with the proper reversal of bias supply polarity connections in a manner well known to those skilled in the art.

Assume that the energy storage means or capacitor 50 is fully charged with electrical energy and that the semiconductor diode 40 is holding its full Zener voltage thereacross. A negative input signal is applied to the input terminal 10. Since the input transistor 20 is illustrated to be of the P-N-P type, the application of this negative signal of the proper magnitude to the base electrode 23 will allow conduction in the emitter 21-collector 22 circuit of the transistor 20. Conduction in the emitter 21-collector 22 circuit of the transistor 20 through the resistors 25 and 35 will apply a positive bias to the base electrode 33 of the transistor 30 with respect to the emitter 31. Since the transistor 30 is illustrated as the N-P-N type, the application of a positive bias of the proper magnitude to the base electrode 33 will allow conduction in the collector 32-emitter 31 circuit. Therefore the input means 15 functions to bias said intermediate transistor means 30 to conduction.

Conduction in the collector 32-emitter 31 circuit of the transistor 30 will short the Zener voltage from the semiconductor diode 40 and allow instantaneous discharge of the stored electrical energy of the capacitor 50 through the rectifying means 51. The discharge of the capacitor 50 resets the double base diode 60 by placing the emitter electrode 61 and the first base electrode 62 of the double base diode 60 at the same potential. Therefore, the first base 62 to second base 63 impedance of the double base diode 60 will increase and decrease conduction therethrough. The non-conduction of the double base diode 63 places a positive bias of the proper magnitude on the base electrode 83 with respect to the

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emitter 81 of the transistor 80. Since the transistor 80 is of the P-N-P type, the positive bias applied to the base electrode 83 thereof will stop conduction in the emitter 81-collector 82 circuit of the transistor 80, and an output will appear at the terminal 100 with respect to ground. This output for the timing circuit will be nearly the value of the B— supply with no load connected to the output terminal 100.

When the negative input signal at the terminal 10 is removed, the input transistor 20 is biased to cutoff by the B+ supply through the current limiting resistor 24. When the conduction through the emitter 21-collector 22 circuit of the transistor 20 ceases, the transistor 30 is biased to cutoff by the voltage drop across resistor 34. The voltage across the resistor 34 is a fraction of the drop across resistor 71. This fraction is determined by the resistors 34 and 35 and the leakage of the transistor 30. The resistor 34 is connected between the emitter 31 and the base electrode 33 of the transistor 30 to prevent the base electrode 33 from becoming too negative with respect to the emitter 31.

When conduction stops in the collector 32-emitter 31 circuit of the intermediate transistor 30, voltage from the B+ supply is again applied across the semiconductor diode 40 in the reverse direction, and the capacitor 50 starts to charge through the potentiometer 53 and the current limiting resistor 52.

The potentiometer 42 is adjusted so that the voltage appearing at the emitter electrode 61 of the double base diode 60 is slightly below the voltage necessary to fire the double base diode 60. The rectifying means 66 prevents charging of the capacitor 50 through the potentiometer 42 whenever the voltage across the capacitor is below the voltage or potential at the emitter electrode 61 of the double base diode 60. The rectifier 65 prevents current flow to the potentiometer 42 when the voltage across the capacitor 50 raises the potential of the emitter 61 of the double base diode 60 above the voltage already set by the potentiometer 42.

When the capacitor 50 charges to the firing potential of the double base diode 60, the capacitor 50 discharges through the emitter 61-first base 62 circuit of the double base diode 60, and the potential at the emitter electrode 61 drops. Current then flows from the potentiometer 42 through the rectifier 65, holding the double base diode 60 in a conducting state.

When the double base diode 60 fires the first base 62 to second base 63 impedance becomes low, allowing the application of a negative biasing potential of the base electrode 83 of the transistor 80. Therefore, the transistor 80 will conduct in its emitter 81-collector 82 circuit and will short the output at the terminal 100 or remove the output from the timing circuit as illustrated in the drawing.

For a more detailed description of the construction, operation and characteristics of a double base diode which may be utilized in this invention, reference is made to "An Introduction to Semiconductors," by W. C. Dunlap, Jr., pp. 365-367, published by John Wiley and Sons, Inc., New York, 1957.

The resistor 67 connected between the second base electrode 63 of the double base diode 60 and the base electrode 83 of the transistor 80 aids in the resetting process of the double base diode 60 when an input is applied to the terminal 10, as hereinbefore described, and the transistor 80 is desired to be cut off.

The function of the semiconductor diode 70 is to keep variation in the supply voltages from affecting the firing point of the double base diode 60. If the voltage at the second base electrode 63 with respect to the emitter electrode 61 can be kept constant before firing, the voltage at which the double base diode 60 fires can be accurately reproduced and is independent of temperature. The impedance 67 may be a positive coefficient thermistor to compensate for the slight increase with temperature of the interbase impedance of the double base diode 60,

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For certain values of the capacitor 50 the circuit will oscillate unless the resistor 71 is added. The resistor 71 increases the time available for the circuit to supply the current to keep the double base diode 60 conducting.

The rectifier 84 functions to prevent the back emitter voltage on the transistor 80 from becoming excessive when the transistor 80 is cut off.

The double base diode 60 is used as a bistable device. If the emitter 61 resistance is made too large the circuit will operate in a non-stable condition and will oscillate. The resistor 41 and the potentiometer 42 may be viewed as supplying current to keep the double base diode 60 on or providing a low impedance load line after the double base diode 60 has fired to insure bistable operation. If the emitter 61 resistance was solely determined by the charging resistors 41 and 42, the charging resistance value would be limited to a maximum value determined by the value of resistance at which the operation of the double base diode 60 switched from bistable to monostable operation. The timer would then have a very limited range for a given value capacitance.

A timing circuit has been described which is accurate, reliable and easily adjustable over a considerable timing range by the setting of the potentiometer 53. Since the circuit is comprised of static semiconductor components, it has inherent maintenance-free, long-life qualities.

In conclusion, it is to be noted that while the illustrated example constitutes a practical embodiment of our invention, we do not limit ourselves to the exact details shown, since modification of the same may be varied without departing from the spirit and scope of this invention.

We claim as our invention:

1. In a timing circuit, in combination; input means for applying a signal to said timing circuit; intermediate and output transistor means each having three electrodes; double base diode means having an emitter electrode, a first base electrode and a second base electrode; electrical energy storage means; and means connecting bias supply means to said timing circuit; said energy storage means being connected to charge from said bias supply means; said intermediate transistor means having two of its said three electrodes connected to discharge said energy storage means in response to a signal applied to said input means; said energy storage means upon discharge being connected through isolating rectifier means to regulate conduction between said first and second base electrodes of said double base diode means; said output transistor means being connected to said first and second base electrodes of said double base diode so that conduction therethrough controls the output state of said output transistor means; said bias supply being connected to supply bias potential to said intermediate transistor means, said output transistor means, and said double base diode means; said bias supply means being connected between said emitter and first base electrode means of said double base diode means through isolating rectifier means.

2. In a timing circuit, in combination; input means for applying a signal to said timing circuit; intermediate and output transistor means each having three electrodes; double base diode means having an emitter electrode, a first base electrode and a second base electrode; electrical energy storage means; and means connecting bias supply means to said timing circuit; said energy storage means being connected to charge from said bias supply means through constant voltage means; said intermediate transistor means having two of its said three electrodes connected to discharge said energy storage means in response to a signal applied to said input means; said energy storage means upon discharge being connected through isolating rectifier means to regulate conduction between said first and second base electrodes of said double base diode means; said output transistor means being connected to said first and second base electrodes of said double base diode so that conduction therethrough con-

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trols the output state of said output transistor means; said bias supply being connected to supply bias potential to said intermediate transistor means, said output transistor means, and said double base diode means; said bias supply means being connected between said emitter and first base electrode means of said double base diode means through isolating rectifier means.

3. In a timing circuit, in combination; input means for applying a signal to said timing circuit; intermediate and output transistor means each having three electrodes; double base diode means having an emitter electrode, a first base electrode and a second base electrode; electrical energy storage means; and means connecting bias supply means to said timing circuit; said energy storage means being connected to charge from said bias supply means through constant voltage means; said intermediate transistor means having two of its said three electrodes connected to discharge said energy storage means through isolating rectifier means shunting charging resistor means for said energy storage means in response to a signal applied to said input means; said energy storage means upon discharge being connected through isolating rectifier means to regulate conduction between said first and second base electrodes of said double base diode means; said output transistor means being connected to said first and second base electrodes of said double base diode so that conduction therethrough controls the output stage of said output transistor means; said bias supply being connected to supply bias potential to said intermediate transistor means, said output transistor means, and said double base diode means; said bias supply means being connected between said emitter and first base electrode means of said double base diode means through isolating rectifier means.

4. In a timing circuit, in combination; input means comprising input switching transistor means for applying a signal to said timing circuit; intermediate and output transistor means each having three electrodes; double base diode means having an emitter electrode, a first base electrode and a second base electrode; electrical energy storage means; and means connecting bias supply means to said timing circuit; said energy storage means being connected to charge from said bias supply means through constant voltage means; said intermediate transistor means having two of its said three electrodes connected to discharge said energy storage means through isolating rectifier means shunting charging resistor means for said energy storage means in response to a signal applied to said input means; said energy storage means upon discharge being connected through isolating rectifier means to regulate conduction between said first and

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second base electrodes of said double base diode means; said output transistor means being connected to said first and second base electrodes of said double base diode so that conduction therethrough controls the output stage of said output transistor means; said bias supply being connected to supply bias potential to said intermediate transistor means, said output transistor means, and said double base diode means; said bias supply means being applied between said emitter and first base electrode means of said double base diode means through isolating rectifier means.

5. In a timing circuit, in combination; input means comprising input switching transistor means for applying a signal to said timing circuit; intermediate and output transistor means each having three electrodes; double base diode means having an emitter electrode, a first base electrode and a second base electrode; electrical energy storage means; and means connecting bias supply means to said timing circuit; said energy storage means being connected to charge from said bias supply means through constant voltage means; said intermediate transistor means having two of its said three electrodes connected to discharge said energy storage means through isolating rectifier means shunting charging resistor means for said energy storage means in response to a signal applied to said input means; said energy storage means upon discharge being connected through isolating rectifier means to regulate conduction between said first and second base electrodes of said double base diode means; said output transistor means being connected to said first and second base electrodes of said double base diode so that conduction therethrough controls the output stage of said output transistor means; said bias supply being connected to supply bias potential to said intermediate transistor means, said output transistor means, and said double base diode means; said bias supply means being connected between said emitter and first base electrode means of said double base diode means through isolating rectifier means; the value of said bias applied to said emitter and first base electrode means of said double base diode means being less than the firing voltage of said double base diode means.

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