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(54) Title: OPERATING MECHANISM FOR TRIPPING A VOLTAGE CIRCUIT BREAKER

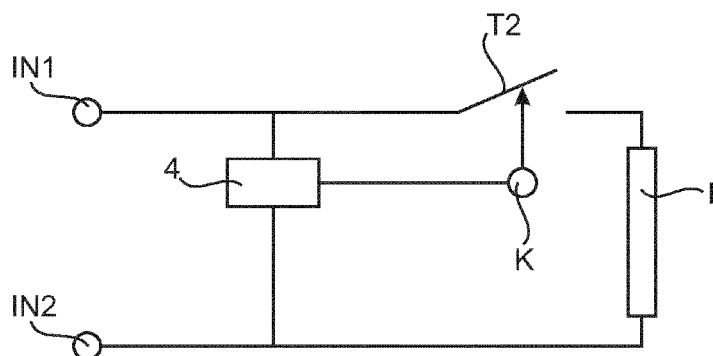


FIG.2

(57) Abstract: Operating mechanism for tripping a circuit- breaker, the operating mechanism comprising a coil (L) having a first terminal and a second terminal, means for generating a first electric impulse, and means for creating, from the first electric impulse, a second electric impulse delayed from the first electric impulse and applied between the first terminal and the second terminal of the coil, characterised in that the means for creating the second electric impulse comprise a delaying circuit (4) and a switch (T2) connected in series with the coil (L), the delaying circuit (4) having an input connected to an output of the means for generating a first electric impulse and an output which delivers the second electric impulse, said second electric impulse being a command signal of the switch (T2).

**OPERATING MECHANISM
FOR TRIPPING A VOLTAGE CIRCUIT BREAKER**

DESCRIPTION

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Technical field and prior art

The invention relates to an operating mechanism for tripping a voltage circuit-breaker and, more particularly, to an operating mechanism for tripping a high and medium voltage circuit-breaker.

The energy to trip a voltage circuit-breaker is stored either in a spring (spring-operated mechanism) or in a hydraulic tank (hydraulic-operated mechanism). The spring is held in its charged position using a latching-system, while the hydraulic tank is kept under pressure by a closed valve. To trip the circuit-breaker, the latching-system or the valve is opened either manually or by a magnetic force created by a current flowing through a coil, the current resulting from an electric impulse applied to the coil.

For some applications, the tripping time of the circuit-breaker has to be prolonged by several milliseconds to meet the requirements of the circuit-breaker.

According to the prior art, an additional mass is attached to the latching-system of the mechanism. Due to the inertia of the additional mass, the tripping-time is delayed.

The Figure 1 shows a latching-system according to the prior art. The additional mass is here a pendulum mass. The latching-system comprises a

magnetic solenoid to pick up the coil 1, a pendulum mass 2 and a damper for pendulum 3.

Such a mechanism has several drawbacks, i.e.:

- 5 - the system is position-dependent (the pendulum must be in vertical position to operate correctly, which presupposes that the mechanism must be fixed to the circuit-breaker in this unique position);
- the pendulum needs a lot of space,
10 enlarging therefore the size of the mechanism;
- the latching-system comprises several mechanical parts, increasing thereby the cost of the mounting and the adjusting of the system;
- the different mechanical parts which
15 constitute the latching-system are exposed to high accelerations and vibrations so that these parts can get loose and defective;
- the time-delay of the mechanical system is depending not only on its mass but also on the force
20 acting to its latch so that adjusting the energy of the mechanism leads to another force on the latch and thus to a change in time-delay;
- the mass of the pendulum rises quadratically to the delay time so that using
25 acceptable mass leads to a delay time limited to about 50 milliseconds.

The operating mechanism for tripping a voltage circuit-breaker of the invention does not have such drawbacks.

Presentation of the invention

The invention relates to an operating mechanism for tripping a circuit-breaker. The operating mechanism comprises a coil having a first terminal and a second terminal, means for generating a first electric impulse, and means for creating, from the first electric impulse, a second electric impulse delayed from the first electric impulse and applied between the first terminal and the second terminal of the coil. The means for creating the second electric impulse comprise a switch connected in series with the coil and a delaying circuit delivers the second electric impulse as a command signal to the switch.

According to the invention, the delaying circuit comprises a timer circuit having an input and an output, an integrating circuit connected at the input of the timer circuit and a driving circuit connected at the output of the timer circuit. The first electric impulse is applied at terminals of the integrating circuit, the logical level at the output of the timer circuit is changed as soon as the voltage at the input of the timer circuit connected to the integrating circuit reaches a trigger-level, and the driving circuit delivers the second electric impulse as a command signal to the switch as soon as the logical level at the output of the timer circuit changes when the voltage at the input of the timer circuit reaches the trigger-level.

The operating mechanism of the invention comprises an electronic component able to delay the

electric impulse applied to the coil by the time required.

According to a preferred embodiment of the invention, the electronic component able to delay the electric impulse is integrated with the coil in a same component.

The operating mechanism of the invention has several advantages, i.e.:

- it is independent of the position of the drive,

- adjusting the energy of the mechanism does not influence the delay-time,

- the operating-mechanism of the invention has less mechanical parts than the operating-mechanism of the prior art, which is much more reliable and cost saving,

- the repeatability of a same delay-time is much more better than the one of the prior art,

- according to the preferred embodiment of the invention, there is no supplementary space needed in the mechanism because the means to delay the impulse is integrated with a coil in a same component.

Brief description of the drawings

Other characteristics and advantages of the invention will become clearer upon reading a preferred embodiment of the invention made in reference to the attached figures, wherein:

- Figure 1 - already described - represents an operating mechanism for tripping a voltage circuit-breaker according to the prior art;

- Figure 2 represents a diagram of an operating mechanism for tripping a voltage circuit breaker according to the invention;
- Figure 3 represents the operating mechanism of the invention represented in Figure 2;
- Figure 4 represents an improvement of the example of operating mechanism represented in Figure 3.

In all the figures, the same references designate the same elements.

Detailed description of the invention

The Figure 2 represents a diagram of an operating mechanism for tripping a voltage circuit breaker according to the invention.

The operating mechanism comprises means for generating an electric impulse (not shown on the figure), means for delaying the electric impulse 4, T2 and a coil L. The means for delaying the electric impulse are a delaying circuit 4 and a switch T2.

The delaying circuit 4 has a first input terminal IN1 connected to a first output of the means for generating the electric impulse, a second input terminal IN2 connected to a second output of the means for generating the electric impulse and an output terminal K connected to the input command of the switch T2.

The coil L is in series with the switch T2. The switch T2 is OFF (open circuit) before the electric impulse is applied between the first terminal IN1 and the second terminal IN2.

When the electric impulse is applied between the terminals IN1 and IN2, the delaying circuit 4 is powered on. When powered on, the delaying circuit 4 comprises means able to output, on the output
5 terminal K, a pulse signal after a duration equal to the time-delay required. This pulse signal switches ON the switch T2 (short circuit) so that a magnetic force is created.

Figure 3 represents an exemplary embodiment
10 of the operating mechanism of the invention.

The operating mechanism comprises the resistors R1, R2, R3, R4, a timer circuit IC, a condenser C1, a diode D, a bipolar transistor T1 and the switch T2. The switch T2 is for example a field
15 effect transistor.

The coil L is in series with the transistor T2. The transistor T1 is in series with the resistors R3 and R4, a first terminal of the resistor R3 being connected to the emitter of the transistor T1 and a
20 first terminal of the resistor R4 being connected to the collector of the transistor T1. The collector of the transistor T1 is connected to the gate of the transistor T2, which gate is the input command of the switch. The second terminal of the resistance R3 is
25 connected to a first terminal of the coil L, the second terminal of which is connected to a first terminal of the switch T2, the second terminal of which is connected to the second terminal of the resistor R4. A first terminal of the resistor R2 is connected to a
30 first terminal of the condenser C1, the second terminal of which is connected to a first terminal of the

resistor R1. The second terminal of the resistor R2 is connected to the second terminal of the resistor R3 and the second terminal of the condenser C1 is connected to the second terminal of the resistor R4. The first
5 terminal of the resistor R1 is also connected to a first terminal of the diode D1, the second terminal of which is connected to the second terminal of the resistor R2. The diode D and the resistor R1 are connected to the timer circuit IC so as to stabilize
10 the supply-voltage of the timer circuit.

The main elements allowing to delay the electric impulse are the timer circuit IC, the condenser C1 and the resistor R2. The first terminal of the condenser C1 is connected to an input TR of the
15 timer-circuit IC. The gate of the transistor T1 is connected to an output Q of the timer circuit IC.

When the electrical impulse is applied between the terminals IN1 and IN2, the timer circuit IC is powered on and, as long as the voltage at the input
20 TR of the timer circuit is lower than a trigger-level, the output Q of the timer circuit IC stays at a logical level "high", keeping the transistor T1 closed. As soon as the trigger-level is reached at the input TR, the output Q turns to a logical level "low", opening
25 thereby the transistor T1. Thus, the gate of the transistor T2 gets charged and the transistor T2 conducts. The coil L is therefore supplied. The transistor T1, together with the resistors R3 and R4 are to drive the transistor T2 from the logical signal
30 output by the timer circuit IC.

It is therefore possible to set the time delay when an electric impulse is applied between the terminals of the coil.

Figure 4 represents an improvement of the example of means represented in Figure 3.

In addition to the elements represented in figure 3, the operating mechanism represented in Figure 4 comprises a rectifier B placed between the terminals IN1 and IN2. This rectifier makes advantageously the circuit independent of polarity and suitable for active current AC and direct current DC.

CLAIMS

1. Operating mechanism for tripping a circuit-breaker, the operating mechanism comprising a
5 coil (L) having a first terminal and a second terminal,
means for generating a first electric impulse, and
means for creating, from the first electric impulse, a
second electric impulse delayed from the first electric
impulse and applied between the first terminal and the
10 second terminal of the coil, characterized in that the
means for creating the second electric impulse comprise
a switch (T2) connected in series with the coil (L) and
a delaying circuit (4) which delivers the second
electric impulse as a command signal to the switch
15 (T2), wherein the delaying circuit (4) comprises a
timer circuit (IC) having an input (TR) and an output
(Q), an integrating circuit (R2, C1) connected at the
input (TR) of the timer circuit (IC) and a driver
circuit (R3, T1, R4) connected at the output (Q) of the
20 timer circuit, the first electric impulse being applied
at terminals of the integrating circuit, the logical
level at the output (Q) of the timer circuit being
changed as soon as the voltage at the input of the
timer circuit connected to the integrating circuit
25 reaches a trigger-level, and the driving circuit
delivering the second electric impulse as a command
signal to the switch (T2) as soon as the logical level
at the output of the timer circuit changes when the
voltage at the input of the timer circuit reaches the
30 trigger-level.

2. Operating mechanism according to claim 1, wherein the integrating circuit comprises a condenser (C1) at the terminals of which the first electric impulse is applied and the driving circuit 5 comprises a PNP transistor (T1) the gate of which is connected to the output of the timer circuit and the collector of which is connected to an input command of the switch (T2).

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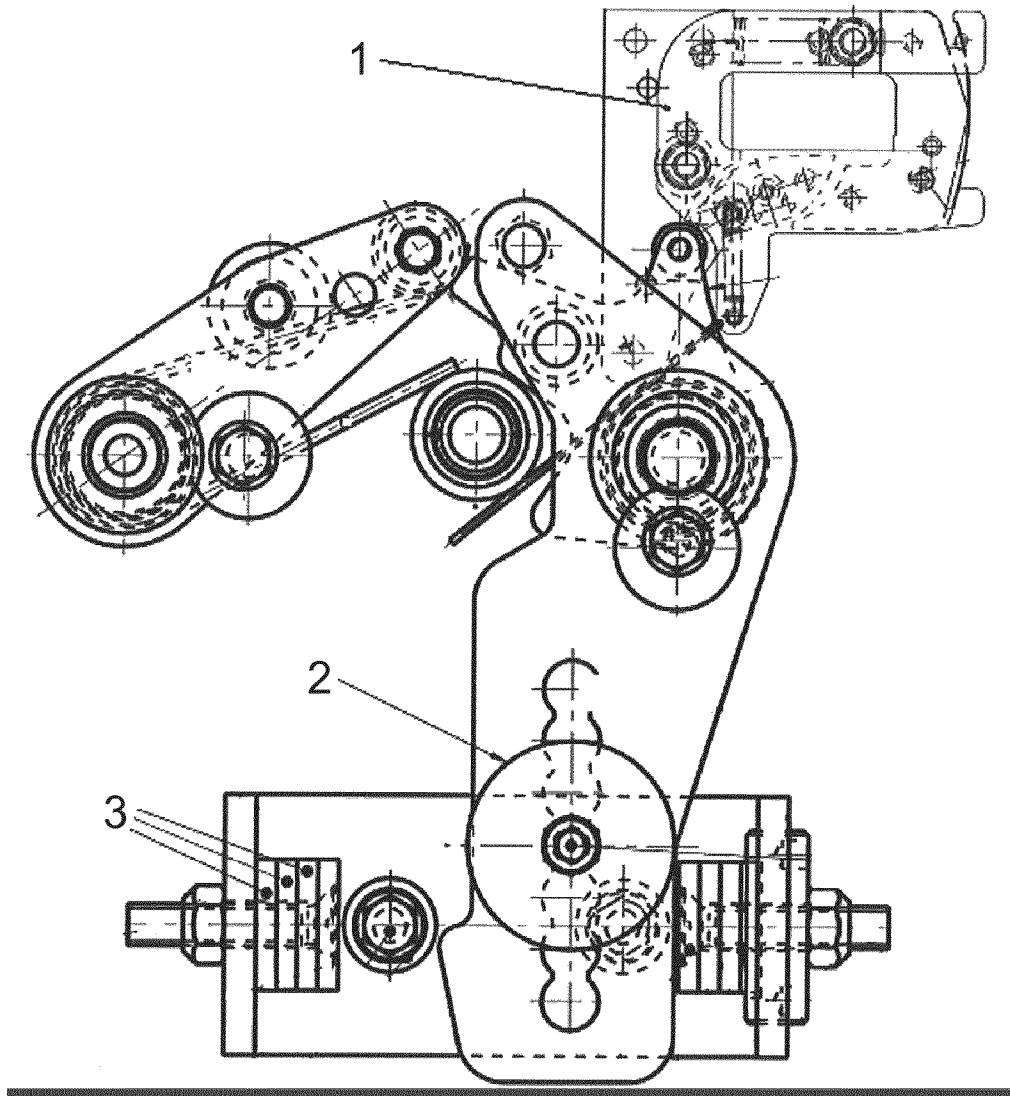


FIG.1

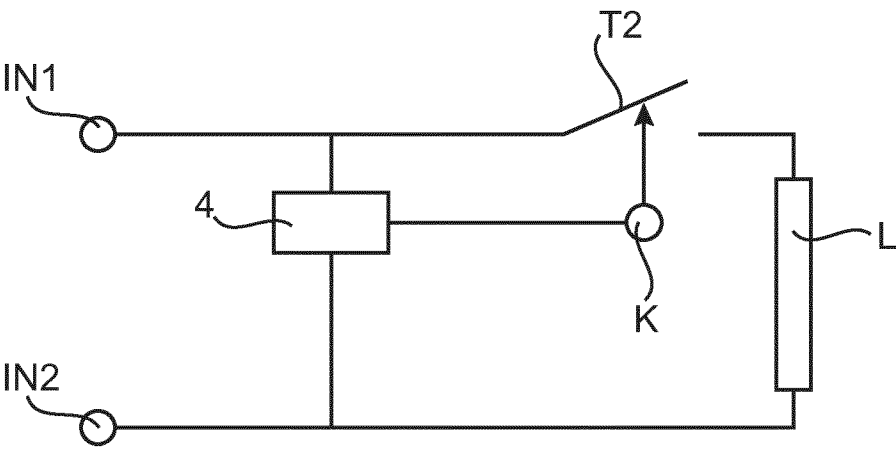


FIG.2

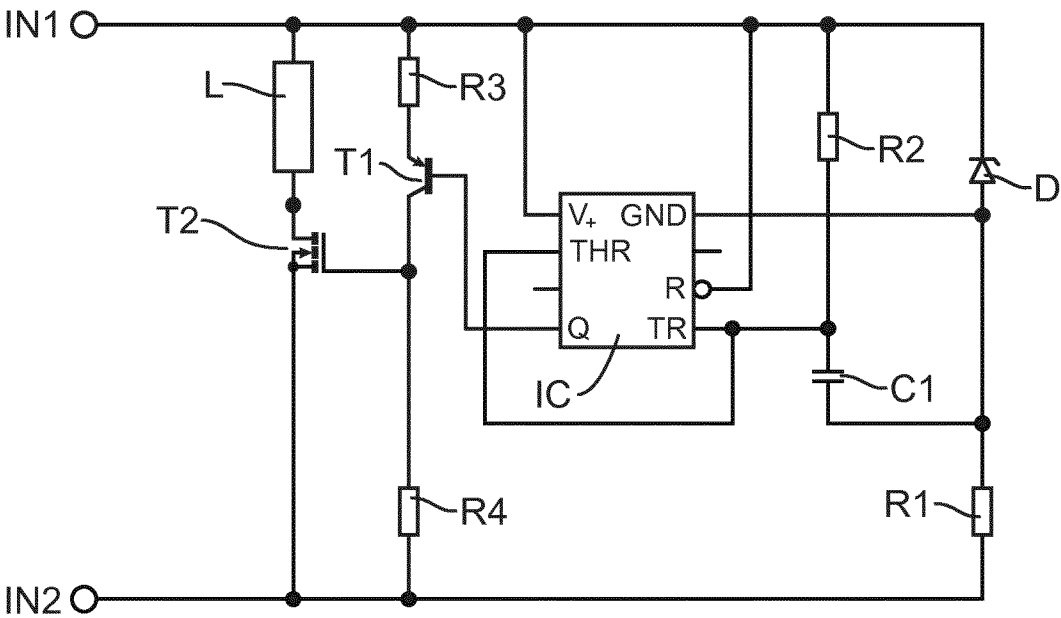


FIG.3

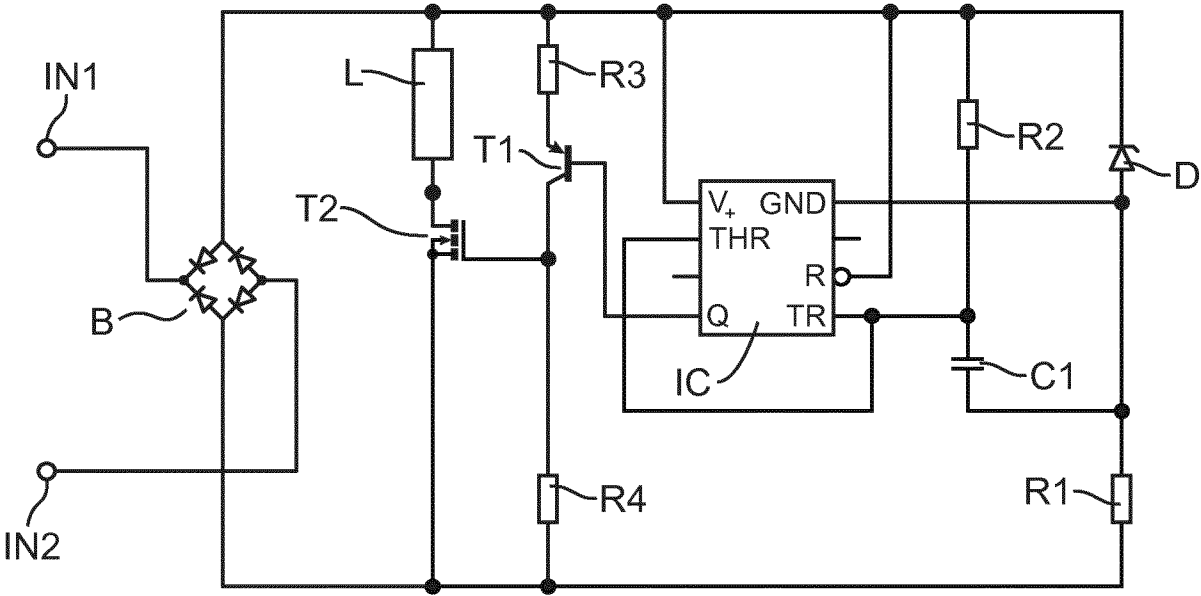


FIG.4

INTERNATIONAL SEARCH REPORT

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A. CLASSIFICATION OF SUBJECT MATTER
INV. H01H71/44 H01H3/30 H01H3/24 H02H3/093
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01H H02H

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 3 329 870 A (DE VINEY TERRENCE E ET AL) 4 July 1967 (1967-07-04) column 1, line 9 - column 7, line 25; figures 1-2 -----	1,2
X	EP 2 164 146 A2 (SIEMENS AG [DE]) 17 March 2010 (2010-03-17) paragraph [0030] - paragraph [0066]; figures 1-4 -----	1,2
A	WO 2010/102989 A1 (AREVA T & D SAS [FR]; BONJEAN MARC [FR]) 16 September 2010 (2010-09-16) page 8, line 25 - page 22, line 24; figures 1-8D -----	1,2



Further documents are listed in the continuation of Box C.



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INTERNATIONAL SEARCH REPORT

Information on patent family members

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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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