

- [54] APPARATUS FOR DISPLAYING LOWER CASE LETTERS**

- | | | | |
|-----------|--------|--------------------|------------|
| 3,130,397 | 4/1964 | Simmons..... | 340/324 AD |
| 3,500,327 | 3/1970 | Belcher et al..... | 340/154 |
| 3,568,178 | 3/1971 | Day..... | 340/324 AD |
| 3,783,331 | 1/1974 | Darnall | 315/18 |

- [75] Inventor: **Aaron J. Fishman**, Framingham,
Mass.

- Primary Examiner*—David L. Trafton
Attorney, Agent, or Firm—Cesari and McKenna

- [73] Assignee: **Digital Equipment Corporation,**
Maynard, Mass.

- [22] Filed: **Sept. 24, 1973**

- [21] Appl. No.: 400,168

- [57]
- ABSTRACT**

- [52] U.S. Cl..... 340/324 AD; 178/30; 315/22;
315/26

- [51] Int. Cl. G08b 5/36

- [58] **Field of Search** .. 340/324 A, 324 AD, 366 CA;
178/15, 30; 315/18, 21 PR, 21 CH, 26

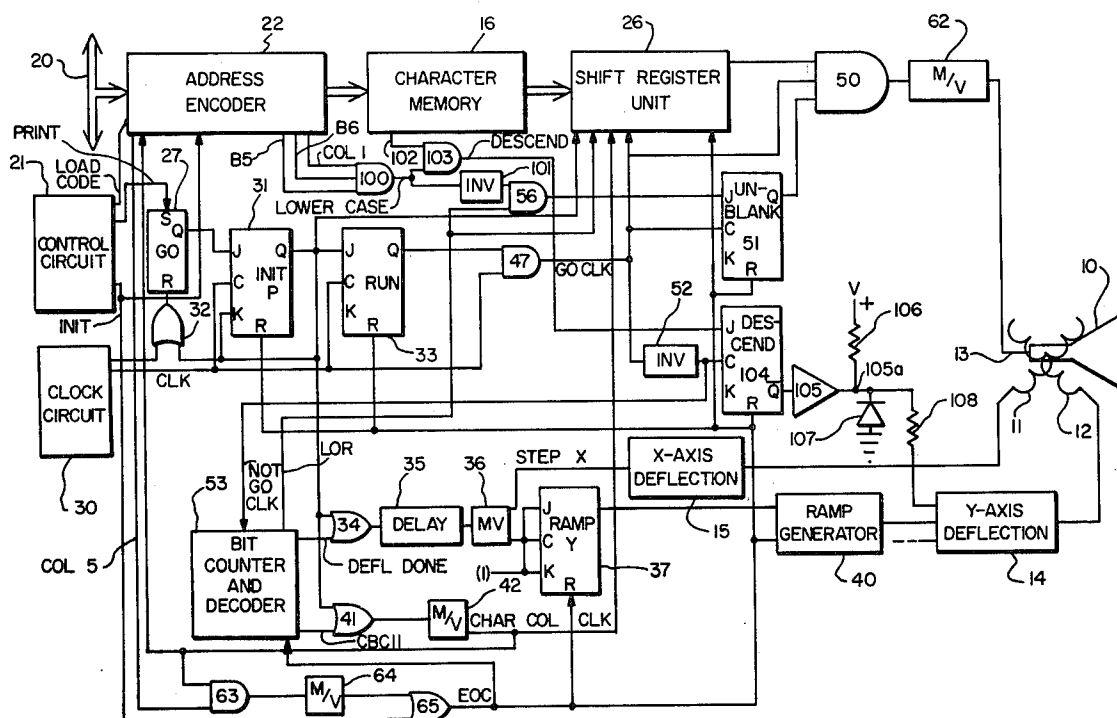
- Circuitry in a matrix display for shifting certain lower case letters downwardly. While a character generator receives information in one column of a matrix for a lower case character, the display of the character is blanked. One bit position in that column indicates whether the character is to be displaced downwardly on the line. Circuitry in the display monitors this bit position and alters the deflection signal to the Y deflection axis to produce the appropriate shift.

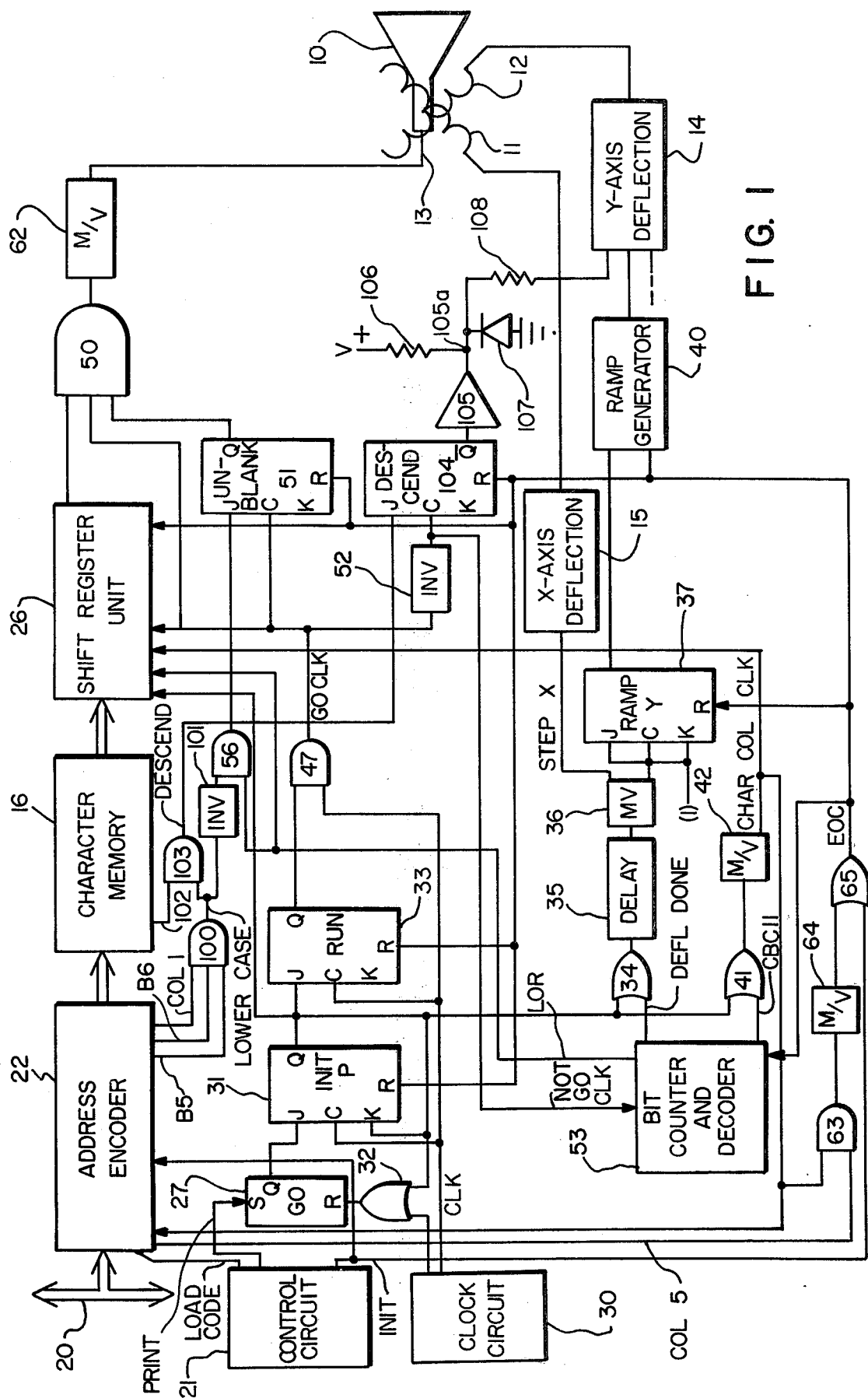
- [56]
- References Cited**

UNITED STATES PATENTS

- | | | | |
|-----------|--------|-------------------|------------|
| 2,987,715 | 6/1961 | Jones et al. | 340/324 AD |
|-----------|--------|-------------------|------------|

- ### 4 Claims, 4 Drawing Figures





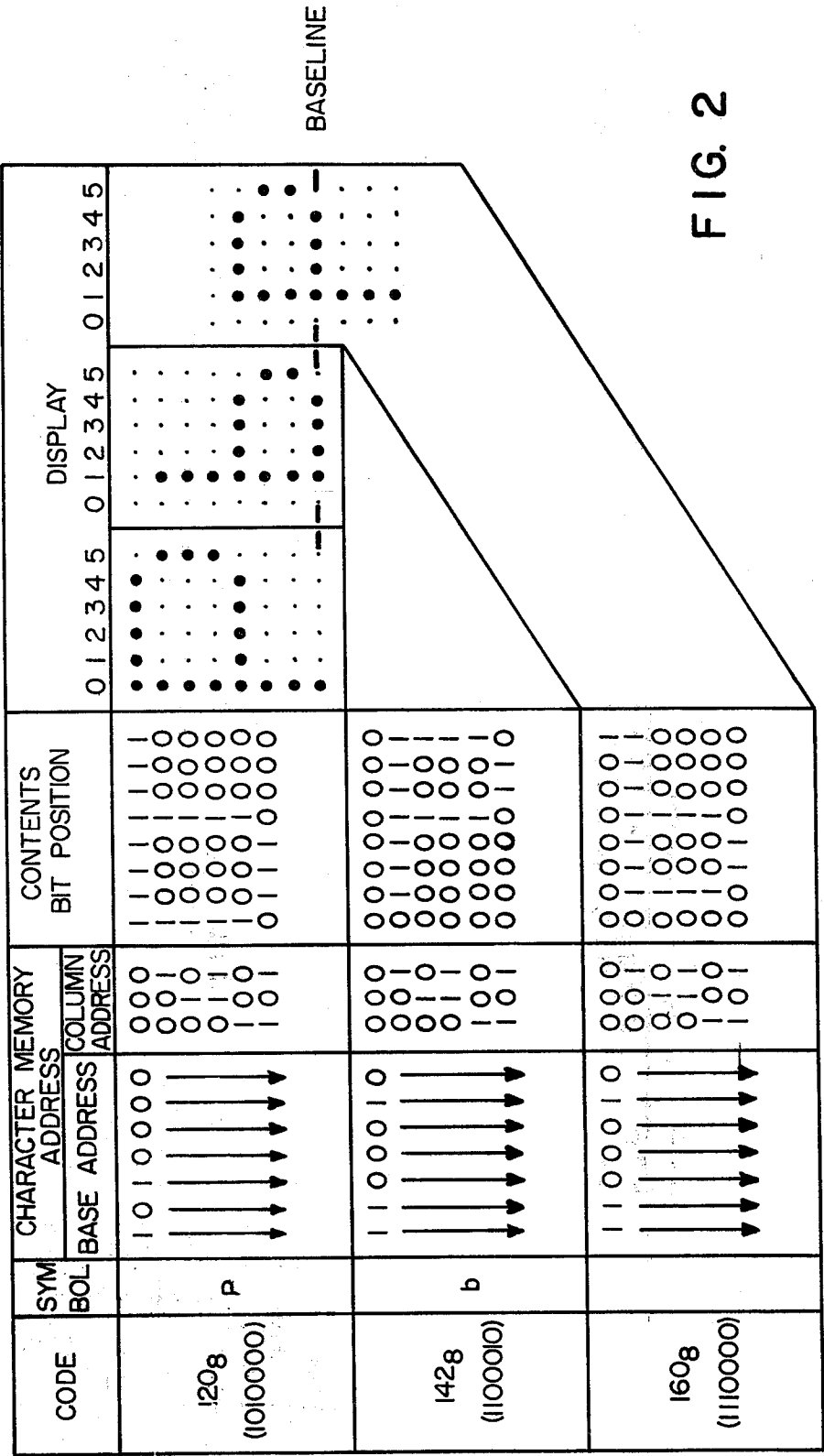


FIG. 2

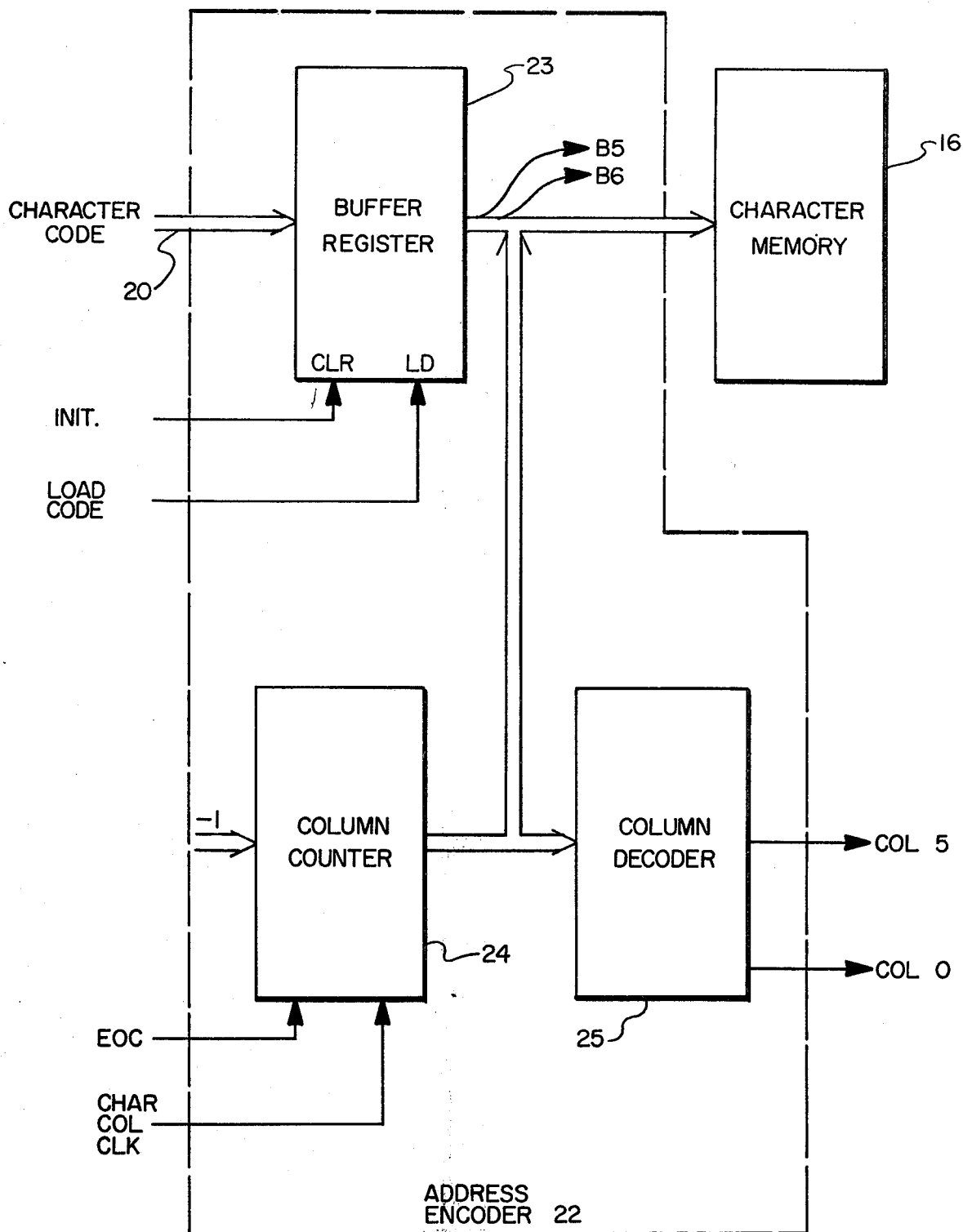


FIG. 3

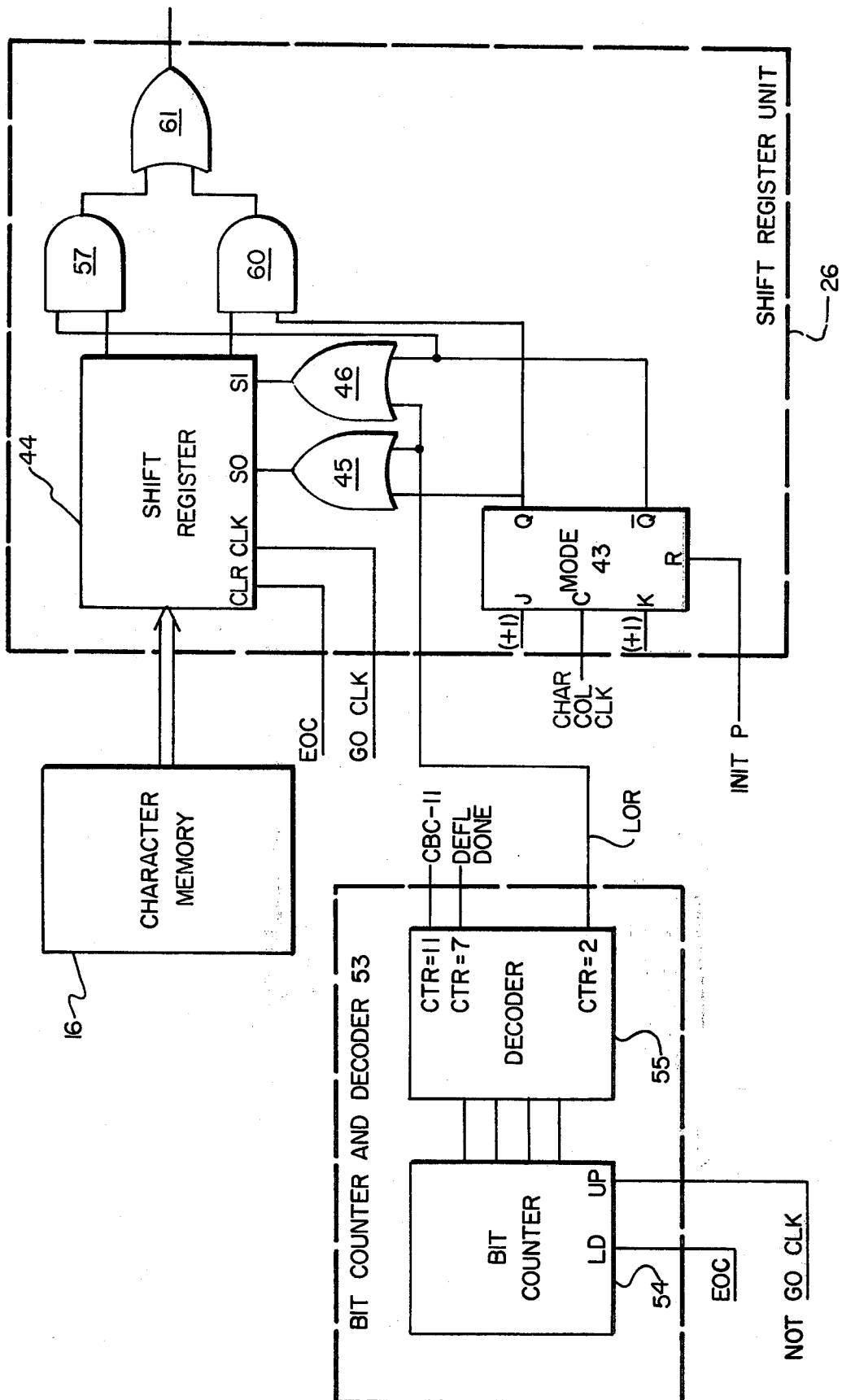


FIG. 4

APPARATUS FOR DISPLAYING LOWER CASE LETTERS

BACKGROUND OF THE INVENTION

This invention relates to character generators and more specifically to devices for displaying lower case letters.

One class of input/output devices used in data processing systems displays symbols. These include cathode ray tube devices and X-Y plotters. With some of these devices, a character memory stores information which controls the blanking of a beam in a cathode ray tube or the position of a pen. Effectively the "beam" or pen "draws" symbols by forming dots selectively on a matrix which X and Y axis deflection signals define.

Normally these devices have the capability of displaying capital letters which are stored in some arbitrary matrix form such as a 6 column by 8 row matrix. These systems "draw" a character with respect to a base line. All capital letters terminate on and extend above the base line. This is not the case when lower case letters are displayed, however. Certain letters, known as "descending characters," such as "g", "j", "p", "q", and "y", include portions or "tails" which do extend below the base line.

There are several ways to store information to assure the proper vertical alignment of descending characters. In one the storage matrix has additional rows so that the base line for the letters on the displayed character coincides with an intermediate row. Thus, the display matrix overlies the entire printing area.

In another approach special decoding networks are enabled during the transmission of a lower case character code. These decoders sense the code and then determine whether the character should descend. If it is, an offset circuit effectively shifts the matrix downwardly. Alternatively, a memory for storing display information has one extra bit position in a location corresponding to the top matrix row for each character. That position contains a ONE if the character is a descending character. Circuitry monitors this bit position and then produces the offset.

Each of these approaches adds circuit expense and complexity. The use of oversized matrices or special decoding networks adds memory or decoding circuit costs. There may be timing problems introduced by special character decoding steps. While the actual number of added bit positions in the last-mentioned approach using an extra bit position does not seem significant, the memory is normally a read-only memory. Additional decoding circuits are necessary to monitor this one position and may require the use of discrete components or inefficient utilization of standard components, especially integrated circuit components.

Thus, it is a primary object of this invention to provide a simple means for displaying lower case characters including descending characters and similar symbols.

Another object of this invention is to provide a device for displaying descending lower case characters without additional memory circuitry.

Still another object of this invention is to provide a system for displaying descending lower case characters without complex decoding circuits.

SUMMARY

In accordance with one aspect of our invention, dis-

play information for lower case characters does not use one column in a storage matrix for upper case characters. One bit position in that column indicates whether the lower case character is a descending character. The electron beam in a CRT device is blanked or a pen is raised during the analysis of this column. Circuitry decodes the one bit position. If the content indicates that the character is descending, the control circuitry introduces an offset into the vertical deflection circuit for the beam or pen and effectively shifts the character downwardly. Thus, there is no added expense for memory and, as becomes apparent, the circuitry for introducing the offset is quite simple to implement.

This invention is pointed out with particularity in the appended claims. The above and further objects and advantages of this invention may be attained by referring to the following description taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a logical diagram, partially in block form, of a cathode ray tube display device incorporating this invention;

FIG. 2 is a chart of representative symbol codes and corresponding information stored in a character memory shown in FIG. 1;

FIG. 3 is a detailed diagram of an address encoder shown in FIG. 1; and

FIG. 4 is a detailed diagram of a bit counter and decoder and a shift register unit shown in FIG. 1.

DESCRIPTION OF AN ILLUSTRATIVE EMBODIMENT

This invention is particularly suited for implementation in a class of output devices which position a printing element with respect to a matrix in an X-Y-plane and selectively enable a printing element. In an X-Y-pen plotter, X and Y-axis signals position a pen as the printing element. A Z-axis signal moves the pen between marking and non-marking positions. A cathode ray tube display device is another device in this class in which a beam is the printing element. The beam is "unblanked" to enable it to mark. FIG. 1 shows a control circuit for a cathode ray tube (CRT) 10. Modifications of the circuitry for use in pen plotters or for other types of matrix display devices will be apparent to those skilled in the art.

The CRT 10 includes an X-axis deflection coil 10 and a Y-axis deflection coil 12 to position an electron beam on the face of the CRT 10 in response to signals from a Y-axis deflection circuit 14 and an X-axis deflection circuit 15. When a Z-axis conductor 13 is energized (i.e. "unblanked"), the electron beam is turned on to illuminate a spot.

There are two basic ways to form symbols on the face of the CRT 10. This invention is particularly adapted for use with those defined as a matrix display. In a matrix display, the beam "moves" from one point to another on a matrix under the control of the deflection circuits 14 and 15, with the Z-axis signals on the conductor 13 being turned on momentarily anytime a position on the matrix is to be illuminated. A control circuit retrieves information from a character memory 16 to turn the beam on or off for each matrix position.

In accordance with standard practices, the matrix positions lie at the intersections of vertical columns and horizontal rows. It is assumed that the beam moves col-

umn by column; that is, the X-axis and Y-axis deflection coils 11 and 12 first position the beam to a first column of the matrix and then raise it through the column row-by-row. When the first column is completed, the control circuit energizes the coils 11 and 12 to shift the beam horizontally to the next column and to trace the second column downwardly. Thus the system "draws" the character by alternately moving up and down each successive column in the matrix. The number of rows and columns is arbitrary. In this specific disclosure, however, the matrix contains six columns and eight rows.

In a digital computer system or other system for supplying information to the display device, some code uniquely identifies each character or symbol. A popular code is the ASCII code. This code, in an octal representation, falls into four sets of code numbers, also expressed as octal numbers. Codes 0_8 through 37_8 designate control functions; codes 40_8 through 77_8 , special symbols and numerals; codes 100_8 through 137_8 , upper case characters and symbols; and codes 140_8 through 177_8 , lower case characters and symbols.

FIG. 2 shows the codes for three representative characters, namely "P," "b," and "p." There is a group of contiguous locations in the character memory 16 which identifies the positions on the matrix to be illuminated for each character. In the system shown in FIG. 1 the character memory 16 has one location corresponding to each column. Each location in the character memory 16, in turn, has one bit position corresponding to each row. Thus, with a six column by eight row matrix, the memory has six locations for each code number (i.e., for each character that may be displayed) and each location has eight bit positions.

In order to simplify retrieval from the character memory 16, the circuit shown in the FIG. 1 uses the ASCII code as a base address by effectively shifting the ASCII code one octal digit to the left. Hence, the first location for "P," which has an octal code of 120_8 , is $1,200_8$. Looking at that character in FIG. 2, location 1200_8 contains all ONE's. This means that the electron beam will energize spots on the face of the CRT 10 (in FIG. 1) corresponding to the intersections of all the rows with the left-hand column (column 0). The next address, 1201_8 contains ONE's in bit positions corresponding to rows 0 and 4. Therefore, the intersections with the column 1 of the topmost row (row 0) and row 4 are illuminated. Corresponding intersections are also illuminated in the columns 2 through 4 as locations 1202_8 through 1204_8 store identical information. Location 1205_8 corresponds to column 5 and has ONE's in bit positions 1 through 3 so the beam illuminates corresponding matrix positions. Once all these dots are displayed, the character "P" appears on the face of the CRT 10 (in FIG. 1).

In FIG. 2 the intersections are widely spaced for purposes of illustration. Actually the intersections are more closely spaced so that the dots apparently merge into continuous character lines.

When lower case letters are displayed, it is not necessary to use column 0 or row 0 with the normal letters such as the "b." With this approach the lower case letters are displayed on a "5×7" sub-matrix of the previously described 6×8 matrix as shown in FIG. 2. This reduction in matrix size proportions the relative character sizes for upper and lower case letters. As no information for display purposes appears in the first column,

location 1420_8 , which corresponds to the first column of the matrix, contains ZERO's for the letter "b." The remaining rows contain ONE's corresponding to various intersections in the matrix as previously discussed.

Now referring to FIG. 1, and still using these specific examples and codes, the character code appears on a bus 20. A control circuit 21 responds to other signals, as known in the art, to transmit a LOAD CODE signal to move the character code from the bus 20 into an address encoder 22. The address encoder 22 serves as a gated input buffer to store the character code and provide address information to the character memory 16.

Now referring to FIG. 1 and to FIG. 3, which shows the address encoder 22 in more detail, the LOAD CODE signal energizes the LD input of a buffer register 23 to store the character code. This code provides the three most significant digits of a four-digit address expressed in the octal notation. The address is for a specific location in the character memory 16. The remaining, or least significant, octal digit is provided by a column counter 24. A column decoder 25 produces signals on conductors corresponding to the respective columns in a matrix, conductors for the left column (col 0) and last or right column (col 5) being shown in FIG. 3. The column counter 24 normally receives a "−1" as an initial value. This corresponds to 7_8 and there are no locations in the character memory 16 with a least significant address digit of 7_8 . As a result, the signals at the input to the character memory 16 initially have no meaning so no data appears at the output of the character memory 16, which is an input to a shift register unit 26 (FIG. 1).

Now referring to FIG. 1, the control circuit 21 transmits a PRINT signal after the LOAD CODE signal. The PRINT signal sets a GO latch 27 and conditions a JK flip-flop designated an INIT P flip-flop 31. A subsequent CLK pulse from a clock circuit 30 to the "C" input of the flip-flop 31 sets this flip-flop. When the INIT P flip-flop 31 sets, its output, an INIT P signal, passes through an OR GATE 32 to immediately reset the GO latch 27. The J input of another JK flip-flop designated a RUN flip-flop 33 also receives the INIT P signal so a succeeding or second CLK pulse can set the RUN flip-flop 33. The INIT P signal also sets the shift register unit 26 to some initial conditions as described later. An OR circuit 34 transfers the INIT P signal to a delay circuit 35 and the delayed INIT P signal triggers a monostable multivibrator 36. The leading edge of the output pulse from the multivibrator 36 is applied to the X-axis deflection circuit 15 to effectively move the beam position one column to the right to provide one column of spacing between characters.

The trailing edge of the same pulse is an input to a JK or RAMP Y flip-flop 37 which controls the ramp slope from a ramp generator 40. As both the J and K inputs are energized, each pulse merely changes the state of the flip-flop 37. When the RAMP Y flip-flop 37 is set, it adds a signal corresponding to a slope of $+2m$ to a normal slope of $-m$ from the ramp generator 40. Thus, the Y-axis deflection circuit 14 receives a signal with a slope of $+m$ when the RAMP Y flip-flop 37 is set and a signal with a slope of $-m$ when the RAMP Y flip-flop 37 is reset.

The timing provides by the delay circuit 35 and the monostable multivibrator 36 are related to the output from the shift register unit 26 so the beam is at a base line and under the control of a positive slope signal

from the ramp generator 40 when the first bit of matrix information is received from the shift register unit 26.

Setting the INIT P flip-flop 31 also energizes an OR gate 41. This triggers another monostable multivibrator 42 to produce a CHAR COL CLK signal which passes to the address encoder 22 to increment the column counter 24 (FIG. 3). As the column counter 24 is initially set to -1, the CHAR COL CLK signal increments the column counter 24 to 0_H so the address encoder 22 thereupon produces a valid memory address. For example, the ASCII code for "P" produces initially the invalid address 1207_H. The CHAR COL CLK pulse changes this to 1200_H and the character memory 16 retrieves the data in that valid location.

Now referring to FIGS. 1 and 4, the shift register unit 26 contains a shift register 44 which shifts data in response to a GO CLK signal in a direction determined by signals at S0 and S1 inputs. A mode flip-flop 43 provides these direction inputs. The set (Q) and reset ($\bar{Q}$) outputs from the MODE flip-flop 43 are coupled to the S0 and S1 inputs respectively through OR gates 45 and 46.

When neither the S0 nor S1 signal is asserted, the shift register 44 inhibits the CLK input, so no shifting occurs. When the S0 input is asserted but the S1 input is not, GO CLK pulses shift the data to the right. Reversing the signals to the S0 and S1 inputs produces shifts to the left. When both S0 and S1 signals are asserted, the shift register 44 loads data in parallel from the character memory 16.

When the INIT P flip-flop 31 sets, it resets the MODE flip-flop 43 as the INIT P signal is an overriding resetting signal. However, no GO CLK pulses appear so no shifting operation occurs. Further, the shift register 44 contains all ZERO's because an EOC signal (described later) previously cleared the shift register 44.

Now referring to FIG. 1, the second CLK pulse from the clock 30 sets the RUN flip-flop 33. This enables an AND gate 47 to pass subsequent CLK pulses from the clock 30 as GO CLK pulses. The first GO CLK pulse to the shift register unit 26 produces no response. The shift register 44 (FIG. 4) was previously cleared and contains all ZERO's. An AND gate 50 which receives the output from the shift register unit 26 in FIG. 1 is also disabled by a signal from an UNBLANK flip-flop 51 which was previously reset.

The GO CLK pulses also are applied through an inverter 52 to a bit counter and decoder 53 as phased clock pulses delayed by 180° (i.e., NOT GO CLK pulses). Referring again to FIG. 4, a bit counter 54 is advanced by the phased NOT GO CLK pulses. The bit counter 54 is preset to a number (for example, 12 in a modulo 16 counter) to provide time delay and synchronizing functions in conjunction with the delay circuit 35 and monostable multivibrator 36 in FIG. 1. Still referring to FIG. 4, the output of the bit counter 54 is connected to a decoder 55. There are three outputs from the decoder 55 which are important for the understanding of this invention: an LOR signal, a DEFL DONE signal and a CBC-11 signal. The LOR signal appears when the bit counter 54 reaches a value "2" and performs two functions. First, it energizes both the OR gates 45 and 46 to load the first column information from the character memory 16 into the shift register 44 on its trailing edge. This LOR signal also energizes a normally enabled AND gate 56 (FIG. 1) so that a succeeding GO CLK pulse may set the UNBLANK flop-

flop 51 to thereby enable the AND gate 50. Conditions for disabling the AND gate 56 are discussed later.

Successive pulses from the clock circuit 30 continue to pass through the AND gate 47 in FIG. 1, as the RUN flip-flop 33 remains set even when the INIT P flip-flop 31 resets. As previously indicated the shift register 44 (FIG. 4) can shift in either direction. As both the J and K inputs to the flip-flop 43 receive ONE signals, successive CHAR COL CLK pulse from the pulses to the C input merely reverse the state of the flip-flop. Thus, the first pulse from the multivibrator 42 in FIG. 1 will have set the MODE flip-flop 43 in FIG. 1 so the S0 signal will be high while the S1 signal is low. Hence the GO CLK pulse after the LOR signal shifts the contents in the register 44 one place to the right.

The MODE flip-flop 43 also controls an output gating circuit. When set, the MODE flip-flop 43 disables an AND gate 57 and enables an AND gate 60 to pass signals from the right-hand end of the register 44 through an OR gate 61 to the AND gate 50 in FIG. 1. During the next column, the MODE flip-flop 43 is reset, so the shift register 44 shifts to the left with the output coming through the AND gate 57 connected to the left-hand end of the register 44 and OR gate 61.

If a bit from the shift register unit 26 in FIG. 1 is a ONE and the UNBLANK flip-flop 51 is set, then a GO CLK pulse passes through the AND gate 50 and triggers a monostable multivibrator 62. The resulting pulse energizes the Z-axis thereby causing a dot to appear. The GO CLK pulse and Y-axis conductor 13 ramping signal are synchronized so that pulses from the monostable multivibrator 62 correspond to the proper row intersections with the column.

Still referring to FIGS. 1 and 4, successive GO CLK pulses advance the bit counter 54. When the bit counter 54 reaches "7_H" (i.e., when the beam is at the row 4) the decoder 55 issues the DEFL DONE signal which energizes the OR gate 34. Actually this signal indicates that the deflection is about to be finished; the subsequent time delays provided by the delay circuit 35 and the monostable multivibrator 36 prevent the column shift and ramp signal reversal from occurring prematurely. When those two circuits time out, the multivibrator 36 issues a STEP X pulse and causes the X-axis deflection circuit 15 to shift the beam position to the next column and, by changing the state of the RAMP Y flip-flop 37, starts the subsequent ramp with a signal of the opposite slope.

Any column is finally drawn when the decoder 55 in FIG. 4 produces the CBC-11 signal. The signal passes through the OR gate 41 in FIG. 1 and enables the monostable multivibrator 42 to produce the CHAR COL CLK pulse. As previously indicated this pulse advances the column counter 24 (FIG. 3) and reverses the MODE flip-flop 43 in FIG. 4.

As previously described, the address encoder 22 transmits the COL 5 signal while the last column in the matrix is being displayed. This signal enables an AND gate 63 in FIG. 1. When the column ends, the CHAR COL CLK pulse advances the column counter 24 to an invalid address and also energizes the AND gate 63 thereby triggering a monostable multivibrator 64 and energizing an OR gate 65 to produce an end of character (EOC) pulse. The EOC pulse clears the shift register 44 (FIG. 4) and loads the preset number into the bit counter 54. The EOC pulse also resets the UNBLANK flip-flop 51, the RUN flip-flop 33, and the RAMP Y

flip-flop 37. Such an EOC pulse resets the INIT P flip-flop 33 directly.

As the DEFL DONE signal will already have been transmitted, the multivibrator 36 deflects the beam one column to the right. Thus, adjacent characters are automatically spaced by to columns as the first CHAR COL CLK pulse for the next character also produces a shift of the beam one column to the right, as previously indicated. The EOC may also be generated whenever the control circuit 21 produces an INIT or initializing signal. The INIT signal also clears the buffer register 23 (FIG. 3).

As previously indicated, ASCII codes for lower case letters and other symbols which can be displayed on a submatrix fall into the range 140₈ to 177₈. Hence the ASCII codes for these letters always contain ONE's in bit positions 5 and 6 of the binary character code, where the least significant bit function is position 0. As specifically shown in FIG. 3, the buffer register 23 contains B5 and B6 conductors connected to its corresponding stages. Both the B5 and B6 conductors are therefore energized whenever a lower case letter is being displayed.

Now referring to FIG. 1, and AND circuit 100 is connected to the B5 and B6 conductors and additionally to the COL 1 conductor from the column decoder 24 in FIG. 3. Thus, the AND circuit 100 is energized whenever the address encoder 22 is addressing a location corresponding to the first column of a lower case letter. As previously indicated, however, no display information appears in this column. Thus, the AND circuit 100 disables the AND gate 56 through an inverter 101 to thereby prevent the UNBLANK flip-flop 51 from setting. This prevents any signal from appearing on the Z-axis conductor 13, so no display can occur.

Now referring to FIG. 2, the character "b" contains all zeros at location 1420₈. But location 1600₈ for "p" contains a ONE in bit position 7. This bit position indicates that the letter is to descend by a fixed amount so that the tail of the "p" extends below the base line. Within the character memory 16 the bits are stored as if the character were to be printed with the bottom of the tail resting on the base line. This simplifies the structure of the memory and eliminates the need for any additional memory locations corresponding to rows below the base line.

Conductor 102 in FIG. 1 connects to the stage in the character memory 16 corresponding to bit position 7. A ONE signal on conductor 102 together with the output from the AND gate 100 energizes an AND gate 103 whenever a lower case letter includes a portion below the base line. The output of the AND gate 103 energizes the J input of a DESCEND flip-flop 104 and a phased NOT GO CLK pulse from the inverter 52 sets the DESCEND flip-flop 104.

When reset, the DESCEND flip-flop 104 energizes an amplifier 105 to thereby maintain a junction 105a of a voltage divider comprising a resistor 106 and a voltage reference 107 at a fixed positive level. A resistor 108 then couples a fixed current increment from the junction to a current summing junction in the Y-axis deflection circuit 14. This increment and the output of the ramp generator 40 are added so that normally the row 7 in the memory corresponds to the base line in the display matrix.

When a descending character is encountered, however, the DESCEND flip-flop 104 is set and the ampli-

fier 105 effectively grounds the junction 105a, thereby removing this incremental current from the Y-axis deflection circuit 14. As a result, the beam is effectively deflected downwardly for the character. The DESCEND flip-flop 104 remains set throughout the character, after which the EOC signal resets it.

A signal appears on the conductor 102 very shortly after the address encoder 22 provides an address for the memory 16. This provides sufficient time for the analog circuits to settle before the first column of data information (i.e., for the second column) is received as the circuit in FIG. 1 processes the first column in the normal manner except for the blanking operation.

Thus, the circuitry in accordance with this invention provides a means for displaying lower case letters which simplifies the structure of the character memory 16. The added circuitry for repositioning characters is inexpensive and simply added.

As apparent, this description of an illustrative embodiment is of only one embodiment. The application of this invention, however, to other types of display devices which use X and Y positioning signals and a blanking signal to control printing on a matrix will be apparent to those of ordinary skill in the art. Similarly, modification to accommodate matrices of different sizes, different sources of data and different timing sequences will also be apparent. Thus, it is the object of the appended claims to cover all such variations and modifications as fall within the true spirit and scope of the claims.

What is claimed as new and desired to be secured by Letters Patent of the United States is:

1. In a matrix display device for displaying symbols in response to representations of those symbols, each symbol being in a first or second class, symbols in the first class being displayed in all the columns of a matrix and symbols in the second class being displayed in a submatrix which omits one column in the matrix, a display unit having a printing element, X and Y axis deflection circuits for positioning the printing element on the matrix and an unblanking circuit for enabling the printing element to make a visible mark, matrix storage means for storing unblanking information for each symbol at a set of addressed locations, each location storing unblanking information corresponding to a column of the matrix, and means responsive to the representation of a symbol for selecting locations in the matrix storage means for retrieving unblanking information, the improvement of control means for the display device comprising:

- A. means for generating a base signal to thereby energize the Y-axis deflection circuit to position the printing element with respect to a base position on the Y-axis,
- B. means for receiving certain unblanking information for the location in the matrix storage means corresponding to the omitted column in the second class of symbols to control the generation of an offset signal,
- C. means responsive to the receipt of the representations of symbols in the second class for disabling the unblanking circuit during the receipt of the certain unblanking information in the omitted column, and
- D. summing means connected to the Y axis deflection circuit and offset signal generating means for combining the offset and base signals thereby to

9

control the vertical position of symbols in the second class in response to said offset signal.

2. A display device as recited in claim 1 wherein the second class of symbols includes lower case characters and the omitted column is the first column, said unblanking circuit disabling means being energized whenever the selecting means addresses a location corresponding to the first column of a lower case character and said offset signal generator being responsive to the content of a predetermined bit position in the first column.

10

3. A display device as recited in claim 2 wherein said offset signal generator is normally enabled, the appearance of a ONE in the predetermined bit position turning off said offset signal generator to thereby lower the character with respect to the base position.

4. A display device as recited in claim 3 additionally comprising means for generating a resetting signal at the end of each character display to reset said offset signal generator.

* * * * *

15

20

25

30

35

40

45

50

55

60

65

UNITED STATES PATENT OFFICE
CERTIFICATE OF CORRECTION

Patent No. 3,877,007 Dated April 8, 1975

Inventor(s) Aaron J. Fishman

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

Column 6, line 29, after "Z-axis" insert --conductor 13--

Column 6, line 30, after "Y-axis" delete "conductor 13"

Column 9, line 7, "ver" should be "ever"

Signed and Sealed this

twentieth Day of April 1976

[SEAL]

Attest:

RUTH C. MASON
Attesting Officer

C. MARSHALL DANN
Commissioner of Patents and Trademarks

UNITED STATES PATENT OFFICE
CERTIFICATE OF CORRECTION

Patent No. 3,877,007 Dated April 8, 1975

Inventor(s) Aaron J. Fishman

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

Column 6, line 29, after "Z-axis" insert --conductor 13--

Column 6, line 30, after "Y-axis" delete "conductor 13"

Column 9, line 7, "ver" should be "ever"

Signed and Sealed this

twentieth Day of April 1976

[SEAL]

Attest:

RUTH C. MASON
Attesting Officer

C. MARSHALL DANN
Commissioner of Patents and Trademarks