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H3P PPMP

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(56) Documents Cited

None

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UK CL (Edition Q) H3P PPMP

INT CL⁶ G09G 3/36, G11C 19/28, H03K 5/15

(54) Abstract Title

Static clock pulse generator for LCD

(57) A static clock pulse generator comprises a cascaded series of RS bistables 3 and gating circuits 4, wherein the RS bistable 3 in each stage 1,2 controls the gating circuit 4 in each stage to supply a clock pulse from the clock input CK to the output of the stage. The bistable 3 is set by the clock pulse output from the previous stage and is reset by a pulse from the succeeding or next-but-one stage. Pulse outputs may be obtained from the bistable output or the gating circuit output, and the pulse outputs may be overlapping or non-overlapping. A delay may be inserted between stages. The clock input may be single phase or two phase, and the circuit may be reversible. The gating circuit may comprise a differential amplifier or a level shifter to allow use of low level clock signals.

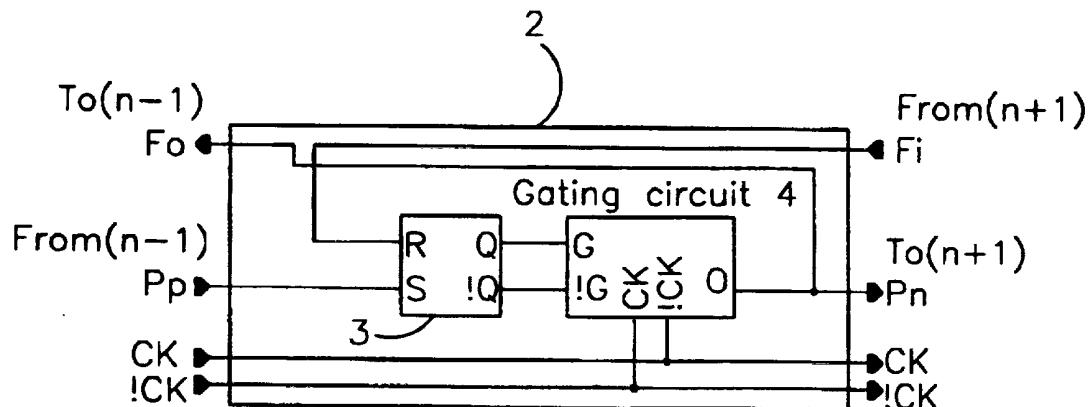


FIG 4

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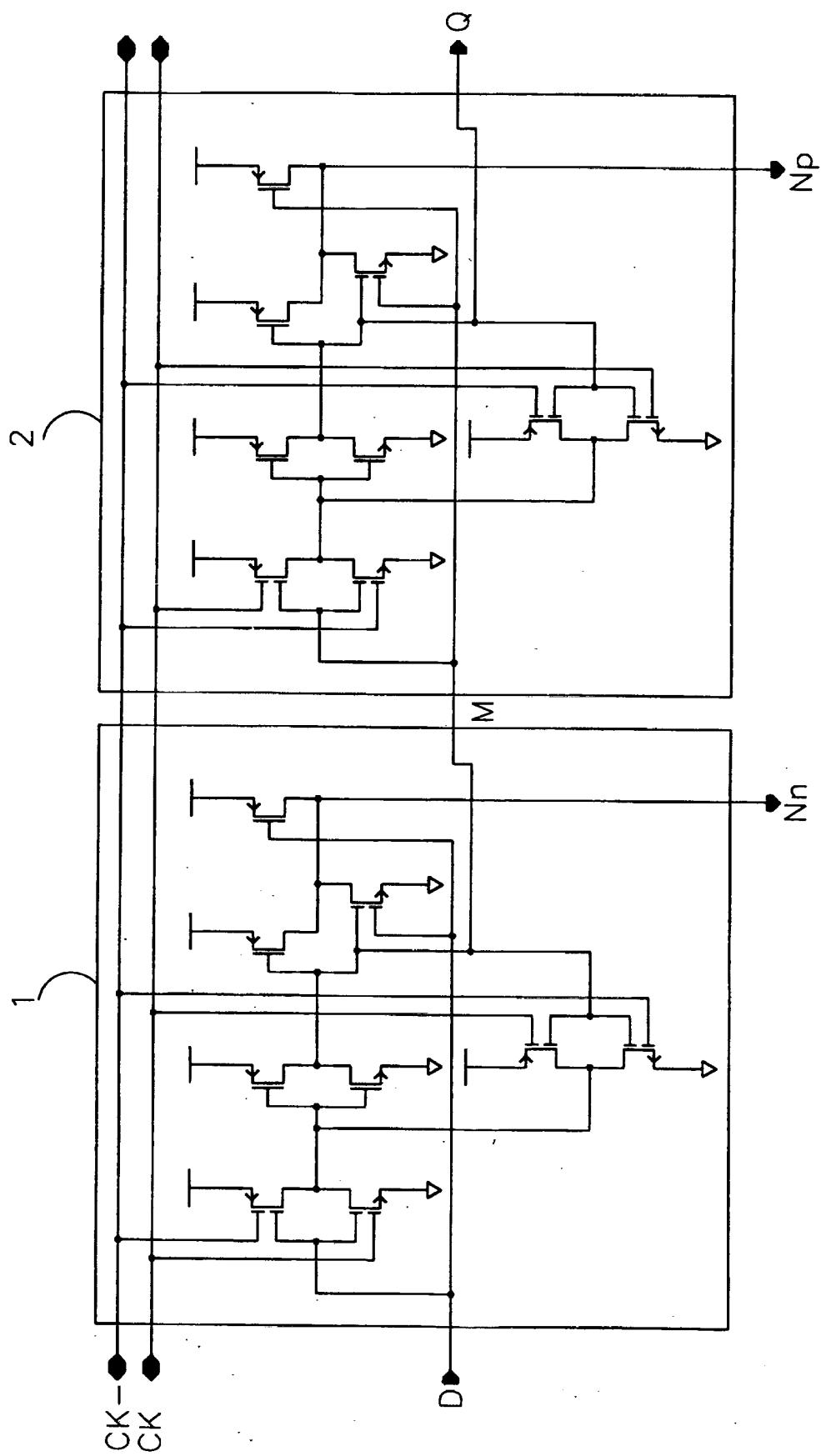


FIG 1

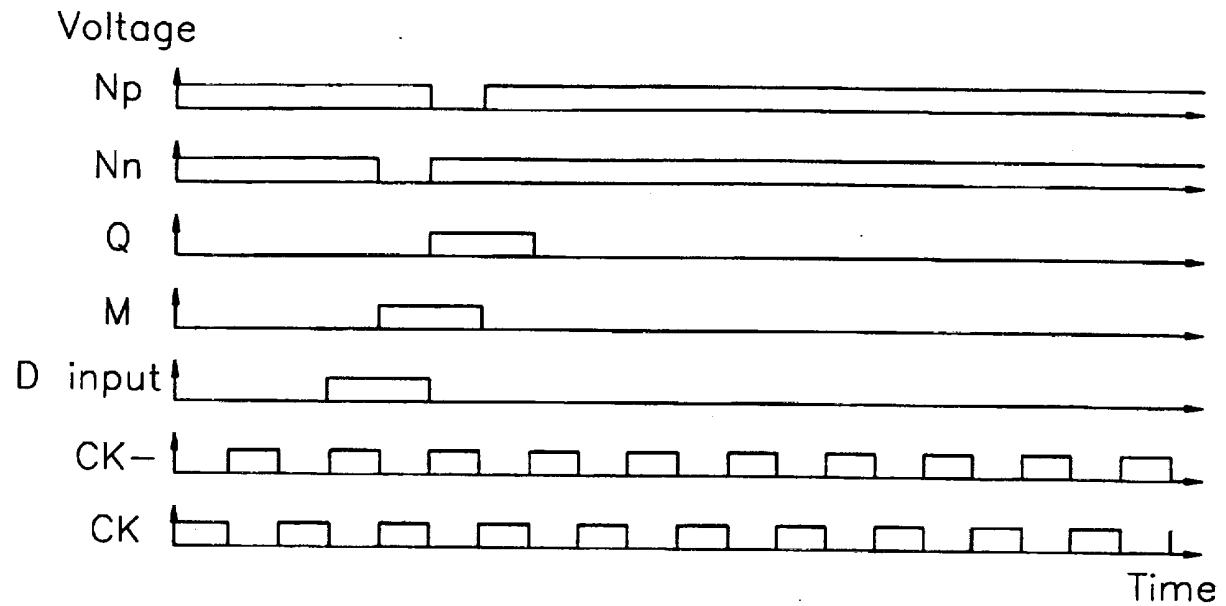


FIG 2

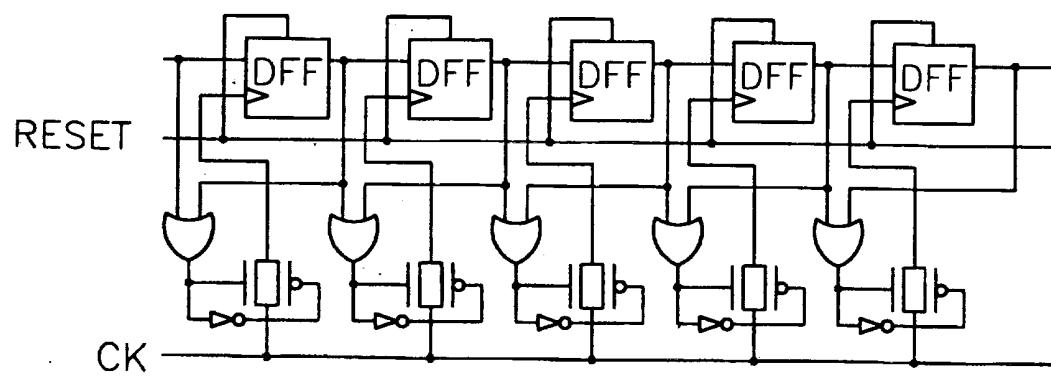


FIG 3

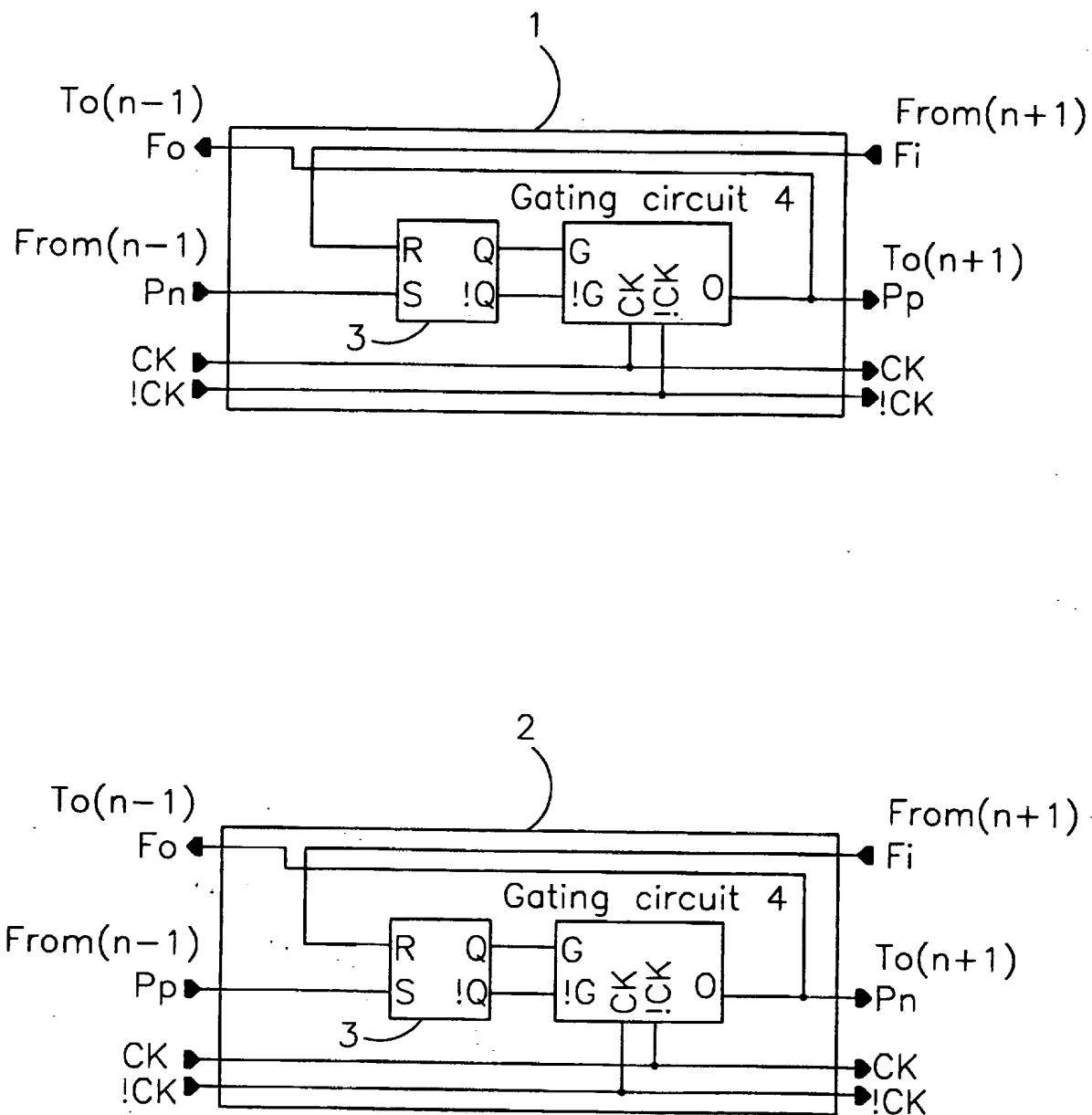
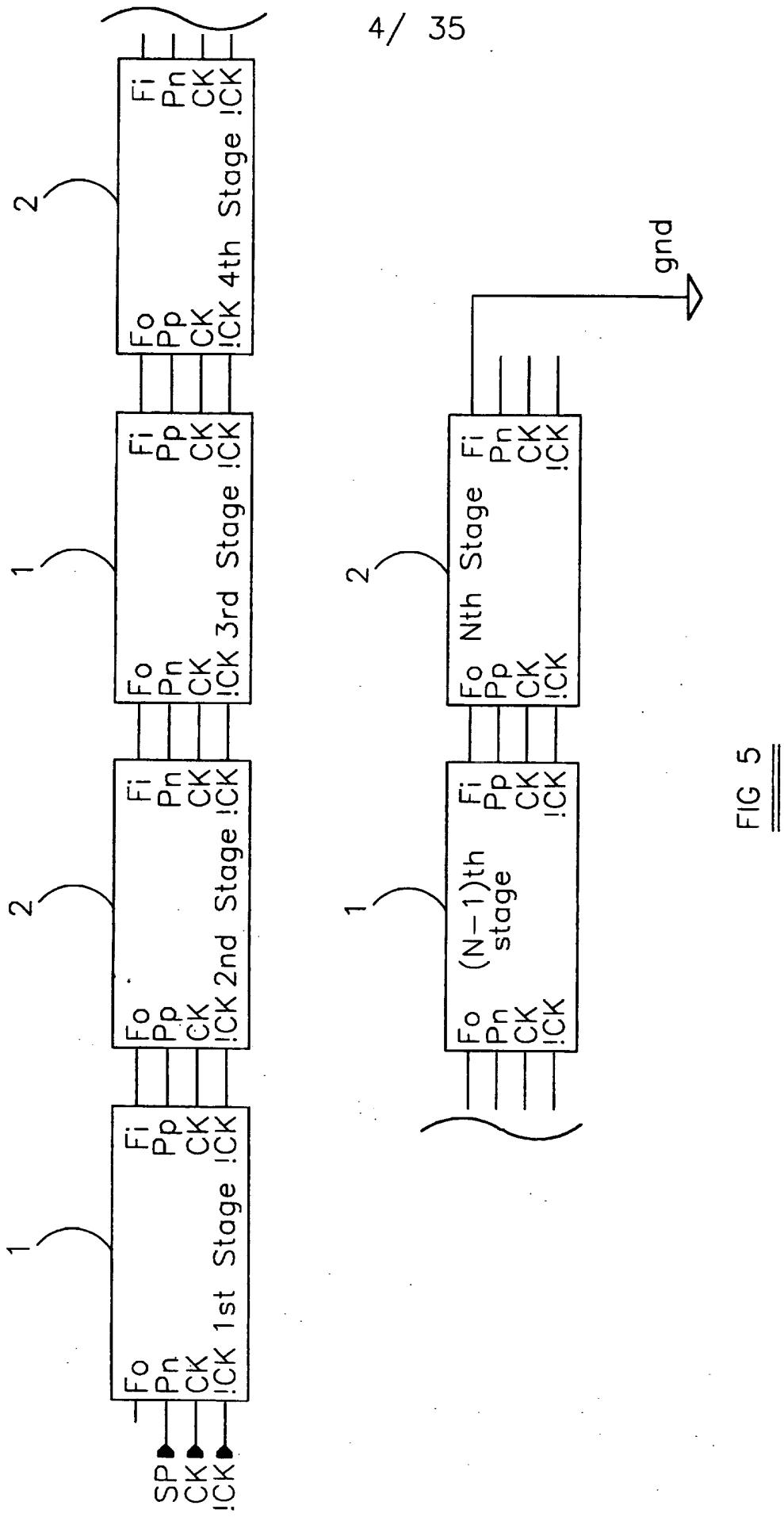


FIG 4



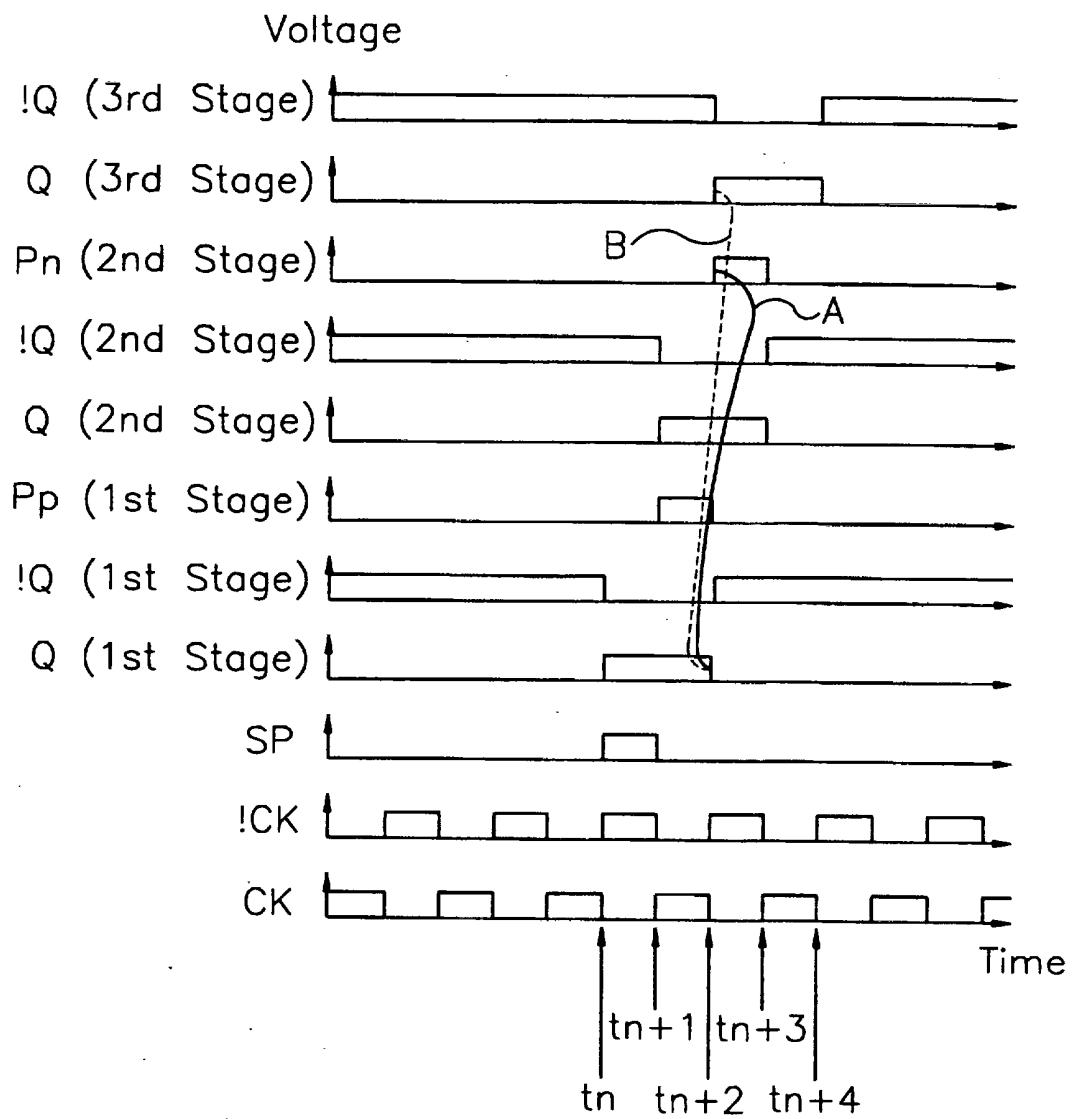


FIG 6

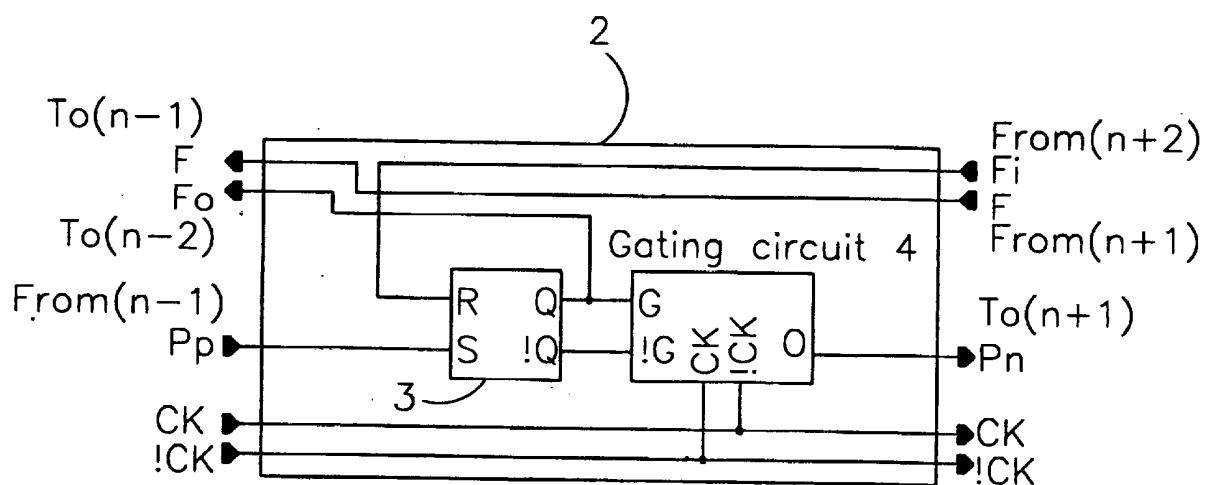
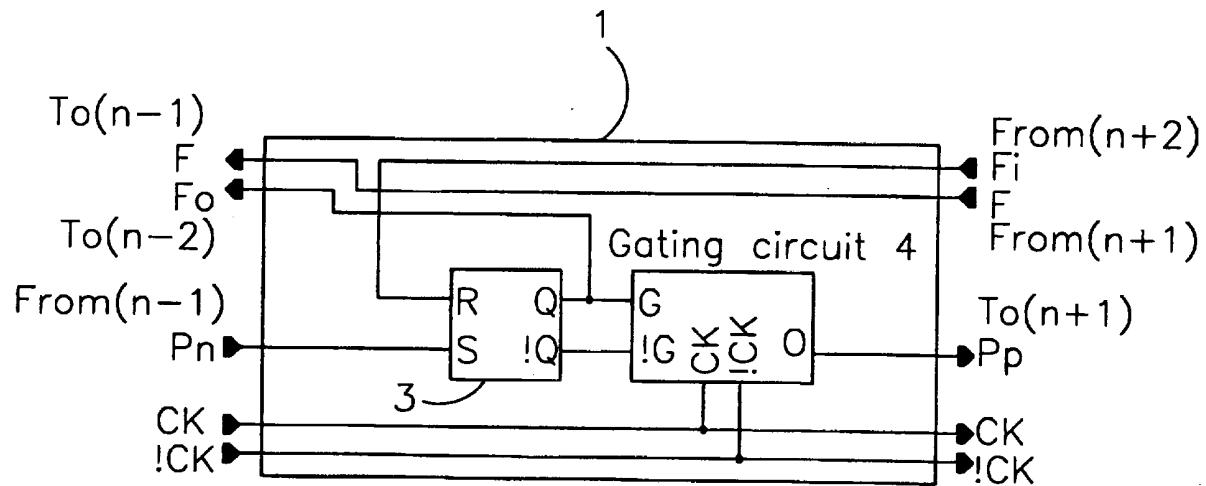


FIG 7

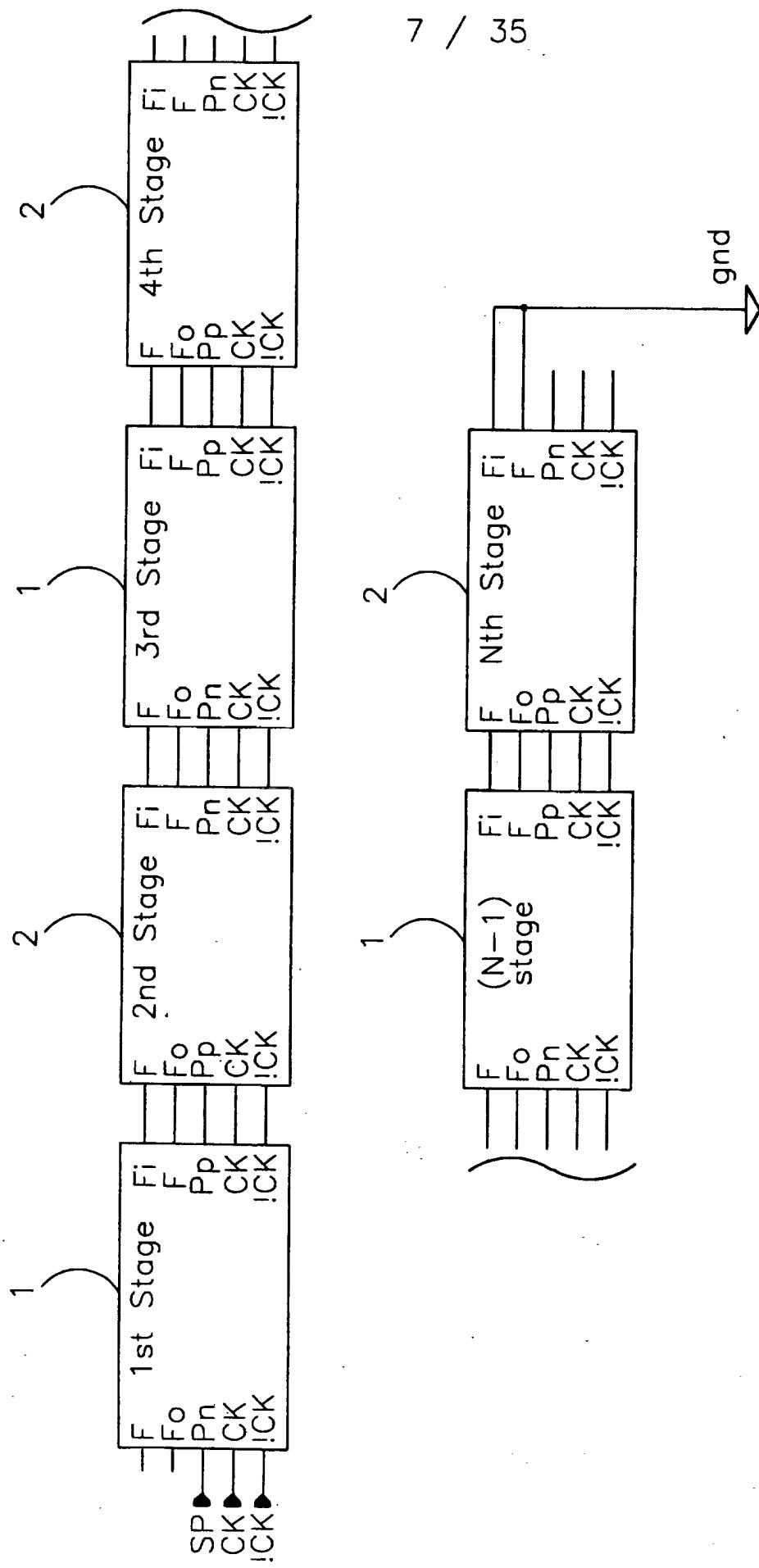


FIG 8

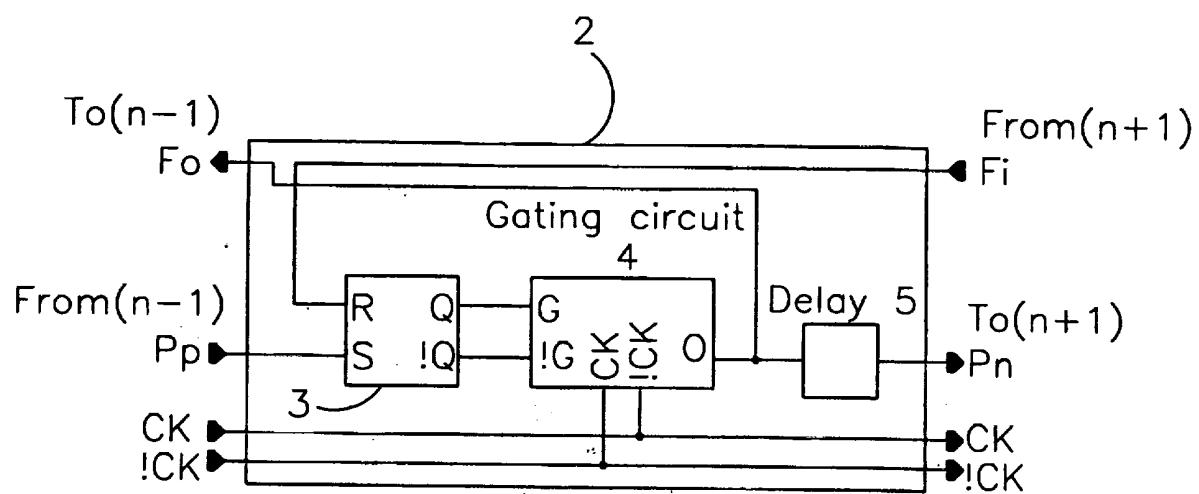
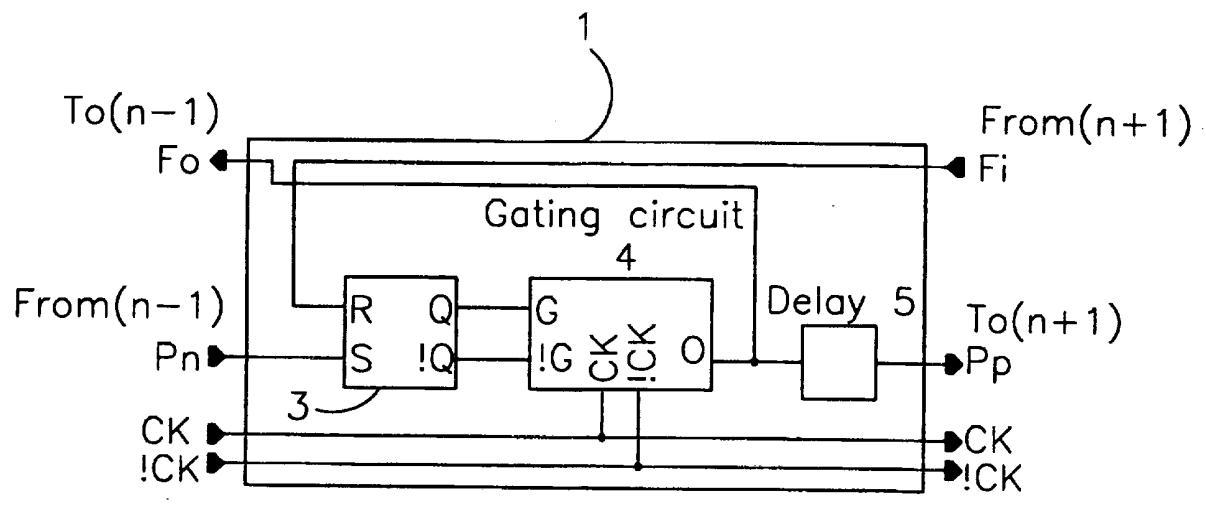


FIG 9

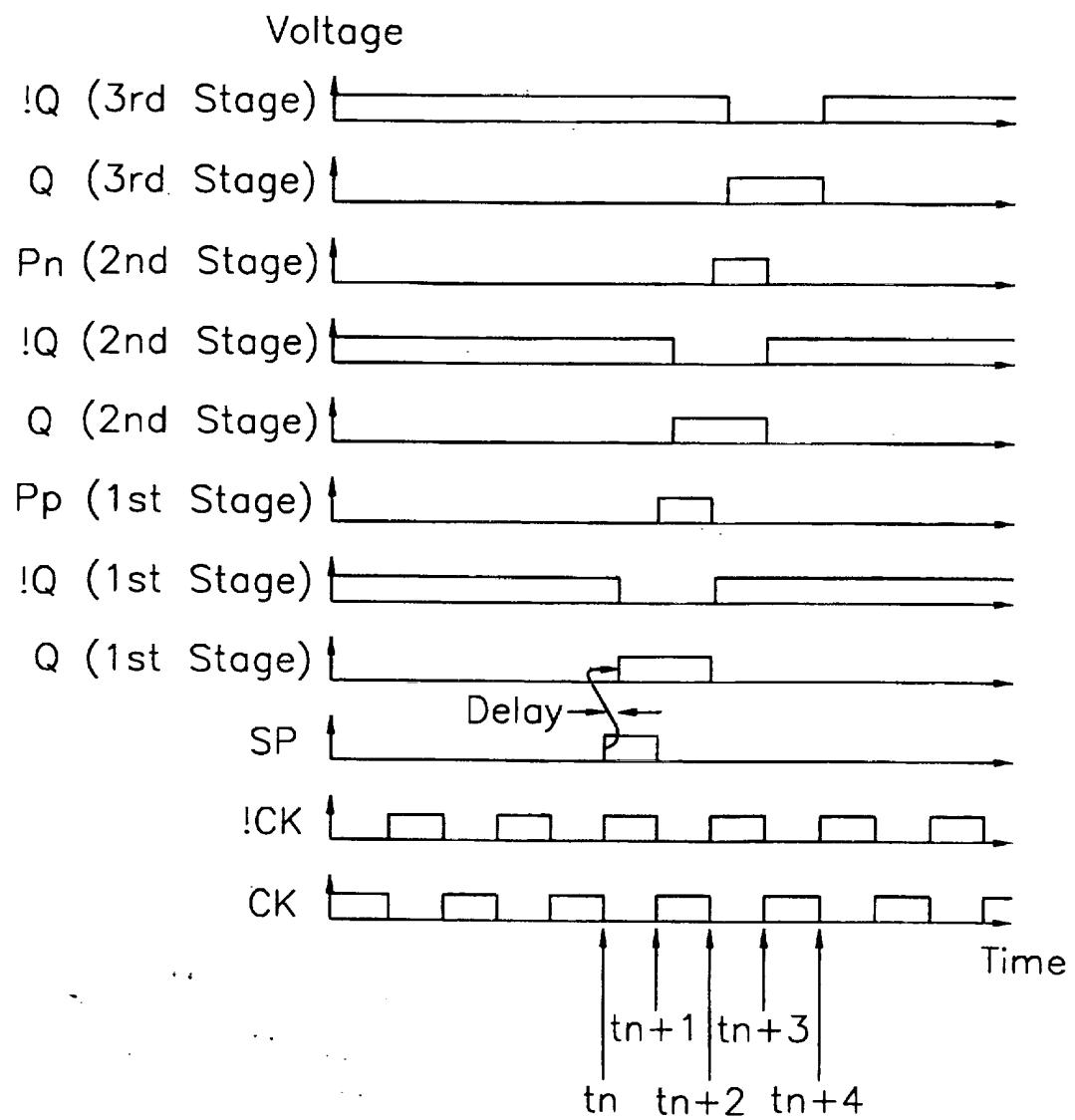


FIG 10

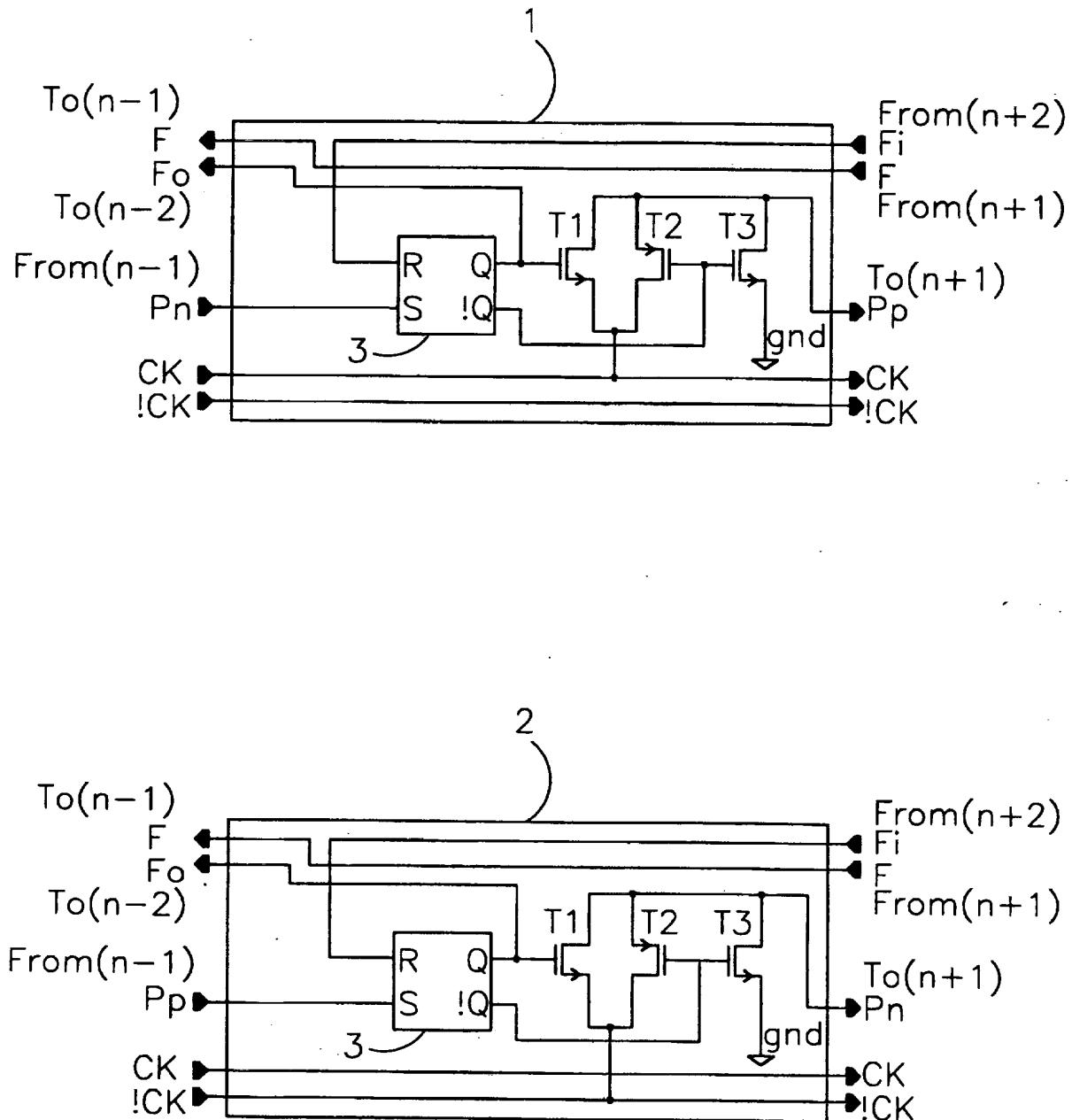


FIG 11

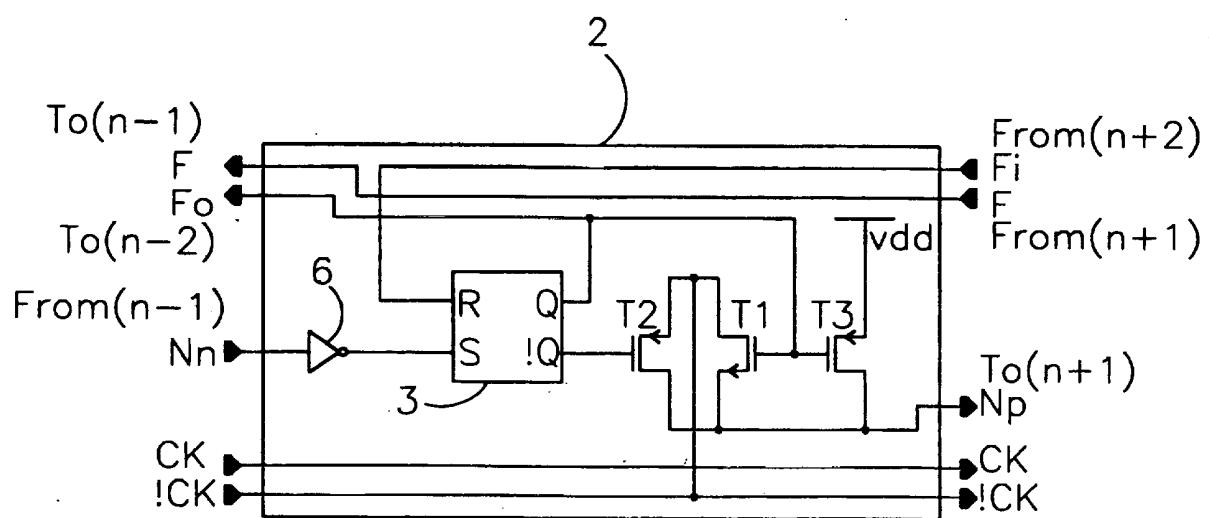
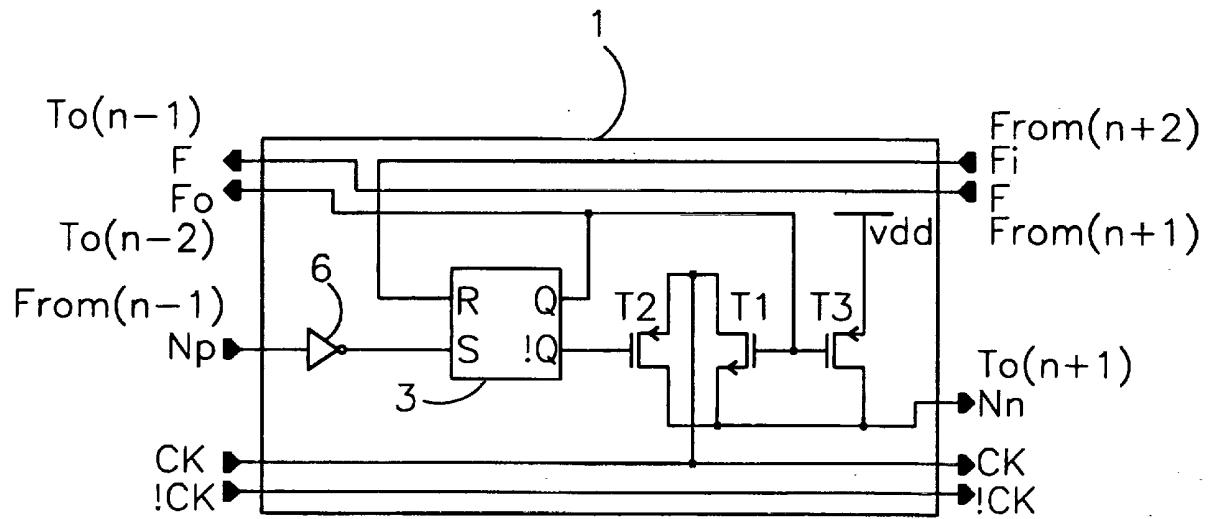


FIG 12

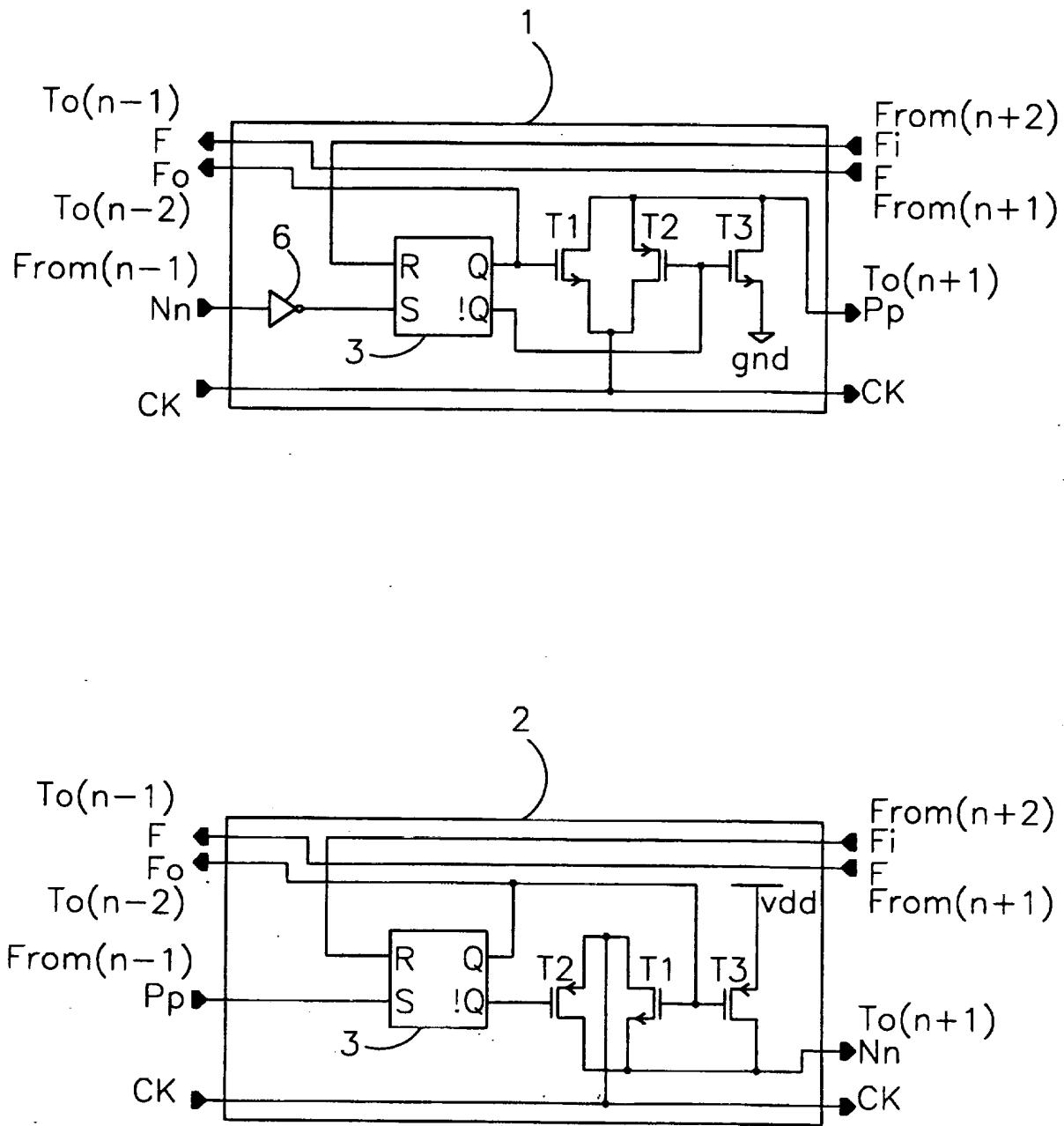


FIG 13

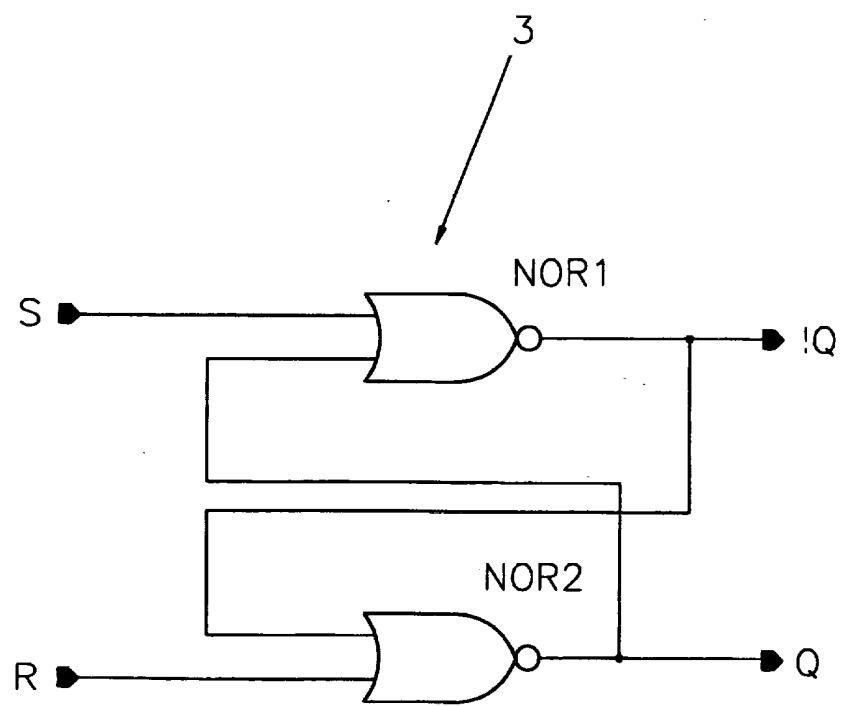


FIG 14

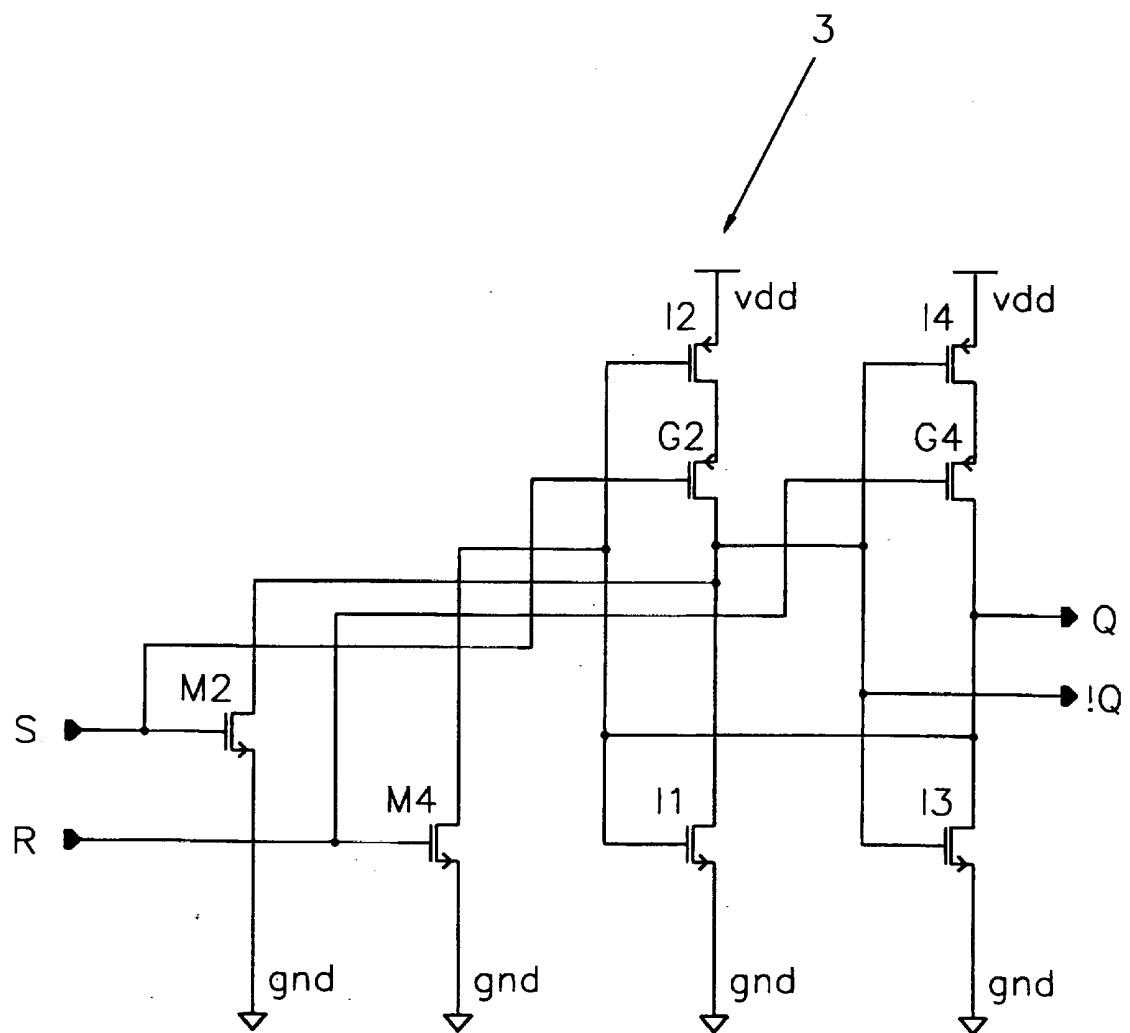


FIG 15

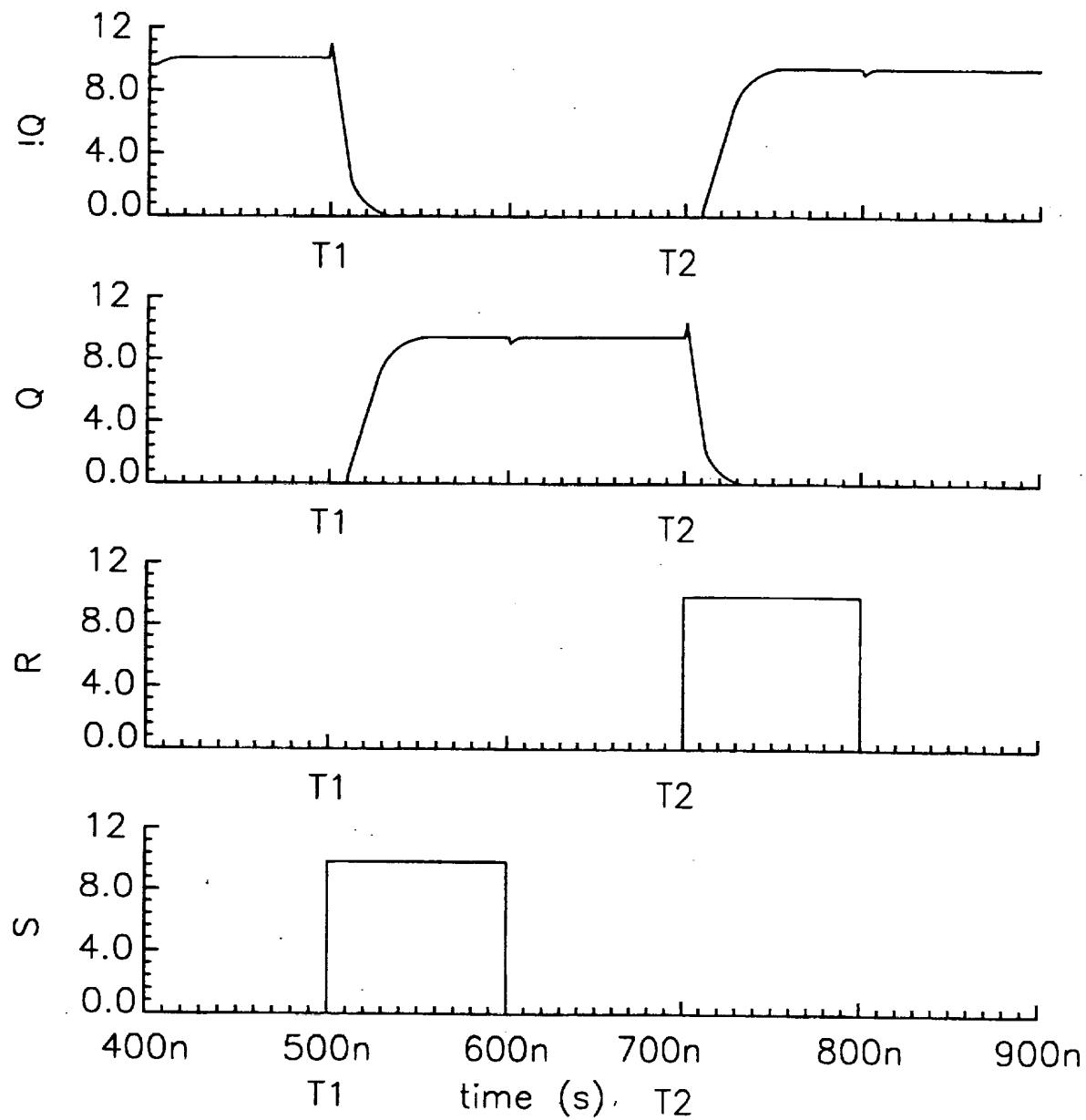


FIG. 16

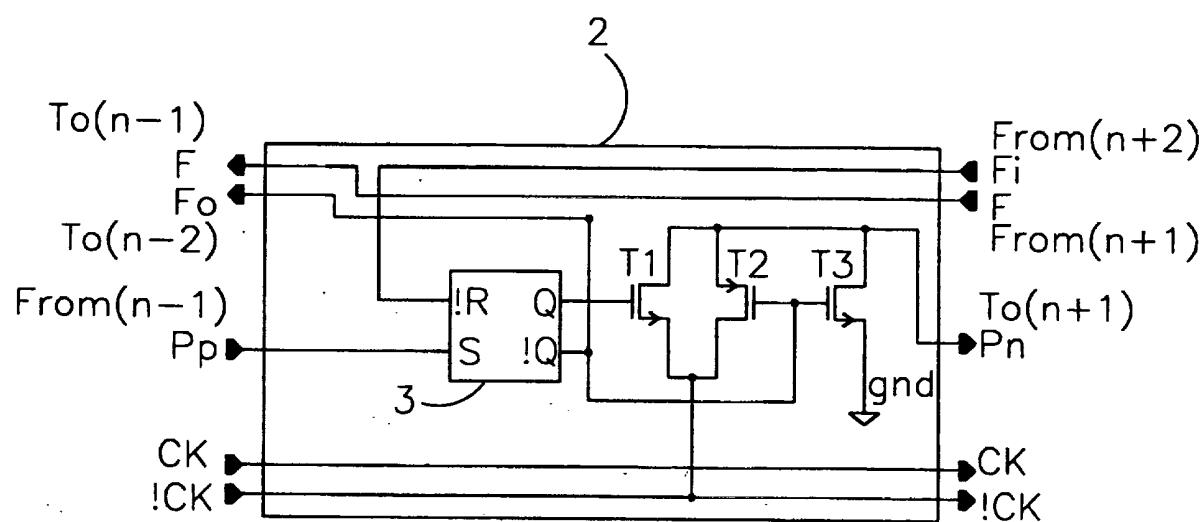
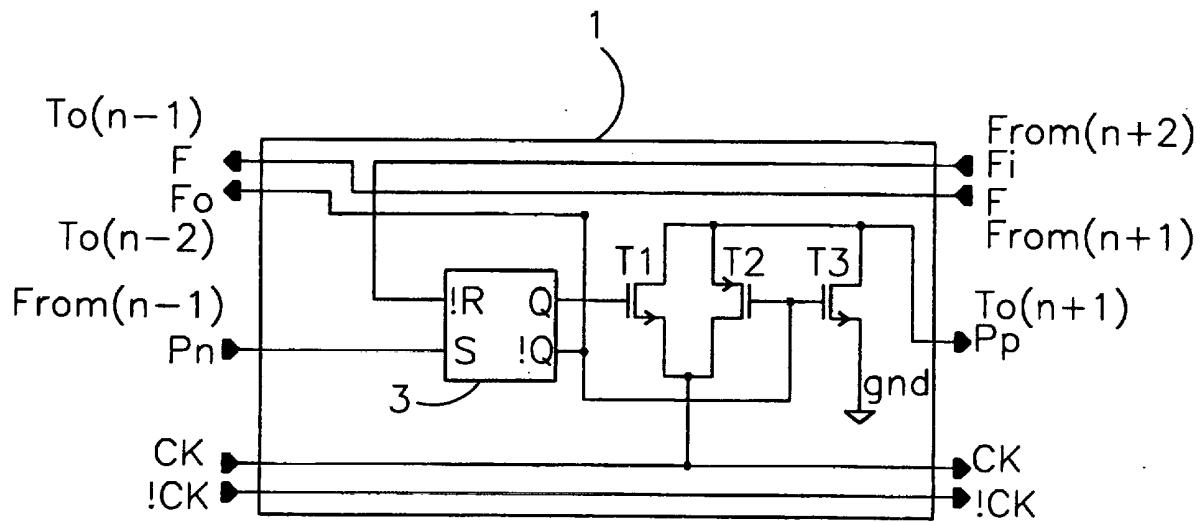


FIG 17

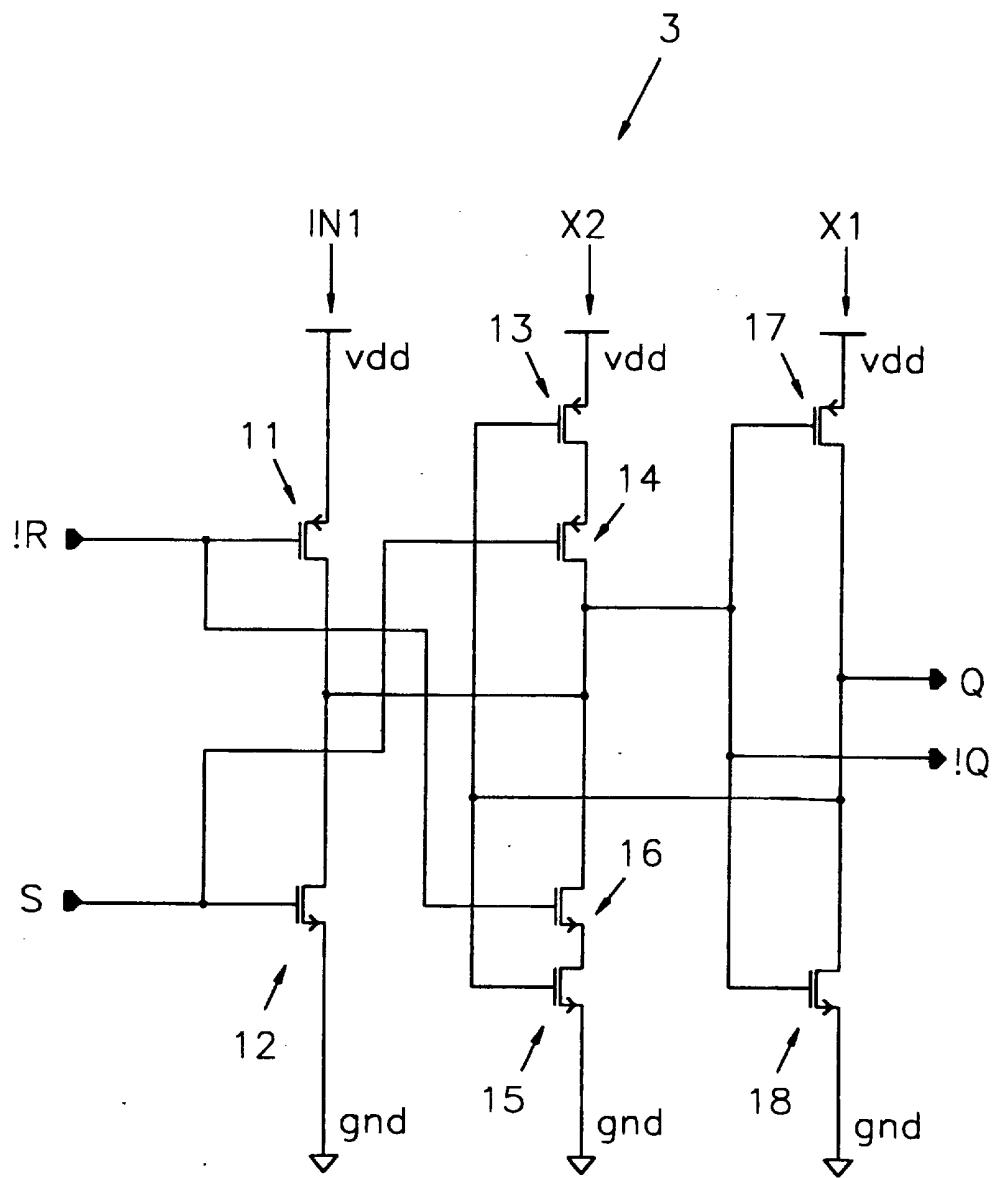


FIG 18

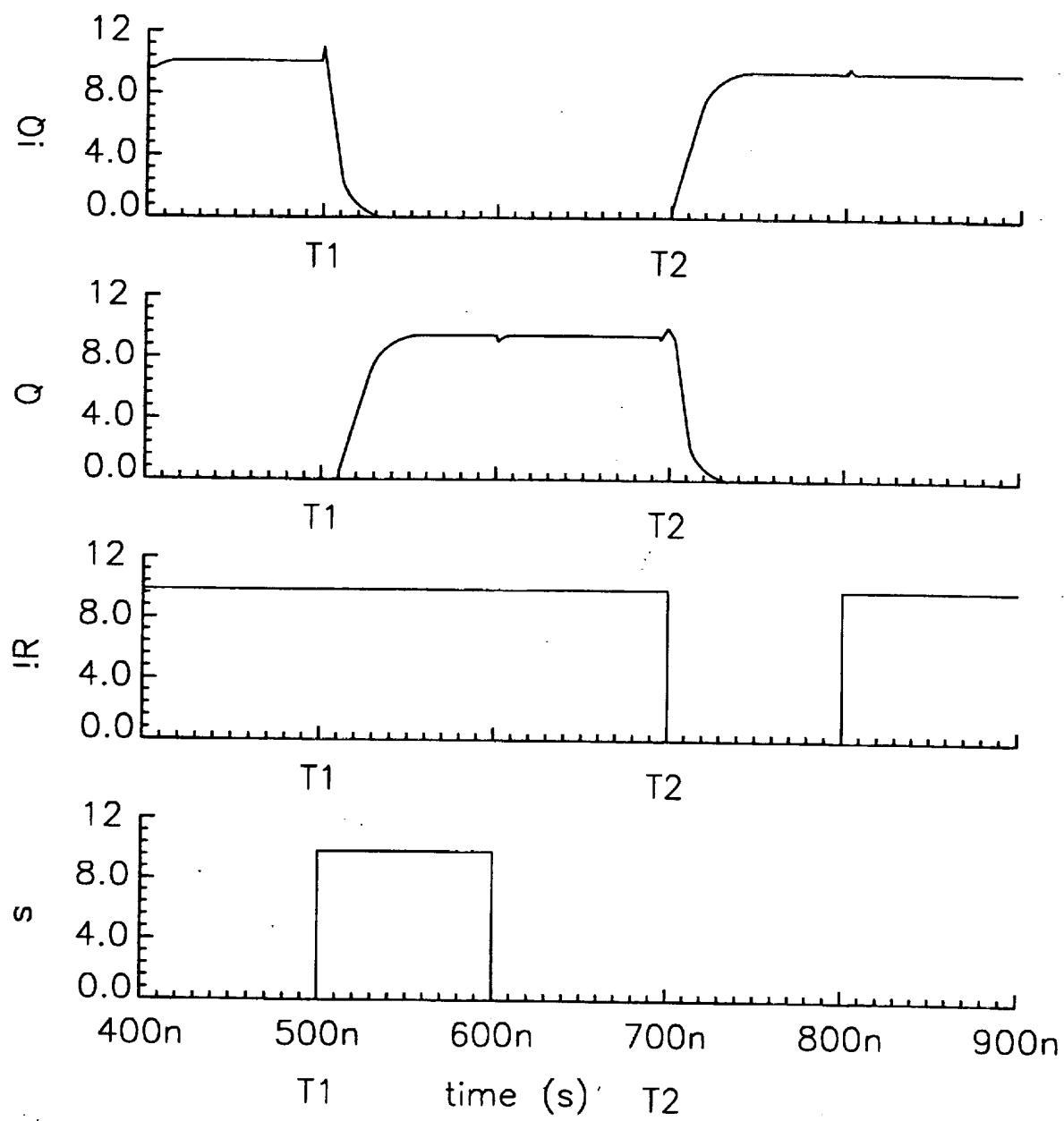


FIG 19

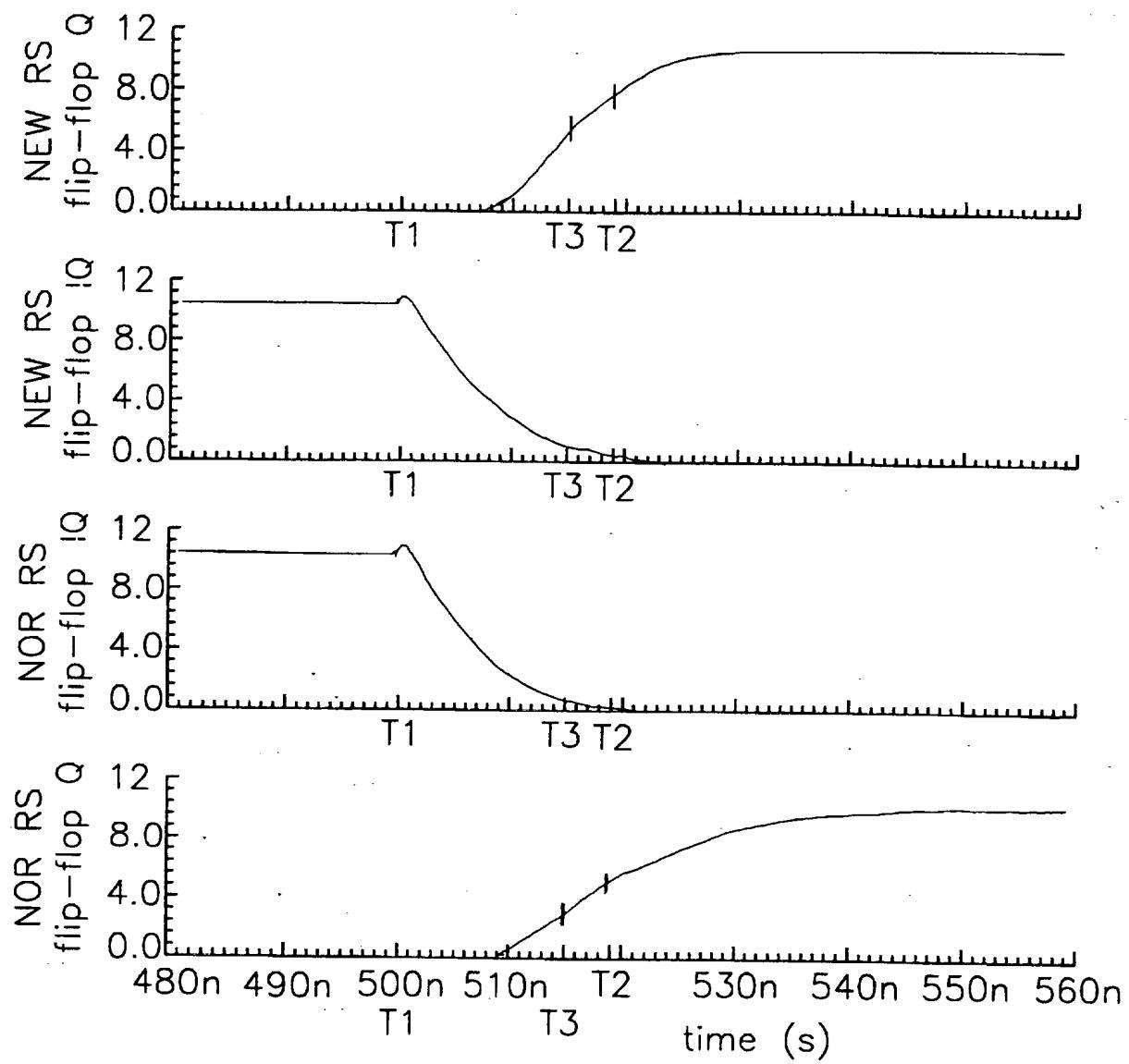


FIG 20

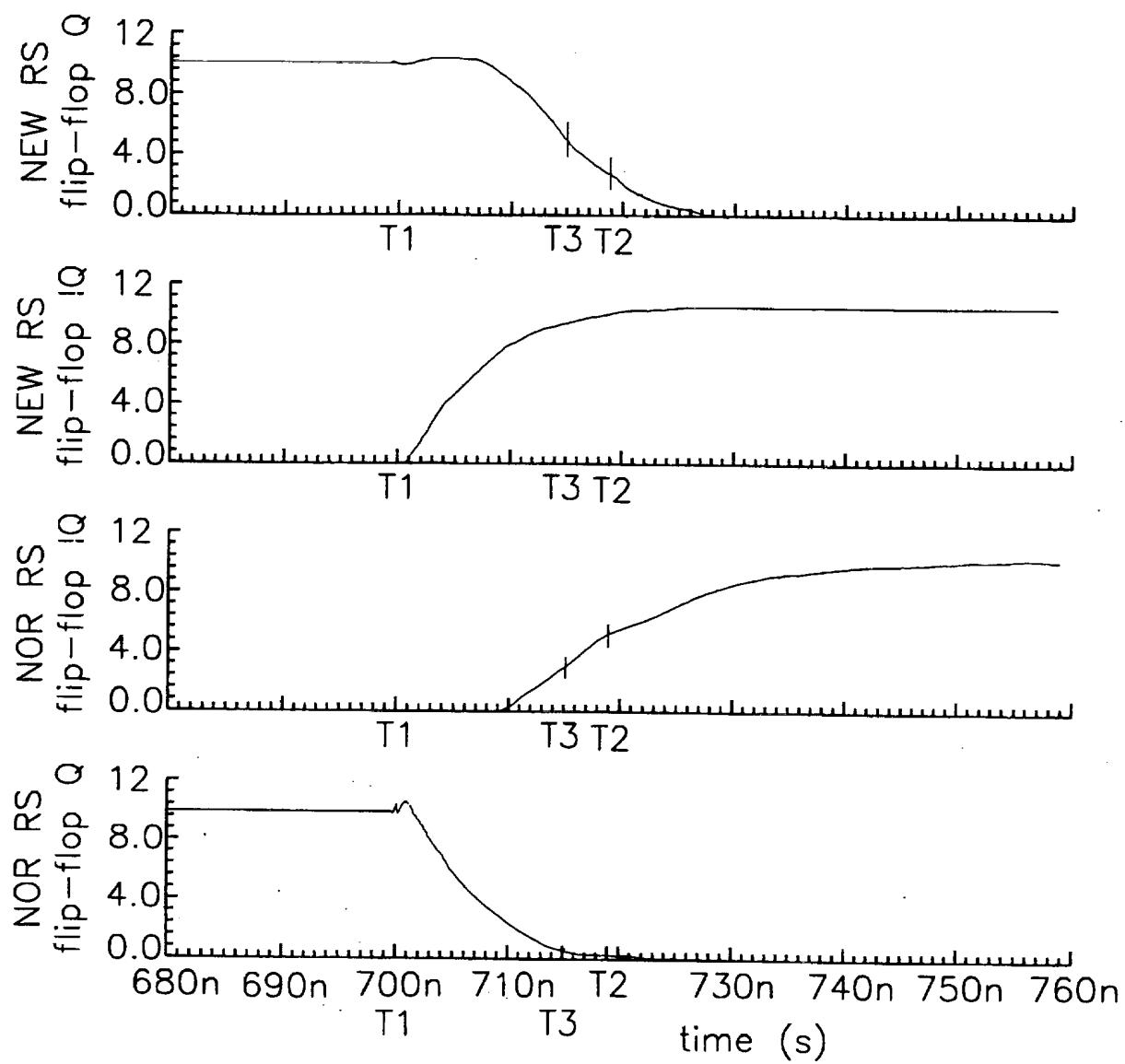


FIG 21

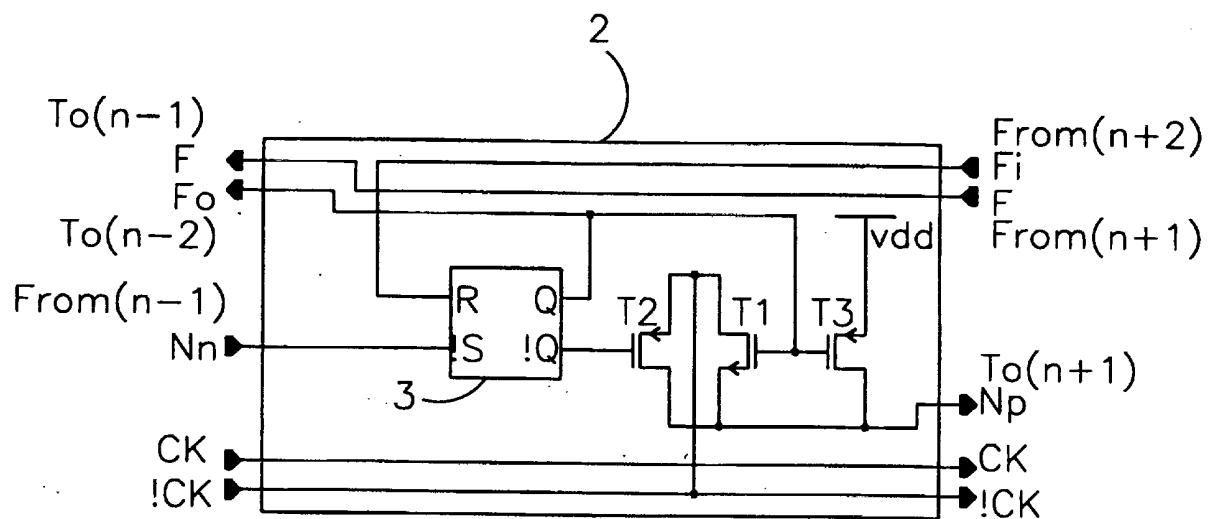
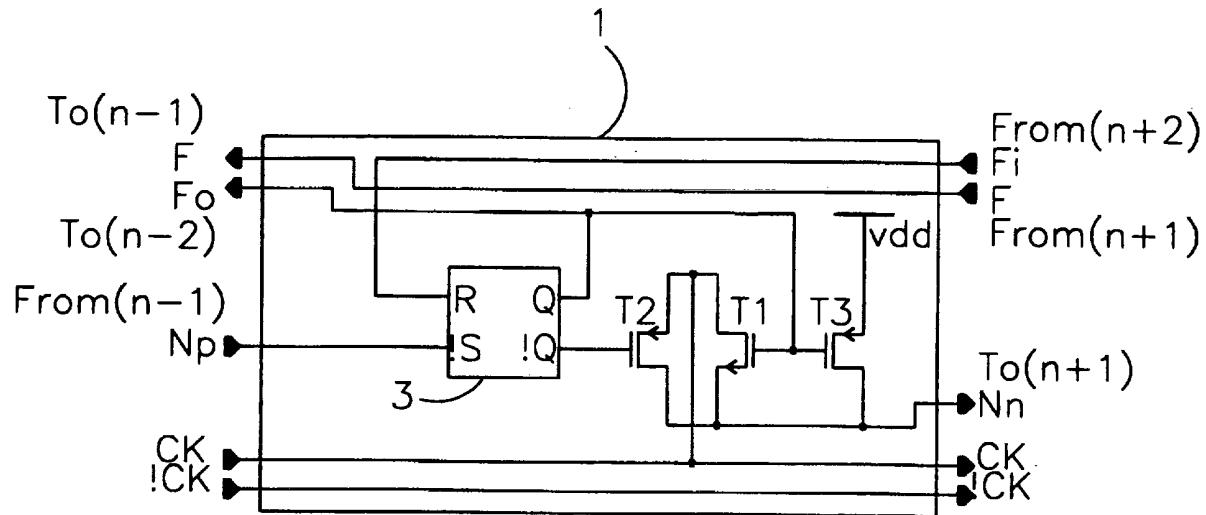


FIG 22

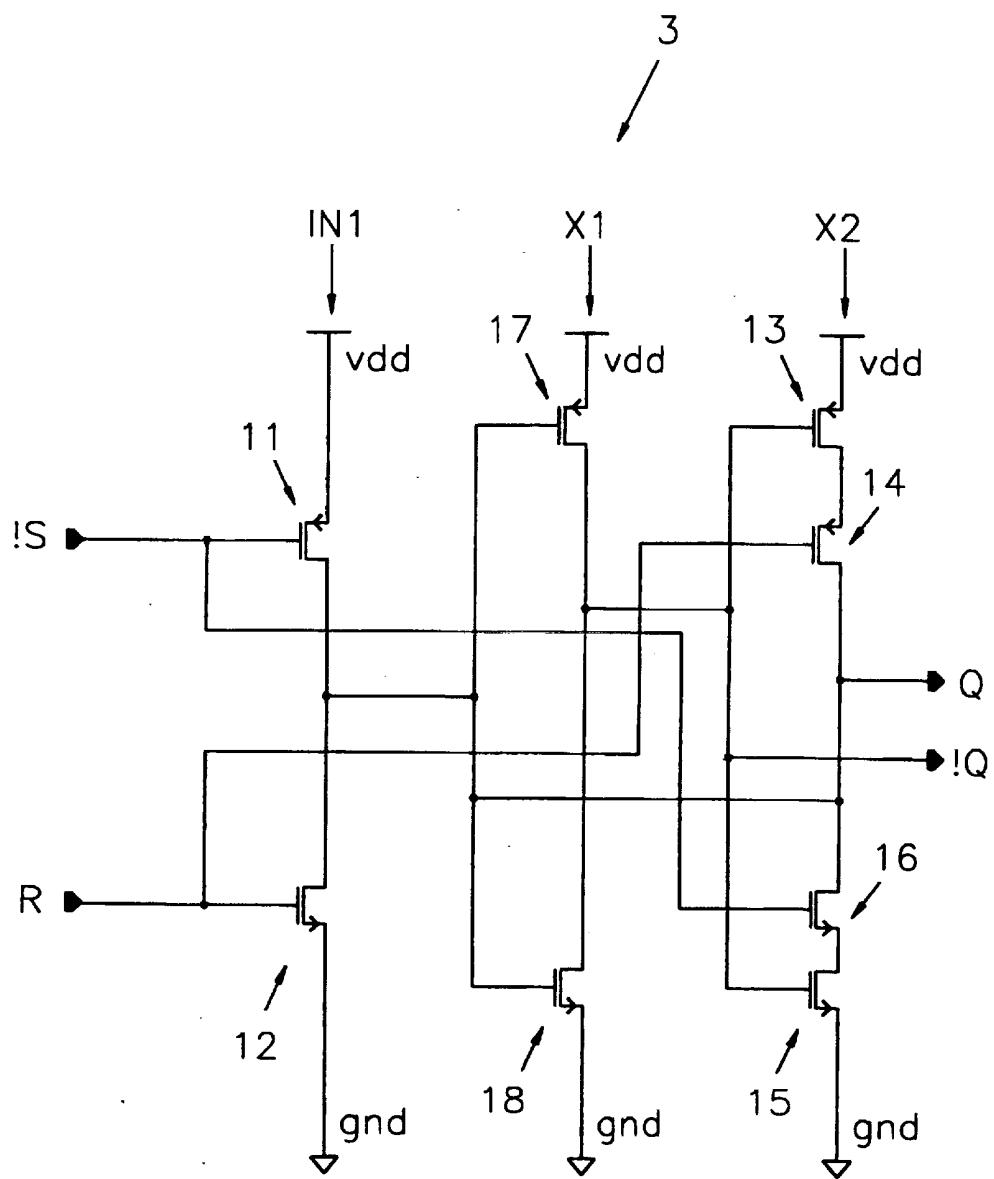


FIG 23

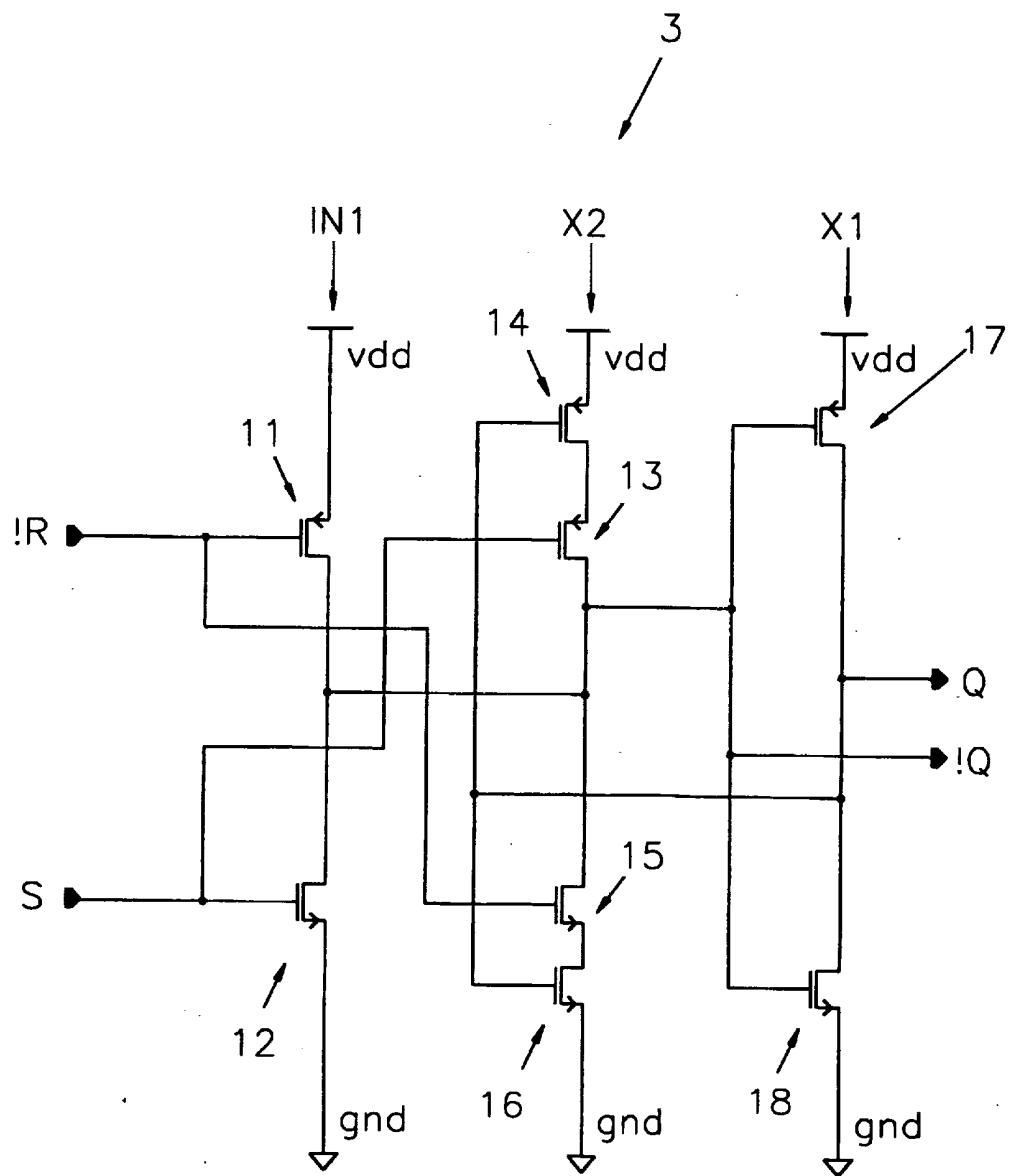


FIG 24

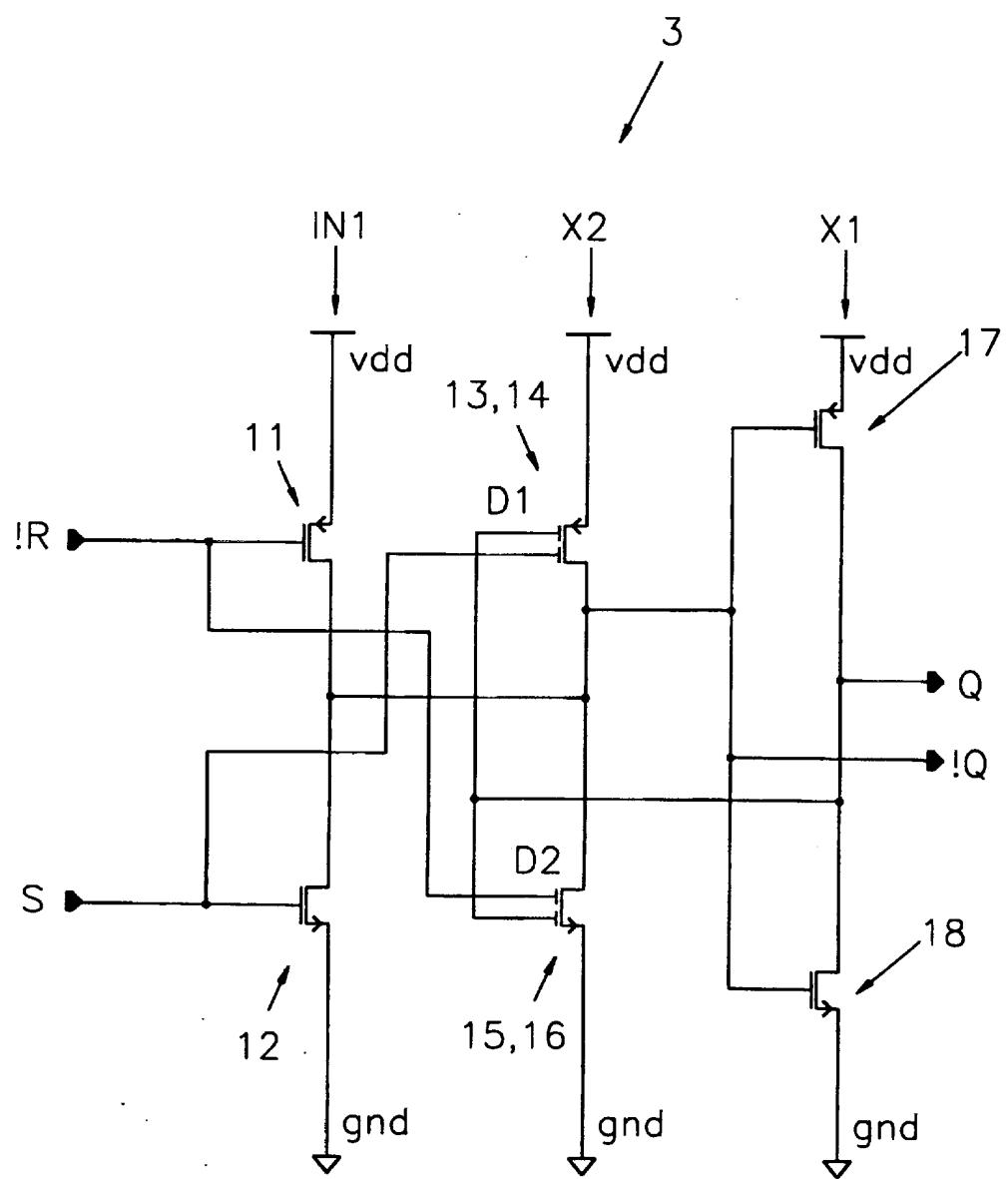


FIG 25

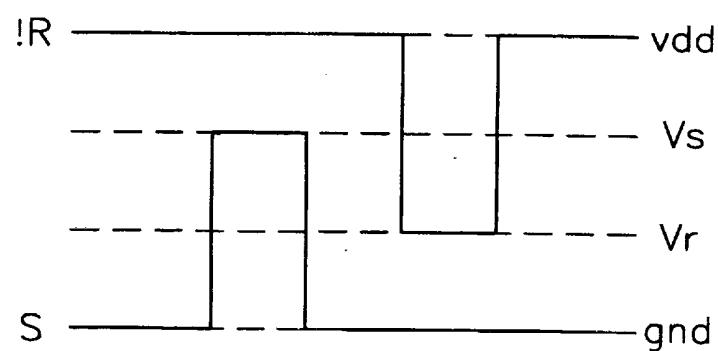


FIG 26

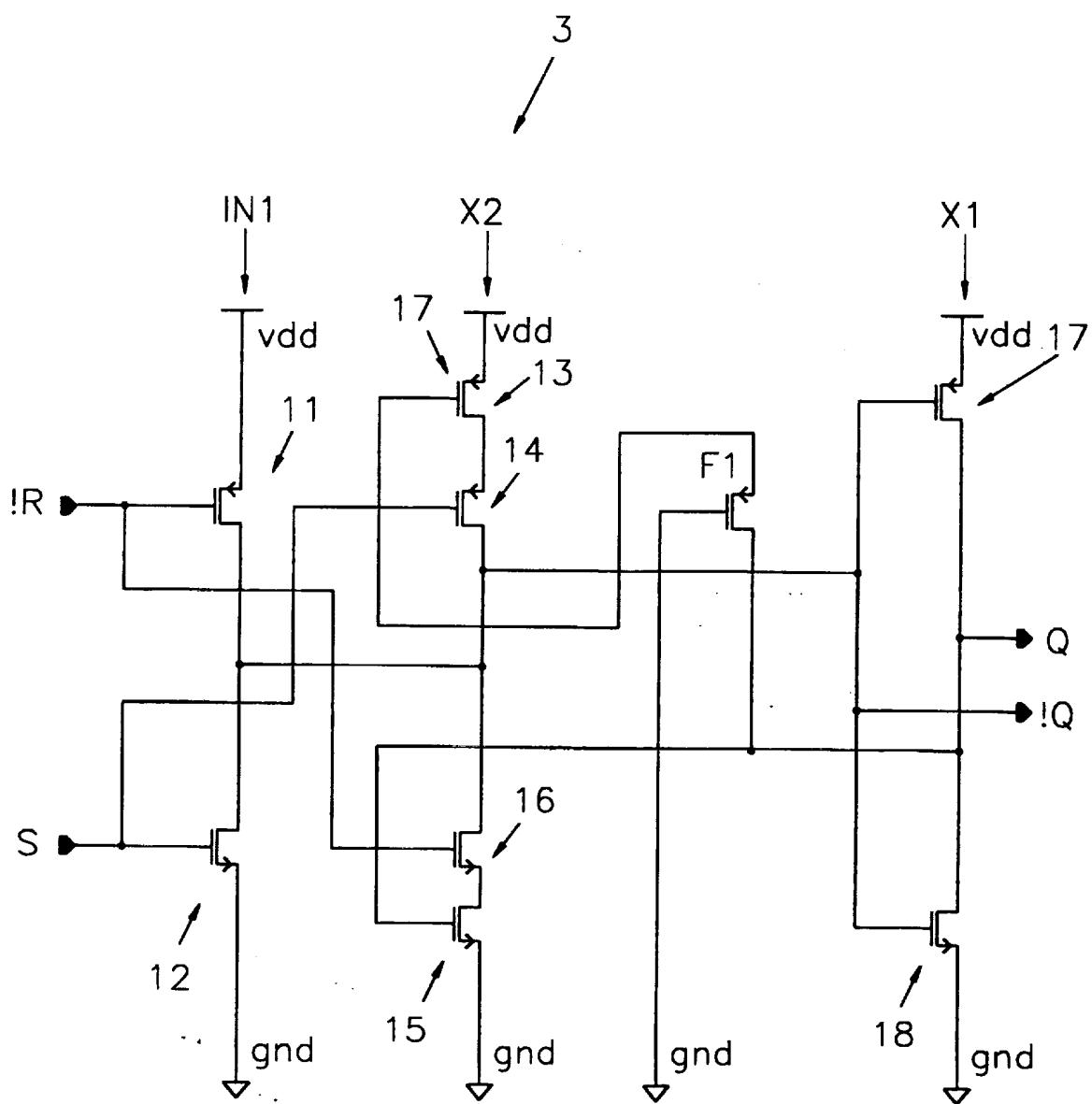


FIG 27

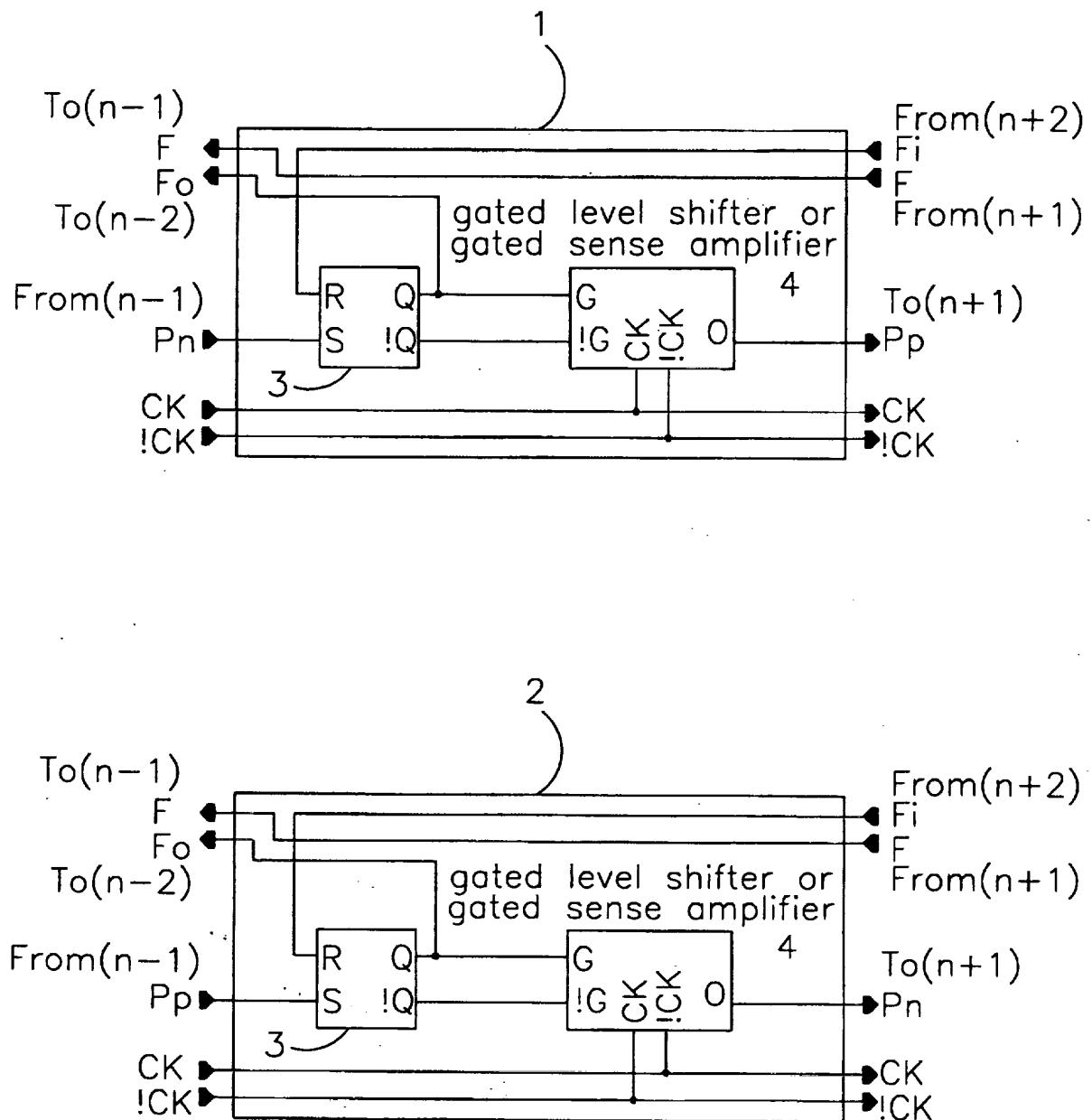


FIG 28

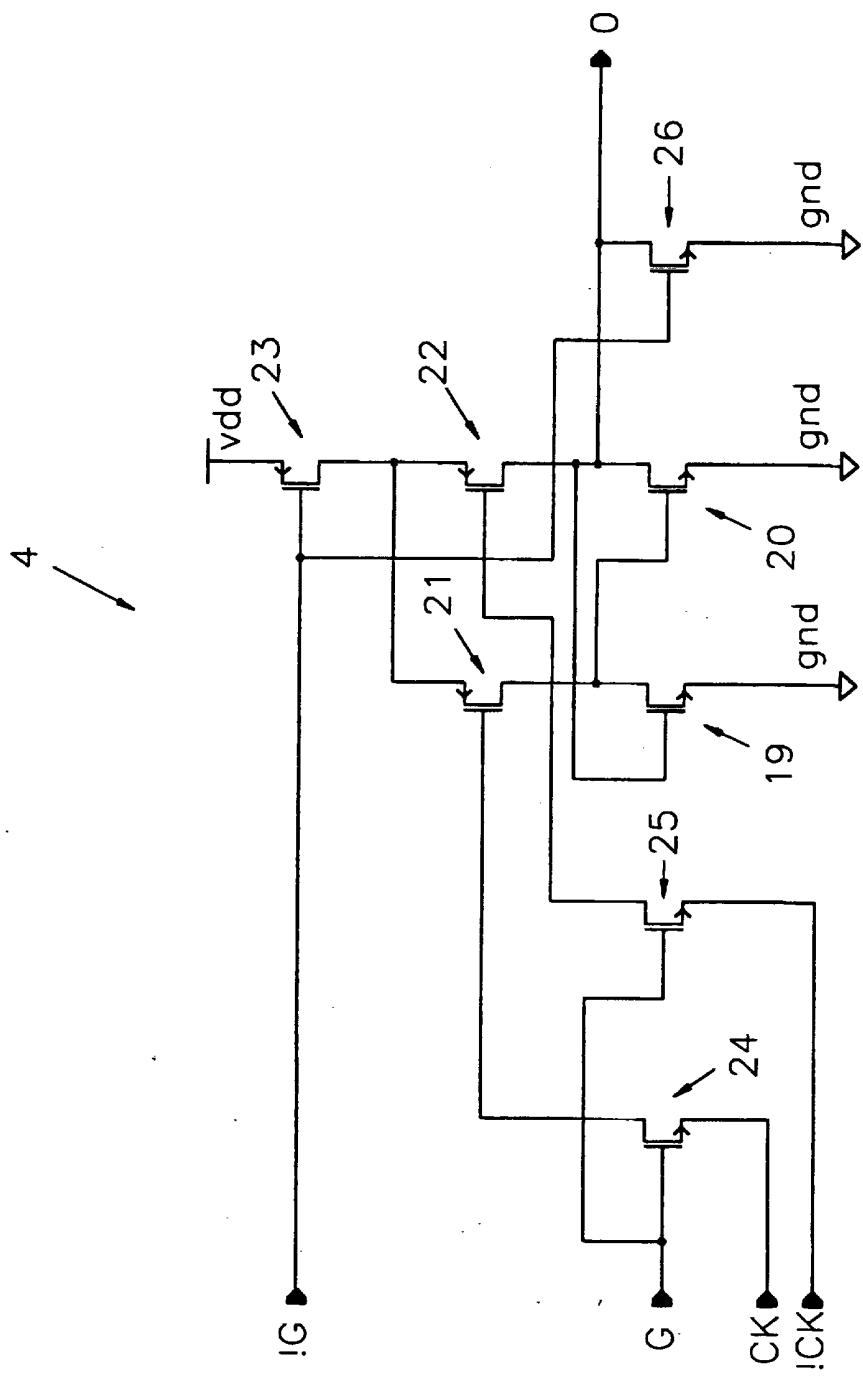


FIG 29

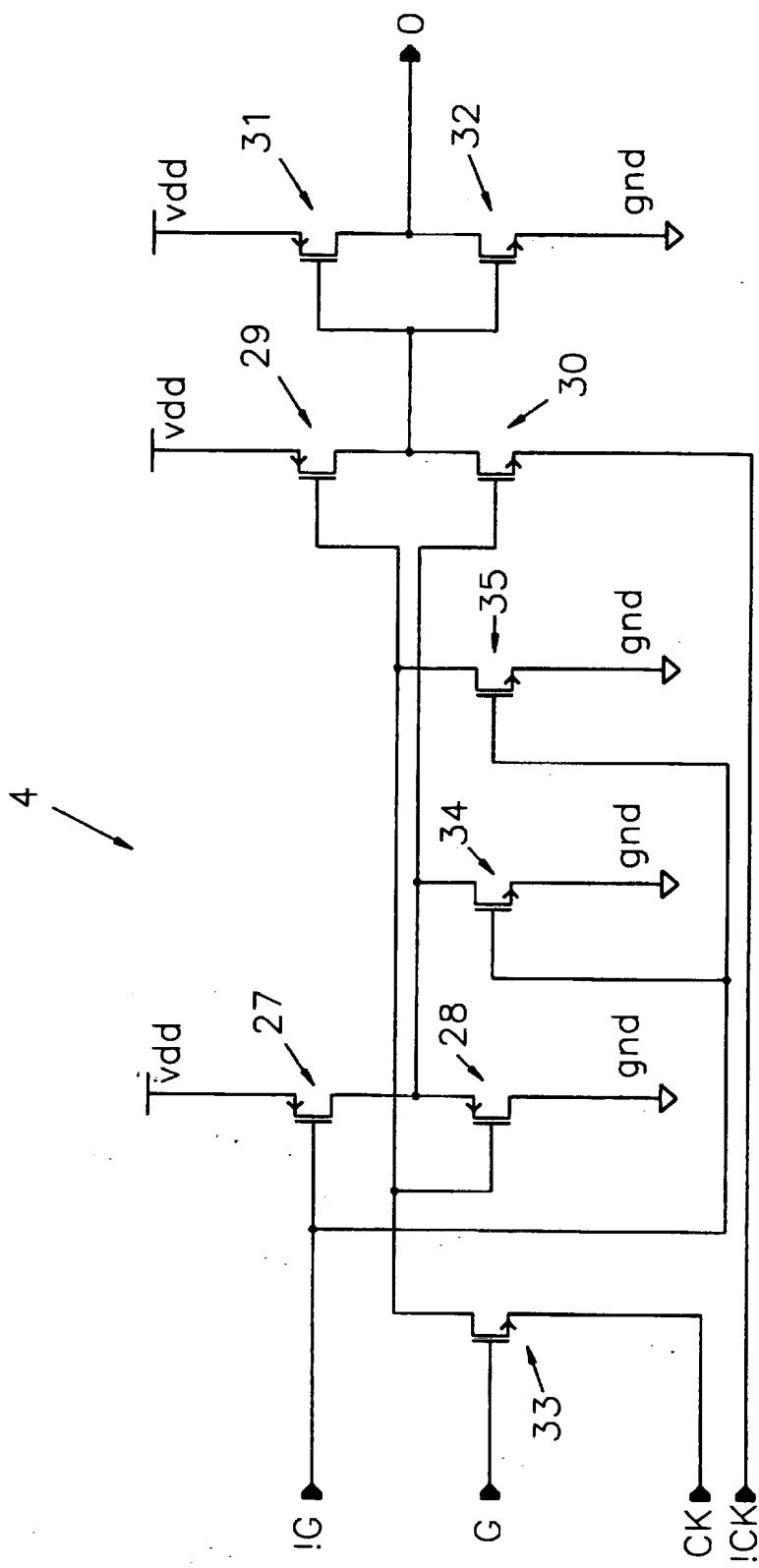


FIG 30

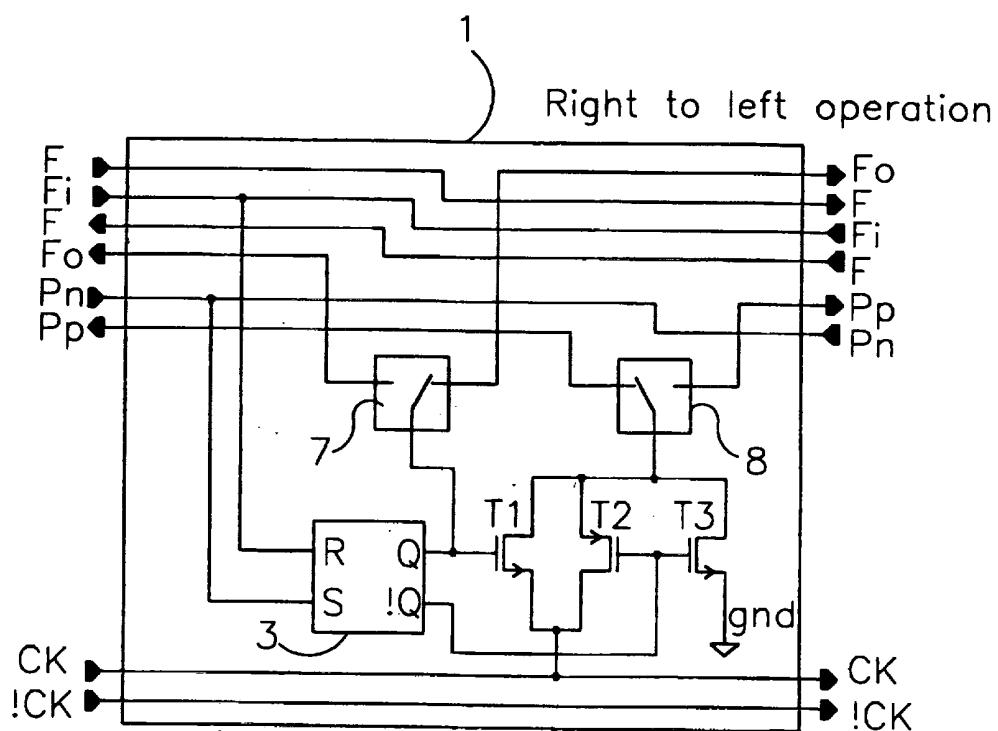
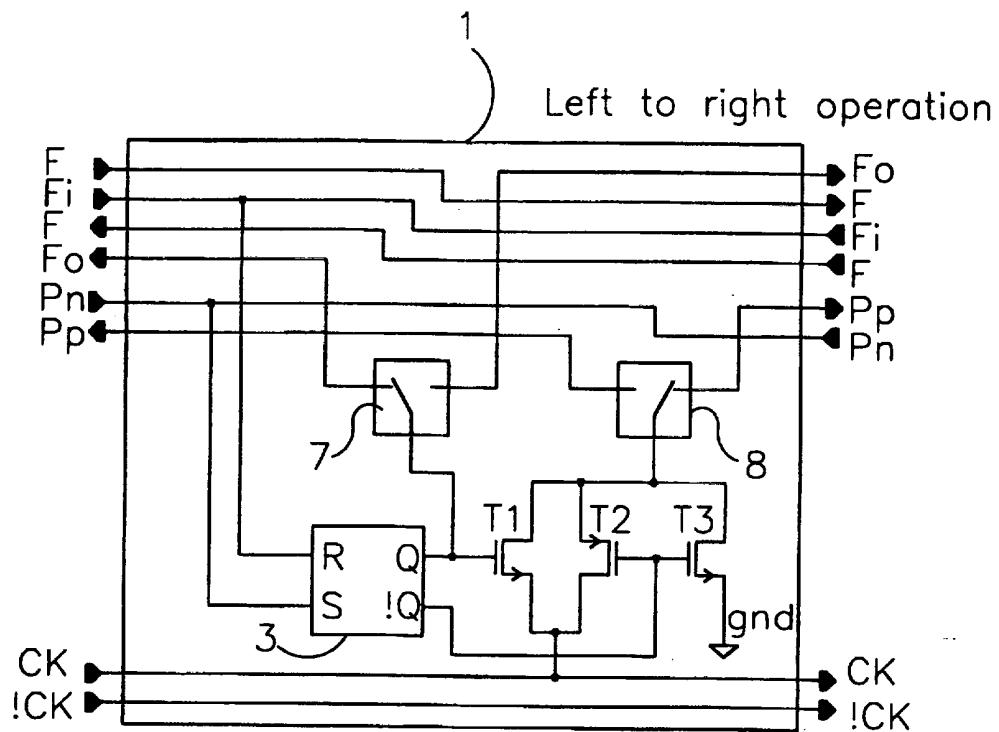


FIG 31

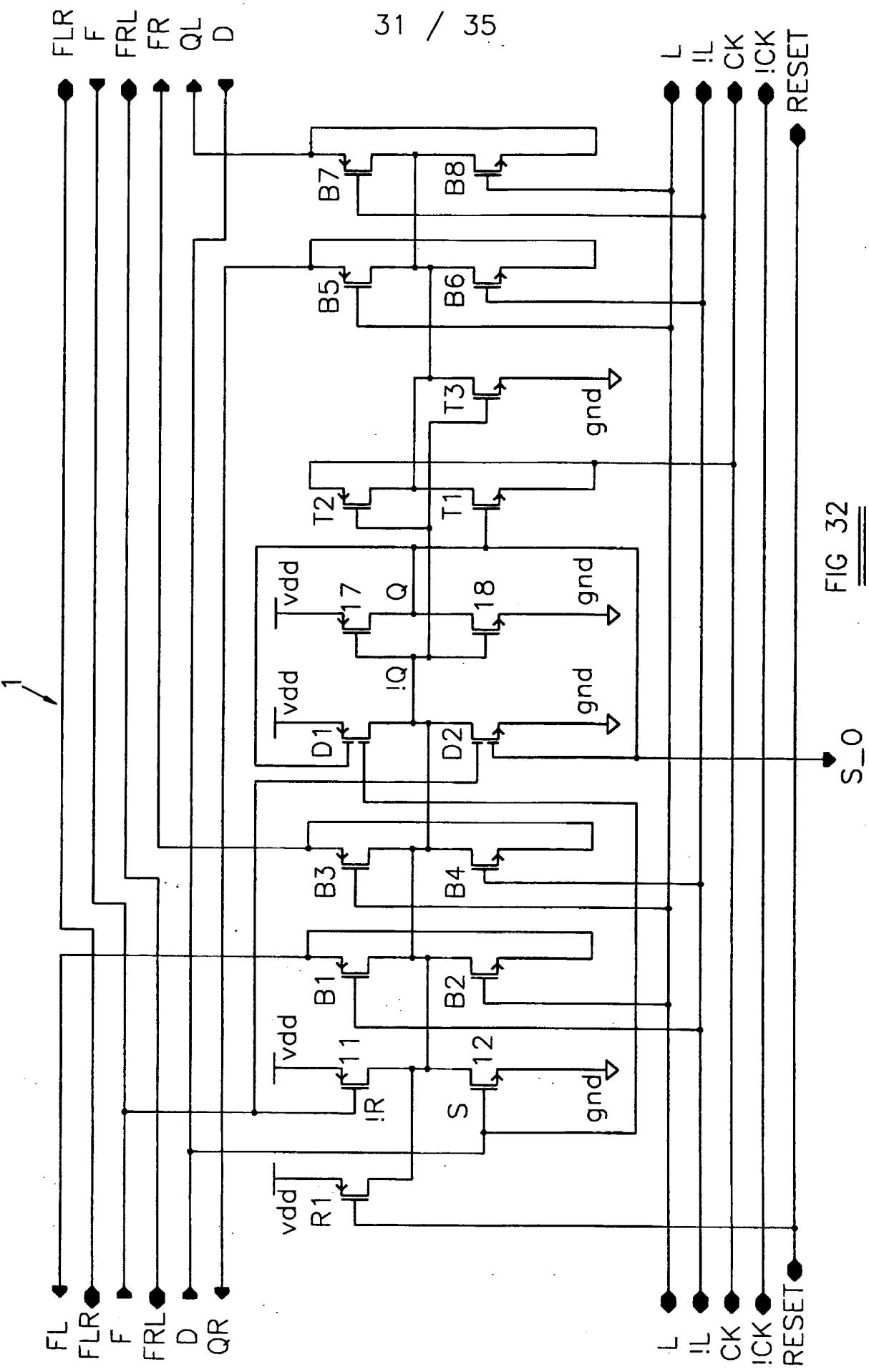


FIG 32

S_O

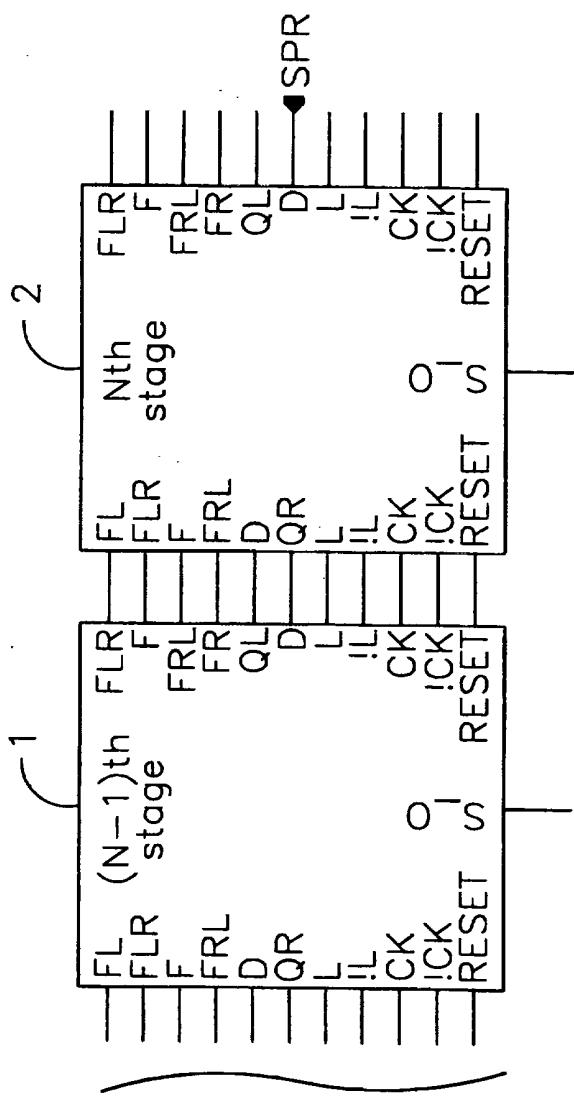
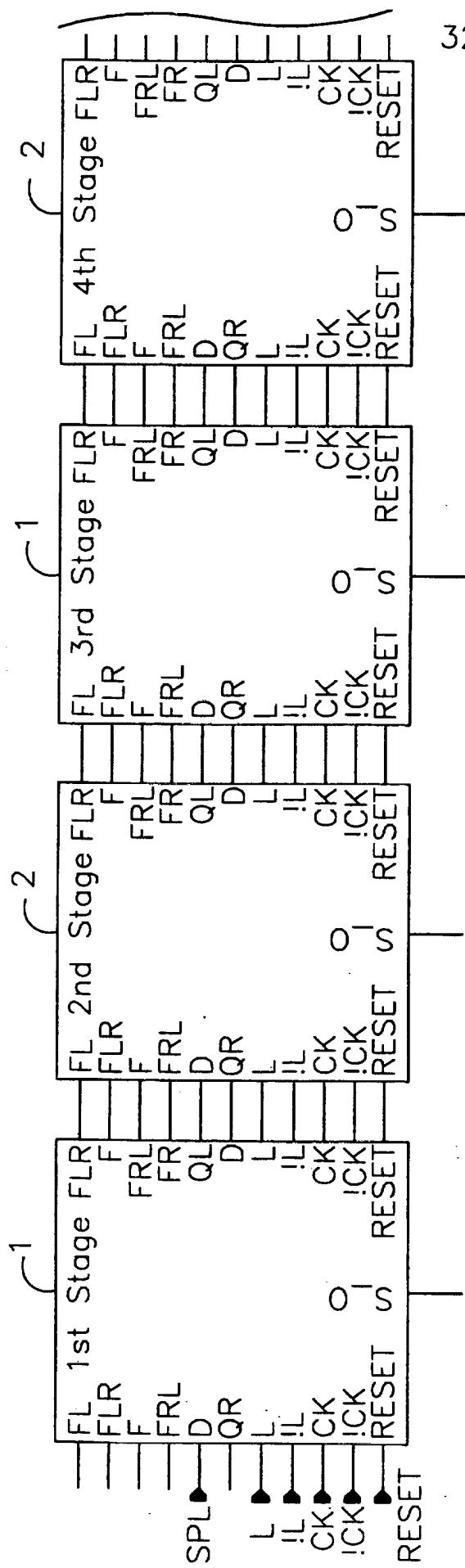


FIG 33

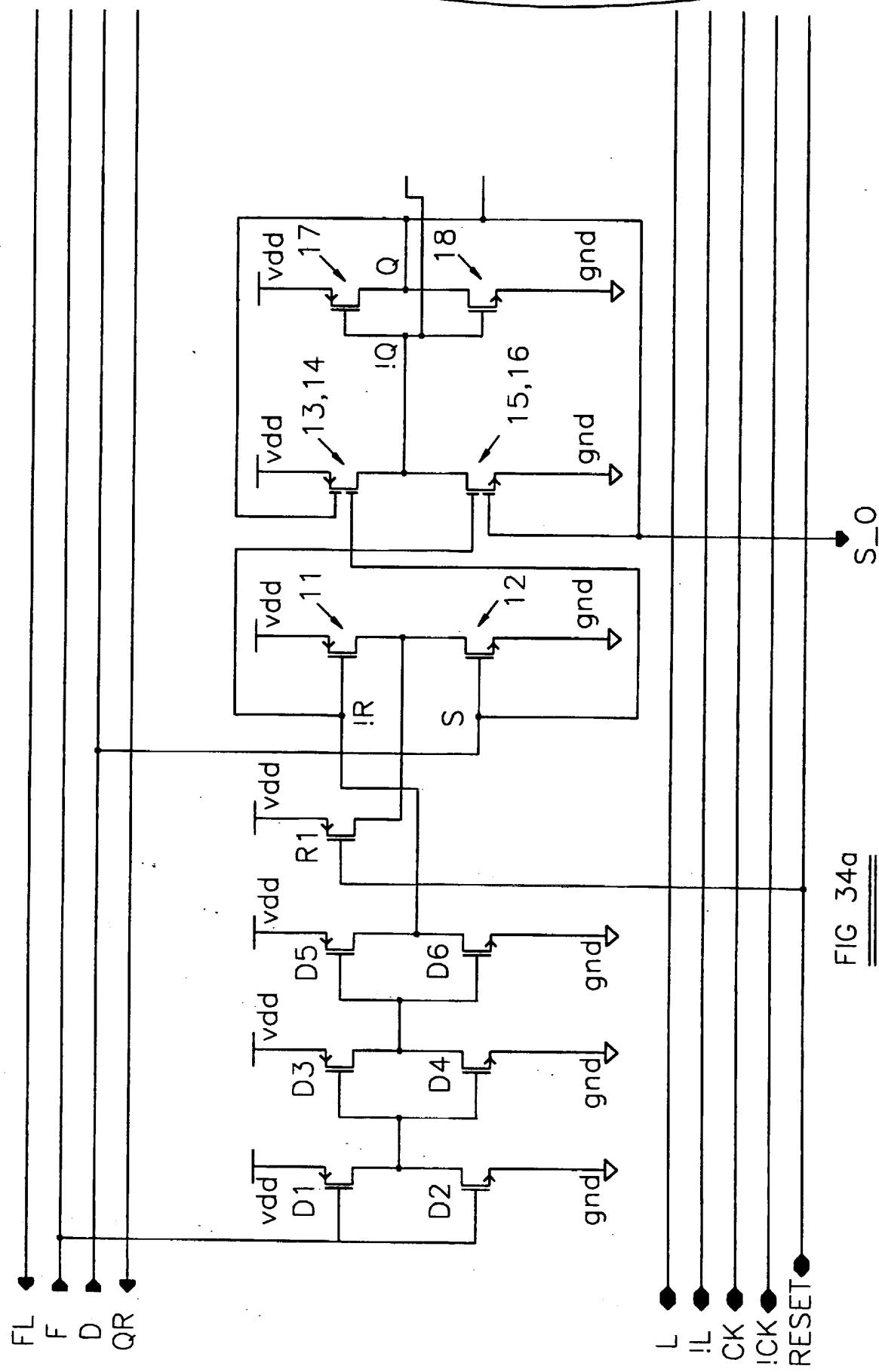


FIG 34a

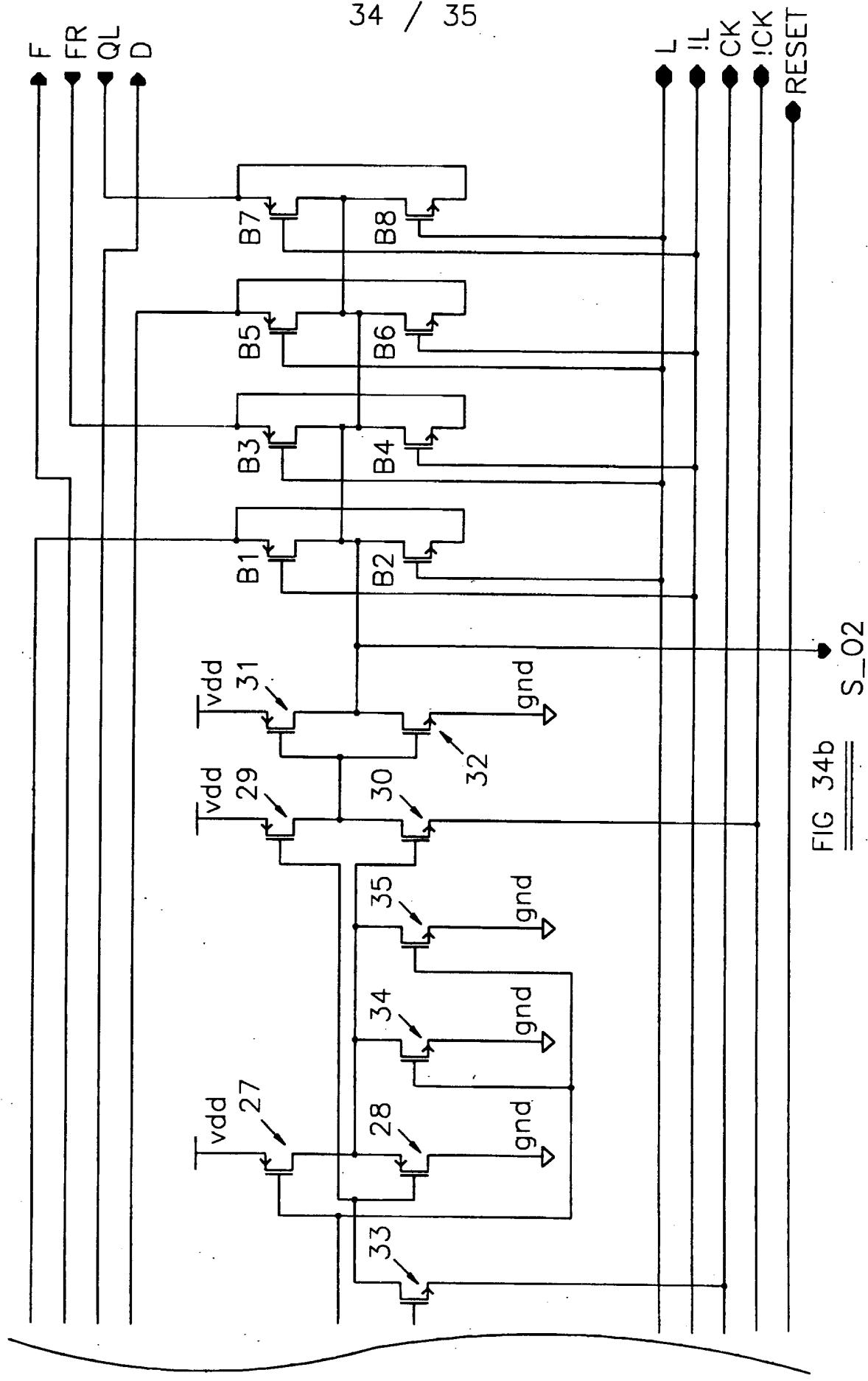


FIG 34b
S_02

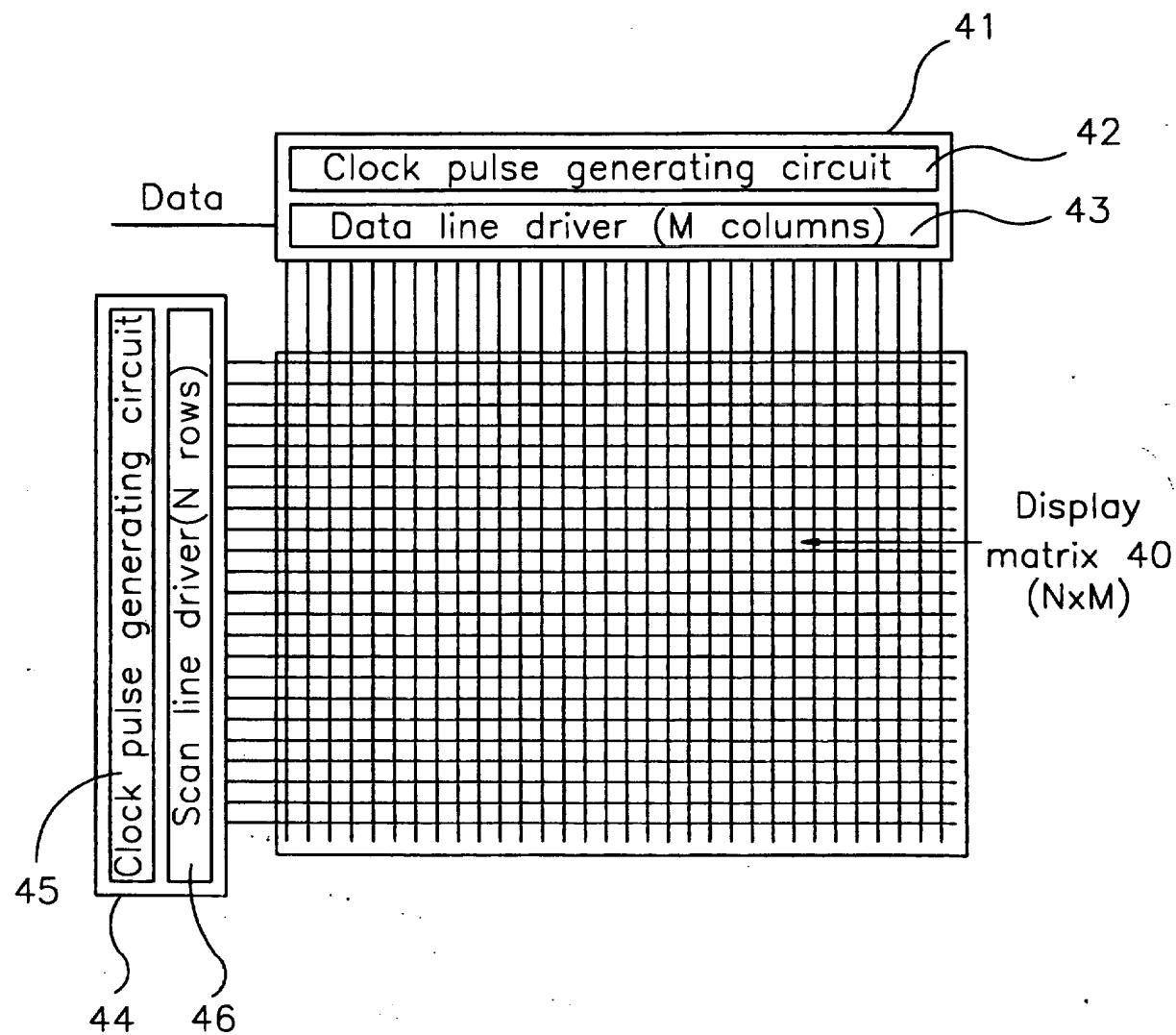


FIG 35

STATIC CLOCK PULSE GENERATOR, SPATIAL LIGHT MODULATOR AND DISPLAY

The present invention relates to a static clock pulse generator. Such a generator may be used in high speed low power controller circuits, for instance in complex very large scale integrated (VLSI) designs including digital signal processing (DSP). The clock pulse generator may advantageously be used in addressing for driver circuits of spatial light modulators and displays, for example of the pixelated matrix type in which a sequence of well-defined pulses must be supplied to circuits which sample high speed video data.

A known type of clock pulse generator is based on a shift register. The shift register comprises a cascaded chain of D-type flip-flops which respond to clock pulses to pass a single stored logic state from one flip-flop to the next in the chain. For a typical clock pulse generation application, all but one of the states of the flip-flops are initialised to a logic low (0) state whereas the remaining flip-flop is initialised to a logic high (1) state. The shift register is clocked at a known frequency and the circulating one state within the shift register is used to generate sequential pulses at the outputs of the flip-flops. This well-known technique is disclosed, for example, in US 4 542 301 and US 4 612 659. An improvement to this technique is disclosed in US 4 785 297. In this case, the "master" and "slave" outputs of each of the flip-flops are used in conjunction with combinational logic gates, such as AND or NAND gates, to reduce the clocking speed of the shift register for a given number of output pulses.

It is also well-known to form clock pulse generating circuits from chained D-type latch circuits. Figure 1 of the accompanying drawings illustrates part of a typical CMOS circuit comprising latches 1 and 2. The construction and operation of such an arrangement is well-known and will not be described in detail. Consecutive latches such as 1 and 2 are transparent on opposite clock phases of a two phase clock represented by CK and CK-. The input and output of each latch are "NANDED" together in order to produce the clock pulses Nn and Np as illustrated in Figure 2 of the accompanying drawings. Figure 2 also illustrates the two phase clock waveforms, the D

input to the first latch 1, the output M of the first latch 1 which is also the input of the second latch 2, and the output Q of the second latch 2.

A disadvantage of this arrangement is that the output pulses Nn and Np cannot be guaranteed to be non-overlapping. This can cause problems in certain applications, for example when the output pulses are used for sampling video data in pixel matrix display drivers.

Various techniques have been disclosed for reducing the capacitive loading of the clock line or lines so as to increase the maximum frequency of operation and reduce clock power consumption. For example, state-controlled clocking techniques have been suggested for use in clock pulse generating circuits. An example of this is disclosed in US 4 746 915, in which the shift register is divided into several sub-registers of flip-flops or latches and another shift register operating at a lower frequency is used selectively to apply the clock signal to each sub-register.

For applications in which the requirement is for a single circulating 1 state, only those flip-flops or latches containing a 1 state or having a 1 state at their input require clocking. As shown in Figure 3, for such applications, the signal generated by "ORing" the input and output of each flip-flop can be used to gate the clock signals supplied to the clock input of the flip-flop. Such an arrangement is disclosed in T. Maekawa et al, "A 1.35-in.-diagonal wide-aspect-ratio poly-Si TFT LCD with 513k pixels" Journal of the Society of Information Display, pp 415-417, 1994. However, such an arrangement requires a full flip-flop and several further transistors per stage. Also, the flip-flop outputs have to drive a relatively large load and this limits the maximum speed of operation.

The term "pass gate" as used herein is defined to mean a semiconductor arrangement having a main conduction path which can be controlled to transmit or block the passage of an input signal.

According to a first aspect of the invention, there is provided a static clock pulse generator comprising a clock input and N stages, each ith one of the stages comprising a reset-set flip-flop having a set input for receiving a set signal from a gating circuit output of the (i-1)th stage and a reset input for receiving a reset signal from an (i+a)th stage, where a is greater than or equal to one, and a gating circuit for passing a clock pulse from the clock input to an output of the gating circuit when the flip-flop is set, where $1 < i \leq (N-a)$.

The gating circuit may be arranged to hold the output of the gating circuit at an inactive state when the flip-flop is reset.

The reset input of the flip-flop of each ith stage may be arranged to receive the reset signal from an output of the flip-flop of the (i+2)th stage.

The reset input of the flip-flop of each ith stage may be arranged to receive the reset signal from the output of the gating circuit of the (i+1)th stage.

The output of the gating circuit of each ith stage may be connected to the set input of the flip-flop of the (i+1)th stage via a delay circuit. Each delay circuit may comprise a plurality of cascade-connected inverters.

Each ith stage may comprise a switching arrangement for selectively causing the flip-flop set input to receive a set signal from the gating circuit of the (i+1)th stage and the flip-flop reset input to receive a reset signal from the (i-a)th stage.

At least some of the gating circuit outputs may constitute outputs of the generator.

At least some of the outputs of the flip-flops may constitute outputs of the generator.

The gating circuits may have inputs connected to the clock input.

Each of the gating circuits may comprise a pass gate and a holding device for holding the output of the pass gate at an inactive state when the flip-flop is reset.

Each of the pass gates may be a transmission gate comprising opposite conductivity metal-oxide-silicon field effect transistors whose source-drain paths are connected in antiparallel and whose gates are connected to direct and complementary outputs of the flip-flop.

The clock input may be a two phase input. The pass gates of consecutive stages may be connected to different clock input phases. The clock pulses passed by the pass gates of the stages may be of the same polarity.

The holding device of each stage may comprise a pull-down transistor whose control electrode is connected to a or the complementary output of the flip-flop.

The holding device of each stage may comprise a pull-up transistor whose control electrode is connected to a or the direct output of the flip-flop.

The clock input may be a single phase clock input. The clock pulses passed by the pass gates of consecutive stages may be of opposite polarity. The holding devices of the stages may comprise alternating pull-down and pull-up transistors, the control electrode of each pull-down transistor being connected to the complementary output of the associated flip-flop and the control electrode of each pull-up transistor being connected to the direct output of the associated flip-flop.

Each of the gating circuits may comprise a gated sense amplifier.

Each of the gating circuits may comprise a gated level shifter.

Each of the flip-flops may comprise: a first inverter, at least one of whose input and output constitutes an output of the flip-flop; a second controllable inverter, whose input and output are connected to the output and input, respectively, of the first inverter; and

an input circuit having first and second inputs constituting inputs of the flip-flop, the input circuit being arranged to supply to the input of the first inverter a signal corresponding to the states of the first and second inputs and to control the second inverter so as to switch the output of the second inverter to a high impedance state when the first or second input receives an active signal.

The first input may be an active high input and the second input may be an active low input. The input circuit may comprise: a first active device connected between a first power supply input and the input of the first inverter and having a control electrode constituting the second input; and a second active device, of opposite conduction type to the first active device, connected between a second power supply input and the input of the first inverter and having a control electrode constituting the first input. Each of the first and second active devices may be connected in an inverting configuration.

The second inverter may comprise third and fourth active devices of a first conduction type connected in series between a or the first power supply input and the output of the second inverter and fifth and sixth active devices of a second conduction type opposite the first type connected in series between a or the second power supply input and the output of the second inverter, the third and fifth active devices having control electrodes connected to the input of the second inverter and the fourth and sixth active devices having control electrodes connected to first and second inputs, respectively, of the input circuit. The control electrode of at least one of the third and fifth active devices may be connected to the input of the second inverter via a further active device. The or each further active device may have a control electrode connected to the first or second power supply input.

The first inverter may comprise a seventh active device connected between a or the first power supply input and the output of the first inverter and an eighth active device, of opposite conduction type to the seventh active device, connected between a or the second power supply input and the output of the first inverter, the seventh and eighth active devices having control electrodes connected to the input of the first inverter.

The generator may comprise a CMOS integrated circuit.

According to a second aspect of the invention, there is provided a spatial light modulator comprising a generator according to the first aspect of the invention.

The modulator may comprise a liquid crystal device.

According to a third aspect of the invention, there is provided a display comprising a modulator according to the second aspect of the invention.

It is thus possible to provide a clock pulse generator which is fully static. Such a generator is robust to capacitive interference and charge leakage and can operate at very low frequencies.

It is also possible to provide a clock pulse generator having a very high maximum frequency of operation. In particular, it is possible to provide a generator in which the clock pulses are required to charge only two transistor gates at a time (in addition to any external load when the gating circuit outputs constitute the outputs of the generator). Also, the clock signal can be fully gated. This is important for two reasons. Firstly, transistor loading of the clock signal limits its rise and fall times and hence the maximum frequency. With the present arrangement, loading of the clock is mainly due to parasitic elements so that high speed can be maintained for relatively large clock pulse generators.

Secondly, the capacitive loading of the clock signal by transistor gates can be minimised. In particular, only the gates of transistors in stages which are in their switching state are charged. This results in reduced power dissipation in the track resistance of circuit tracks carrying the clock signal.

The output pulses may be exact copies of the clock signal (degraded only by passage through the gating circuits). The gating circuits may be embodied as pass gates, which

may be made relatively large so that the drive capability is high. The output pulses when taken from the pass gates are guaranteed to be non-overlapping.

Although some embodiments require a two phase clock, others require only a single phase clock.

A variety of useful signals may be generated from each pair of consecutive stages and these include:

- (i) Independent non-overlapping (positive or negative) pulses of duration substantially equal to the clock pulse high period and synchronised with the clock rising edge;
- (ii) Independent non-overlapping (positive or negative) pulses of duration substantially equal to the clock low period and synchronised to the clock falling edge;
- (iii) Independent overlapping positive and negative pulses of duration substantially equal to the clock period and synchronised to the clock rising edge;
- (iv) Independent overlapping positive and negative pulses of duration substantially equal to the clock period and synchronised to the clock falling edge.

In the case of the non-overlapping pulses, the relative pulse widths may be changed merely by changing the mark-to-space ratio of the clock signal used to drive the clock pulse generator.

In some embodiments, voltage level shifting can be provided. In particular, the clock signal may be of lower voltage than the generator supply voltage so that a reduction in power consumption can be achieved. In some of these embodiments, the output pulses may have amplitudes corresponding to substantially the whole supply voltage despite operating with clock signals of substantially lower amplitude. Also, in some embodiments, the generator can operate selectively in either direction ("forward" or

“reverse”). This is advantageous in some applications, such as display driving in which the displayed image may need to be spatially inverted.

The invention will be further described, by way of example, with reference to the accompanying drawings, in which:

Figure 1 is a circuit diagram of two stages of a known type of shift register;

Figure 2 is a diagram illustrating waveforms occurring in the stages shown in Figure 1;

Figure 3 is a block circuit diagram of a known type of clock pulse generator;

Figure 4 is a circuit diagram of two stages of a static clock pulse generator constituting an embodiment of the invention;

Figure 5 is a block diagram of the clock pulse generator whose stages are shown in Figure 4;

Figure 6 is a timing diagram illustrating waveforms occurring in the clock pulse generator shown in Figures 4 and 5;

Figure 7 is a circuit diagram of two stages of a static clock pulse generator constituting an embodiment of the invention;

Figure 8 is a block diagram of a clock pulse generator whose stages are illustrated in Figure 7;

Figure 9 is a circuit diagram of two stages of a static clock pulse generator constituting an embodiment of the invention;

Figure 10 is a timing diagram illustrating waveforms occurring in a clock pulse generator whose stages are shown in Figure 9;

Figure 11 is a circuit diagram of two stages of a static clock pulse generator constituting an embodiment of the invention;

Figure 12 is a circuit diagram of two stages of a static clock pulse generator constituting an embodiment of the invention;

Figure 13 is a circuit diagram of two stages of a static clock pulse generator constituting an embodiment of the invention;

Figure 14 is a schematic diagram of a reset-set flip-flop which may be used in the stages illustrated in Figures 4, 7, 9 and 11 to 13;

Figure 15 is a circuit diagram of the flip-flop shown in Figure 14;

Figure 16 is a timing diagram illustrating waveforms occurring in the flip-flop of Figure 15;

Figure 17 is a circuit diagram of two stages of a static clock pulse generator constituting an embodiment of the invention;

Figure 18 is a circuit diagram of a reset-set flip-flop which may be used in the stages shown in Figure 17;

Figure 19 is a timing diagram illustrating waveforms occurring in the flip-flop of Figure 18;

Figure 20 is a timing diagram illustrating output waveforms of the flip-flops of Figures 15 and 18 during a set operation;

Figure 21 is a timing diagram illustrating output waveforms of the flip-flops of Figures 15 and 18 during a reset operation;

Figure 22 is a circuit diagram of two stages of a static clock pulse generator constituting an embodiment of the invention;

Figure 23 is a circuit diagram of a reset-set flip-flop which may be used in the stages shown in Figure 22;

Figure 24 is a circuit diagram of a modified flip-flop of the type shown in Figures 18 and 23;

Figure 25 is a circuit diagram of another modified flip-flop of the type shown in Figures 18 and 23;

Figure 26 is a diagram illustrating low input voltage operation ;

Figure 27 is a circuit diagram of a flip-flop of the type shown in Figures 18 and 23 modified for low input voltage operation;

Figure 28 is a circuit diagram of two stages of a static clock pulse generator constituting an embodiment of the invention;

Figure 29 is a circuit diagram of a gated sense amplifier which may be used in the stages shown in Figure 28;

Figure 30 is a circuit diagram of a gated differential voltage level shifter which may be used in the stages shown in Figure 28;

Figure 31 comprises circuit diagrams of one stage of a bi-directional static clock pulse generator constituting an embodiment of the invention;

Figure 32 is a more detailed circuit diagram of a bi-directional stage similar to that shown in Figure 31;

Figure 33 is a block diagram of the clock pulse generator, one of whose stages is shown in Figure 32;

Figures 34a and 34b are a circuit diagram of one stage of another bi-directional static pulse generator constituting an embodiment of the invention; and

Figure 35 is a block schematic diagram of a spatial light modulator constituting an embodiment of the invention.

Like reference numerals refer to like parts throughout the drawings.

In the following description, four types of pulses (each of half the clock pulse period) are identified as follows:

Pp: positive pulses: coinciding with positive-going pulses of clock signal CK;

Pn: positive pulses: coinciding with negative-going pulses of clock signal CK;

Np: negative pulses: coinciding with positive-going pulses of clock signal CK;

Nn: negative pulses: coinciding with negative-going pulses of clock signal CK;

Figure 4 shows two stages 1 and 2 of a static clock pulse generator. The stage 1 comprises a reset-set (RS) flip-flop 3 having a reset input R, a set input S, a direct output Q and a complementary or inverted output !Q. The set input S is connected to an input of the stage for receiving a set signal Pn from the preceding or (n-1)th stage,

which signal is also the output signal of the preceding stage. The reset input R is connected to an input F_i for receiving a reset signal from the $(n+1)$ th stage.

The outputs Q and \bar{Q} of the flip-flop 3 are connected to gate inputs G and \bar{G} , respectively, of a gating circuit 4, which has complementary clock inputs CK and \bar{CK} , which are connected to the complementary phases of a two phase clock input CK and \bar{CK} , respectively. However, depending on the actual arrangement of the gating circuit 4, only one of the flip-flop outputs may be used for a gating circuit 4 having a single gate input. Similarly, the gating circuit 4 may have a single clock input connected to one of the clock phases or to a single clock phase. The output O of the gating circuit 4 is connected to the output P_p of the stage 1 for supplying a set signal to the following or $(n+1)$ th stage. Also, the output O of the gating circuit 4 is connected to an output F_o for supplying a reset signal to the preceding or $(n-1)$ th stage.

The stage 2 shown in the lower part of Figure 4 differs from the stage 1 in that the stage 2 receives a set signal P_p from the $(n-1)$ th stage and supplies a set signal P_n to the $(n+1)$ th stage. Also, the gating circuit 4 of the stage 1 is arranged to supply positive pulses P_p coinciding with the positive-going pulses of the clock signal CK whereas the stage 2 is arranged to supply at its output positive pulses P_n coinciding with negative-going pulses of the clock signal CK (which coincide with positive-going pulses of the complementary clock signal \bar{CK}).

The gating circuit 4 is controlled by either or both outputs Q and \bar{Q} of the flip-flop 3 in each stage so as to transmit a single clock pulse from one of the clock inputs CK and \bar{CK} . When the gating input signals to the circuit 4 are inactive, i.e. when the flip-flop 3 is reset, the output O of the circuit 4 and hence of the stage 1 or 2 is held low.

Figure 5 shows part of a static clock pulse generator which comprises N stages 1, 2 connected in cascade. The stages 1 alternate with the stages 2. The set signal input P_n of the first stage is arranged to receive a start pulse SP whereas the clock inputs are connected to receive complementary clock signals CK and \bar{CK} from the two phase

clock input. The input F_i of each stage 1, 2 is connected to the output F_o of the following stage. The input F_i of the last or N th stage is connected to ground gnd.

Operation of the static clock pulse generator is illustrated by the timing diagram of Figure 6 which illustrates various waveforms occurring in the first three stages of the generator of Figure 5. Initially, the flip-flops 3 of all of the stages 1, 2 are in a reset state so that the direct outputs Q are low, the complementary outputs \bar{Q} are high and the outputs P_n and P_p are all low.

At time t_n , a start pulse SP is supplied to the input P_n of the first stage 1. The flip-flop 3 of this stage is set so that the output Q goes high and the complementary output \bar{Q} goes low. The gating circuit 4 is thus switched on and the output signal P_p of the first stage follows the clock signal CK .

At time t_{n+1} , the clock signal CK goes high so that the output signal P_p of the first stage 1 goes high. The flip-flop 3 of the second stage 2 is set so that its outputs Q and \bar{Q} go high and low, respectively. The gating circuit 4 of the second stage 2 is switched on so that the output signal P_n of the second stage 2 follows the complementary clock signal \bar{CK} .

At time t_{n+2} , the complementary clock signal \bar{CK} goes high and hence so does the output signal P_n of the second stage 2. The flip-flop of the third stage 1 is thus set and its output Q goes high. The signal P_n is fed back to the reset input R of the flip-flop 3 of the first stage 1, which is therefore reset (as illustrated at A in Figure 6). The gating circuit 4 of the first stage 1 is switched off so that the output P_p of the first stage 1 remains held at ground potential until another start pulse is received.

The stages 1 and 2 shown in Figure 7 differ from those shown in Figure 4 in the feedback arrangements of resetting pulses. Each stage 1, 2 has an input F for receiving a reset signal from the $(n+1)$ th stage and for routing this to an output F in order to supply the reset signal to the $(n-1)$ th stage. In each stage 1, 2, the reset signal is supplied by the Q output of the flip-flop 3 via the output F_o to the $(n-1)$ th stage. Similarly, the reset

input R of the flip-flop 3 connected to the input F_i receives a reset signal from the $(n+2)$ th stage.

Because the flip-flop outputs respond to the pulses generated by the gating circuits 4, the delay between each gated pulse and the response of the flip-flop is small. The timing of signals occurring in the clock pulse generator shown in Figure 8 and comprising the stages 1 and 2 shown in Figure 7 are therefore similar to those occurring in the clock pulse generator shown in Figure 5 so that the waveforms are almost identical to those illustrated in Figure 6. However, as illustrated by the broken line B in Figure 6, the rising edge of the flip-flop output Q of the third stage resets the signal Q of the first stage so that these signals are guaranteed to be overlapping. This may be an important feature if further logic signals of a certain type are required to be generated from the outputs Q of the flip-flops 3 by combinational logic.

Conversely, some applications require that the outputs Q of every other stage should be non-overlapping, in which case the stages 1 and 2 shown in Figure 9 may be used. The stages 1 and 2 shown in Figure 9 differ from those shown in Figure 4 in that the output of each stage is connected to the output O of the gating circuit 4 via a delay circuit 5, which may be embodied as an even number of series connected or cascaded inverters. However, the feedback reset signal to the preceding stage is supplied directly from the output O of the gating circuit 4 via the output F_o and so is not delayed. This ensures that the flip-flop of the preceding stage is reset before the flip-flop of the succeeding stage is set. Figure 10 illustrates the effect of this on the outputs Q and \bar{Q} of the flip-flops of consecutive stages. This may be used by suitable combinational logic to derive further logic signals.

Figure 11 shows stages 1 and 2 of the type shown in Figure 7 in which the gating circuits 4 are embodied in the form of transmission gates. In particular, the outputs Q and \bar{Q} of each flip-flop 3 are connected to the gates of transistors T1 and T2, respectively, whose source-drain paths are connected in antiparallel to form a transmission gate. The input of the transmission gate T1, T2 is connected to the phase CK or the phase \bar{CK} of the two phase clock input in the stage 1 or the stage 2,

respectively. The output of the transmission gate T1, T2 is connected to the output Pp or Pn of the stage 1 or 2, respectively. A pull-down transistor T3 has a source connected to a ground or power supply input gnd, a drain connected to the output Pp of the stage 1 or Pn of the stage 2, and a gate connected to the complementary output !Q of the flip-flop 3.

When the flip-flop 3 is in its reset state, the transmission gate T1, T2 is switched off and the transistor T3 holds the output of the stage at ground potential. When the flip-flop 3 is in its set state, the transmission gate T1, T2 is switched on to connect the stage output to the appropriate clock phase and the pull-down transistor T3 is disabled.

The stages 1 and 2 shown in Figures 4, 7, 9 and 11 supply positive pulses at the outputs Pp and Pn synchronised with the rising edges of the clock pulses CK and !CK. However, it is also possible to provide a static clock pulse generator which supplies negative output pulses Nn and Np. Figure 12 illustrates stages 1 and 2 which provide such pulses and which may be connected together as shown in Figure 8 to form a static clock pulse generator.

The stage 1 shown in Figure 12 differs from that shown in Figure 11 in that an inverter 6 is connected between the input Np and the set input S of the flip-flop 3 and the output Nn is provided with a pull-up transistor T3 whose source is connected to a power supply input vdd and whose gate is connected to the direct output Q of the flip-flop 3. Similarly, the stage 2 shown in Figure 12 differs from that shown in Figure 11 in that an inverter 6 is connected between the input Nn and the set input S of the flip-flop 3 and the output Np is provided with a pull-up transistor T3 whose gate is connected to the direct output Q of the flip-flop 3.

Figure 13 illustrates stages 1 and 2 which may be connected together as shown in Figure 8. The stage 1 supplies positive going output signals Pp whereas the stage 2 supplies negative going output signals Nn. The stage 1 differs from that shown in Figure 11 in that an inverter 6 is provided between the input Nn and the set input S of the flip-flop 3. The stage 2 differs from that shown in Figure 12 in that the inverter 6 is omitted and the

input of the transmission gate T1, T2 is connected to the single phase clock input CK. Thus, the whole static clock pulse generator requires a single phase clock input CK and alternate stages provide opposite polarity output signals or pulses.

The flip-flops 3 may be embodied in any suitable way. For example, a known type of RS flip-flop comprises a pair of cross-coupled NOR gates as shown in Figure 14 and as disclosed in F. Hill and G. Peterson, "Digital Logic and Microprocessors", John Wiley and Sons, 1984. The flip-flop comprises a pair of two input gates NOR1 and NOR2. One of the inputs of the gate NOR1 comprises a set input S whereas one of the inputs of the gate NOR2 comprises a reset input R. The output of the gate NOR1 comprises a complementary output \bar{Q}_t of the flip-flop and is connected to the second input of the gate NOR2. The output of the gate NOR2 comprises an output Q of the flip-flop and is connected to the second input of the gate NOR1. The output Q and the complementary output \bar{Q}_t respond to set and reset signals in accordance with the following truth table:

S	R	Q_t	\bar{Q}_t
0	0	Q_{t-1}	\bar{Q}_{t-1}
0	1	0	1
1	0	1	0
1	1	Undefined	

where 0 and 1 represent logic low and logic high levels, Q_t and \bar{Q}_t represent the current states of the outputs and Q_{t-1} and \bar{Q}_{t-1} represent the preceding states of the outputs.

Thus, when the set and reset signals S and R are both 0, the outputs Q and \bar{Q} retain their prior states and are thus latched. When the set input S goes high, the flip-flop is set and the output Q goes high. When the reset input R goes high, the flip-flop is reset and the output Q goes low. The output states are undefined when the set and reset inputs are both high and a designer must ensure that this condition does not occur.

The RS flip-flop shown in Figure 14 may be embodied as an eight transistor CMOS integrated circuit of known type as shown in Figure 15. The gate NOR1 comprises P-type transistors I2 and G2 and N-type transistors M2 and I1 whereas the gate NOR2 comprises P-type transistors I4 and G4 and N-type transistors M4 and I3.

Figure 16 of the accompanying drawings is a graph showing four waveform diagrams against a common time axis of signals occurring at the inputs R and S and at the outputs Q and !Q. The waveforms represent a simulation of the flip-flop illustrated in Figure 15 using arbitrary voltage levels and poor transistor performance to emphasise the relative timing of signal edges. For the purposes of the simulation, all of the transistors are of equal size and the outputs Q and !Q are each loaded with a unit inverter.

The stages 1, 2 shown in Figure 17 differ from those shown in Figure 11 in that the flip-flop 3 has an active low reset input !R. Also, the reset signals fed back from each stage to the stage before the preceding stage are supplied by the complementary output !Q of the flip-flop 3.

The stages 1, 2 as shown in Figure 17 allow the flip-flops 3 to be embodied by an improved type of flip-flop as shown in Figure 18. The flip-flop 3 comprises an input circuit IN1 comprising a first P-type transistor 11 and an N-type transistor 12 connected in series between a first power supply input or line vdd and a ground or second power supply input or line gnd. The first transistor 11 has a gate which is connected to an active low reset input !R. The reset signal supplied to the input !R is therefore normally at logic high or 1, for example at the voltage of the supply line vdd, and switches to the logic low or 0, such as zero or ground voltage, when the flip-flop is to be reset. The gate of the second transistor 12 is likewise connected to a set input S which is active high i.e. normally at logic low but switching to logic high when the flip-flop is to be set.

The flip-flop further comprises a first inverter X1 and a second controllable inverter X2. The second inverter X2 comprises third and fourth P-type transistors 13 and 14 and fifth and sixth N-type transistors 15 and 16 connected in series between the supply lines vdd and gnd. The sources of the third and fifth transistors 13 and 15 are connected to the supply lines vdd and gnd, respectively whereas the gates are connected together to form the input of the inverter X2. The drains of the third and fifth transistors 13 and 15 are connected to the sources of the fourth and sixth transistors 14 and 16, respectively. The drains of the fourth and sixth transistors 14 and 16 are connected together to form the

output of the second inverter X2. The gate of the fourth transistor 14 is connected to the set input S whereas the gate of the sixth transistor 16 is connected to the reset input !R.

The first inverter X1 comprises a seventh P-type transistor 17 and an eighth N-type transistor 18 which are connected in series between the supply lines vdd and gnd. The gates of the transistors 17 and 18 are connected together to form the input of the first inverter X1 whereas the drain of the transistors 17 and 18 are connected together to form an output Q of the flip-flop. The input of the first inverter X1 is connected to the output of the second inverter X2 and to a complementary output !Q of the flip-flop. The output of the first inverter X1 is connected to the input of the second inverter X2. The input of the first inverter X1 is connected to the output of the input circuit IN1 formed by the drains of the transistors 11 and 12.

Because the flip-flop shown in Figure 18 has an active high set input S and an active low reset input !R, its response to logic level signals differs from the arrangement illustrated in Figures 14 and 15. The response to the various combinations of logic level input signals is as follows:

S	!R	Q _t	!Q _t
0	1	Q _{t-1}	!Q _{t-1}
0	0	0	1
1	1	1	0
1	0	Undefined	

where the symbols are as described hereinbefore. When the set signal is inactive (logic 0) and the reset signal is inactive (logic 1), the transistors 11 and 12 are switched off whereas the transistors 14 and 16 are conductive. The inverter X2 therefore functions

as an inverter such that the signal at its output is the logical complement of the signal at its input. The flip-flop therefore comprises cross-coupled inverters with the outputs Q and !Q locked in opposite logic states which depend on whether the flip-flop was more recently set or reset.

If the flip-flop was more recently reset such that the output Q is at logic level 0 and the output !Q is at logic level 1, the flip-flop may be set by applying an active set signal (logic 1) to the set input S while the reset input !R remains at logic level 1 corresponding to the inactive reset signal. The second transistor 12 is thus turned on whereas the fourth transistor 14 is turned off so as to isolate the output of the second inverter X2 from the first supply line vdd. The input of the first inverter X1, which is connected to the output of the second inverter X2, is therefore pulled low by the transistor 12 so that the output Q is set to logic 1. This is fed back to the transistor 15, which ensures that the input of the inverter X1 is held at logic 0 after the set signal has ceased and the transistor 12 is switched off. The transistor 13 is similarly switched off by the feedback signal.

If the flip-flop was more recently set such that the output Q is at logic 1 and the output !Q is at logic 0, the flip-flop can be reset by an inactive set signal (logic 0) and an active reset signal (logic 0). In this case, the first transistor 11 is turned on by the active reset signal whereas the transistor 16 is turned off. A logic level 1 is supplied to the input of the inverter X1 which therefore supplies a logic 0 signal at the output Q. This is fed back to the input of the second inverter X2 so that the transistor 13 conducts and the transistor 15 is switched off. When the reset signal returns to its inactive (logic 1) level, the cross-coupled inverters X1 and X2 retain the reset state.

As described hereinbefore, the output states for both the set and the reset signals being active are not defined. If both signals were active, then both transistors 11 and 12 would conduct between the supply lines vdd and gnd and the output of the input circuit IN1 would be undefined. It is therefore essential for a designer to ensure that the input signals of the flip-flop cannot both be active at the same time.

Figure 19 illustrates input and output waveforms of the circuit of Figure 18 for set and reset operations. These waveforms were obtained by simulation using the same parameters as were used to obtain the waveforms shown in Figure 16. At time T1, the flip-flop of Figure 18 is set and the complementary output \bar{Q} responds before the output Q . Similarly, at time T2, the flip-flop is reset and the complementary output \bar{Q} responds before the output Q . The flip-flop therefore provides the more desirable symmetrical switching behaviour which is advantageous in high speed logic circuits.

Figures 20 and 21 compare the performance of the flip-flop of Figure 18 with that of the flip-flop of Figure 15 for set and reset transitions, respectively. These waveforms were obtained by simulation using the same parameters, namely equal-sized transistors of identical performance with each of the outputs driving a unit inverter load and the voltage waveforms being measured at the inputs of these inverters.

As shown in Figure 20, the flip-flops are set at time T1. The outputs \bar{Q} of the "New RS flip-flop" of Figure 18 and of the "NOR RS flip-flop" of Figure 15 discharge at approximately the same rate. However, the speed of response of the outputs Q is substantially different. The output Q of the "new" flip-flop reaches the logic high state at a time T3, which is approximately 20% faster than the time taken for the output Q of the known circuit to reach the same logic level (at time T2).

As shown in Figure 21, the flip-flops are reset at time T1. The output Q of the flip-flop of Figure 15 and the output \bar{Q} of the flip-flop of Figure 18 discharge and charge, respectively, at approximately the same rate. However, the output Q of the flip-flop of Figure 18 reaches the logic low state at time T3 substantially faster than the output \bar{Q} of the flip-flop of Figure 15 reaches the logic high state at time T2.

Figure 22 illustrates stages 1 and 2 which differ from those shown in Figure 12 in that the inverters 6 are omitted and the flip-flops 3 have active low set inputs \bar{S} . These stages may make use of flip-flops having substantially the same architecture as illustrated in Figure 18. A suitable flip-flop of this type is illustrated in Figure 23, in which the inputs and outputs have been swapped. In this case, the gate of the first

transistor 1 is connected to an active low set input \bar{S} whereas the gate of the second transistor 2 is connected to an active high reset input R . The output of the inverter X_1 is connected to the complementary output \bar{Q} whereas the output of the inverter X_2 is connected to the output Q . With this configuration, the transitions at the output Q always precede the corresponding transitions at the output \bar{Q} . Otherwise, the operation of the flip-flop of Figure 23 is substantially the same as that of Figure 18. The corresponding truth table for the flip-flop of Figure 23 is as follows:

\bar{S}	R	Q_t	\bar{Q}_t
1	0	Q_{t-1}	\bar{Q}_{t-1}
1	1	0	1
0	0	1	0
0	1	Undefined	

The relative position of the transistors 13 and 14 and of the transistors 15 and 16 in the second inverter is not important to the correct operation of the flip-flop. For example, as shown in Figure 24, the transistor 14 may be disposed between the first supply line vdd and the transistor 13 and the transistor 16 may be disposed between the second supply line gnd and the transistor 15. Also, pairs of transistors with their source-drain paths connected in series maybe replaced by multiple gate devices. For example, as shown in Figure 25, the transistor 13 and 14 are replaced by a dual gate transistor D_1 and the transistors 15 and 16 are replaced by a dual gate transistor D_2 .

Although the flip-flops described hereinbefore with reference to Figures 18 and 23 to 25 are intended to operate with standard logic level signals such that the logic level 1 signal has the value of the voltage on the first power supply line vdd and the logic level 0 signal has the voltage on the second supply line gnd , these embodiments are capable operating on lower voltage input signals and may therefore perform level shifting. For example, as shown in Figure 26, the set input S is capable of responding to an active high set signal having a voltage of V_s which is less than the supply voltage vdd (relative to the ground potential). Similarly, the active low reset input \bar{R} of the embodiment of Figure 18 is capable of responding to a reset signal whose voltage V_r is greater than the

ground potential. For example, during a set operation of the flip-flop of Figure 18, the transistor 12 can be turned on with a gate-source voltage which is less than the supply voltage. However, the transistor 14 may not be completely turned off because its gate-source voltage is equal to the difference between the supply voltage and the voltage of the set signal. There may therefore be a momentary conflict between the operation of the transistor 12 and the transistors 13 and 14 and, depending on the actual magnitude of the set signal and the threshold voltages of the transistors, the flip-flop may or may not change state. The minimum value of the magnitude of the set signal required for the flip-flop to change state and become set may be increased by making the transistor 12 large in comparison to the transistors 13 and 14. This is the usual configuration for fast circuits with high drive capability outputs.

The flip-flop shown in Figure 27 represents a modified version of that shown in Figure 18 and is further optimised for low input voltage operation. A further P-type transistor F1 arranged as a pass transistor is connected between the output of the first inverter X1 and the gate of the transistor 13. The gate of the transistor F1 is connected to the second supply line gnd.

The operation of the flip-flop of Figure 27 relies on the fact that the transistor F1 can only pass a logic level 0 degraded by a threshold voltage. Thus, following a reset operation, the condition of the flip-flop is such that the gate of the transistor 13 is at a potential close to the threshold voltage of the transistor F1. This ensures that the transistor 13 is only weakly turned on and that the combined pull-up drive of the transistors 13 and 14 is reduced. Consequently, during a subsequent setting operation, the flip-flop can be set with a lower input voltage Vs than could otherwise be achieved.

The same technique may be applied to increase the minimum active low resetting voltage. In this case, an N-type transistor arranged as a pass gate is connected between the output of the inverter X1 and the gate of the transistor 15 with its gate electrode connected to the first supply line vdd.

The modifications illustrated in Figures 24, 25 and 27 may equally be applied to the flip-flops illustrated in Figures 18 and 23.

Figure 28 illustrates modified stages 1 and 2 which employ an alternative technique for providing low voltage operation. This technique may be used with single phase or two phase clock signals of amplitudes substantially lower than the power supply voltage. The stages 1 and 2 shown in Figure 28 differ from those shown in Figure 4 in that each of the gating circuits 4 is embodied as a gated level-shifter or gated sense amplifier. Thus, the gating circuits performs voltage level-shifting of the clock pulses.

Figure 29 illustrates in more detail a gated sense amplifier which may be used as the gating circuit 4. The amplifier comprises ninth and tenth N-type transistors 19 and 20 and eleventh to thirteenth P-type transistors 21 to 23 arranged as a cross-coupled sense amplifier, for instance of the type disclosed in A. Bellaouar and M. Elmasry, "low-power digital VLSI design circuits and systems", Kluwer Academic Publishers, 1995. The sources of the transistors 19 and 20 are connected to ground whereas the drains thereof are connected to the drains of the transistors 21 and 22 and to the gates of the transistors 20 and 19, respectively. The sources of the transistors 21 and 22 are connected to the drain of the transistor 23 whose source is connected to the supply input vdd. The gate of the transistor 23 is connected to the complementary gate input !G.

The amplifier further comprises fourteenth to sixteenth N-type transistors 24 to 26. The sources of the transistors 24 and 25 are connected to the direct and complementary clock inputs CK and !CK whereas the gates thereof are connected together to the gate input G. The drains of the transistors 24 and 25 are connected to the gates of the transistors 21 and 22, respectively. The source-drain path of the transistor 26 is connected between the output O and ground gnd whereas the gate thereof is connected to the complementary gate input !G.

When the gated sense amplifier 4 is enabled such that the gating signals G and !G are high and low, respectively, the transistors 24 and 25 pass the clock signals to the gates of the transistors 21 and 22. The transistor 23 is grounded such that the sense amplifier

operates with a high tail current. The transistor 26 is switched off so that the output O follows the logic state of the clock input CK with an appropriate level shift.

The amplifier is disabled when the signals G and !G are low and high, respectively, so that the transistors 24 and 25 isolate the clock inputs. The transistor 23 is turned off so as to stop current flow through the amplifier. The pull-down transistor 26 is turned on so that the output O is held at its default logic low state.

Figure 30 illustrates a gated level shifter which may be used as the gating circuit 4. The level shifter comprises seventeenth to nineteenth P-type transistors 27 to 29 and a twentieth N-type transistor 30. The sources of the transistors 27 and 29 are connected to the power supply input vdd. The gate of the transistor 27 is connected to the complementary gate input !G whereas the drain thereof is connected to the source of the transistor 28. The drain of the transistor 28 is connected to ground. The drain of the transistor 29 is connected to the drain of the transistor 30, whose source is connected to the complementary clock input !CK and whose gate is connected to the source of the transistor 28.

The drains of the transistors 29 and 30 are connected to the gate of a twenty first P-type transistor 31 and a twenty second N-type transistor 32. The sources of the transistors 31 and 32 are connected to the power supply inputs vdd and gnd, respectively, whereas the drains thereof are connected together and to the output O.

A twenty third N-type transistor 33 has a drain connected to the gates of the transistors 28 and 29, a source connected to the clock input CK and a gate connected to the gate input G. Twenty fourth and twenty fifth N-type transistors 34 and 35 have gates connected to the complementary gate input !G, sources connected to ground gnd, and drains connected to the gates of the transistors 30 and 29, respectively.

When the level shifter is enabled by high and low gating signals G and !G, respectively, the transistor 33 passes the clock signals to the gates of the transistors 29 and 30. The transistors 27 and 28 operate as a source follower with the transistor 27 switched hard

on so as to provide maximum boost to the input signal. The transistors 34 and 35 are switched off and the circuit operates as a differential input level shifter so that the output O follows the logic state of the clock phase CK.

When the level shifter is disabled by low and high inputs G and !G, respectively, the transistors 34 and 35 are turned on so as to ensure that the transistor 30 is turned off, the transistor 29 is turned on and the output of the inverter formed by the transistors 31 and 32 is held low. The transistor 33 isolates the clock phase CK.

In the arrangements shown in Figures 29 and 30, the clock phases CK and !CK do not drive transistor gates directly but instead are gated by the transistors 24, 25, 30 and 33 which act as pass gates.

Figure 31 illustrates a stage 1 of the type shown in Figure 11 modified for bi-directional operation. The upper part of Figure 31 illustrates the configuration for generating pulses in sequence from left to right whereas the lower part of Figure 31 illustrates the configuration for generating pulses in sequence from right to left. Similar modifications may be made in the other types of stages described hereinbefore.

The modification comprises providing electronic switches 7 and 8, for instance in the form of transmission gates, for controlling the directions in which set and reset pulses are passed from stage to stage. Thus, the stage 1 has left and right feed back connections Fo which are selectively connected to the output Q of the flip-flop by the switch 7. Similarly, the stage has left and right outputs Pp for set pulses supplied from the output of the transmission gate T1, T2 in accordance with the position of the switch 8. As shown in the upper part of Figure 31, for operation from left to right, the switch 7 directs reset pulses from the output Q of the flip-flop to the left and via the preceding stage to the stage before the preceding stage where such pulses are used to reset the flip-flop. The output pulses from the transmission gate T1, T2 are supplied to the succeeding stage for setting the flip-flop thereof.

As shown in the lower part of Figure 31, operation from right to left occurs when the switches 7 and 8 are in their alternative positions. In this case, the reset pulses from the output Q of the flip-flop are supplied to the right via the following stage to the stage after the following stage for resetting the flip-flop thereof. The switch 8 directs the output signal to the left to the preceding stage for setting the flip-flop thereof.

Figure 32 illustrates a bi-directional stage of the type shown in Figure 31 but rearranged slightly for use with flip-flops 3 of the type shown in Figure 25. The switch 7 is embodied by two transmission gates formed by transistors B1 to B4 whereas the switch 8 is embodied by transmission gates formed by transistors B5 to B8. The direction of operation is controlled by direction control signals on lines L and !L. The output of the stage is indicated at S_O.

The transistors B1, B2, B7 and B8 are turned on and the transistors B3, B4, B5 and B6 are turned off for operation from left to right. Conversely, the transistors B3, B4, B5 and B6 are turned on and the transistors B1, B2, B7 and B8 are turned off for operation from right to left. The transmission gates B5, B6 and B7, B8 supply the clock pulse output to output terminals QR and QL, respectively, depending on the direction of operation. The transmission gates B1, B2 and B3, B4 pass the signal from the complementary output !Q to the stage two places to the left or right, respectively, in order to reset the flip-flop thereof at the appropriate time. A reset transistor R1 is connected between a supply line vdd and the drains of the transistors 11 and 12 and has a gate connected to a reset line RESET. This arrangement ensures that all of the flip-flops of the stages are reset in response to a single signal, for instance when power is supplied to the generator. The various inputs and outputs D, FRL, F, FLR, FL and FR provide routing between stages for the various signals.

The stage 1 shown in Figure 32 is of the type which provides positive output pulses Pp synchronised with the rising edge of the clock signals CK. A stage 2 for providing positive output pulses Pn synchronised with the rising edge of the complementary clock signal !CK differs from the stage shown in Figure 32 in that the input of the transmission gate T1, T2 is connected to the complementary clock line !CK.

Figure 33 illustrates a static clock pulse generator comprising stages of this type arranged in cascade. This drawing illustrates the interconnections between consecutive stages. In addition to a start pulse SPL for operation from left to right, a start pulse SPR is required for the Nth stage for operation from right to left. Direction control lines L and !L receive complementary signals for determining whether operation is from left to right or from right to left. A common reset line receives a common reset signal RESET for resetting the flip-flops 3 of all of the stages before commencing operation.

When stages of the type shown in Figure 32 are operated with low voltage clock inputs, several of the transistors are redundant and may be omitted. For example, if the clock pulses are of much lower voltage than the power supply voltage, the P-type device T2 is superfluous and the N-type device T1 can easily pass the lower voltage signal. If the clock signals swing between gnd and vdd supply lines, the device T1 can only pass a logic high stage degraded by its threshold voltage to the transistors 11 and 12 of the succeeding stage. However, because the flip-flop devices can be optimised, the flip-flop may still be set with such a signal. If the transistor T2 is omitted, the P-type devices B5 and B7 are not required.

The feedback signal passed by the transmission gates B1, B2 and B3, B4 is a negative going pulse. All transistors may not be needed because the P-type devices B1 and B3 can pass the logic low signal, possibly with acceptable degradation, sufficiently well to force resetting of the flip-flop.

Figures 34a and 34b illustrate another type of bi-directional stage for a static clock pulse generator. This stage comprises a flip-flop formed by transistors 11 to 18 as shown in Figure 25 and a gated level shifter formed by transistors 27 to 35 as shown in Figure 30. The transmission gate transistors B1 to B8 correspond to and perform the same functions as the transistors B1 to B8 shown in Figure 32. Transistors D1 to D6 form a delay circuit of the type illustrated in at 5 in Figure 9 so as to ensure that the outputs S_O of every other stage do not overlap. A reset transistor R1 as shown in Figure 32 is

also provided. This stage is shown as providing output signals S_O and S_O2, either or both of which may be used depending on the circuit application.

The stage illustrated in Figures 34a and 34b provides positive pulses Pp synchronised with the positive-going pulses of the clock signal CK. However, in order to provide positive pulses Pn coinciding with the negative-going pulses of the clock signal CK, it is merely necessary to swap the clock input connections CK and !CK.

The static clock pulse generator may be embodied as or as part of a CMOS integrated circuit. For use in a picture element (pixel) matrix display, such a generator may be implemented in LSI (large scale integration) driver integrated circuits or on the display substrate using any suitable silicon-on-insulator technology.

Figure 35 illustrates a display comprising a display matrix 40 of N rows by M columns of pixels, for instance in the form of a spatial light modulator comprising a liquid crystal device. The display further comprises an address signal generator 41 comprising a clock pulse generating circuit 42 and a set of data line drivers 43. The clock pulse generating circuit 42 comprises a generator of any of the types described hereinbefore and illustrated in Figures 4 to 34b. A scan signal generator 44 supplies scan signals to the rows of pixels and comprises a clock pulse generating circuit 45 and a set of scan line drivers 46. The clock pulse generating circuit 45 comprises a generator of any of the types described hereinbefore and illustrated in Figures 4 to 34b. The clock pulse generating circuits generate clock pulses at pixel data rate for the circuit 42 and at line data rate for the circuit 45.

CLAIMS:

1. A static clock pulse generator comprising a clock input and N stages, each ith one of the stages comprising a reset-set flip-flop having a set input for receiving a set signal from a gating circuit output of the (i-1)th stage and a reset input for receiving a reset signal from an (i+a)th stage, where a is greater than or equal to one, and a gating circuit for passing a clock pulse from the clock input to an output of the gating circuit when the flip-flop is set, where $1 < i \leq (N-a)$.
2. A generator as claimed in claim 1, in which the gating circuit is arranged to hold the output of the gating circuit at an inactive state when the flip-flop is reset.
3. A generator as claimed in claim 1 or 2, in which the reset input of the flip-flop of each ith stage is arranged to receive the reset signal from an output of the flip-flop of the (i+2)th stage.
4. A generator as claimed in claim 1 or 2, in which the reset input of the flip-flop of each ith stage is arranged to receive the reset signal from the output of the gating circuit of the (i+1)th stage.
5. A generator as claimed in any one of the preceding claims, in which the output of the gating circuit of each ith stage is connected to the set input of the flip-flop of the (i+1th) stage via a delay circuit.
6. A generator as claimed in claim 5, in which each delay circuit comprises a plurality of cascade-connected inverters.
7. A generator as claimed in any one of the preceding claims, in which each ith stage comprises a switching arrangement for selectively causing the flip-flop set input to receive a set signal from the gating circuit of the (i+1)th stage and the flip-flop reset input to receive a reset signal from the (i-a)th stage.

8. A generator as claimed in anyone of the preceding claims, in which at least some of the gating circuit outputs constitute outputs of the generator.
9. A generator as claimed in any one of the proceeding claims, in which at least some of the outputs of the flip-flops constitute outputs of the generator.
10. A generator as claimed in any one of the preceding claims, in which the gating circuits have inputs connected to the clock input.
11. A generator as claimed in any one of the preceding claims, in which each of the gating circuits comprises a pass gate and a holding device for holding the output of the pass gate at an inactive state when the flip-flop is reset.
12. A generator as claimed in preceding claim 11, in which each of the pass gates is a transmission gate comprising opposite conductivity metal-oxide-silicon field effect transistors whose source-drain paths are connected in antiparallel and whose gates are connected to direct and complementary outputs of the flip-flop.
13. A generator as claimed in any one of the preceding claims, in which the clock input is a two phase clock input.
14. A generator as claimed in claim 13 when dependent on claims 10 and 11, in which the pass gate inputs of consecutive stages are connected to different clock input phases.
15. A generator as claimed in claim 14, in which the clock pulses passed by the pass gates of the stages are of the same polarity.
16. A generator as claimed in claim 15, in which the holding device of each stage comprises a pull-down transistor whose control electrode is connected to a or the complementary output of the flip-flop.

17. A generator as claimed in claim 15, in which the holding device of each stage comprises a pull-up transistor whose control electrode is connected to a or the direct output of the flip-flop.
18. A generator as claimed in any one of claims 1 to 12, in which the clock input is a single phase clock input.
19. A generator as claimed in claim 18 when dependent on claim 11, in which the clock pulses passed by the pass gates of consecutive stages are of opposite polarity.
20. A generator as claimed in claim 19, in which the holding devices of the stages comprise alternating pull-down and pull-up transistors, the control electrode of each pull-down transistor being connected to the complementary output of the associated flip-flop and the control electrode of each pull-up transistor being connected to the direct output of the associated flip-flop.
21. A generator as claimed in any one of preceding claims 1 to 10, in which each of the gating circuits comprises a gated sense amplifier.
22. A generator as claimed in any one of claims 1 to 10, in which each of the gating circuits comprises a gated level shifter.
23. A generator as claimed in any one of the preceding claims, in which each of the flip-flops comprises: a first inverter, at least one of whose input and output constitutes an output of the flip-flop; a second controllable inverter, whose input and output are connected to the output and input, respectively, of the first inverter; and an input circuit having first and second inputs constituting inputs of the flip-flop, the input circuit being arranged to supply to the input of the first inverter a signal corresponding to the states of the first and second inputs and to control the second inverter so as to switch the output of the second inverter to a high impedance state when the first or second input receives an active signal.

24. A generator as claimed in claim 23, in which the first input is an active high input and the second input is an active low input.

25. A generator as claimed in claim 24, in which the input circuit comprises: a first active device connected between a first power supply input and the input of the first inverter and having a control electrode constituting the second input; and a second active device, of opposite conduction type to the first active device, connected between a second power supply input and the input of the first inverter and having a control electrode constituting the first input.

26. A generator as claimed in claim 25, in which each of the first and second active devices is connected in an inverting configuration.

27. A generator as claimed in any one of claims 24 to 26, in which the second inverter comprises third and fourth active devices of a first conduction type connected in series between a or the first power supply input and the output of the second inverter and fifth and sixth active devices of a second conductive type opposite the first type connected in series between a or the second power supply input and the output of the second inverter, the third and fifth active devices having control electrodes connected to the input of the second inverter and the fourth and sixth active devices having control electrodes connected to the first and second inputs, respectively, of the input circuit.

28. A generator as claimed in claim 27, in which the control electrode of at least one of the third and fifth active devices is connected to the input of the second inverter via a further active device.

29. A generator as claimed in claim 28, in which the or each further active device has a control electrode connected to the first or second power supply input.

30. A generator as claimed in any one of claims 23 to 29, in which the first inverter comprises a seventh active device connected between a or the first power supply input and the output of the first inverter and an eighth active device, of opposite conduction

type to the seventh active device, connected between a or the second power supply input and the output of the first inverter, the seventh and eighth active devices having control electrodes connected to the input of the first inverter.

31. A generator as claimed in any one of the preceding claims, comprising a CMOS integrated circuit.

32. A spatial light modulator comprising a generator as claimed in any one of the preceding claims.

33. A modulator as claimed in claim 32, comprising a liquid crystal device.

34. A display comprising a modulator as claimed in claim 32 or 33.



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Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.Q): H3P (PPMP)

Int Cl (Ed.6): H03K (5/15) G11C (19/28) G09G (3/36)

Other:

Documents considered to be relevant:

Category	Identity of document and relevant passage	Relevant to claims
	None.	

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