Aug. 29, 1967 C. F. WEISS, JR 3,339,191

CORE DRIVER TEST APPARATUS

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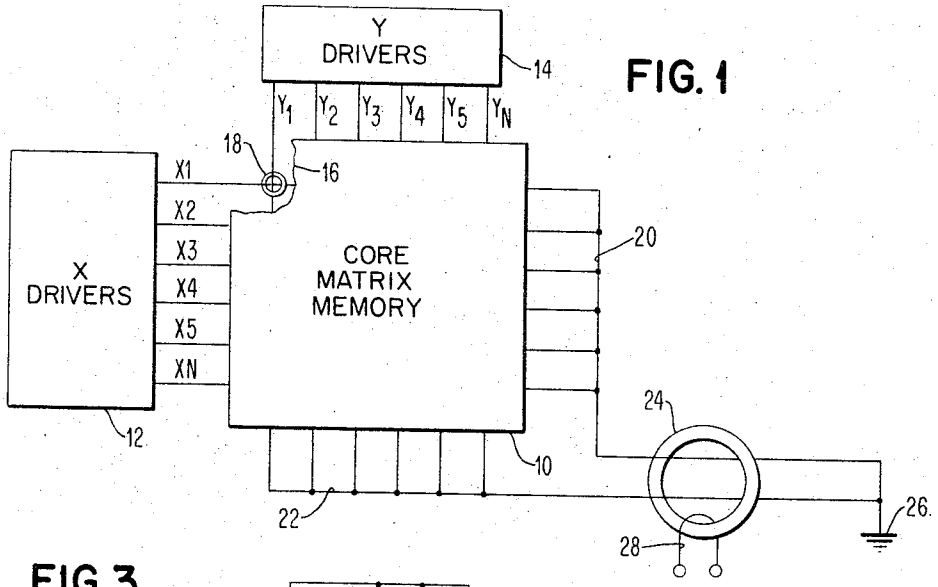
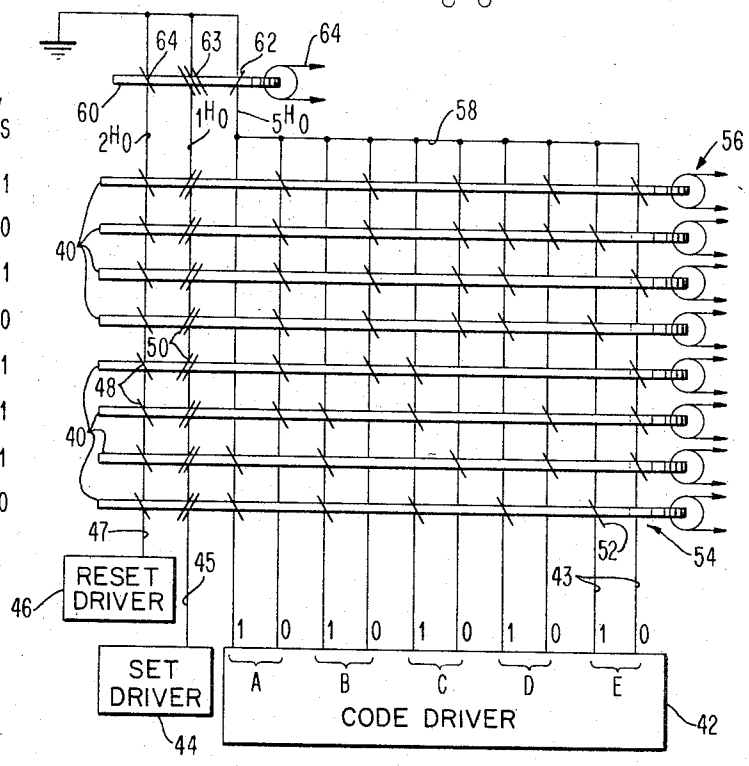


FIG. 1

FIG. 3

65 CODE	66 DRIVERS
00000	11111
00001	11110
00010	11101
00011	11100
00110	11001
01100	10011
11000	00111
11111	00000



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CORE DRIVER TEST APPARATUS

Filed Sept. 29, 1958 2 Sheets-Sheet 2

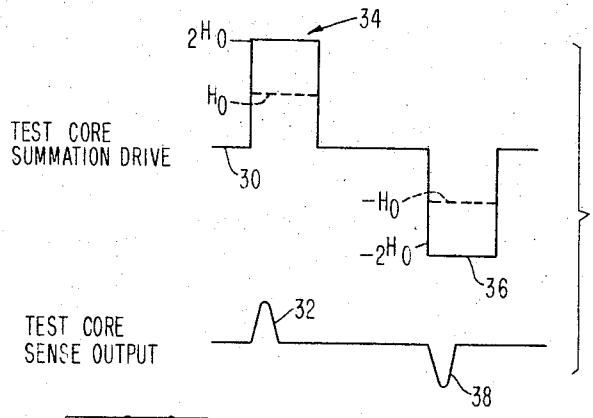

FIG. 2

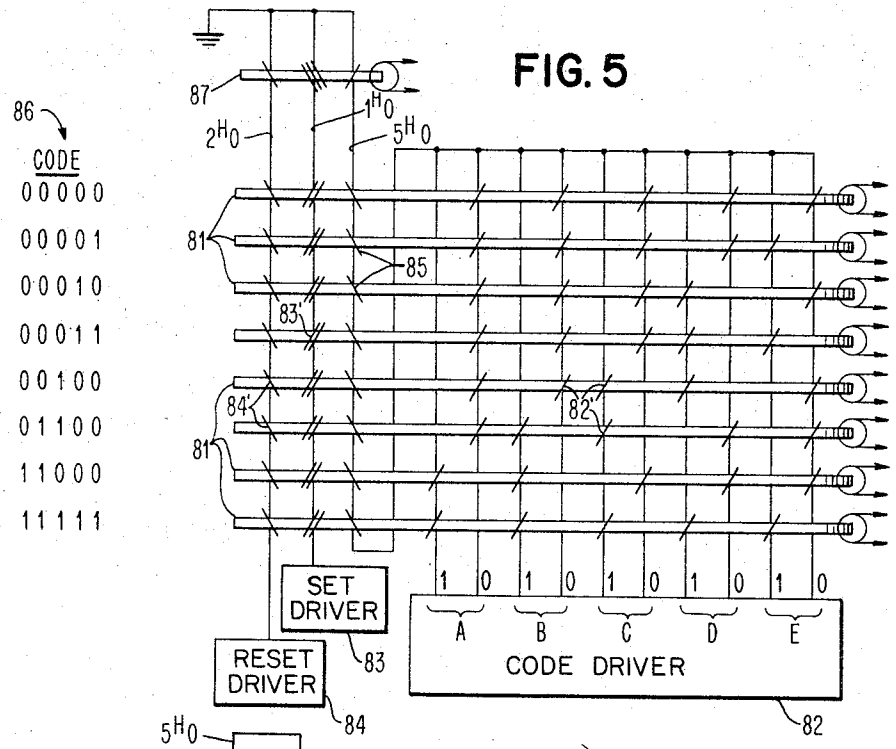

FIG. 5

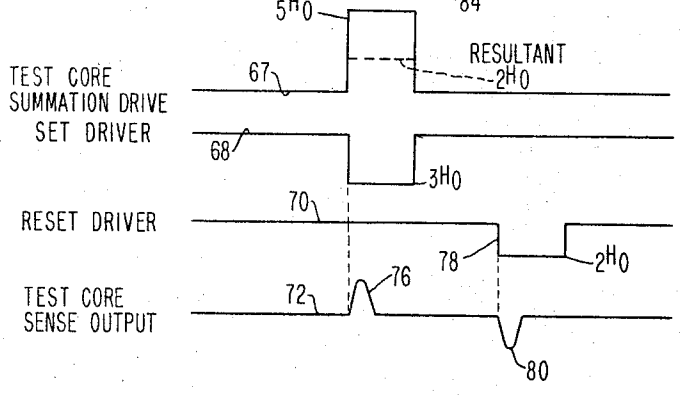

FIG. 4

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CORE DRIVER TEST APPARATUS

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2 Claims. (Cl. 340—174)

This invention relates to core driver test apparatus and more particularly to apparatus for testing each operation of driving means in a core selector system.

Various core systems are well known in the art. These systems include the so called coincident drive system for a two dimensional array of cores employed for the storage of binary information. This type of system is shown, for example, in the patent to Rajchman et al. 2,784,391. Core systems are also employed for the purpose of code translation. Systems of this type are shown in the patent to Rajchman 2,734,182 and in the patent to Rajchman et al. 2,691,153.

It is the object of the present invention to provide, in association with a core system, an additional test core driven by the driving currents employed in the core system in such a manner as to provide a test for proper operation of the driving current circuits.

The invention involves the use of a test core in association with a core system in which there is employed the same number of driving circuits for each operation of the core system. This type of operation is found in the type of core memory system noted above and in the type of core translation system noted above.

In a core memory system there may be employed for each operation of the system coincident selection drive currents, conventionally two, one referred to as an x driver and the other referred to as a y driver, in order to effect selection of a desired core. In the code translation system there may be employed an input code comprising code bit combinations, each having a fixed number of code bits selected from a greater number of possible input code bits and this fixed number of code bits is converted to an equivalent number of driving currents delivered through selected drive lines upon each operation of the core system. In both of these types of systems it is possible to sum the output of the drive line currents and deliver this summation current to a test core.

In the type of memory system employing x and y drivers, this summation current, when delivered to a test core, can be arranged to provide a selection drive for the test core thus changing the magnetic state of the test core. The absence of either the x or y driver, upon an operation of the core memory system, will provide insufficient current to change the magnetic state of the test core whereupon the test core will fail to produce an output signal and this failure to produce an output signal can be used as an indication of a failure in the operation of the core memory system, and, more particularly, as an indication of a failure of one of the drivers for the core memory system.

Accordingly, more specifically, it is an object of the invention to provide, in association with a core memory system, a test core for testing operation of the x and y coincident current drivers.

In the core systems providing code translation the test core is arranged to receive the summation of the code driver currents. Systems of this type also frequently employ a set driver which, as will be hereinafter described, generally serves to set a selected core. In this type of system the set driver current is also delivered to the test core and in opposing relation to the code driver currents. Thus, the test core serves to test both the set driver and the code drivers.

Additionally, these latter types of systems also employ a reset driver. The reset driver current is also delivered to the test core in order to reset the test core. Thus, the reset driver is also tested by the test core.

Accordingly, more specifically, it is an object of the invention to provide, in association with a code translation system, a test core for testing operation of code drivers, a set driver and a reset driver.

Other objects of the invention will be pointed out in the following description and claims and illustrated in the accompanying drawings, which disclose, by way of example, the principle of the invention and the best mode, which has been contemplated, of applying the principle.

In the drawings:

FIGURE 1 shows a bi-dimensional storage system driven by conventionally designated x and y drivers and employing the test core in accordance with the invention;

FIGURE 2 shows diagrammatically the summation of the input currents to the test core and the output sense pulses produced by the test core of FIGURE 1;

FIGURE 3 shows a code translator or switching system employing a plurality of driving circuits variously selected from a greater number of drivers and having associated therewith a test core in accordance with the invention;

FIGURE 4 shows diagrammatically input and output pulses of the test core shown in FIGURE 3; and

FIGURE 5 shows an alternative form of code translator or switching systems having a test core associated therewith in accordance with the invention and having input and output pulses in accordance with the diagram of FIGURE 4.

In FIGURE 1 there is shown at **10** a bi-dimensional core memory of conventional type provided with parallel rows of drivers **12** serving to drive x lines as indicated at X_1, X_2 . . . X_n, and provided with y drivers **14** for driving the y drive lines Y_1, Y_2 . . . Y_n. This type of coincident current system is well known and includes a plurality of cores such as the one shown in the cut away region **16** and indicated therein at **18** through which the X_1 and Y_1 drive lines pass providing, upon the existence of coincidence pulses in these two lines, for a change of magnetic state of the core **18**.

The X lines leaving the core matrix are summed as indicated at **20** and the Y lines are summed as indicated at **22**. These two summation lines pass to ground as indicated at **26**. However, before passing to ground the summation lines pass through a test core **24** in an additive manner. The test core is selected to be of such a nature that the summation current in one of the lines provides only a $_1H_0$ pulse, i.e. a half select pulse, for the test core and thus coincident currents are required in the two summation lines in order to change the magnetic state of the test core. The test core is linked with an output line **28** which may be connected to suitable indicating or recording means and which provides, by its indication of the change of state of the test core, an indication of proper operation of the two drivers involved in the coincident current operation of the core matrix memory system.

This operation is shown in FIGURE 2 in which the summation of the matrix x and y drive currents passing through the test core is indicated on line **30**. It has been noted that each of the summation currents provides a $_1H_0$ pulse for the test core, and the summation of these currents provides a $_2H_0$ pulse indicated at **34** suitable for changing the magnetic state of the test core. The $_2H_0$ pulse produces an output pulse from the core sense line as indicated at **32**.

The bi-dimensional core matrix memory system employs drivers providing current of opposite polarities

upon successive operations. Accordingly, upon a set operation of the core matrix memory a first drive pulse of one polarity is delivered to the test core as is indicated at **34** and upon the reset operation of the matrix memory a second drive pulse of opposite polarity is delivered to the test core as is indicated at **36**. As previously noted the first test core drive pulse provides a first sense output pulse of one polarity as indicated at **32** and obviously the opposite polarity drive pulse **36** provides an opposite polarity sense output pulse as indicated at **38**.

It will be evident from the diagram of FIGURE 2 that the failure of one of the core matrix coincident drivers upon operation of the core matrix memory system will fail to set the selected core in the memory system. This failure will be reflected as the absence of a sense output pulse from the test core by reason of the fact that the test core will witness only a $_1H_0$ pulse in its drive line.

In FIGURE 3 there is shown a so called negative logic core system which may be employed as a code translator or as a switching circuit. The system employs a plurality of cores indicated by elongated rectangles **40**, each rectangle **40** indicating one core. Drivers for these cores are shown as a code driver **42**, a set driver **44** and a reset driver **46**. The code driver has a plurality of output lines as indicated at **43** providing a five bit code output in the form of two lines for each code bit for selectively indicating a one or a zero indicating the presence or absence, respectively, of that particular code bit for a given code selection. The set driver **44** has an output line **45** and the reset driver **46** has an output line **47**.

The reset driver output line **47** passes through each of the cores with one turn as indicated by the bars **48**, and the direction of the bar indicates the polarity of the turn.

The set driver output line **45** passes through each of the cores **40** with two turns of opposite polarity from that of the reset driver turns as indicated by the two bars **50** on each of the cores **40**.

Each of the code driver output lines **43** passes through some of the cores and does not pass through other of the cores. Cores through which output lines **43** pass are indicated by bars such as the bar **52**, indicating that the driver E1 forms one turn with the lowermost core. The driver E0 does not pass through this core as indicated at **54** by the absence of a bar.

Each of the cores **40** is provided with an output line **56** which is coiled around the core with a sufficient number of turns to provide a desired output signal amplitude. The code driver lines are connected together at **58**, thus summing the drive currents which have passed through core system and this summation is passed through a test core **60** in a line forming one turn thereon of a first polarity as indicated by the bar **62**. The set driver line **45** passes through the test core **60** with three turns of opposite polarity as indicated by the bars **63**, and the reset driver line **47** passes through the test core **60** with one turn of the same polarity as the set driver turns as indicated by the bar **64**.

In the core system shown, five of the ten code driver circuits and the set driver are energized in order to select a desired core and this selection is accomplished in accordance with an input code. For example, the code for the uppermost core **40** is 00000. This is shown under the head "CODE" indicated generally at **65** in FIGURE 3. In the negative logic system, as is well known in the art, the code drivers employed for selection of code 00000 are the drivers 11111 as is shown under the heading "DRIVERS" indicated generally at **66**. Each of the code drive lines employed carries a $_1H_0$ or half select current. Coincidently with the code driver current pulses, the set driver produces a $_1H_0$ pulse which passes through two coil turns on each core in opposite polarity from any code driver coil turns thereon. Thus, if any of these code drive lines passes through a core with one turn it will inhibit switching of the core by the set driver. Only the selected core is not inhibited by code driver pulses and thus only this core is switched by the set driver.

The core system is reset by the reset driver output which has a $_2H_0$ current passing through one turn on each core, as indicated at **48**, of opposite polarity from the set driver coils thus providing a $_2H_0$ pulse for each core. It will be evident that this pulse will reset the core which was switched by the set driver.

The test core receives the five $_1H_0$ code driver pulses through the single turn **62**. This drive current is opposed by 3 turns **63** of the $_1H_0$ pulse in the set driver. Thus, as shown in FIGURE 4, the summation of the core driver currents provides a $_5H_0$ summation current in the test core drive as indicated at $_5H_0$ on the drive current line **67**. The set drive current, shown on line **68** in FIGURE 4, provides a $_3H_0$ drive for the test core in the opposite direction. These two drives are in opposition and the resulting $_2H_0$ drive is indicated on the line **67**. This resulting $_2H_0$ drive switches the core **60** giving rise to an output on the sense line as indicated at **76** on the sense output line **72** in FIGURE 4.

When the core matrix is reset by the reset driver **46**, a $_2H_0$ pulse is passed through the single turn **64** on the test core producing as indicated on the reset drive line **70** in FIGURE 4, a $_2H_0$ pulse **78** serving to reset the test core and giving rise to an output pulse **80** in the opposite direction from the output pulse **76**. Thus, each set and reset operation of the system is indicated by a test core output pulse.

In FIGURE 5 there is shown a positive logic system employing a return bias and a set driver. In this system a plurality of cores **81** are selectively driven by coded drivers provided by a code driver **82**. The driving coils on the cores are one turn coils and are indicated by bars **82'**. The code drivers are summed and the summation line is passed through a single coil on each of the cores as indicated at **85**. The code driver delivers five $_1H_0$ pulses to a selected core and less than five $_1H_0$ pulses to each non-selected core. The five $_1H_0$ pulses in the selected core are opposed and cancelled by the $_5H_0$ drive on the bias or summation line. Coincidentally, with the code driver pulses, the set driver produces a $_1H_0$ pulse which passes through two turns on each core as is indicated by the bars **83'**, of opposite polarity from the bars **85** of summation line. Thus, a selected core will be set by the set driver. Non-selected cores will have less than five $_1H_0$ code drivers but will have a $_5H_0$ bias applied thereto, and thus the bias will inhibit selection of the other cores by the set driver.

As previously noted, the system is a positive logic system and, as indicated at **86**, each core is represented by a code and the driver currents in the code driver line correspond to the actual code bits of the code for each core. A selected core is reset by the reset driver **48** which provides a $_2H_0$ pulse through one turn on each core as indicated by the bars **84'**.

The summation bias winding carrying the $_5H_0$ pulse is passed through one coil turn on a test core **87**. The coincident set pulse of $_1H_0$ is passed through three one coil turns on the test core **87**. These two pulses act in opposition in the test core producing respectively a $_5H_0$ and a $_3H_0$ pulse therein to produce a resultant $_2H_0$ pulse which changes the state of the core and produces an output pulse in the manner as described in connection with the diagrams of FIGURE 4. Similarly, the test core **87** is reset by the core system reset driver **84** in the manner of the reset of the test core system as indicated in FIGURE 4. Thus, the arrangement shown in FIGURE 5 produces test core sense output pulses equivalent to those indicated at **76** and **80** in FIGURE 4.

The effectiveness of the test apparatus described herein will be evident from the following:

In the core matrix memory system described in connection with FIGURE 1 an increase in current level in either or both of a pair of selected X-Y drivers will serve

to set the test core producing a normal test core output indicating no failure. However, such increase in current level or levels may cause a failure by selecting more than one core address but such an erroneous selection would read out more than one address and would thus be dectable by the memory output receiving apparatus. If one of the *x* or *y* drivers, or both of these drivers should fail, then the test core will not be set and hence no test core output will occur. This absence of test core output will then indicate a failure. Accordingly, the test core will indicate any condition of failure that is reasonably liable to arise which will produce an improper operation of the core matrix memory not detectable by memory output receiving apparatus.

The various possible improper drive conditions that may occur in the arrangement shown in FIGURE 3 and the resulting effects on the core matrix and on the test core are as follows:

Code Drivers	Resulting Effects
Loss of one or fall in one.	Set drive may select a second matrix core. Test core is not set, therefore, an error signal is produced.
Gain of one	No matrix core selected, therefore, no matrix output is produced. This is an error detectable by output code receiving apparatus. Test core is set, therefore, no error signal is produced.
Rise in one	Only selected matrix core is set. Test core is set, therefore, no error signal is produced.
Set Driver:	
Drop	No matrix core is selected, therefore, no matrix output is produced. This failure of operation is detectable by apparatus receiving the matril output. Test core is set, therefore, no error signa is produced.
Rise	Set drive may select a second matrix core. Test core is not set, therefore, an error signal is produced.
Reset Driver:	
Drop	No matrix core is reset. Test core is not reset, therefore, an error signal is produced.
Rise	Matrix core is reset. Test core is reset, therefore, no error signal is produced.

The possible conditions of improper operation and results produced thereby that may occur in the arrangement shown in FIGURE 5 are listed as follows:

Code Driver Operation	Resulting Effects
Loss of one or fall in one	Set drive may select a second matrix core. Test core is not set, therefore, an error signal is produced.
Gain in one or rise in one	Only selected matrix core is set. Test core is set, therefore, no error signal is produced.
Set Driver [1]	
Reset Driver [1]	

[1] Same as listed above for the arrangement shown in Figure 3.

From the foregoing it will be evident that any possible failure in the driver systems which will produce an erroneous result in the operation of the core system will be indicated by the absence of a signal of the test core. On the other hand, those improper operations of the drive systems which will not produce erroneous results are not indicated by the test core. Those improper operations of the drivers which will result in the production of no output signal by the core system are not indicated by the test core, however, the absence of an output signal from the core matrix will be immediately recognized by subsequent equipment in the particular logical system following the core matrix.

It will be evident that the test apparatus disclosed herein provides a relatively simple and extremely versatile type of check on the proper functioning of drivers for a core selector system. The apparatus involved is relatively inexpensie and yet, as discussed above, provides a check for any condition of malfunctioning of the drive system which would produce an improper output from the core system.

While there have been shown and described and pointed out the fundamental novel features of the invention as applied to a preferred embodiment, it will be understood that various omissions and substitutions and changes in the form and details of the device illustrated and in its operation may be made by those skilled in the art without departing from the spirit of the invention. It is the intention therefore, to be limited only as indicated by the scope of the following claims.

What is claimed is:

1. In a core selection system, means including driving circuits from which driving currents are selectively produced and a set circuit from which a set current is produced for successively operating the system, an additional bistable magnetic test core, first winding means on said test core coupled to all of said driving circuits for conducting each driving current through the test core in one direction, second winding means on said test core coupled to said set circuit for conducting the set current through the test core in the opposite direction, the respective coupling strengths of said first and second winding means being such that said test core is changed from one stable state to another only upon operation of a predetermined number of said driving currents coincidently with operation of said set circuit, and means for sensing a change of magnetic state of said test core as an indication of the character of operation of said core selection system.

2. In a core selection system, means including driving circuits from which driving currents are selectively produced for successively operating the system to effect core selection and a reset circuit from which a reset current is produced for resetting the system after each operation, an additional test core, means wound through said test core for conducting all of said driving currents for changing the magnetic state of said test core upon each operation of a predetermined number of driving circuits of said system and not changing the magnetic state of said test core upon operation of less than said predetermined number of driving circuits of said system, said means also conducting said reset current for rechanging the magnetic state of said test core upon each operation of said reset circuit and not rechanging the magnetic state of said test core upon failure of operation of said reset circuit, and means for sensing a change of magnetic state of said test core as an indication of proper operation of said system driving circuits and reset circuit.

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