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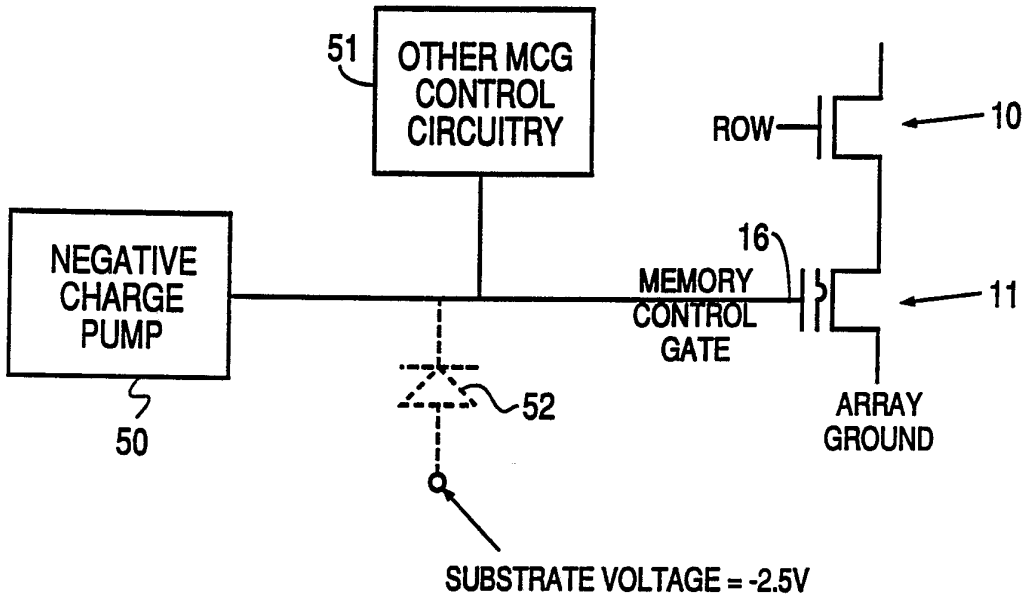
(54) Title: METHOD OF PROGRAMMING ELECTRICALLY ERASABLE PROGRAMMABLE READ-ONLY MEMORY



(57) Abstract

The apparent voltage used to program an EEPROM cell is increased by applying a negative voltage to the memory control gate (16) of the sense transistor (11) in the cell. This method is applicable to devices in which the substrate is negatively biased.

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METHOD OF PROGRAMMING ELECTRICALLY ERASABLE PROGRAMMABLE READ-ONLY MEMORY

FIELD OF THE INVENTION

This invention relates to electrically erasable programmable read-only memories and in particular to such devices which employ floating gate technology.

BACKGROUND OF THE INVENTION

A typical electrically erasable programmable read-only memory (EEPROM) cell includes two MOS transistors connected in series. An EEPROM of this kind is shown schematically in Figure 1 and structurally in Figure 2. It includes a select transistor 10 and a sense transistor 11, which are connected in series between a bit line 13 and an array ground 17. The gate of select transistor 10 is connected to a row line 12. Sense transistor 11 is controlled by a memory gate 16 and a floating gate 15. When the state of the cell is to be read, select transistor 10 is turned on via a voltage applied to row line 12, and a read voltage is applied to bit line 13 to determine the conductive state of sense transistor 11. If sense transistor 11 is conductive (programmed) a current will flow; if it is non-conductive (erased) a current will not flow.

Sense transistor 11 is programmed or erased by applying an appropriate voltage between memory control gate 16 and bit line 13, with select transistor 10 turned on. If memory control gate 16 is grounded and a positive programming voltage (typically about 14.5 V) is applied to bit line 13, electrons tunnel from floating gate 15 through a very thin tunnel oxide layer 18 (shown in Figure 2) to the N^+ region designated 14 in Figure 2, leaving

floating gate 15 with a net positive charge. In this state, the cell is programmed. If bit line 13 is grounded and a positive programming voltage is applied to memory control gate 16, the reverse occurs. Electrons tunnel from N^+ region 14 through the very thin oxide layer 18 into floating gate 15, leaving floating gate 15 with a net negative charge. In this state, the cell is erased.

The charge on floating gate 15 determines the threshold voltage of sense transistor 11. If floating gate 15 is positively charged, sense transistor 11 has a relatively low threshold voltage V_{TL}. If floating gate 15 is negatively charged, sense transistor 11 has a relatively high threshold voltage V_{TH}. Normally, a reference voltage V_{ref} about halfway between V_{TH} and V_{TL} is applied to memory control gate 16. Thus, if sense transistor 11 has been programmed, it will be conductive; if it has been erased, it will be an open circuit.

It is desirable to have the margin between V_{TH} and V_{TL} be as large as possible because a large margin provides for a strong cell current and longer data retention.

For a particular tunnel oxide layer thickness, the margin is primarily determined by two factors: (i) the coupling ratio and (ii) the voltage difference between memory control gate 16 and the common point between sense transistor 10 and select transistor 11 when the cell is being programmed or erased. The latter in turn is proportional to the voltage difference applied between cell memory control gate 16 and bit line 13. With smaller cells and greater cell densities, both of these factors have a tendency to reduce the margin. The coupling ratio is established by the layout of the cell, and a smaller layout tends to reduce the coupling ratio. As explained below, smaller cell dimensions also tend to limit the voltage difference that can be used in programming and erasing the cell.

Figure 3 illustrates V_{TH} and V_{TL} as a function of the potential difference (V_{pp}) between the memory control gate

and the bit line during the erase and programming operations, respectively. As Figure 3 indicates, V_{TH} increases with increasing V_{pp} and V_{TL} decreases with increasing V_{pp}. Thus, the margin (V_{TH} - V_{TL}) also increases as V_{pp} increases.

The desire for a large margin is in conflict with the increasing miniaturization of EEPROM cells. With thinner oxides, tighter design rules and more highly doped and shallower junctions, breakdown voltages such as punch through, field-aided junction breakdown, and field device turn on tend to decrease. For example, referring to Figure 2, as the thickness of gate oxide 20 decreases, the field-aided junction breakdown voltage (BVDSS) of select transistor 10 decreases as a result of breakdown at the PN junction in the area designated 21 in Figure 2. Thus, while a thinner gate oxide has the beneficial effect, for example, of increasing the transconductance (G_m) in select transistor 10, the price of greater transconductance is a lower BVDSS. This in turn limits the voltage which can be used in programming or erasing the cell and makes it more difficult to obtain a wide margin. The relationship between G_m and BV_{DSS}, respectively, and the thickness of gate oxide 20 is illustrated in Figure 4.

SUMMARY OF THE INVENTION

The method of this invention allows the potential difference used in programming an EEPROM cell to be increased without raising the chances of voltage breakdown. This is accomplished using an EEPROM cell with a negatively biased substrate. The memory control gate of the sense transistor is pumped to a negative voltage using a charge pump. Because the substrate is negatively biased, this can be done without the risk of N-channel source-drain diffusion forward-biasing the associated PN junction, which could initiate latch up. The margin is increased one volt for every volt that the memory control gate is negatively biased.

DESCRIPTION OF THE DRAWINGS

Figure 1 is a schematic diagram of a typical EEPROM cell.

Figure 2 illustrates the structure of the cell shown in Figure 1.

Figure 3 is a graph of V_{TH} and V_{TL} as a function of the programming voltage.

Figure 4 is a graph of the transconductance and the source-to-drain breakdown voltage of select transistor 10 as a function of the thickness of the gate oxide.

Figure 5 illustrates an arrangement in accordance with this invention.

DESCRIPTION OF THE INVENTION

It is known in the art to back-bias the substrate of an MOS device. The primary purpose of this is to reduce junction capacitance and thereby increase the speed of the cell. Typically, the substrate is biased to approximately -2.5 V.

The lower threshold voltage V_{TL} of the sense transistor in an EEPROM is determined by the coupling ratio and the potential difference between the memory control gate and the drain of the sense transistor during the programming operation. Since the select transistor is turned on during programming, the drain potential of the sense transistor is essentially equal to the voltage applied to the bit line. Normally, the memory control gate is grounded, and thus V_{TL} is proportional to the positive voltage applied to the bit line. As noted previously, this voltage cannot be increased beyond a certain level without raising the risk of breakdown. The primary concern is field-aided junction breakdown in a select transistor contained in a cell other than the one being programmed.

With a back-biased substrate, the potential difference between the memory control gate and the bit line during programming may be increased by reducing the

voltage of the memory control gate. This has the same effect on V_{TL} as increasing the programming voltage on the bit line by an equivalent amount.

A structure for doing this is illustrated in Figure 5. The EEPROM cell consisting of select transistor 10 and sense transistor 11 is identical to the cell illustrated in Figure 1. A negative charge pump 50 is connected to memory control gate 16. The box labeled 51 represents other control circuitry, such as the circuitry which controls memory gate 16 during the erase and read cycles.

The substrate of the cell pictured in Figure 5 is biased to a voltage of -2.5 V. The diode 52 shown in hatched form in Figure 5 represents a PN junction somewhere on the same chip which could be forward-biased if the voltage of memory control gate 16 falls below the voltage of the substrate. Since diode 52 has a threshold voltage of 0.7 V, the voltage applied by negative charge pump 50 to memory control gate 16 could, in theory, be reduced to -3.2 V without creating a forward-biased PN junction in diode 52 that could initiate latch-up. In reality, there may be other parasitic devices which limit the degree to which the voltage at memory control gate 16 may be reduced.

Assuming that negative charge pump 50 applies a voltage of -1.5 V to memory control gate 16, the hatched line 30 in Figure 3 illustrates the V_{TL} curve for the device shown in Figure 5. The V_{TL} curve for the cell shown in Figure 1 has been displaced downward approximately 1.5 V. The margin has increased an equivalent amount.

Accordingly, using the method and structure of this invention, the margin of an EEPROM cell may be increased, yielding a larger current in the cell and longer data retention, without increasing the programming voltage or increasing the risk of field-aided junction voltage breakdown.

The foregoing description of an embodiment of this invention is intended to be illustrative and not limiting.

Other embodiments and methods in accordance with this invention will be apparent, all of which are within the broad scope of this invention.

CLAIMS

I claim:

1. A method of programming an EEPROM cell which includes a sense transistor formed in a substrate, said substrate being negatively biased, the method comprising the step of maintaining a memory control gate of said sense transistor at a negative voltage during the programming of said cell.

2. An arrangement for programming an EEPROM cell comprising a means for negatively biasing a memory control gate of a sense transistor in said cell.

3. The arrangement of Claim 2 wherein said means comprises a negative charge pump.

4. The arrangement of Claim 3 wherein said sense transistor is formed in a substrate, said substrate being maintained at a negative voltage.

5. An EEPROM cell comprising:

a select transistor;

a sense transistor having a memory control gate; and

a means for maintaining said memory control gate at a negative voltage.

6. The EEPROM cell of Claim 5 wherein said means comprises a negative charge pump.

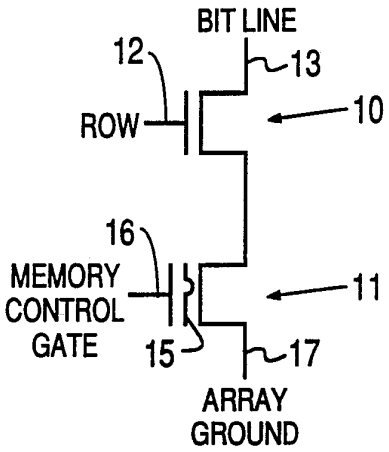

FIG. 1
(PRIOR ART)

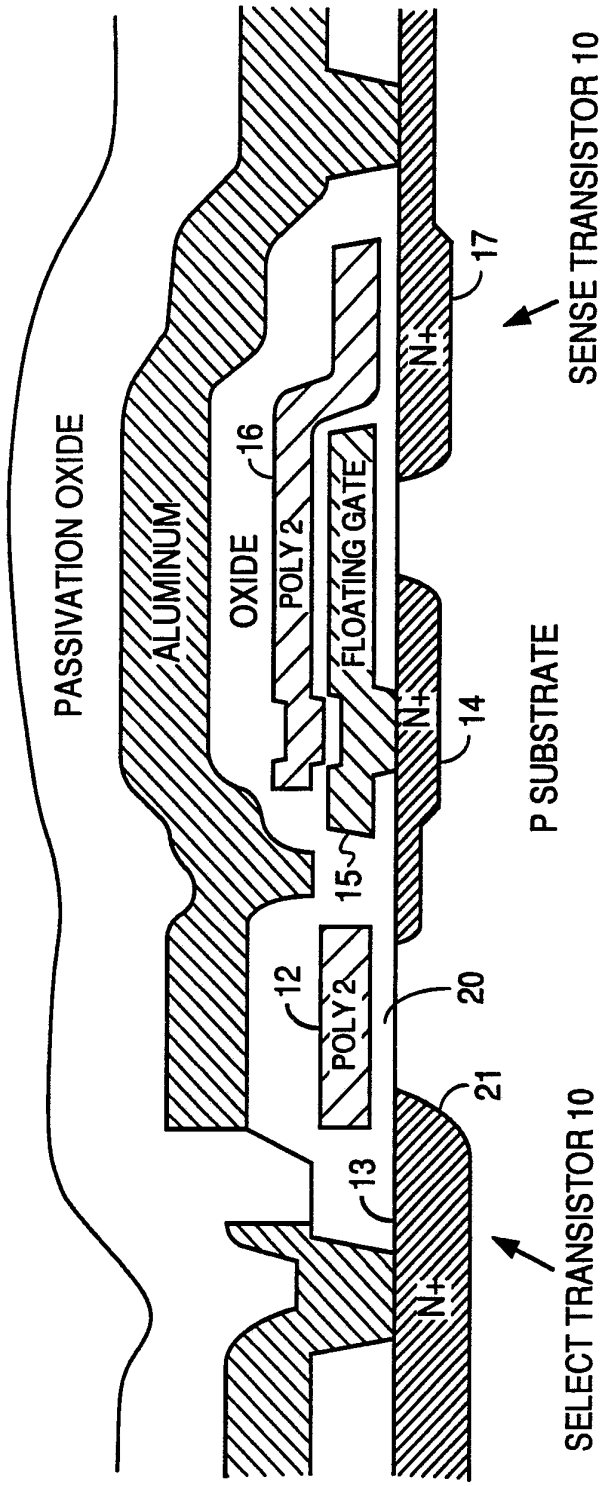

FIG. 2
(PRIOR ART)

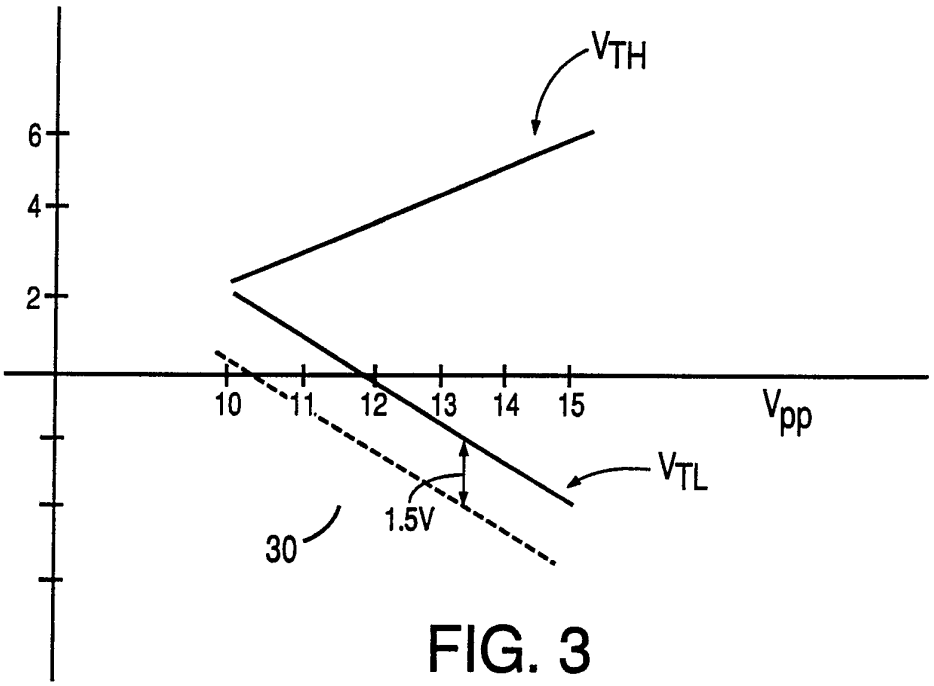
V_{TH}
6
4
2
10
11
12
13
14
15
V_{pp}
V_{TL}
1.5V
30

FIG. 3

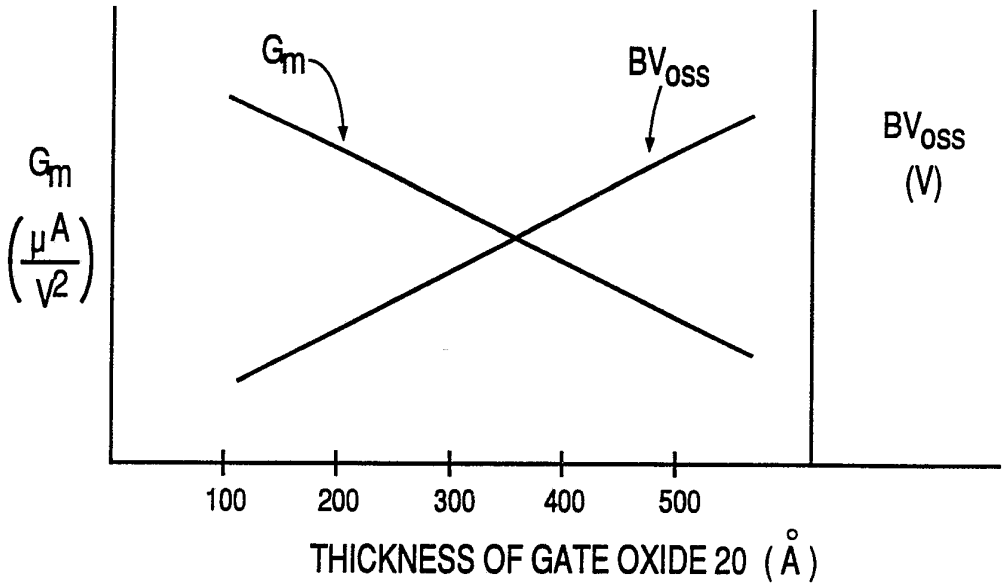
G_m
BV_{oss}
G_m
$\left(\frac{\mu A}{V^2}\right)$
BV_{oss}
(V)
100
200
300
400
500
THICKNESS OF GATE OXIDE 20 (Å)

FIG. 4

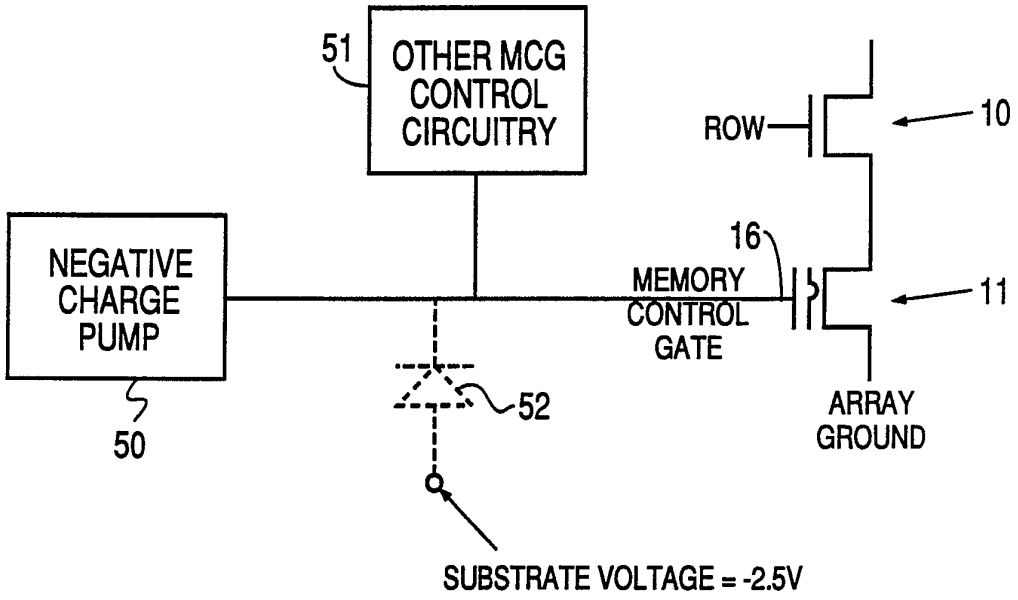
51
OTHER MCG CONTROL CIRCUITRY
ROW
10
16
MEMORY CONTROL GATE
11
NEGATIVE CHARGE PUMP
50
52
ARRAY GROUND
SUBSTRATE VOLTAGE = -2.5V

FIG. 5

INTERNATIONAL SEARCH REPORT

...ernational application No.
PCT/US92/06947

A. CLASSIFICATION OF SUBJECT MATTER

IPC(5) :G11C 11/40
US CL :365/185,189.09;307/296.2,469
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 365/185,189.09;307/296.2,469

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	IBM TECHNICAL DISCLOSURE BULLETIN, July 1973 Volume 16, number2, James, "electronically Rewritable nonvolatice storage having reduced write voltage" Pages 690-691, See figure 1-3 and biasing on page 691.	5 1-4,6
Y	US,A, 4,388,537 (KANUMA), 14 JUNE 1983, See col 1, lines 16-20.	3,4,6
Y	IBM TECHNICAL DISCLOSURE Bulletin, January 1975, Vol. 17 November 8, R. Dockerty "Non-Volatice memory array with a single famos device per cell, "Pages 2314-2315 See figures 1,2 and page 2315.	1-4

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

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C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	IBM TECHNICAL DISCLOSURE Bulletin, January 1975, volume 15 number 8 N. Anantha et al. "Electrically erasable floating gate field effect transistor memory cell" pages 2311-2313, note V_{sx}=-3 and VG=-30 for write in figure 4,	1-4
A	US,A, 4,884,239 (ONO ET AL.), 28 NOVEMBER 1989, See negative biasing, of substrate, gate in figures 5,6A,6B.	1-6