



- (51) **International Patent Classification:**  
*H01L 23/498* (2006.01)
- (21) **International Application Number:**  
PCT/US2015/033004
- (22) **International Filing Date:**  
28 May 2015 (28.05.2015)
- (25) **Filing Language:** English
- (26) **Publication Language:** English
- (30) **Priority Data:**  
14/291,874 30 May 2014 (30.05.2014) US
- (71) **Applicant:** INVENSAS CORPORATION [US/US];  
3025 Orchard Parkway, San Jose, CA 95134 (US).
- (72) **Inventors:** CO, Reynaldo; 3025 Orchard Parkway, San Jose, CA 95134 (US). ZOHNI, Wael; 3025 Orchard Parkway, San Jose, CA 95134 (US). SAGA CIZEK, Rizza Lee; 3025 Orchard Parkway, San Jose, CA 95134 (US). KATKAR, Rajesh; 3025 Orchard Parkway, San Jose, CA 95134 (US).
- (74) **Agents:** NEFF, Daryl et al.; Lerner, David, Littenberg, Krumholz & Mentlik, LLP, 600 South Avenue West, Westfield, New Jersey 07090 (US).
- (81) **Designated States** (*unless otherwise indicated, for every kind of national protection available*): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY,

BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

- (84) **Designated States** (*unless otherwise indicated, for every kind of regional protection available*): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

**Declarations under Rule 4.17:**

- as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))
- as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))

**Published:**

- without international search report and to be republished upon receipt of that report (Rule 48.2(g))

(54) **Title:** WIRE BOND SUPPORT STRUCTURE AND MICROELECTRONIC PACKAGE INCLUDING WIRE BONDS THEREFROM

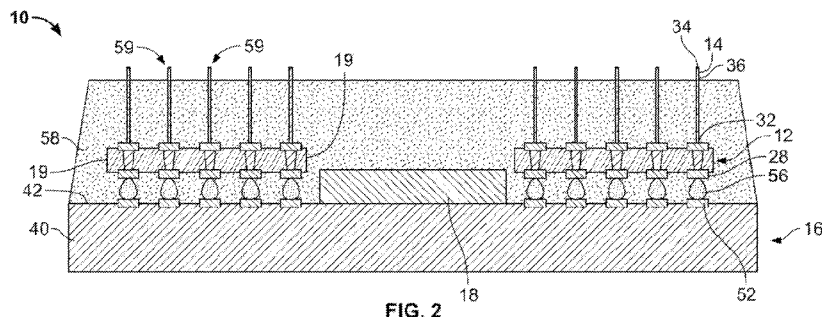


FIG. 2

(57) **Abstract:** A microelectronic package may include a substrate (40) having first and second regions (46,48), a first surface (42) and a second surface (44) remote from the first surface; at least one microelectronic element (18) overlying the first surface (42) within the first region (46); electrically conductive elements (52) at the first surface within the second region (48); a support structure (20) having a third surface (24) and a fourth surface (22) remote from the third surface and overlying the first surface (42) within the second region (48) in which the third surface (42) faces the first surface (42), second and third electrically conductive elements (28, 26) exposed respectively at the third and fourth surfaces and electrically connected to the conductive elements (52) at the first surface (42) in the first region; and wire bonds (14) defining edge surfaces (36) and having bases (32) electrically connected through ones of the third conductive elements (26) to respective ones of the second conductive elements (28) and ends (34) remote from the support structure and the bases.



WIRE BOND SUPPORT STRUCTURE AND MICROELECTRONIC PACKAGE  
INCLUDING WIRE BONDS THEREFROM

CROSS REFERENCE TO RELATED APPLICATIONS

**[0001]** The present application is a continuation of U.S. Patent Application No. 14/291,874, filed May 30, 2014, the disclosure of which is incorporated herein by reference.

BACKGROUND OF THE DISCLOSURE

**[0002]** Microelectronic devices such as semiconductor chips typically require many input and output connections to other electronic components. The input and output contacts of a semiconductor chip or other comparable device are generally disposed in grid-like patterns that substantially cover a surface of the device (commonly referred to as an "area array") or in elongated rows which may extend parallel to and adjacent to each edge of the device's front surface, or in the center of the front surface. Typically, devices such as chips must be physically mounted on a substrate such as a printed circuit board, and the contacts of the device must be electrically connected to electrically conductive features of the circuit board.

**[0003]** Semiconductor chips are commonly provided in packages that facilitate handling of the chip during manufacture and during mounting of the chip on an external substrate such as a circuit board or other circuit panel. For example, many semiconductor chips are provided in packages suitable for surface mounting. Numerous packages of this general type have been proposed for various applications. Most commonly, such packages include a dielectric element, commonly referred to as a "chip carrier" with terminals formed as plated or etched metallic structures on the dielectric. These terminals typically are connected to the contacts of the chip itself by features such as thin traces extending along the chip carrier itself and by fine

leads or wires extending between the contacts of the chip and the terminals or traces. In a surface mounting operation, the package is placed onto a circuit board so that each terminal on the package is aligned with a corresponding contact pad on the circuit board. Solder or other bonding material is provided between the terminals and the contact pads. The package can be permanently bonded in place by heating the assembly so as to melt or "reflow" the solder or otherwise activate the bonding material.

**[0004]** Many packages include solder masses in the form of solder balls, typically about 0.1 mm and about 0.8 mm (5 and 30 mils) in diameter, attached to the terminals of the package. A package having an array of solder balls projecting from its bottom surface is commonly referred to as a ball grid array or "BGA" package. Other packages, referred to as land grid array or "LGA" packages are secured to the substrate by thin layers or lands formed from solder. Packages of this type can be quite compact. Certain packages, commonly referred to as "chip scale packages," occupy an area of the circuit board equal to, or only slightly larger than, the area of the device incorporated in the package. This is advantageous in that it reduces the overall size of the assembly and permits the use of short interconnections between various devices on the substrate, which in turn limits signal propagation time between devices and thus facilitates operation of the assembly at high speeds.

**[0005]** An interposer can be provided as an interconnection element having contacts and top and bottom surfaces thereof electrically connected with one or more packaged or unpackaged semiconductor dies at one of the top or bottom surface thereof, and electrically connected with another component at the other one of the top or bottom surfaces. The

other component may in some cases be a package substrate which in turn may be electrically connected with another component which may be or may include a circuit panel.

**[0006]** Despite all of the above-described advances in the art, still further improvements in interconnection elements incorporating a bond via array and methods of making such interconnection elements would be desirable.

#### SUMMARY OF THE DISCLOSURE

**[0007]** In accordance with an embodiment of the disclosure, a microelectronic package may include a substrate having a first region and a second region, the substrate having a first surface and a second surface remote from the first surface; at least one microelectronic element overlying the first surface within the first region; electrically conductive elements at the first surface of the substrate within the second region; a support structure having a third surface and a fourth surface remote from the third surface and overlying the first surface within the second region in which the third surface faces the first surface, the support structure having second and third electrically conductive elements exposed respectively at the third and fourth surfaces, the second electrically conductive elements being electrically connected to the conductive elements at the first surface of the substrate in the first region; and wire bonds defining edge surfaces and having bases electrically connected through ones of the third conductive elements to respective ones of the second conductive elements and ends remote from the support structure and the bases.

**[0008]** In accordance with an embodiment of the disclosure, a microelectronic package may include a substrate having a first region and a second region, the substrate having a first surface and a second surface remote from the first surface; at least one microelectronic element overlying the

first surface within the first region; electrically conductive elements exposed at the first surface of the substrate within the second region; wire bonds defining edge surfaces, having ends electrically connected to respective ones of the conductive elements at the first surface in the first region through respective second electrically conductive elements and having bases remote from the substrate and the ends; third electrically conductive elements respectively overlying and electrically connected with the bases of the wire bonds; and a dielectric encapsulation layer extending from at least one of the first or second surfaces and covering portions of the third electrically conductive elements and covering the wire bonds such that the wire bonds are separated from one another by the encapsulation layer, the encapsulation layer overlying at least the second region of the substrate, and, wherein unencapsulated portions of the third electrically conductive elements are defined by portions of the third electrically conductive elements that are uncovered by the encapsulation layer, the unencapsulated portions including surfaces of the third electrically conductive elements remote from the bases.

**[0009]** In accordance with an embodiment of the disclosure, a method of making a structure may include joining a support structure including wire bonds to a substrate, wherein the substrate has a first surface and a second surface remote from the first surface and a plurality of conductive elements at a the first surface, wherein a support structure has a third surface and a fourth surface remote from the third surface and second and third electrically conductive elements exposed respectively at the third and fourth surfaces, the second electrically conductive elements being electrically connected to the conductive elements at a first portion of the first surface of the substrate, wherein the wire bonds

define edge surfaces and have bases electrically connected through ones of the third conductive elements to respective ones of the second conductive elements and ends remote from the support structure and the bases; and forming a continuous dielectric encapsulation element on the substrate and the support structure, wherein the dielectric element is formed overlying and extending from the first portion of the first surface and filling spaces between and covering portions of the wire bonds such that the covered portions of the wire bonds are separated from one another by the encapsulation element, wherein unencapsulated portions of the wire bonds are defined by portions of the wire bonds that are uncovered by the encapsulation element, the unencapsulated portions including the ends, the encapsulation element overlying at least the first portion and the fourth surface of the support structure and defining a second portion of the first surface, the second portion being other than the first portion and having an area sized to accommodate an entire area of a microelectronic element, and at least some of the conductive elements at the first surface are at the second portion and configured for connection with the microelectronic element.

**[0010]** In accordance with an embodiment of the disclosure, a method of making a structure may include joining wire bonds of a support structure to a substrate having a first region and a second region, wherein the substrate has a first surface and a second surface remote from the first surface and a plurality of conductive elements at the first surface, wherein a support structure has a third surface and a fourth surface remote from the third surface and second electrically conductive elements exposed at the third surface, the second electrically conductive elements being electrically connected to the conductive elements at a first portion of the first surface of the substrate by wire bonds, wherein the wire

bonds define edge surfaces, have ends and have bases remote from the ends and electrically connected to the second electrically conductive elements, wherein the joining includes bonding the ends with respective ones of the conductive elements at the second region of the first surface of the substrate by flowing third electrically conductive elements through which the respective ones of the conductive elements at the first surface are electrically connected with the ends of the wire bonds; and forming a dielectric element on the substrate and removing support structure, wherein the dielectric element is formed overlying and extending from the second region of the first surface and filling spaces between and covering portions of the wire bonds such that the covered portions of the wire bonds are separated from one another by the encapsulation element, wherein unencapsulated portions of the second electrically conductive elements are defined by portions of the second electrically conductive elements that are uncovered by the encapsulation layer when the support structure is removed, the unencapsulated portions including surfaces of the second electrically conductive elements remote from the bases of the wire bonds, the dielectric element overlying at least the first region of the first surface, the first region being other than the second region and having an area sized to accommodate an entire area of at least one microelectronic element.

**[0011]** In accordance with an embodiment of the disclosure, a structure may include a substrate having a first surface and a second surface remote from the first surface, and conductive vias extending therein; first and second electrically conductive elements exposed respectively at the first and second surfaces; a plurality of wire bonds defining edge surfaces and having bases electrically connected through ones of the first conductive elements and

ones of the conductive vias to respective ones of the second conductive elements and ends remote from the substrate and the bases, the edge surface of each wire bond being separated from the edge surface of adjacent wire bonds, wherein the substrate defines at least one opening interior of portions of the first surface having an area sized to accommodate an entire area of a microelectronic element.

#### BRIEF DESCRIPTION OF THE DRAWINGS

**[0012]** Fig. 1A is a diagrammatic sectional view of an in-process unit according to an embodiment of the disclosure.

**[0013]** Fig. 1B is a diagrammatic sectional view of a microelectronic assembly according to an embodiment of the disclosure.

**[0014]** Fig. 1C is a top plan view of the in-process unit of Fig. 1A.

**[0015]** Fig. 2 is a diagrammatic sectional view of a microelectronic package including the in-process unit of Fig. 1A and the microelectronic assembly of Fig. 1B according to an embodiment of the disclosure.

**[0016]** Fig. 3 is a diagrammatic sectional view of an in-process unit according to another embodiment of the disclosure.

**[0017]** Fig. 4 is a diagrammatic sectional view of an in-process unit according to another embodiment of the disclosure.

**[0018]** Figs. 5-9 are diagrammatic sectional views illustrating stages in a method of fabricating a microelectronic package according to an embodiment of the disclosure.

**[0019]** Fig. 10 is a diagrammatic sectional of a microelectronic package including a redistribution layer at an outer surface of the package according to an embodiment of the disclosure.



**[0020]** Fig. 11 is a diagrammatic sectional of a microelectronic package including a thermally conductive element according to an embodiment of the disclosure.

**[0021]** Fig. 12 is diagrammatic sectional of an in-process unit including a plurality of thermally conductive elements according to an embodiment of the disclosure.

**[0022]** Fig. 13 is a diagrammatic sectional view of a microelectronic package including the in-process unit of Fig. 12 and a microelectronic assembly according to an embodiment of the disclosure.

#### DETAILED DESCRIPTION

**[0023]** A microelectronic package 10 may be fabricated by joining and electrically connecting wire bonds 14 extending from a support structure 12 with a microelectronic assembly 16 including a microelectronic element 18, such as a semiconductor chip, in accordance with an embodiment of the disclosure, as shown in Figs. 1A, 1B, 1C and 2. The chip may embody a plurality of active devices (e.g., transistors, diodes, etc.), a plurality of passive devices (e.g., resistors, capacitors, inductors, etc.), or both active devices and passive devices. In a particular embodiment, the chip may be configured to have a predominant function as a logic chip, e.g., a programmable general or special purpose processor, a microcontroller, a field programmable gate array ("FPGA") device, an application specific integrated circuit ("ASIC"), a digital signal processor, among others, or a predominant function other than as a logic chip, such as a memory, for example, a volatile memory storage area, e.g., dynamic random access memory ("DRAM"), static random access memory ("SRAM"), a nonvolatile memory storage array such as flash memory or magnetic random access memory ("MRAM"). As such, the embodiment of Fig. 2 is in the form of a packaged

microelectronic element such as a semiconductor chip assembly that is used in computer or other electronic applications.

**[0024]** Referring to Figs. 1A and 1C, the support structure 12 may include a substrate 20 having a first surface 22 and a second surface 24, and opposing edge surfaces 19 extending from the surface 22 to the surface 24. The substrate 20 typically is in the form of a dielectric element, which is substantially flat. The dielectric element may be sheet-like and may be thin. In particular embodiments, the dielectric element can include one or more layers of organic dielectric material or composite dielectric materials, such as, without limitation: polyimide, polytetrafluoroethylene ("PTFE"), epoxy, epoxy-glass, FR-4, BT resin, thermoplastic, or thermoset plastic materials.

**[0025]** The first surface 22 and second surface 24 may be substantially parallel to each other and spaced apart at a distance perpendicular to the surfaces 22, 24 defining the thickness of the substrate 12. The thickness of substrate 12 may be within a range of generally acceptable thicknesses for the present application. In an embodiment, the distance between the first surface 22 and the second surface 24 is between about 10-500  $\mu\text{m}$ . For purposes of this discussion, the first surface 22 may be described as being positioned opposite or remote from second surface 24. Such a description, as well as any other description of the relative position of elements used herein that refers to a vertical or horizontal position of such elements is made for illustrative purposes only to correspond with the position of the elements within the drawings, and is not limiting.

**[0026]** Electrically conductive elements 26 and 28, in the form of contacts or pads, may be arranged, respectively, at the first and second surfaces 22, 24. As used in the present description, when an electrically conductive element is

described as being "at" the surface of another element having dielectric structure, it indicates that the electrically conductive structure is available for contact with a theoretical point moving in a direction perpendicular to the surface of the dielectric structure toward the surface of the dielectric structure from outside the dielectric structure. Thus, a conductive structure that is exposed at a surface of a dielectric structure may project from such surface; may be flush with such surface; or may be recessed relative to such surface and exposed through a hole or depression in the dielectric. The conductive elements 26, 28 may be flat, thin elements which are respectively aligned in a direction of the thickness of the substrate 20. The conductive elements 26, 28 may be a solid metal material, such as copper, gold, nickel, Palladium or other materials that are acceptable for such an application, including various alloys including one or more of copper, gold, nickel, palladium or combinations thereof.

**[0027]** At least some of conductive elements 26 may be interconnected to corresponding conductive elements 28. Such an interconnection may be completed using vias 30 formed in substrate 20 that can be lined or filled with conductive metal 33 that can be formed of the same material as conductive elements 26, 28.

**[0028]** A plurality of wire bonds 14 may be joined electrically with at least some of the conductive elements 26. The wire bonds 14 may be bonded at a base 32 thereof, such as a ball bond or a wedge bond, to the conductive element 26. Each of the wire bonds 14 may extend to a free end 34 remote from the base 32 of such wire bond and remote from substrate 20, and include an edge surface 36 extending from the free end 34 to the base 32. As described below, the ends 34 of wire bonds 14 are characterized as being free in

that they are not electrically connected or otherwise joined to microelectronic element 18 or any other conductive features within microelectronic package 10 that are, in turn, connected to microelectronic element 18. In other words, free ends 34 are available for electrical connection, either directly or indirectly as through a solder ball or other features discussed herein, to a conductive feature external to package 10 when the wire bonds 14 are joined to the microelectronic assembly 16. The fact that ends 34 are held in a predetermined position by, for example, an encapsulation layer in the package 10 as discussed herein (see Fig. 2) or otherwise joined or electrically connected to another conductive feature does not mean that they are not "free" as described herein, so long as any such feature is not electrically connected to microelectronic element 18. Conversely, base 32 is not free as it is either directly or indirectly electrically connected to microelectronic element 18, as described herein. The particular size and shape of base 32 can vary according to the type of material used to form wire bond 14, the desired strength of the connection between wire bond 14 and conductive element 26, or the particular process used to form wire bond 14. The wire bonds 14 may have a construction and be formed on the substrate 20 extending from the conductive elements 26 in any suitable manner, such as described in U.S. 2013/0093087, filed Feb. 24, 2012, incorporated by reference herein.

**[0029]** The substrate 20 having the wire bonds 14 joined with the conductive elements 26 at the surface 22 and extending therefrom, and the conductive elements 26 electrically connected to respective conductive elements 28 at the surface 24 through the vias 30, may serve as an in-process unit in the form of the support structure 12 that supports the wire bonds 14 before the wire bonds are joined

with the microelectronic assembly 16, such as illustrated in Figs. 1B and Fig. 2 and discussed in detail below. In one embodiment, the support structure 12 may be configured in the form of a frame surrounding an open, interior region 38 having dimensions sufficient to receive components therein, such as a microelectronic element 18 as shown in Fig. 2.

**[0030]** Referring to Fig. 1B, the microelectronic assembly 16 may include a substrate 40 having a first surface 42 and a second surface 44. The substrate 40 may have a similar shape and configuration as the substrate 20, as described above. The substrate 40, unlike the substrate 20, may have terminals for further electrical interconnection with a circuit panel, e.g., a circuit board. Alternatively, the substrate 40 can be a circuit panel or circuit board. In one example thereof, the substrate 40 can be a module board of a dual-inline memory module ("DIMM"). In yet another variation, the substrate 40 can be a microelectronic element such as a semiconductor chip embodying a plurality of active devices, e.g., in form of an integrated circuit or otherwise. In one embodiment, the substrate 40 may be considered as divided into a first region 46 and a second region 48. The first region 46 lies within the second region 48 and includes a central portion of the substrate 40 and extends outwardly therefrom. The second region 48 substantially surrounds the first region 46 and extends outwardly therefrom to the outer edges of the substrate 40. In this embodiment, no specific characteristic of the substrate 40 itself physically divides the two regions; however, the regions are demarked for purposes of discussion herein with respect to treatments or features applied thereto or contained therein.

**[0031]** The microelectronic element 18 may be mounted to first surface 42 of the substrate 40 within first region 46. Microelectronic element 18 may be a semiconductor chip or

another comparable device. In the embodiment of Fig. 1B, the microelectronic element 18 is mounted to the first surface 42 as a "flip-chip" configuration, where contacts (not shown) on the microelectronic element 18 may be connected to conductive elements 50 at the surface 42 within the first region 46, such as by solder bumps or the like (not shown) that are positioned beneath microelectronic element 18. In an embodiment, conductive elements 50 are formed from materials similar to those from which the elements 26, 28 are formed.

**[0032]** The conductive elements 50 may further include pads or contacts 52 within the second region 48 at the surface 42. At least some of conductive elements 50 may be interconnected to the pads 52, and at least some of the conductive elements 50 and pads 52 may be connected to conductive pads or terminals (not shown) at the surface 44 of the substrate 40. Such an interconnection can be completed using vias (not shown) formed in the substrate 40 that can be lined or filled with conductive metal, similarly as described above for the support structure 20. Optionally, conductive elements 50 and pads 52 can be further interconnected to one another by traces on the substrate 40.

**[0033]** Third conductive elements 54, such as formed of a conductive paste or solder or other conductive masses, may overlie and contact surfaces 56 of the pads 52 remote from and opposite the surface 42 of the substrate 40. In one embodiment, stenciling, dispensing, screen printing, controlled spraying, e.g., a process similar to inkjet printing, or transfer molding may be used to form conductive elements 54 on the pads 52. The elements 54 may be a bond material metal or bond metal, similar to the elements 50. The pads 52 may be arranged in a pattern within the second region 48 so as to be aligned in a thickness direction of the assembly 16 with respective pads 28 of the support structure

12, which are arranged in a predetermined pattern, when the wire bonds 14 of the support structure 12 are joined with the assembly 16 as shown in Fig. 2, to form the microelectronic package 10. In the microelectronic package 10, corresponding pads 28 are joined and electrically connected to pads 52 through the conductive elements 56, and the wire bonds 14 hence may be electrically connected to contacts of the microelectronic element 18 and conductive elements of the assembly 16.

**[0034]** Microelectronic assembly 10 further may include an encapsulation layer 58 formed from a dielectric material. In the embodiment of Fig. 2, encapsulation layer 58 is formed, such as by film-assisting molding or like techniques, over the portions of first surface 42 of substrate 40 that are not otherwise covered by or occupied by microelectronic element 18, or conductive elements 50. Similarly, encapsulation layer 58 is formed over the portions of conductive elements 52 that are not otherwise covered by the conductive elements 56, uncovered portions of the conductive elements 56, uncovered portions of the conductive elements 26, 28, portions of the surfaces 22, 24 not otherwise covered by the conductive elements 26, 28, and the edges 19 of the support structure 12. Encapsulation layer 58 may also substantially cover the microelectronic element 18, the wire bonds 14, including the bases 32 and at least a portion of edge surfaces 36 thereof. A portion of wire bonds 14 may remain uncovered by encapsulation layer 58, which can also be referred to as unencapsulated portions 59, thereby making the wire bond available for electrical connection to a feature or element located outside of encapsulation layer 58. In embodiments, at least end surfaces 34 of wire bonds 14 and optionally portions of the edges surfaces 36 may remain uncovered by encapsulation layer 58, such as described in US

2013/0093087, incorporated by reference herein. In other words, encapsulation layer 58 may cover all of microelectronic package 10 from first surface 42 and above, with the exception of a portion of the wire bonds 14, such as end surfaces 34, edge surfaces 36 or combinations of the two.

**[0035]** Encapsulation layer 58, which can be an integral, continuous layer, serves to protect the other elements within microelectronic package 10, particularly wire bonds 14. This allows for a more robust structure that is less likely to be damaged by testing thereof or during transportation or assembly to other microelectronic structures. Encapsulation layer 58 may be formed from a dielectric material with insulating properties such as that described in U.S. Patent App. Pub. No. 2010/0232129, which is incorporated by reference herein.

**[0036]** Advantageously, the microelectronic assembly 16 may be fabricated completely and independently, and the wire bonds 14 may be joined thereto using the support structure 12, which is also fabricated independently, to obtain the microelectronic package 10.

**[0037]** In another embodiment as shown in Fig. 3, a support structure 112 having components the same or similar to the support structure 12 as described above, may further include a redistribution layer 120 of dielectric material extending along the surface 24. Traces 122 at surface 124 of the redistribution layer 120, the surface 124 being remote from surface 22 of the support structure 12 and remote from and opposite surface 126 of the redistribution layer 120, may be electrically connected to contact pads 28. Traces 122 of the redistribution layer 120 can be electrically coupled between the electrically conductive elements 28 and pads 130 at the surface 126. The pads 130 are arranged at the surface 126, such that similar to the support structure 12 and as



shown in FIG. 1, wire bonds 14 may be electrically connected with at least some of the pads 52, through traces 122 connected with pads 130 which are aligned with the pads 52 at the surface 42 of the assembly 16. In one embodiment, the redistribution layer 120 may overlie only a portion of the surface 24 of the support structure 12 and the pads 28. The redistribution layer 120, in effect, serves as what is known as a fan-out layer that may allow the support structure 12 to connect to an array of different configurations of pads 52 at the surface 42 of the microelectronic assembly 16 than the array of conductive elements 26 at the surface 22 of the support structure 112 would otherwise permit.

**[0038]** In another embodiment as shown in Fig. 4, a support structure 212 having components the same or similar to the support structure 12 as described above, may include a redistribution layer 220 of dielectric material extending along the surface 22. Traces 222 of the redistribution layer 220 may be electrically coupled between the electrically conductive elements 26 and electrically conductive elements 230 at a surface 226 of the redistribution layer. In one embodiment, the traces can be at the surface 224 facing the surface 22 of the support structure 212 and remote from and opposite the surface 226 of the redistribution layer 220, and may be electrically connected to contact pads 225 at the surface 224. The pads 225 may be arranged at the surface 224 to contact the pads 26 at the surface 22. The pads 230 at the surface 226 may be joined to bases of wire bonds 14, similar to the connection with the pads 26 in the support structure 12 and as shown in Fig. 1A. The redistribution layer 212, thus, may provide that the wire bonds 14 may be electrically connected with at least some of the pads 26, through traces 222 electrically connected with pads 230 and pads 225 which are aligned with the pads 26 at the surface 22

of the support structure 212. In one embodiment, the redistribution layer 220 may overlies only a portion of the surface 22 of the support structure 212 and the pads 26. The redistribution layer 220, in effect, serves as a fan-out layer that may allow the support structure 212 to connect to an array of different configurations of pads 52 at the surface 42 of the microelectronic assembly 16 than the conductive element 26 array at the surface 22 of the support structure 212 would otherwise permit.

**[0039]** In a further embodiment, a support structure may have a redistribution layer at a surface of the support structure that can be joined with a surface of a microelectronic assembly, such as the assembly 16, and the surface of the support structure to which the wire bonds are joined and extend therefrom.

**[0040]** Figs. 5-9 show steps for manufacturing a microelectronic package 400 in accordance with another embodiment of the disclosure. Referring to FIG. 5, a first metallization layer 402, such as including copper or like conductive materials, may be deposited on a surface 404 of a release layer 406, which is attached at a surface 408, remote from the surface 404, to a temporary substrate 409 using an adhesive layer 411. The metal layer 402 may be deposited in some manner, such as by patterning of a metal foil, such as a copper foil, as suitable, to obtain conductive elements 410, in the form of pads or contacts similar to the conductive elements 26 as described above, arranged on the release layer 406.

**[0041]** Referring to FIG. 6, wire bonds 414 having bases 416 and free ends 418 remote from the bases, such as described above for the wire bonds 14, may be electrically connected to the conductive elements 410, for example, by joining bases 416 which are in the form of ball bonds or

wedge bonds to surfaces 419 of the elements 410 which are remote from the surface 404 of the release layer 406. The structure as illustrated in Fig. 6 is an in-process unit 440 including wire bonds 414 arranged for joining to contact pads of a microelectronic assembly, such as assembly 500 as shown in Fig. 7. As the wire bond array of the unit 440 is formed separately from the microelectronic assembly 500, potential contamination of the contact surfaces of the wire bonds during manufacture of the microelectronic assembly may be avoided.

**[0042]** Referring to Fig. 7, the microelectronic assembly 500 may be assembled to provide for electrical connections between a microelectronic element 502 thereof and the wire bonds 414 of the in-process unit 440, when the wire bonds 414 are joined to the assembly 500 to form the package 400 as illustrated in Figs. 8-9. The assembly 500 may include a substrate 504, which may include logic components and electrical connections thereto (not shown), having a first surface 506 and a second surface 508 remote from the first surface 506. The substrate 504 may have a similar shape and configuration as the substrate 20, as described above. In one embodiment, the substrate 504 may be considered as divided into a first region 510 and a second region 512. The first region 510 lies within the second region 512 and includes a central portion of the substrate 504 and extends outwardly therefrom. The second region 512 substantially surrounds the first region 510 and extends outwardly therefrom to the outer edges of the substrate 504.

**[0043]** The microelectronic element 502, which may be a semiconductor chip or another comparable device, may be mounted to the first surface 506 of the substrate 504 within first region 510 as a flip-chip configuration, similar to the microelectronic element 18 of the assembly 16. Contacts 513

on the microelectronic element 502 at a surface 515 facing the surface 506 may be electrically connected to conductive elements 514 within the first region 510 at the surface 506 by conductive masses 516, such as solder bumps, conductive paste or the like, positioned beneath the microelectronic element 502. In an embodiment, the conductive elements 514 are formed from materials similar to those from which the conductive elements of the package 10 are formed.

**[0044]** The conductive elements 514 may further include pads or contacts 518 within the second region 512 at the surface 506. At least some of conductive elements 514 may be interconnected to the pads 518 through electrically conductive traces (not shown), and also electrically connected with electronic components (not shown) in the substrate 504 through the conductive traces within the substrate 504. At least some of the conductive elements 514 and pads 518 may be connected to conductive pads or terminals (not shown) at the surface 508 of the substrate 504. Such an interconnection can be completed using vias (not shown) formed in the substrate 504 lined or filled with conductive metal, similarly as described above for the assembly 16. In this manner, the first microelectronic element 502 may be electrically interconnected with the at least some of the contacts or terminals at the surface 508. Optionally, conductive elements 514 and pads 518 can be further interconnected to one another by traces on the substrate 504.

**[0045]** Electrically conductive masses 520, such as formed of a conductive paste, solder or like materials, may overlie and contact surfaces 522 of the pads 518 remote from and opposite the surface 506 of the substrate 504. The masses 520 may be made of the same or similar material as the masses 516, and be formed on the surface 506 in any order or simultaneously with respect to formation of the masses 516,

using the same or similar techniques as described above for the masses 56.

**[0046]** Microelectronic assembly 500 further may include an encapsulation layer 530 formed from a dielectric material. In the embodiment of Fig. 7, the encapsulation layer 530 may be formed, such as by molding, over portions of the conductive elements 514 and contacts 513 of the microelectronic assembly 502 not otherwise covered by the masses 514, portions of the masses 516 that are uncovered, and portions of the first surface 506 of substrate 504 in the region 510 that are not otherwise covered by another element. In addition, the encapsulation layer 530 may be formed over opposing side surfaces 503, 505 of the microelectronic element 502 that extend from the surface 515 to a surface 507 of the element 502 remote from and opposite the surface 515. The layer 530 may protect microelectronic element 502 to avoid electrical short circuiting between wire bonds 414 when the wire bonds 414 are joined with the assembly 500, so to help avoid malfunction or possible damage due to unintended electrical contact between a wire bond 414 and the microelectronic element 502. In one embodiment, the layer 530 may mechanically reinforce the joints between contacts 513 of the microelectronic element and the corresponding contacts 514 to which they are joined.

**[0047]** In one embodiment, the conductive masses 520 may be formed over the pads 518 subsequent to formation of the dielectric layer 530 covering the microelectronic element 502 and a portion of the surface 506 at the region 510.

**[0048]** Referring to Figs. 6-8, the pads 518 may be arranged in a pattern within the second region 512 so as to be aligned in a thickness direction of the assembly 500 with respective ends 418 of wire bonds 414, which are arranged in a predetermined pattern, when the in-process unit 440 is

joined with the assembly 500, during a step of fabricating the package 400. In the package 400, respective pads 518 may be electrically connected with pads 410 through the masses 520 and the wire bonds 414. In one embodiment, the conductive masses 520 may be caused to reflow, after which the in-process unit 440 may be joined with the assembly 500 by being joined with respective ends 418 of the wire bonds 414.

**[0049]** In one embodiment, when joining the in-process unit 440 with the assembly 500, spacers or stand-offs 535, such as made of dielectric material, may be provided extending from the surface 506 of the assembly 500 to a surface 433 of the release layer 406 of the in-process unit 440 facing the surface 506 of the assembly 500. The spacers 535 may avoid the free standing wire bonds 414 of the in-process unit 440 from bending or becoming deformed due to the mass of the unit 440, before dielectric material is provided between the surfaces 433 and 506 as discussed below.

**[0050]** Subsequent to the wire bonds 414 being joined respectively with the pads 518 through the conductive masses 520, a second encapsulation layer 550 formed from a dielectric material may be formed over uncovered portions of surfaces of components between, and uncovered portions of surfaces of, the release layer 406 and the surface 506. In the embodiment of Fig. 8, the encapsulation layer 550 may be formed over portions of the pads 518 and pads 410 not otherwise covered by the masses 520 and the bases 416 of the wire bonds 414, uncovered portions of the wire bonds 414 and the masses 520, portions of the surface 506 of substrate 504 in the region 510 or 512 (shown in Fig. 7) that are not otherwise covered by another element, an uncovered outer surface 532 of the encapsulation layer 530, and any uncovered portions of the surfaces 503, 505 or 507 of the microelectronic element 502. The encapsulation layer 550 may

define a major surface 554, which is remote from the surface 506 of the substrate 504 and is adjacent a surface 433 of the release layer 406 facing the surface 506. Surfaces 470 of the conductive elements 410, which are remote from the surfaces of the elements 410 to which the bases 416 are joined, remain uncovered by the encapsulation layer 550 within the major surface 554.

**[0051]** Referring to Fig. 9, after the encapsulation layer 550 is formed, the release layer and the temporary substrate may be removed from the encapsulation layer 550, such as by applying a suitable chemical to dissolve the release layer which may be an adhesive. In one embodiment, the release layer may be from a water soluble plastic material such that it can be removed by exposure to water without affecting the other components of the in-process unit or the package. In another embodiment, the release layer may be removed from the encapsulation layer 550 after exposure to ultraviolet light. After removal of the release layer and the temporary substrate, the surfaces 470 remain uncovered and, thus, available for electrical connection and being joined to other components, such as traces, pads or terminals of another microelectronic assembly or package.

**[0052]** In one embodiment, referring to Fig. 10, the package 400 may further include a redistribution layer 600 of dielectric material extending along the surface 554. Traces 602 of the redistribution layer 600 may be electrically coupled between the conductive elements 410 and electrically conductive pads 612 at a surface of the redistribution layer 600. In one embodiment, as shown in Fig. 9, traces 602 may extend along the surface 604 facing the surface 554 and remote from surface 606 of the redistribution layer 600, and may be electrically connected with the conductive elements 410 by contacting the surfaces 470 thereof. The traces 602

may be coupled to the pads 612 by electrically conductive structure such as vias extending through the redistribution layer 600 to pads 612 at the surface 606. The pads 612 may be arranged at the surface 606 to provide for connection to external electrically conductive elements of another external component, such that the wire bonds 414 may electrically connect the microelectronic element 502 with the external component through the traces 602 connected with pads 612, which are aligned in a direction of the thickness of the package 400 with the surfaces 470 of the pads 410. The redistribution layer 600, in effect, serves as a fan-out layer of the interconnects of the assembly 500, which are limited to the periphery of the top surface of the assembly 500, to the full area array at a top surface 554 of the encapsulation layer 550.

**[0053]** In another embodiment, referring to FIG. 11, a microelectronic package 400A may have a similar construction to the package 400 as described above, except that the package 400A may further include a thermally conductive element or heat spreader 650 to remove heat generated by the microelectronic element. The thermally conductive element 650 may be disposed overlying the surface 507 of the microelectronic element 502 and respective portions 506A of the surface 506 of the substrate 504 extending away from the element 502 from locations aligned in a direction of the thickness of the package 400A with the side surfaces 503, 505. A portion of the encapsulation layer 550 may separate the heat spreader 650 from the wire bonds 414 and any electrically conductive elements joined with and extending away from the bases of the wire bonds, so as to electrically insulate the heat spreader 650 from such any other electrically conductive component of the package. In one embodiment, a portion 580 of the encapsulation layer 550



overlying the microelectronic element 502 and the portions 506A of the surface 506 may be removed by photolithography or like techniques, to define an open recess 580. In one example, laser ablation can be used to recess the encapsulation layer 550 uniformly to form a planar recessed surface 581 within the portion 580 extending from the surface 507 of the microelectronic element 502. Techniques that can be used to remove at least portions of the encapsulation layer selectively may include "wet blasting" techniques. In wet blasting, a stream of abrasive particles carried by a liquid medium is directed towards a target to remove material from the surface of the target. The stream of particles may sometimes be combined with a chemical etchant which may facilitate or accelerate the removal of material selectively to other structure such as the conductive elements 410 which are to remain after wet blasting.

**[0054]** The heat spreader 650, which may include copper or like thermally conductive material, may then be deposited or patterned at the surface 554 so as to be formed in the recess 580. A thermally conductive material in the form of an adhesive or grease 582, which may be applied first on the surface 507 or a portion of the surface 652 to confront the surface 507, may attach the element 650 to the microelectronic element 502. In one embodiment, the thermally conductive material is not electrically conductive so that the element 650 is electrically isolated from the microelectronic element 502. The thermally conductive material 582 may transfer heat between the microelectronic element 502 and the element 650 so as to remove heat from the package 400A.

**[0055]** In another embodiment, spreader 650 similar to that shown in Fig. 11 may be formed during formation of a first metallization layer 402 shown in Fig. 5. The same

metal of the layer 402, such as copper, may be patterned to form the pads 410 at a periphery of the layer 402, while a larger microelectronic element attach pad serving as spreader 650 is formed at an interior or center portion of the layer 402. Thermal paste 582 may be applied at the surface 507 of the microelectronic element 502 in the assembly 500. The in-process-unit formed from the metal layer 402 as described in this embodiment may then be joined with the assembly 500, similarly as described above.

**[0056]** In another embodiment, a microelectronic package 400B, as illustrated in Fig. 13, may include thermally conductive elements to remove heat from a microelectronic element and a substrate of a microelectronic assembly, such as the microelectronic assembly 500 illustrated in Fig. 7. The package 400B may be formed similarly and include similar components as described above for the package 400, except that an in-process unit 940, which includes similar components as the in-process unit 440 depicted in Fig. 6 and further includes thermal elements 950 and 960 as shown in Fig. 12 to provide for thermal dissipation, may be used to join wire bonds 414 and the thermal elements to the assembly 500. Referring to Fig 12, thermal element 950 may be attached to surface 404 with an adhesive in a first region 404A that lies within a second region 404B of the release layer 406 and includes a central portion of the in process-unit 940 and extends outwardly therefrom. The second region 404B substantially surrounds the region 404A and extends outwardly therefrom to a third region 404C, which substantially surrounds the region 404B and extends outwardly therefrom to the outer edges of the in-process unit 940. The wire bonds 414 and the conductive elements 410 are within the region 404B. The thermal element 950 may be mounted at a surface 951 thereof remote from a surface 952 by adhesive

(not shown) to the surface 404 within first region 404A, and the thermal element 960 may be mounted by adhesive at a surface 961 remote from a surface 962 to the surface 404 within the region 404C. The in-process unit 940 may then be joined to the microelectronic assembly 500, which is in a same or similar processing state as illustrated in Fig. 7, where, similarly as in the package 400, the ends 418 of the wire bonds 414 are joined through the conductive masses 520 to the conductive elements 518. In addition, thermally conductive material 582, which may be at a portion of the surface 506 facing the surface 962 or on the surface 962, may attach the element 960 with the surface 506. In one embodiment, the thermally conductive element 960 may have a frame shape so as least partially surround the region 404B of surface 506 of the package 404A at which the wire bonds 414 are disposed.

**[0057]** After joining the wire bonds 414 and thermal elements 950 and 960 to the assembly 550, an encapsulation layer 550A from a dielectric material may be formed over uncovered portion between the release layer 406 of the in process unit 940 and the surface 506, similarly as described above. In the embodiment of Fig. 13, the encapsulation layer 550A may be formed over the same uncovered portions and elements as in the package 400 illustrated in Fig. 8. In addition, the encapsulation layer 550A may be formed on portions of surface 952 of the thermal element 950 not covered by thermal adhesive 582, and opposing surfaces 953 of the thermal element 950 extending from the surface 951 to the surface 952, and a surface 963 of the thermal element 960 extending from the surface 961 and 962 and facing the wire bonds 414. The encapsulation layer 550A may define a major surface 554A, which is remote from the surface 506 of the substrate 504. Similarly as in the package 400, after

removal of the release layer and temporary substrate, surfaces 470 of the conductive elements 410, which are remote from the surfaces of the conductive elements 410 to which the bases 416 are joined, remain uncovered by the encapsulation layer 550 within the major surface 554A, and furthermore surfaces 961 and 951 of the thermal elements 960 and 950, respectively, remain uncovered. Accordingly, heat generated during operation of the package by the microelectronic element 502 and the substrate 504 may be transferred away therefrom by the thermal elements 950 and 960 and the thermally conductive material 582, thereby avoiding damage to the package's electronic circuitry due to overheating.

**[0058]** The above-described embodiments and variations of the invention can be combined in ways other than as specifically described above. It is intended to cover all such variations which lie within the scope and spirit of the invention.

## CLAIMS

1. A microelectronic package comprising:

a substrate having a first region and a second region, the substrate having a first surface and a second surface remote from the first surface;

at least one microelectronic element overlying the first surface within the first region;

electrically conductive elements at the first surface of the substrate within the second region;

a support structure having a third surface and a fourth surface remote from the third surface and overlying the first surface within the second region in which the third surface faces the first surface, the support structure having second and third electrically conductive elements exposed respectively at the third and fourth surfaces, the second electrically conductive elements being electrically connected to the conductive elements at the first surface of the substrate in the first region; and

wire bonds defining edge surfaces and having bases electrically connected through ones of the third conductive elements to respective ones of the second conductive elements and ends remote from the support structure and the bases.

2. The microelectronic package of claim 1 further comprising:

a dielectric layer extending from at least one of the first or second surfaces and covering portions of the wire bonds such that covered portions of the wire bonds are separated from one another by the encapsulation layer, the encapsulation layer overlying at least the second region of the substrate and the fourth surface of the support structure, wherein unencapsulated portions of the wire bonds are defined by portions of the wire bonds that are uncovered

by the encapsulation layer, the unencapsulated portions including the ends.

3. The microelectronic package of claim 1 further comprising:

a redistribution layer extending along at least a portion of at least one of the third surface or the fourth surface,

wherein the redistribution layer includes a redistribution substrate having a fifth surface adjacent the least one of the third surface or the fourth surface and a sixth surface remote from the fifth surface, first electrically conductive pads at the fifth surface of the redistribution substrate aligned with and contacting respective ones of the second or third electrically conductive elements at the third or fourth surfaces, and second electrically conductive pads at the sixth surface of the redistribution substrate electrically connected to the first conductive pads.

4. The microelectronic package of claim 1, wherein the second conductive elements are bonded to respective ones of the conductive elements at the first surface of the substrate by a conductive bonding material.

5. The microelectronic package of claim 1, wherein the bases of the wire bonds are ball bonds and conductive vias of the support structure electrically connect ones of the bases of the wire bonds with respective ones of the second conductive elements at the third surface of the support structure.

6. A microelectronic package comprising:

a substrate having a first region and a second region, the substrate having a first surface and a second surface remote from the first surface;

at least one microelectronic element overlying the first surface within the first region;

electrically conductive elements exposed at the first surface of the substrate within the second region;

wire bonds defining edge surfaces, having ends electrically connected to respective ones of the conductive elements at the first surface in the first region through respective second electrically conductive elements and having bases remote from the substrate and the ends;

third electrically conductive elements respectively overlying and electrically connected with the bases of the wire bonds; and

a dielectric encapsulation layer extending from at least one of the first or second surfaces and covering portions of the third electrically conductive elements and covering the wire bonds such that the wire bonds are separated from one another by the encapsulation layer, the encapsulation layer overlying at least the second region of the substrate, and, wherein unencapsulated portions of the third electrically conductive elements are defined by portions of the third electrically conductive elements that are uncovered by the encapsulation layer, the unencapsulated portions including surfaces of the third electrically conductive elements remote from the bases.

7. The microelectronic package of claim 6, wherein the second electrically conductive elements include at least one of solder or a conductive paste.

8. The microelectronic package of claim 6, wherein the encapsulation layer includes a surface remote from the substrate uncovering the unencapsulated portions of the third electrically conductive elements.

9. The microelectronic package of claim 6 further comprising:

a redistribution layer extending along at least a portion of a surface of the encapsulation layer remote from the first surface of the substrate and defining the uncovered portions of the third electrically conductive elements,

wherein the redistribution layer includes a redistribution substrate having a third surface adjacent the surface of the encapsulation layer and a fourth surface remote from the third surface, first electrically conductive pads at the third surface of the redistribution substrate aligned with respective ones of the bases of the wire bonds facing the uncovered portions of the third electrically conductive elements, and second electrically conductive pads at the fourth surface of the redistribution substrate electrically connected with the first conductive pads.

10. The microelectronic package of claim 6 further comprising:

a thermally conductive element overlying and in thermal communication with a surface of the microelectronic element remote from the first surface of the substrate and disposed within a recess of the encapsulation layer.

11. The microelectronic package of claim 6 further comprising:



a thermally conductive element overlying and in thermal communication with portions of the first surface in the second region.

12. A method of making a structure comprising:

joining a support structure including wire bonds to a substrate, wherein the substrate has a first surface and a second surface remote from the first surface and a plurality of conductive elements at a the first surface, wherein a support structure has a third surface and a fourth surface remote from the third surface and second and third electrically conductive elements exposed respectively at the third and fourth surfaces, the second electrically conductive elements being electrically connected to the conductive elements at a first portion of the first surface of the substrate, wherein the wire bonds define edge surfaces and have bases electrically connected through ones of the third conductive elements to respective ones of the second conductive elements and ends remote from the support structure and the bases; and

forming a continuous dielectric encapsulation element on the substrate and the support structure, wherein the dielectric element is formed overlying and extending from the first portion of the first surface and filling spaces between and covering portions of the wire bonds such that the covered portions of the wire bonds are separated from one another by the encapsulation element, wherein unencapsulated portions of the wire bonds are defined by portions of the wire bonds that are uncovered by the encapsulation element, the unencapsulated portions including the ends, the encapsulation element overlying at least the first portion and the fourth surface of the support structure and defining a second portion of the first surface, the second portion being other

than the first portion and having an area sized to accommodate an entire area of a microelectronic element, and at least some of the conductive elements at the first surface are at the second portion and configured for connection with the microelectronic element.

13. The method of claim 12 further comprising:

forming a redistribution layer extending along at least a portion of at least one of the third surface or the fourth surface,

wherein the redistribution layer includes a redistribution substrate having a fifth surface adjacent the least one of the third surface or the fourth surface and a sixth surface remote from the fifth surface, first electrically conductive pads at the fifth surface of the redistribution substrate aligned with respective ones of the second or third electrically conductive elements at the third or fourth surfaces, and second electrically conductive pads at the sixth surface of the redistribution substrate electrically connected to the first conductive pads.

14. The method of claim 13, wherein the bases of the wire bonds are ball bonds and conductive vias of the support structure electrically connect ones of the bases of the wire bonds with respective ones of the second conductive elements at the third surface of the support structure.

15. A method of making a structure comprising:

joining wire bonds of a support structure to a substrate having a first region and a second region, wherein the substrate has a first surface and a second surface remote from the first surface and a plurality of conductive elements at the first surface, wherein a support structure has a third

surface and a fourth surface remote from the third surface and second electrically conductive elements exposed at the third surface, the second electrically conductive elements being electrically connected to the conductive elements at a first portion of the first surface of the substrate by wire bonds, wherein the wire bonds define edge surfaces, have ends and have bases remote from the ends and electrically connected to the second electrically conductive elements, wherein the joining includes bonding the ends with respective ones of the conductive elements at the second region of the first surface of the substrate by flowing third electrically conductive elements through which the respective ones of the conductive elements at the first surface are electrically connected with the ends of the wire bonds; and

forming a dielectric element on the substrate and removing support structure, wherein the dielectric element is formed overlying and extending from the second region of the first surface and filling spaces between and covering portions of the wire bonds such that the covered portions of the wire bonds are separated from one another by the encapsulation element, wherein unencapsulated portions of the second electrically conductive elements are defined by portions of the second electrically conductive elements that are uncovered by the encapsulation layer when the support structure is removed, the unencapsulated portions including surfaces of the second electrically conductive elements remote from the bases of the wire bonds, the dielectric element overlying at least the first region of the first surface, the first region being other than the second region and having an area sized to accommodate an entire area of at least one microelectronic element.

16. The method of claim 15, wherein the third electrically conductive elements include at least one of solder or a conductive paste.

17. The method of claim 15, wherein the encapsulation layer includes a surface remote from the substrate uncovering the unencapsulated portions of the second electrically conductive elements.

18. The method of claim 15, further comprising:

forming a redistribution layer extending along at least a portion of a surface of the encapsulation layer remote from the first surface of the substrate and defining the uncovered portions of the second electrically conductive elements,

wherein the redistribution layer includes a redistribution substrate having a fifth surface adjacent the surface of the encapsulation layer and a sixth surface remote from the fifth surface, first electrically conductive pads at the fifth surface of the redistribution substrate aligned with respective ones of the bases of the wire bonds facing the uncovered portions of the third electrically conductive elements, and second electrically conductive pads at the fourth surface of the redistribution substrate electrically connected with the first conductive pads.

19. The method of claim 15 further comprising:

forming a thermally conductive layer element overlying and in thermal communication with a surface of the microelectronic element remote from the first surface of the substrate and disposed within a recess of the encapsulation layer.

20. The method of claim 15 further comprising:

forming thermally conductive elements overlying and in thermal communication with a surface of the microelectronic element remote from the first surface of the substrate and portions of the first surface at the second region, wherein the encapsulation layer is formed after the forming of the thermally conductive elements.

21. A structure comprising:

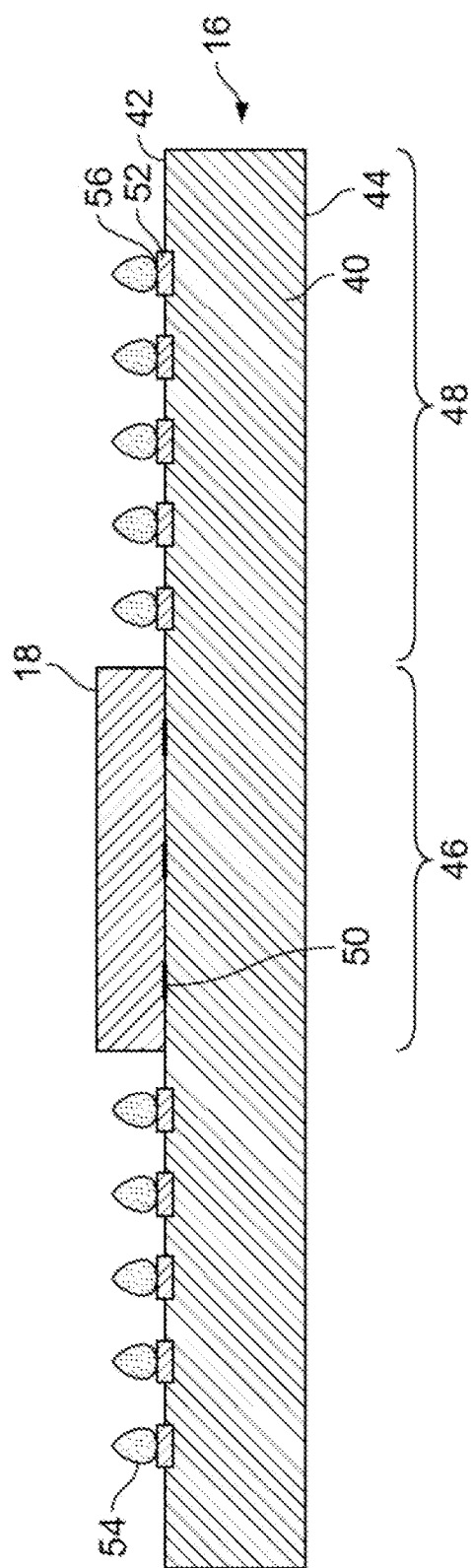
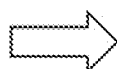
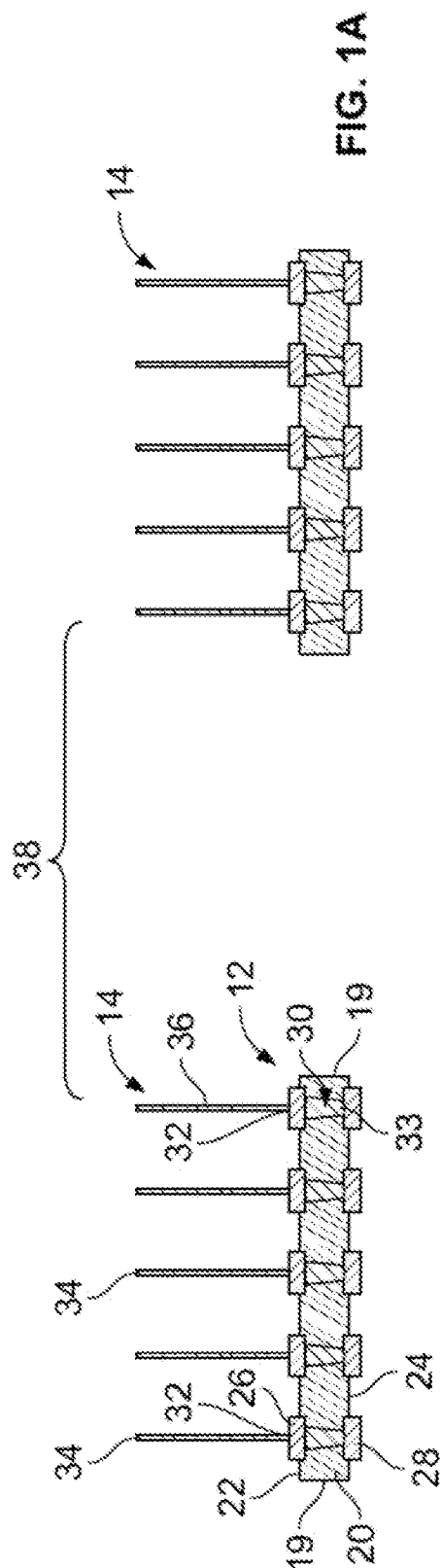
a substrate having a first surface and a second surface remote from the first surface, and conductive vias extending therein;

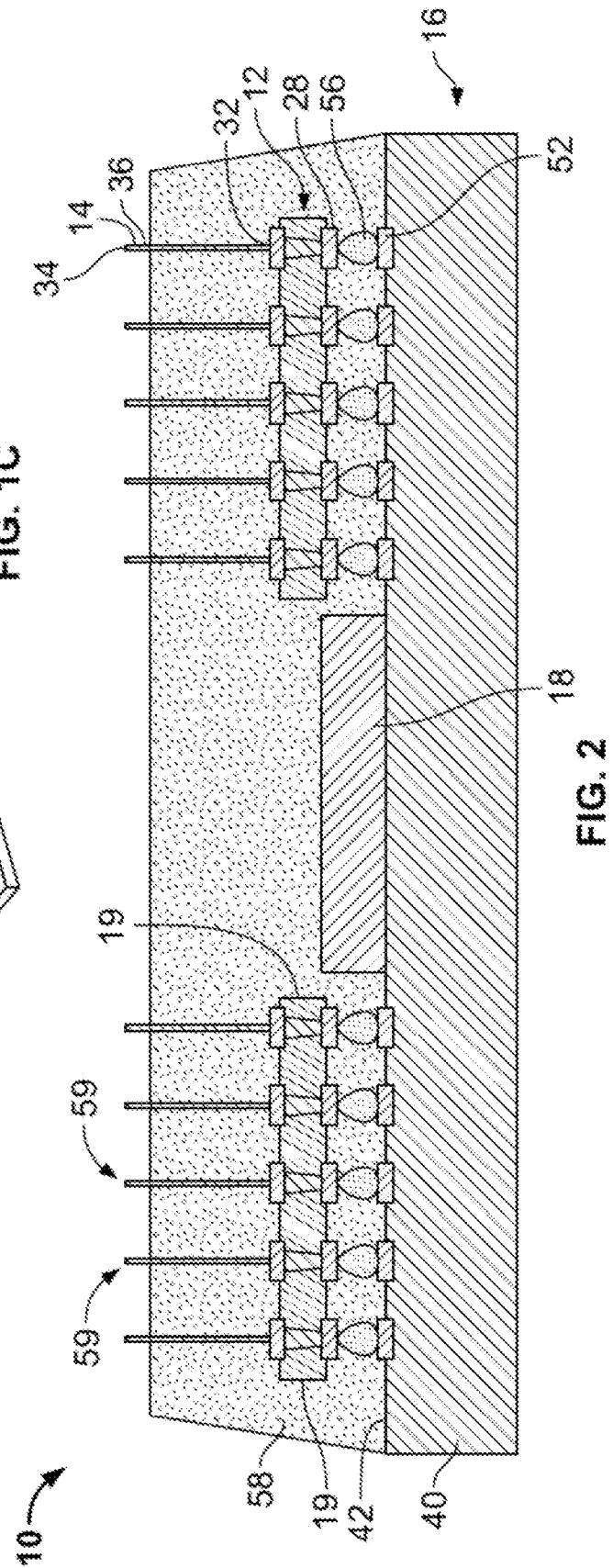
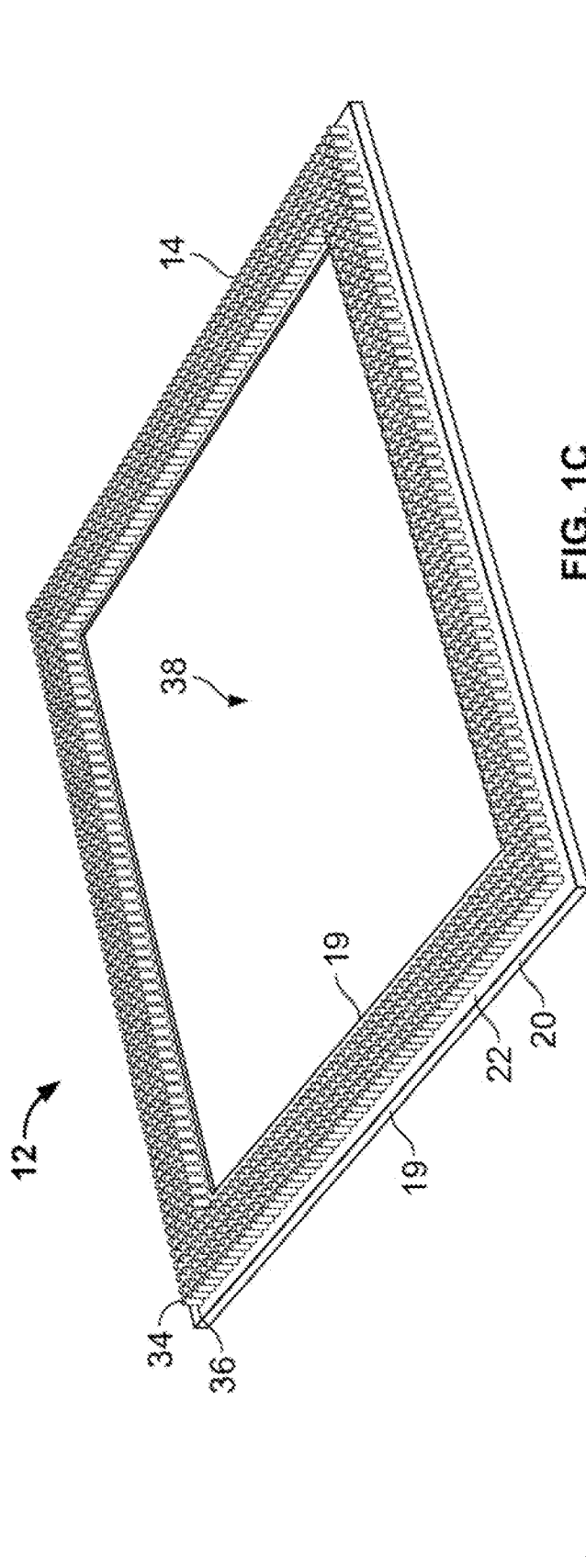
first and second electrically conductive elements exposed respectively at the first and second surfaces; and

a plurality of wire bonds defining edge surfaces and having bases electrically connected through ones of the first conductive elements and ones of the conductive vias to respective ones of the second conductive elements and ends remote from the substrate and the bases, the edge surface of each wire bond being separated from the edge surface of adjacent wire bonds,

wherein the substrate defines at least one opening interior of portions of the first surface having an area sized to accommodate an entire area of a microelectronic element.

22. The structure of claim 21, wherein the substrate defines a plurality of openings interior of the portions of the first surface each having an area sized to accommodate an entire area of a microelectronic element or a stack of microelectronic elements.





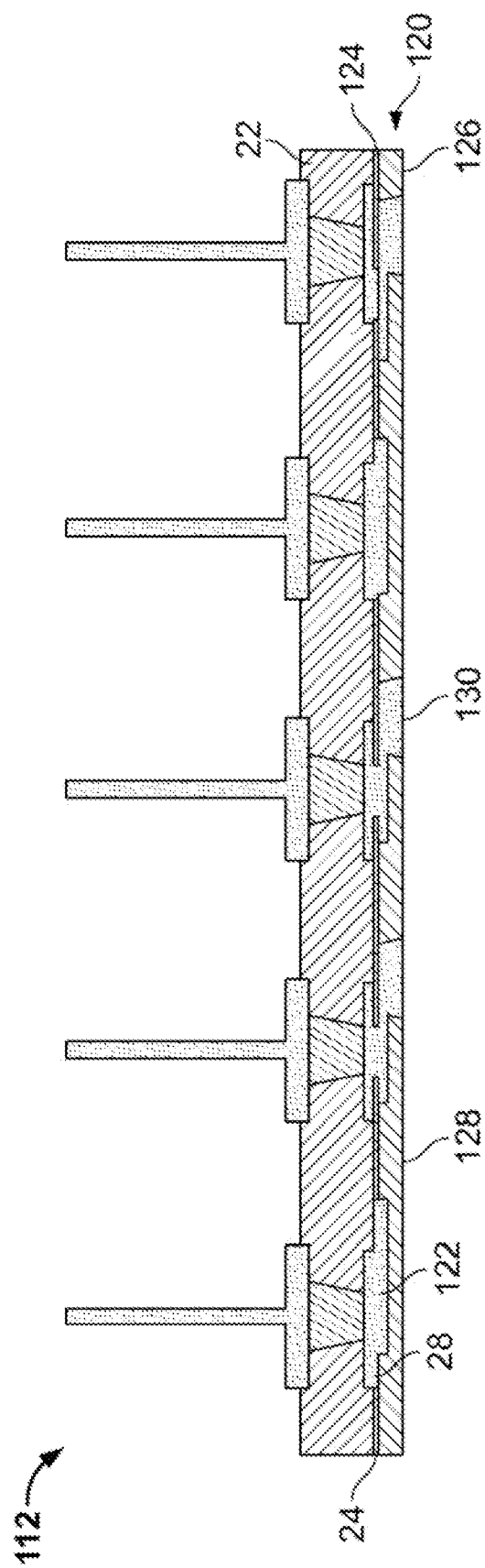


FIG. 3

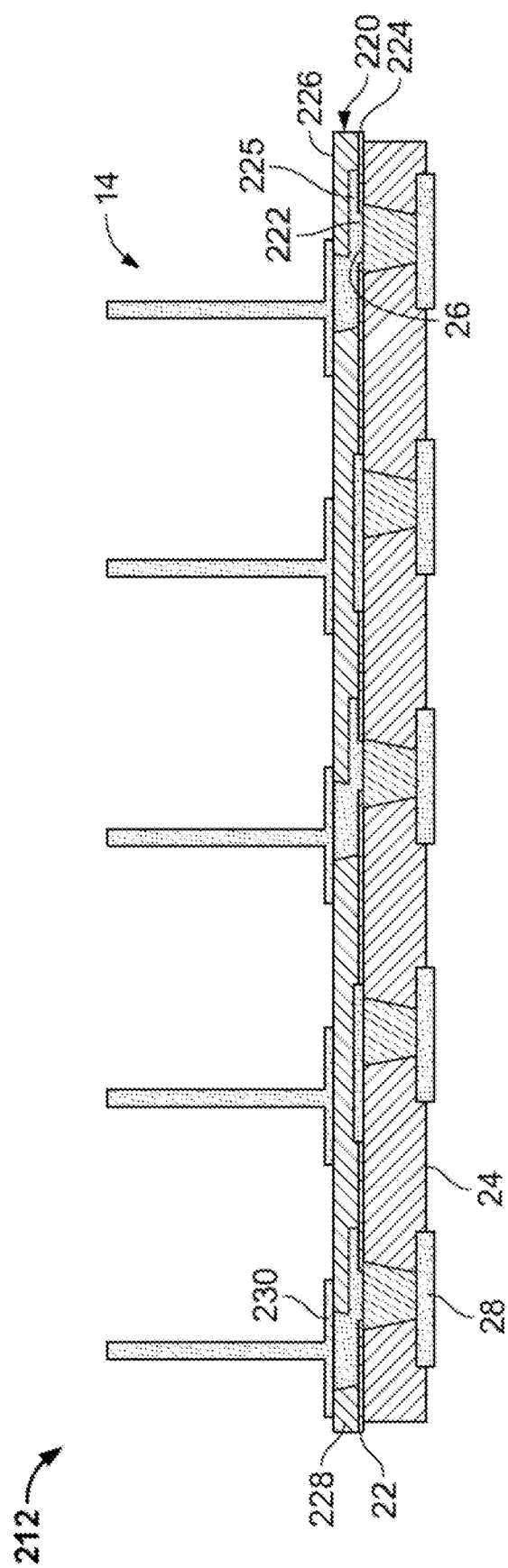


FIG. 4



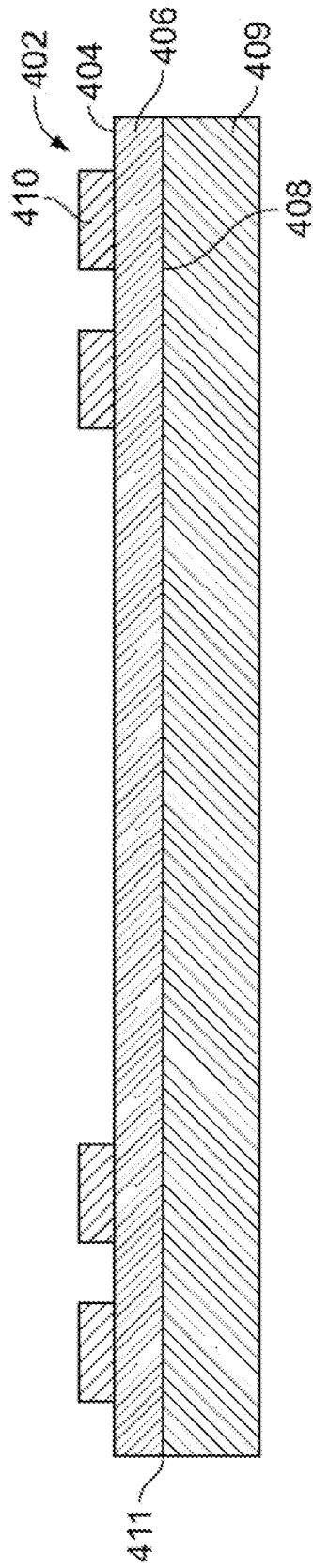


FIG. 5

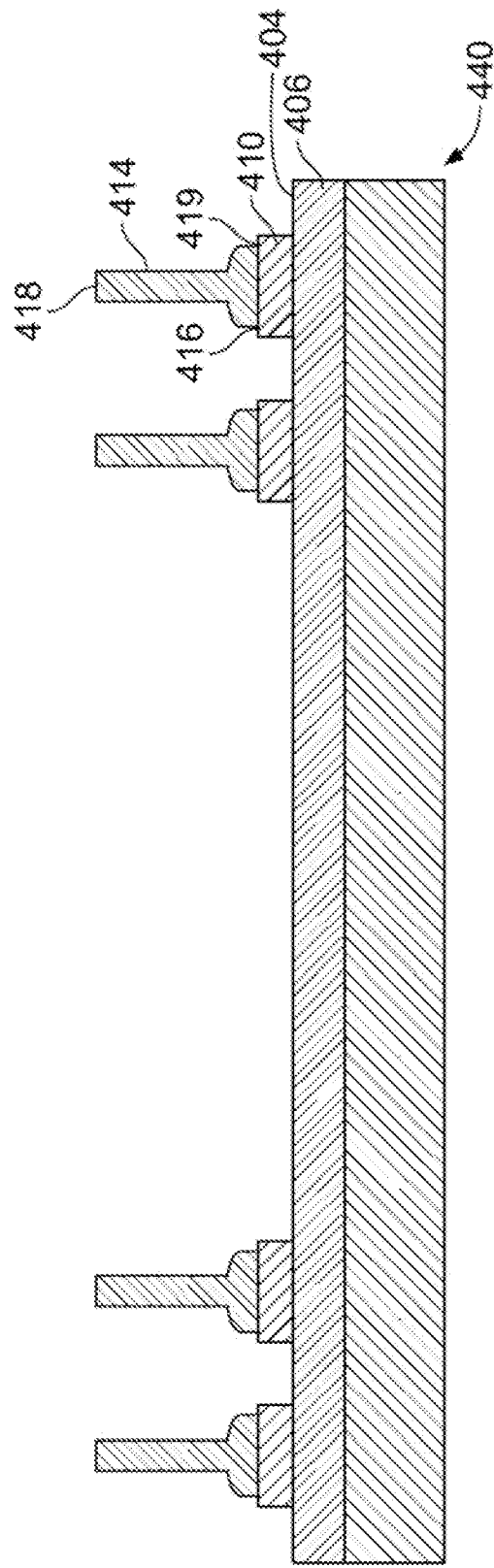
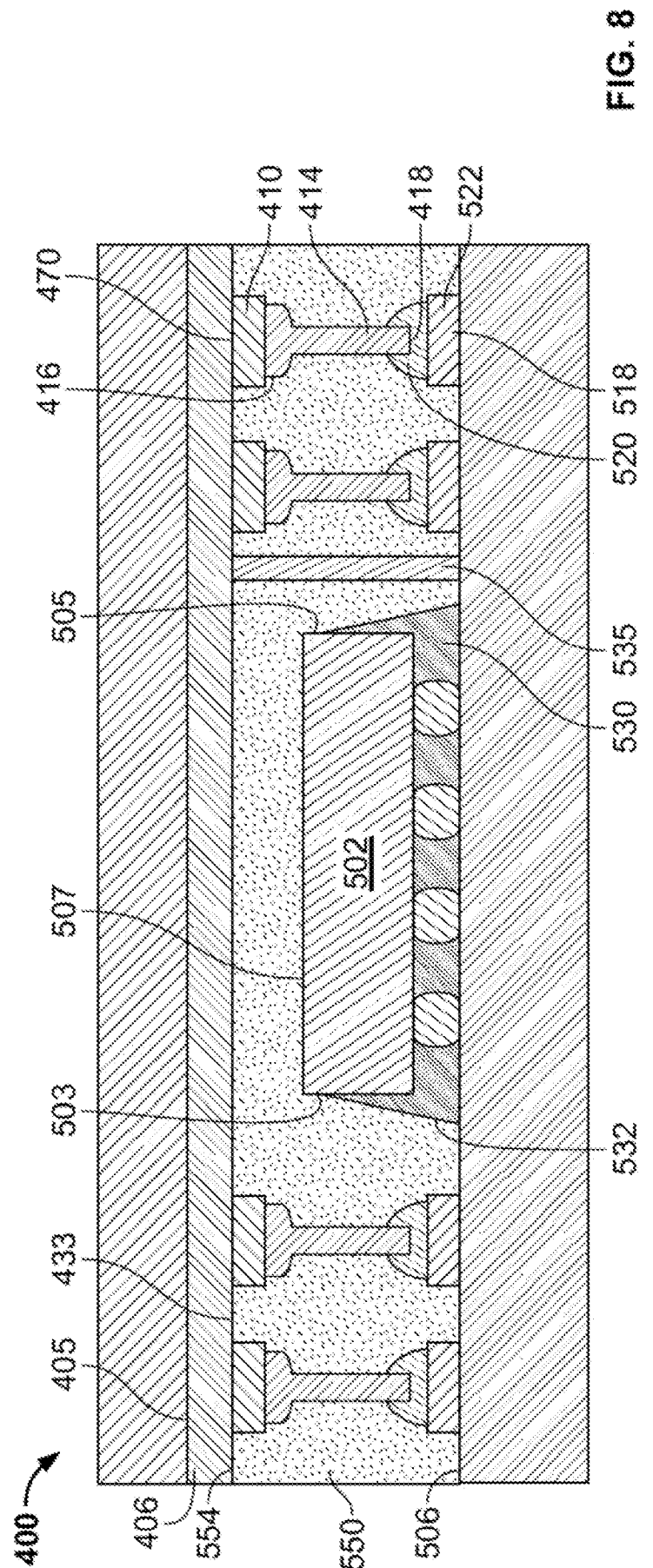
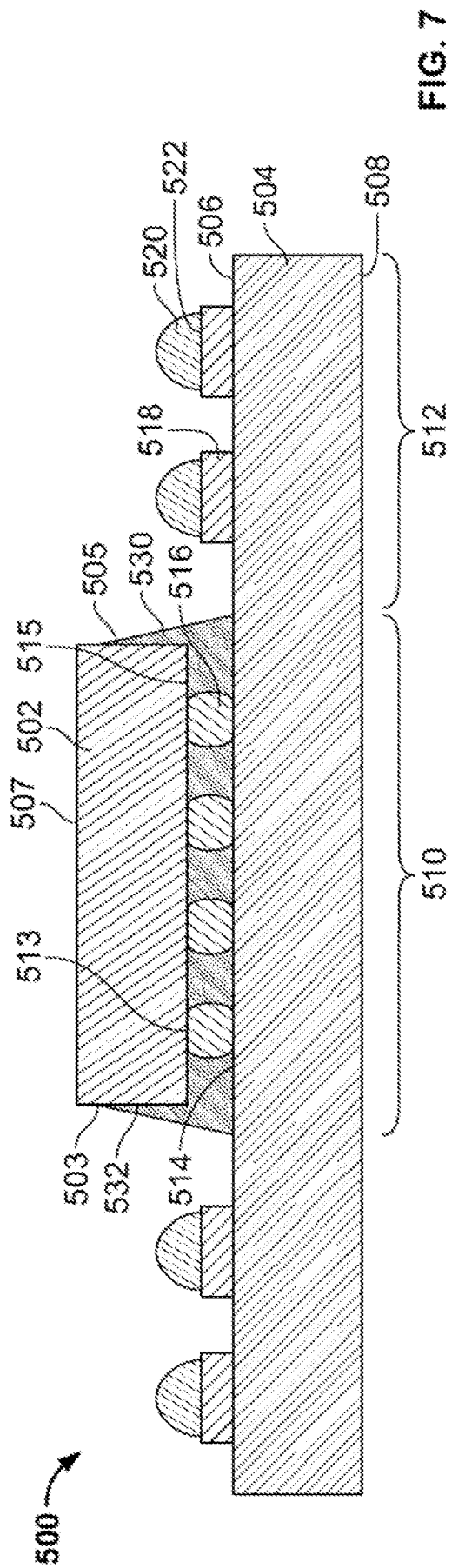


FIG. 6



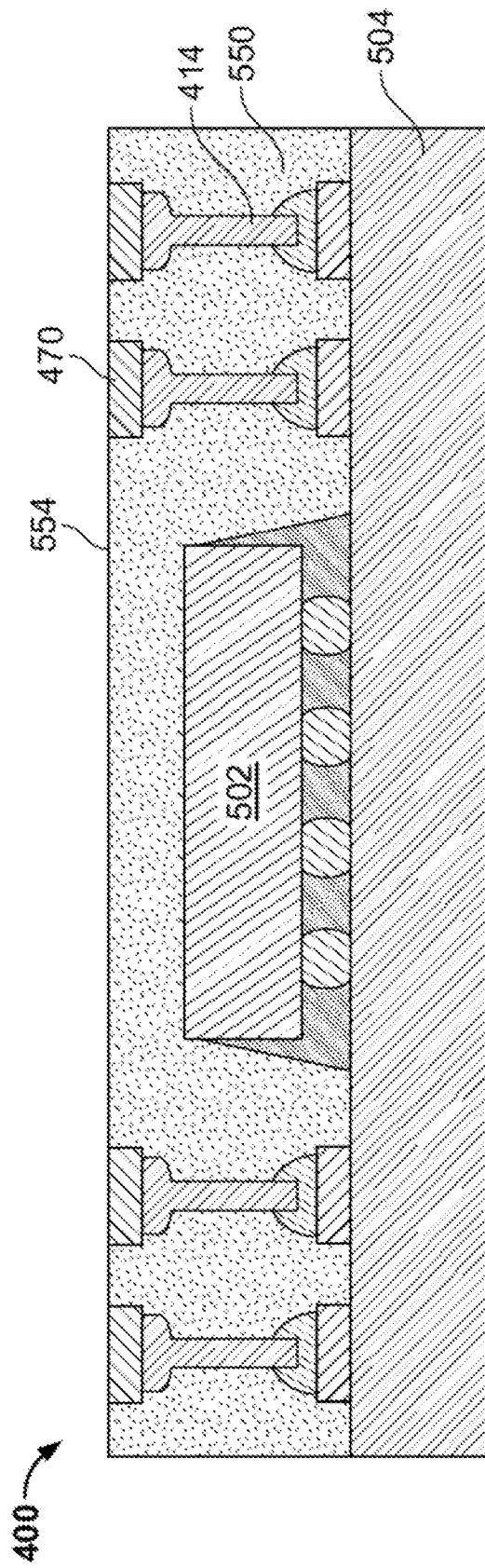


FIG. 9

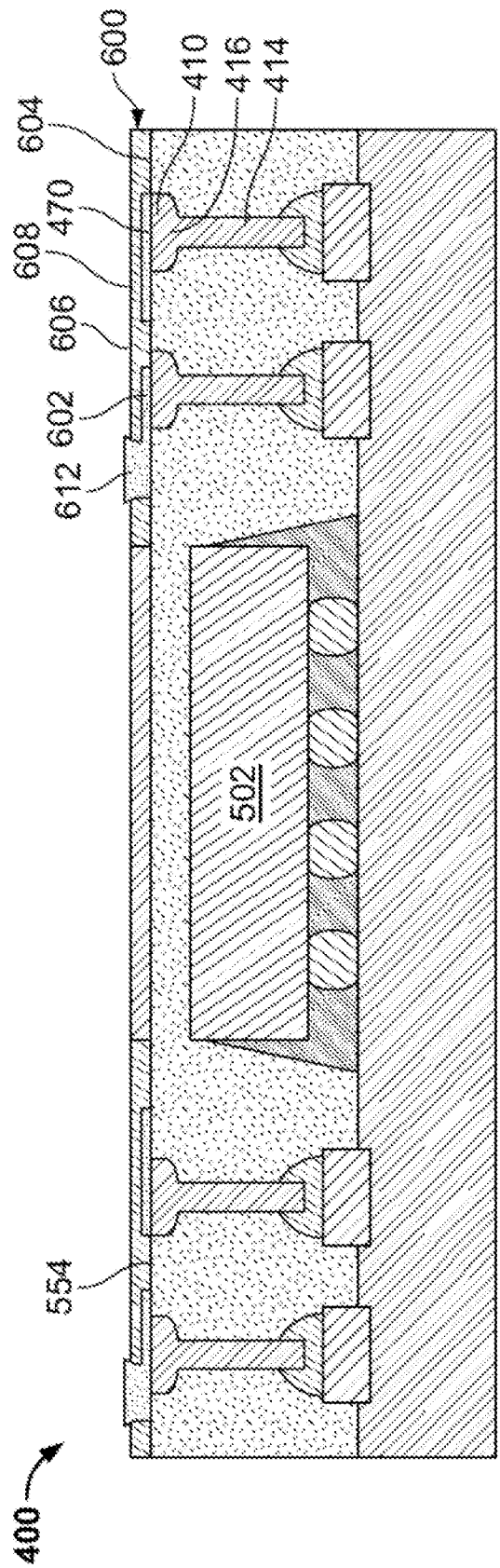


FIG. 10

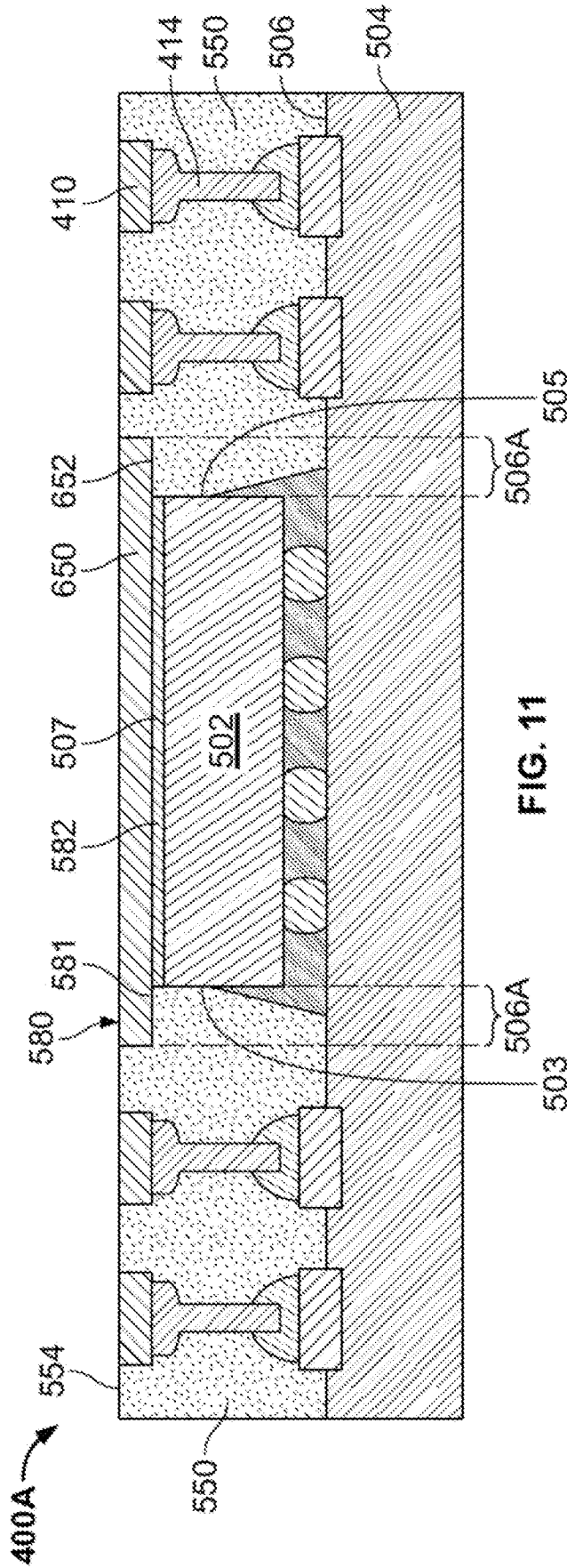


FIG. 11

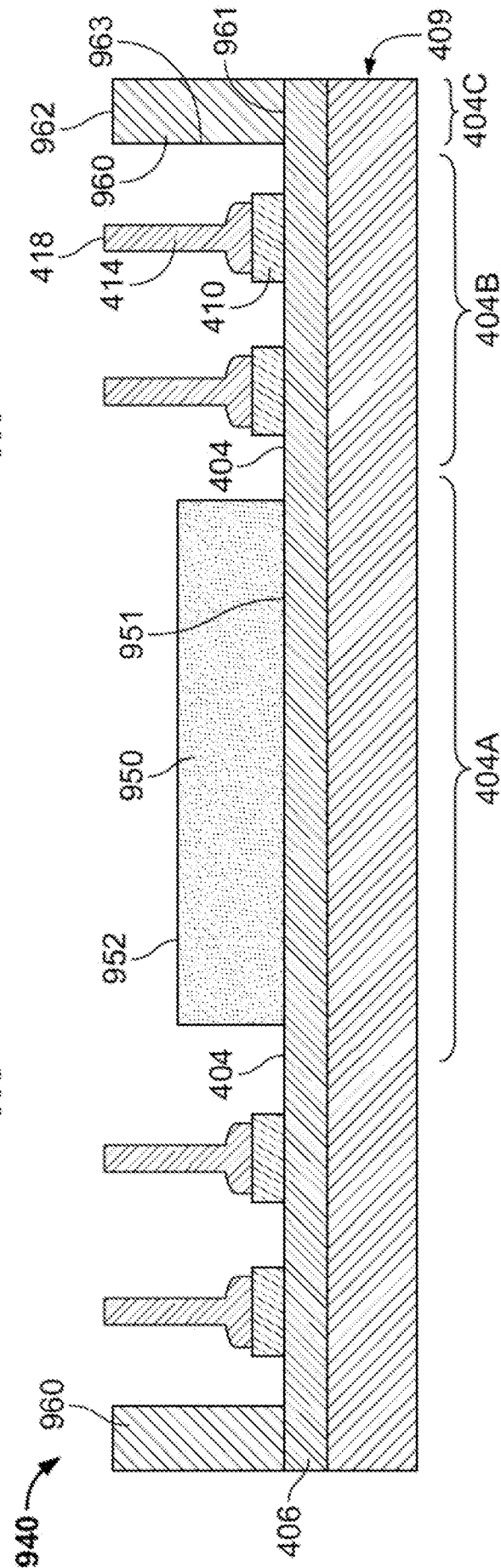


FIG. 12

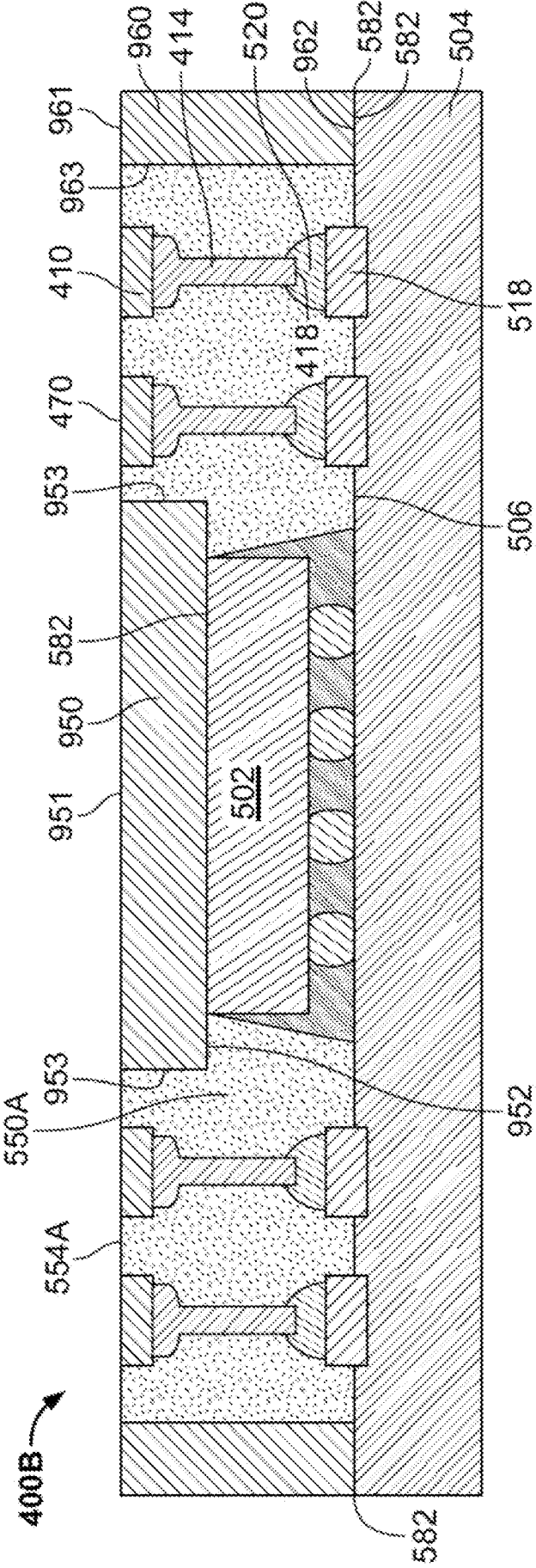


FIG. 13