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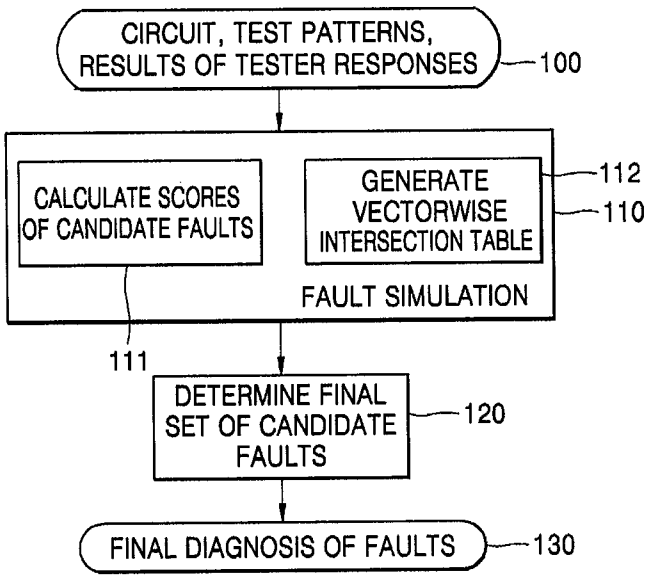
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(54) **Title:** MATCHING METHOD FOR MULTIPLE STUCK-AT FAULTS DIAGNOSIS



(57) **Abstract:** Provided is a matching method of diagnosing multiple stuck-at faults, which can accurately diagnose the multiple stuck-at faults using a single stuck-at fault simulator. The matching method includes calculating scores of candidate faults; generating a vectorwise intersection table; and determining a final set of candidate faults. The operations of calculating scores of the candidate faults and generating the vectorwise intersection table are serially performed during the simulation. The faults are classified as a vectorwise intersection, an intersection, a misprediction, a nonprediction, and a no error, and the calculation of the scores is performed for each of the classifications.

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MATCHING METHOD FOR MULTIPLE STUCK-AT FAULTS DIAGNOSIS

TECHNICAL FIELD

The present invention relates to a semiconductor testing method, and more particularly, to a matching algorithm for diagnosing multiple stuck-at faults.

BACKGROUND ART

As the complexity of VLSI (Very Large Scale Integration) has increased, and thus, the demands for diagnosing faults has also increased. The fault diagnosis refers to a process of deducing locations of defects and kinds of defects causing an operational error. An exact fault diagnosis can identify both design and process errors, which results in a yield improvement. Therefore, it is important to develop an effective fault diagnosis method for improving the quality of chips and reducing fabrication costs.

As such, a rank matching algorithm generally assumes the single fault assumption. While the single fault assumption simplifies the diagnosis process, it leads to problems with multiple or complex faults.

According to the invention of Korean Registered Patent No. 10-0334473, the operations of a semiconductor integrated circuit device are simulated at a switch level using a test vector set in an apparatus for diagnosing faults of the semiconductor integrated circuit device, and thus, simulation results are generated. In addition, the semiconductor integrated circuit device is tested using the test vector set to generate a test result. Then, a first set of combinations of circuit elements is defined based on a circuit data of the test circuit device. Here, the semiconductor circuit device is composed of the circuit elements. A final set of candidate faults is estimated from the first set of combinations based on the simulation result and the test result for each of the test vectors, and then, the final set of candidate faults is outputted.

In the thesis of "Poirot: Applications of a logic fault diagnosis tool / Venkataraman, S.; Drummonds, S.B. / Design & Test of Computers, IEEE Volume 18, Issue 1, Jan.-Feb. 2001 Page(s):19-30", the type of faults is diagnosed by counting the cases of Vectorwise intersection, Intersection, Nonprediction, and Misprediction, and then, the candidate fault is determined to coincide with the actual defect when there are

a lot of Vectorwise intersections. Then, the fault is diagnosed in the order of the Intersection, Nonprediction, and Misprediction.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a flowchart illustrating a process of diagnosing multiple stuck-at faults according to an embodiment of the present invention;

FIG. 2 is a diagram showing an example of a process of ranking candidate faults; and

FIG. 3 is a diagram showing an example of a process of determining a final set of candidate faults.

DETAILED DESCRIPTION OF THE INVENTION

TECHNICAL PROBLEM

The present invention has been developed to solve problems of the conventional art and to lessen the problem in that the time to perform a fault simulation using a multiple stuck-at fault simulator is long. The present invention can greatly reduce the simulating time by using a single stuck-at fault simulator. In addition, fault scores and a vectorwise intersection table are generated by outputting the simulation result, and positions of the faults are determined based on the fault scores and the vectorwise intersection table. Therefore, the time for storing and searching for the simulation result is not required, and hardware for storing the simulation results is also not required.

Therefore, the present invention provides a matching algorithm for diagnosing multiple stuck-at faults using a single stuck-at fault simulator, and can diagnose the multiple stuck-at faults using a small number of candidate faults through a ranking method for improving identification between the multiple stuck-at faults.

TECHNICAL SOLUTION

According to an aspect of the present invention, there is provided a matching method of diagnosing multiple stuck-at faults, the method including: performing a single stuck-at fault simulation using a circuit design file, test patterns, and tester response results of a faulty chip; calculating scores of candidate faults during the performing of the single stuck-at fault simulation; generating a vectorwise intersection table during the

performing of the single stuck-at fault simulation; and determining a final set of candidate faults using the scores of the candidate faults and the vectorwise intersection table after completing the single stuck-at fault simulation,

In the calculating of the candidate faults scores, the faults may be classified as a vectorwise intersection, an intersection, a misprediction, a nonprediction, and a no error, and the calculation of the scores may be performed for each of the classifications. In the generating of the vectorwise intersection table, the patterns showing the vectorwise intersections may be stored by the fault unit to generate the vectorwise intersection table.

The vectorwise intersection in the calculation of the candidate fault scores may be a case where errors are generated in both the tester response and the simulation response, and the score may be increased by the number of all primary outputs.

The intersection in the calculation of the candidate fault scores may be a case where errors are generated in both the tester response and the simulation response and the errors do not coincide with each other, and the score may be increased by the number of primary outputs showing the errors in both the tester response and the simulation response and the score is reduced by the number of primary outputs showing the errors in one of the tester response and the simulation response.

The misprediction in the calculation of the candidate fault scores may be a case where an error is not shown in the tester response and an error is shown in the simulation response, and the score may be reduced by the number of primary outputs showing the errors in the simulation response.

The nonprediction in the calculation of the candidate fault scores may be a case where an error is not shown in the simulation response and an error is shown in the tester response, and the score may be reduced by the number of primary outputs showing the errors in the tester response.

The no error in the calculation of the candidate fault scores may be a case where no error is shown in both the tester response and the simulation response, and the score may not be changed.

The determination of the final candidate faults may include: (a) arranging the candidate faults in an order of scores; (b) selecting the candidate fault mostly showing the vectorwise intersection portion among the candidate faults having the highest score so as to be included in a final set of the candidate faults; (c) when the test result shows

an error and there is no candidate fault having the vectorwise intersection portion with respect to the fail pattern in the final set of the candidate faults, the candidate fault having the vectorwise intersection portion to the pattern and having the highest score in the final set of the candidate faults is included; (d) repeating operation (c) until the faults having the vectorwise intersection portions with respect to all of the tester response showing the errors are included in the final set of the candidate faults.

ADVANTAGEOUS EFFECTS

According to the present invention, a single stuck-at fault simulator is used, and the simulating time can be reduced. In addition, since the simulation result is not stored, hardware for storing the simulation result is not required, and thus, the time for storing and searching for the simulation result is not required. Even if the plurality of multiple stuck-at faults exists, the multiple stuck-at faults can be exactly diagnosed from a few sets of candidate faults using an effective fault diagnosing algorithm.

BEST MODE

Hereinafter, embodiments of a matching method of diagnosing multiple stuck-at faults according to the present invention will be described with reference to accompanying drawings.

FIG. 1 illustrates a flowchart of the matching method according to an embodiment of the present invention. For performing a fault diagnosis, a design file of a circuit, a test pattern, and a test response result of a chip in which an error occurs are input (operation 100). A single stuck-at fault simulation is performed when the above elements are input (110), and ranks of each candidate fault is calculated during the single stuck-at fault simulation (111) so as to generate a vectorwise intersection table (112). After completing the single stuck-at fault simulation, a final set of candidate faults is determined based on the ranks of the candidate faults and the vectorwise intersection table (120), and then, a final fault diagnosis result is output (130).

Hereinafter, technical elements in each of the above operations will be described in more detail as follows.

(1) calculating ranks of the candidate faults (111)

The process of calculating the ranks of the candidate faults (111) is performed

during the single stuck-at fault simulation process (110) that is performed in a double-loop form, that is, simulating all of the patterns with respect to a selected fault in a fault list. The simulation for a pattern is performed, the score is calculated using the matching algorithm, and the scores of all the patterns are summed to determine the score of the selected fault.

According to the matching method of the current embodiment, the faults are classified as the following five kinds, and the calculation method is determined.

(a) vectorwise intersection : Errors occur both in the response of the tester and in the response of the simulation, and coincide with each other. In this case, the score is increased by the number of primary outputs.

(b) intersection : Errors occur in both the response of the tester and the response of the simulation, however, do not completely coincide with each other. The score is increased by the number of primary outputs, in which the errors occur in both the tester and the simulation, and the score is reduced by the number of the primary outputs, in which the error occurs only in one of the tester and the simulation.

(c) misprediction : The error does not occur in the response of the tester, however, the error occurs in the response of the simulation. In this case, the score is reduced by the number of primary outputs, in which the error occurs in the response of the simulation.

(d) nonprediction : The error does not occur in the response of the simulation, however, occurs in the response of the tester. The score is reduced by the number of the primary outputs, in which the error occurs in the response of the tester.

(e) no error : The errors do not occur both in the response of the tester and the response of the simulation. The score does not change.

In a case of the vectorwise intersection, weighed values are applied as the number of primary outputs, and thus, a size of the circuit can be dealt with flexibly. In addition, even when the responses of the tester and the simulation coincide with each other, the vectorwise intersection and the no error area are distinguished according to the existence of the fault. Therefore, a problem in that the fault that less propagates has a higher score and a higher rank, in the no error area can be prevented.

The process of calculating the score will be described in detail with reference to FIG. 2. The values shown in FIG. 2 are signature values, in which '0' represents that

there is no error and '1' represents that there is an error. With respect to a test pattern 1, the signature values of the tester response and the candidate fault No. 1 are both 00110, which represents errors, and the same type values are shown with respect to all primary outputs, and thus, the candidate fault No. 1 is calculated as the vectorwise intersection. In addition, since this system of the current embodiment includes five main primary outputs, the candidate fault No. 1 increases a score of 5. With respect to the test pattern No. 1, a candidate fault No. 2 is calculated as the nonprediction since there is an error in the tester response and there is no error in the simulation response of the candidate fault. In this case, since the tester response shows the error twice, a score of 2 is reduced. Then, with respect to the test pattern No. 1, a candidate fault No. 3 is calculated as the intersection since the errors are shown in both the tester response and the simulation response of the candidate fault, however, the errors do not coincide with each other.

Here, since the error is shown at the same output end once, a score of 1 is increased, and then, since the error is shown in one of the tester response and the simulation response twice, a score of 2 is reduced, and thus, a score of 1 is finally reduced. When the sum of the scores with respect to all of the test patterns is calculated as described above, the candidate fault No. 1 has a score of 5, the candidate fault No. 2 has a score of - 6, and the candidate fault No. 3 has a score of - 4. Therefore, the candidate fault No. 1 can be determined to be similar to the actual defect since the candidate fault 1 has the highest score.

(2) vectorwise intersection table (112)

During the single stuck-at fault simulation process (110), if the vectorwise intersection is shown, the test patterns showing the vectorwise intersections are stored by the fault unit to generate a vectorwise intersection table that is used when the final candidate fault is determined with the scores.

(3) determination of the final set of candidate faults (120)

After the single stuck-at fault simulation process (110) is completed, the scores representing the similarity between the tester responses and each of the candidate faults and the vectorwise intersection table aid to determine the final set of candidate fault. The final set of the candidate fault is determined based on the above two

standards.

The final set of the candidate faults is determined through following processes.

1. The candidate faults are arranged in an order of the scores.

2. The candidate fault mostly showing the vectorwise intersections is selected among the candidate faults having the highest score, and then, the selected candidate fault is included in the final set of the candidate faults.

3. In a case where the candidate fault, showing the error in the test response and no vectorwise intersection with respect to that pattern, is not in the final set of the candidate faults, the candidate fault having the vectorwise intersection with respect to the pattern and having the highest score is included in the final set of the candidate faults.

4. The above process 3 is repeated until the candidate faults having vectorwise intersections with respect to the test responses showing the errors are included in the final set of the candidate faults. If there is no candidate fault having the vectorwise intersection with respect to the test response, this process is omitted

The above operations are described with reference to FIG. 3. In FIG. 3, the circuit has five candidate faults, and score of each of the candidate faults is determined through the process of calculating scores of the candidate faults (111) as described in the above paragraph (1). In FIG. 3, a sign of ▣ represents the vectorwise intersection. Hence, since the errors must be shown in both the tester response and the simulation response in the vectorwise intersection, the patterns stored in the vectorwise intersection must be the patterns showing the errors in the tester responses. When the faults are arranged in an order of the scores through a first process, the faults are arranged as shown in FIG. 3. In a second process, the fault mostly having the vectorwise intersection is selected among the faults having the highest score. In the example shown in FIG. 3, the candidate fault 1 has the highest score, and thus, the fault No. 1 is selected. However, if there are faults having the highest scores, the fault mostly having the vectorwise intersection is selected. In addition, if there are faults having the vectorwise intersection that is the same as each other, all of the candidate faults are included in the final set of the candidate faults. Then, in a third operation, the fault No. 4 showing the vectorwise intersection with respect to the pattern No. 3 is included in the final set of the candidate faults. The final set of the candidate faults that includes the fault No. 1 and the fault No. 4, and the diagnosis result is output.

Multiple stuck-at faults cannot be diagnosed by simply selecting the candidate faults having the highest score because even if one fault is diagnosed as the first rank, other faults may be located at lower ranks. In order to solve the above problem, even if the candidate fault is located at the low rank, it can be included in the final set of the candidate faults when the vectorwise intersection with respect to the pattern that is not described by the faults in the set of the candidate faults is there. Through the above processes, the final diagnosis result is output.

CLAIMS

1. A matching method of diagnosing multiple stuck-at faults, the method comprising:

performing a single stuck-at fault simulation using a circuit design file, test patterns, and tester response results of a faulty chip;

calculating scores of candidate faults during the performing of the single stuck-at fault simulation;

generating a vectorwise intersection table during the performing of the single stuck-at fault simulation; and

determining a final set of candidate faults using the scores of the candidate faults and the vectorwise intersection table after completing the single stuck-at fault simulation,

wherein in the calculating of the candidate faults scores, the faults are classified as a vectorwise intersection, an intersection, a misprediction, a nonprediction, and a no error, and the calculation of the scores is performed for each of the classifications,

in the generating of the vectorwise intersection table, the patterns showing the vectorwise intersections are stored by the fault unit to generate the vectorwise intersection table.

2. The matching method of claim 1, wherein the vectorwise intersection in the calculation of the candidate fault scores is a case where errors are generated in both the tester response and the simulation response, and the score is increased by the number of all primary outputs.

3. The matching method of claim 1, wherein the intersection in the calculation of the candidate fault scores is a case where errors are generated in both the tester response and the simulation response and the errors do not coincide with each other, and the score is increased by the number of primary outputs showing the errors in both the tester response and the simulation response and the score is reduced by the number of primary outputs showing the errors in one of the tester response and the simulation response.

4. The matching method of claim 1, wherein the misprediction in the calculation of the candidate fault scores is a case where an error is not shown in the tester response and an error is shown in the simulation response, and the score is reduced by the number of primary outputs showing the errors in the simulation response.

5. The matching method of claim 1, wherein the nonprediction in the calculation of the candidate fault scores is a case where an error is not shown in the simulation response and an error is shown in the tester response, and the score is reduced by the number of primary outputs showing the errors in the tester response.

6. The matching method of claim 1, wherein the no error in the calculation of the candidate fault scores is a case where no error is shown in both the tester response and the simulation response, and the score is not changed.

7. The matching method of claim 1, wherein the determination of the final candidate faults comprises:

(a) arranging the candidate faults in an order of scores;

(b) selecting the candidate fault mostly showing the vectorwise intersection portion among the candidate faults having highest score so as to be included in a final set of the candidate faults;

(c) when the test result shows an error and there is no candidate fault having the vectorwise intersection portion with respect to the pattern showing fail in the final set of the candidate faults, the candidate fault having the vectorwise intersection portion to the pattern and having the highest score in the final set of the candidate faults is included;

(d) repeating operation (c) until the faults having the vectorwise intersection portions with respect to all of the tester response showing the errors are included in the final set of the candidate faults.

FIG. 1

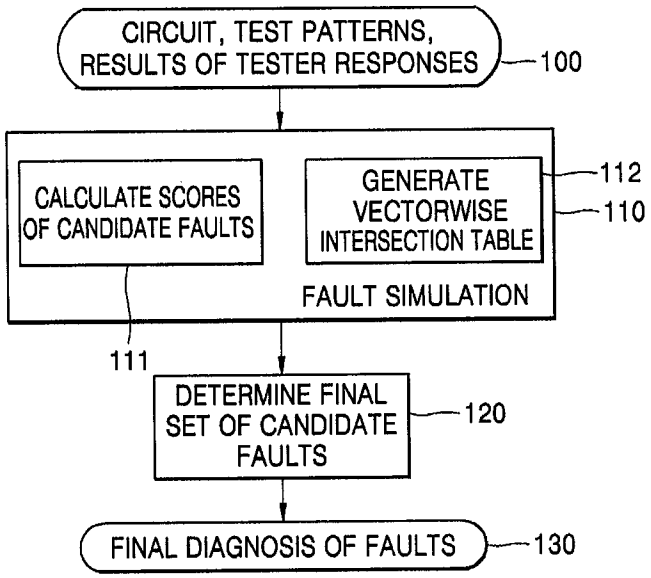


FIG. 2

	TESTER PATTERN No.1	TESTER PATTERN No.2	TESTER PATTERN No.3
TSETER RESPONSE	00110	00000	00110
CANDIDATE FAULT No.1	00110	00000	00010
CANDIDATE FAULT No.2	00000	11000	10011
CANDIDATE FAULT No.3	01100	00001	00000

FIG. 3

	SCORE	PATTERN No.1	PATTERN No.2	PATTERN No.3	PATTERN No.4
FAULT No.1	102	■	■		■
FAULT No.2	98	■	■		
FAULT No.3	87	■			
FAULT No.4	50			■	
FAULT No.5	23		■		

INTERNATIONAL SEARCH REPORT

International application No.
PCT/KR2007/003127

A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/66(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 8 H01L 21/66

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean Utility Models and applications for Utility Models since 1975

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKIPASS(KIPOinternal):"fault, simulation, diagnosing,circuit"

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 6,790,680 B1 (JASON A. GROVER et al.) 14 SEPTEMBER 2004 See ABSTRACT, FIG 6, COLUMN10 LINE 47~COLUMN12 LINE22	1-7
A	US 6,461,882 B2 (MASAHIRO ISHIDA, TAKAHIRO YAMAGUCHI) 8 OCTOBER 2002 See ABSTRACT, FIG22~27, COMUMN23 LINE65~COLUMN28 LINE41	1-7
A	US 5,539,652 A (MAURO V. TEGETHOFF) 23 JULY 1996 See ABSTRACT, FIG 4, COLUMN 15 LINE45~COLUMN 17 LINE 28	1-7

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/KR2007/003127

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