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(54) **CONTACT-FIRST FIELD-EFFECT TRANSISTORS**

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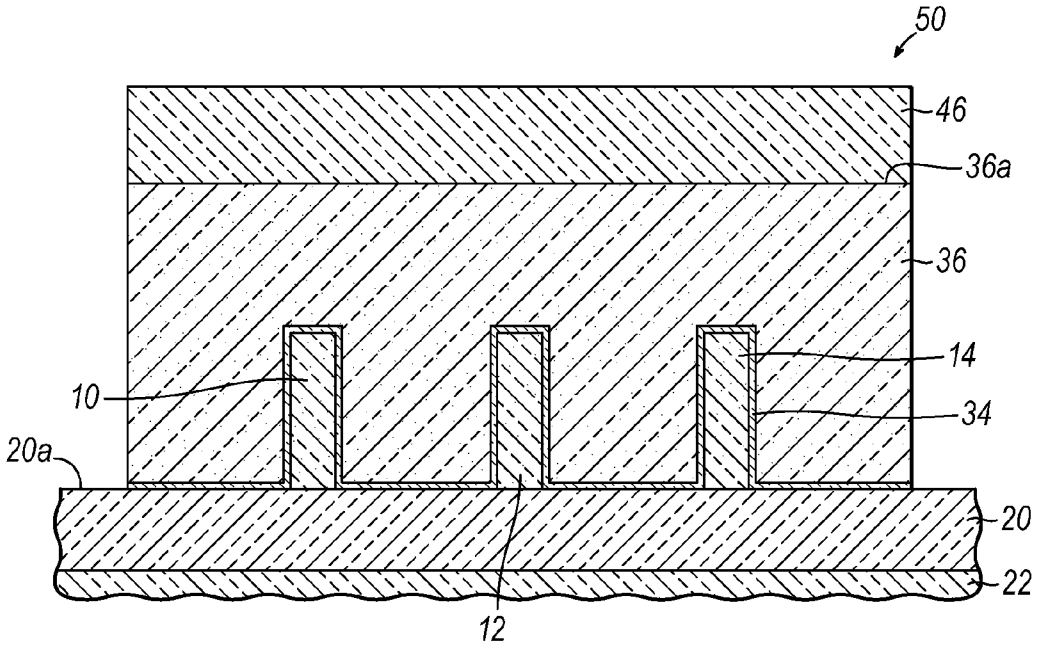
(57) **ABSTRACT**

Device structures and fabrication methods for a fin-type field-effect transistor. A first contact, a second contact, and a gate electrode are formed on a fin comprised of a semiconductor material. The second contact is spaced along a length of the fin from the first contact. The gate electrode is positioned along the length of the fin between the first contact and the second contact.



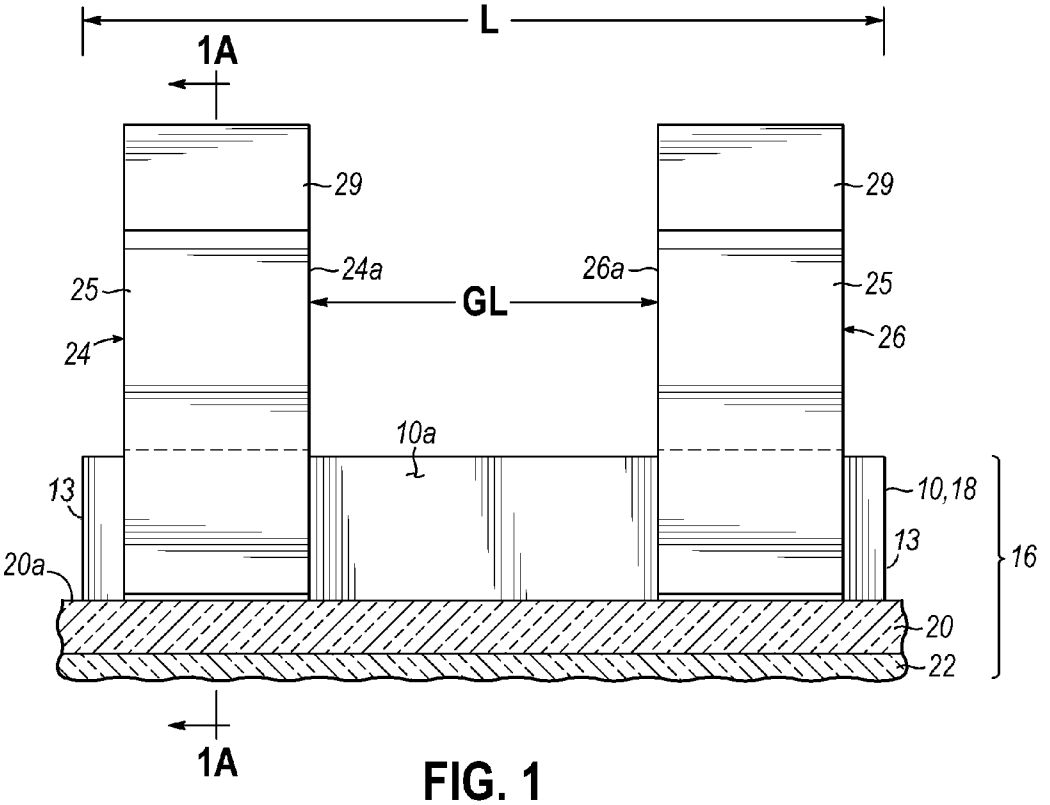

L
1A
29
29
24a
26a
25
GL
25
24
26
10a
13
10,18
13
16
20a
20
22
1A

FIG. 1

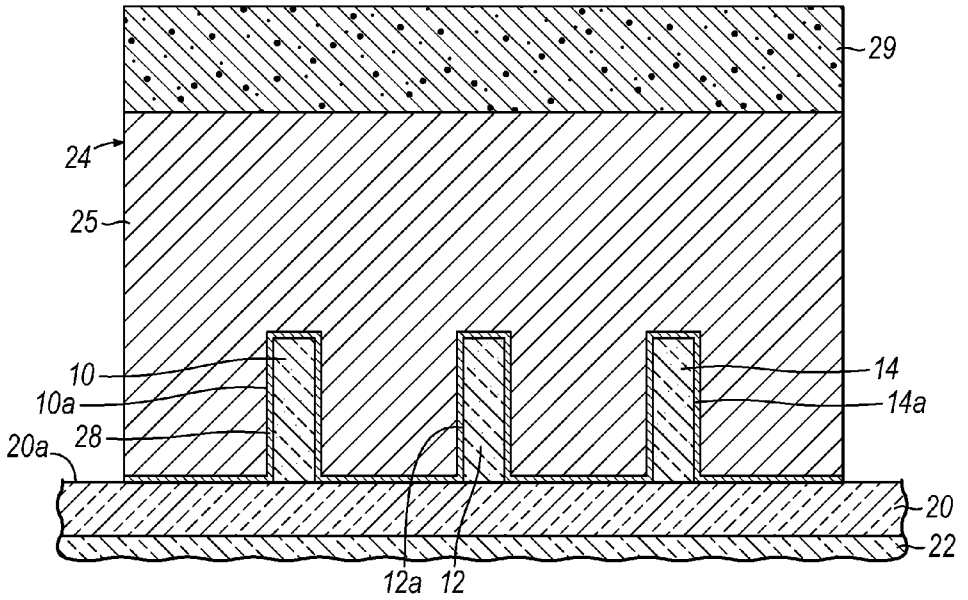

29
24
25
10
10a
20a
28
14
14a
20
22
12a
12

FIG. 1A

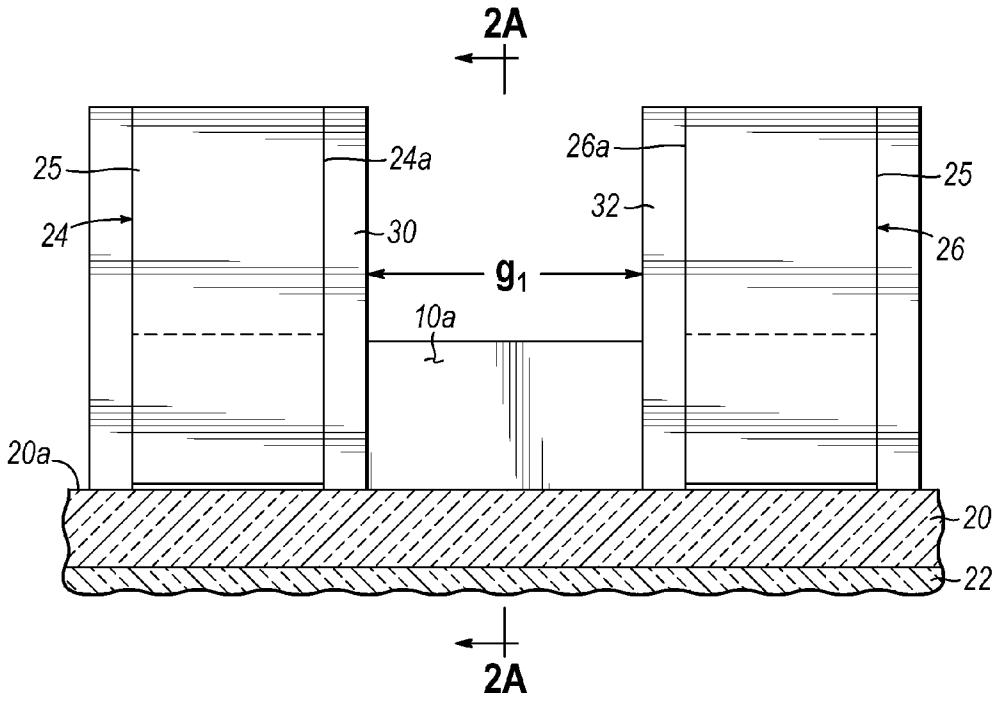


FIG. 2

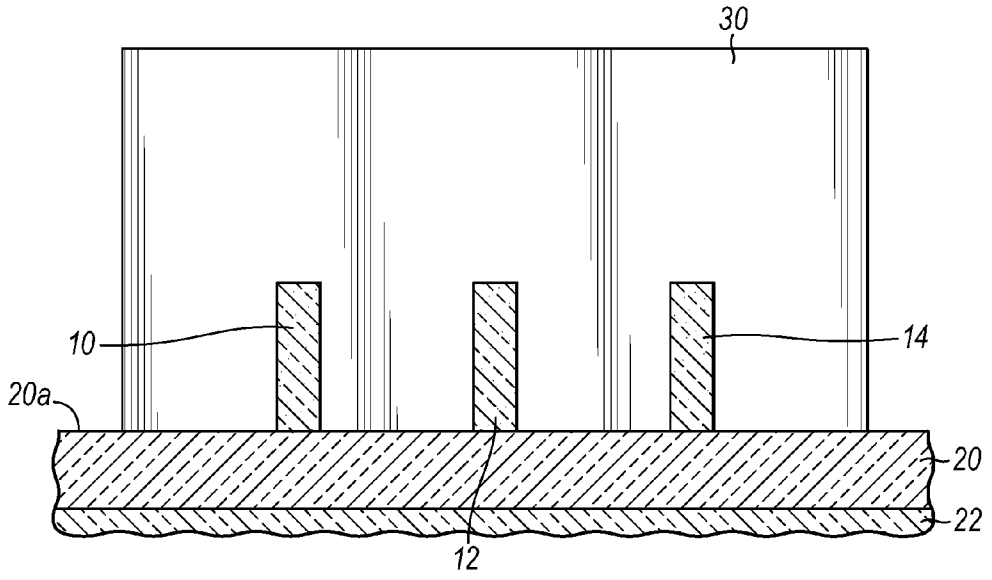


FIG. 2A

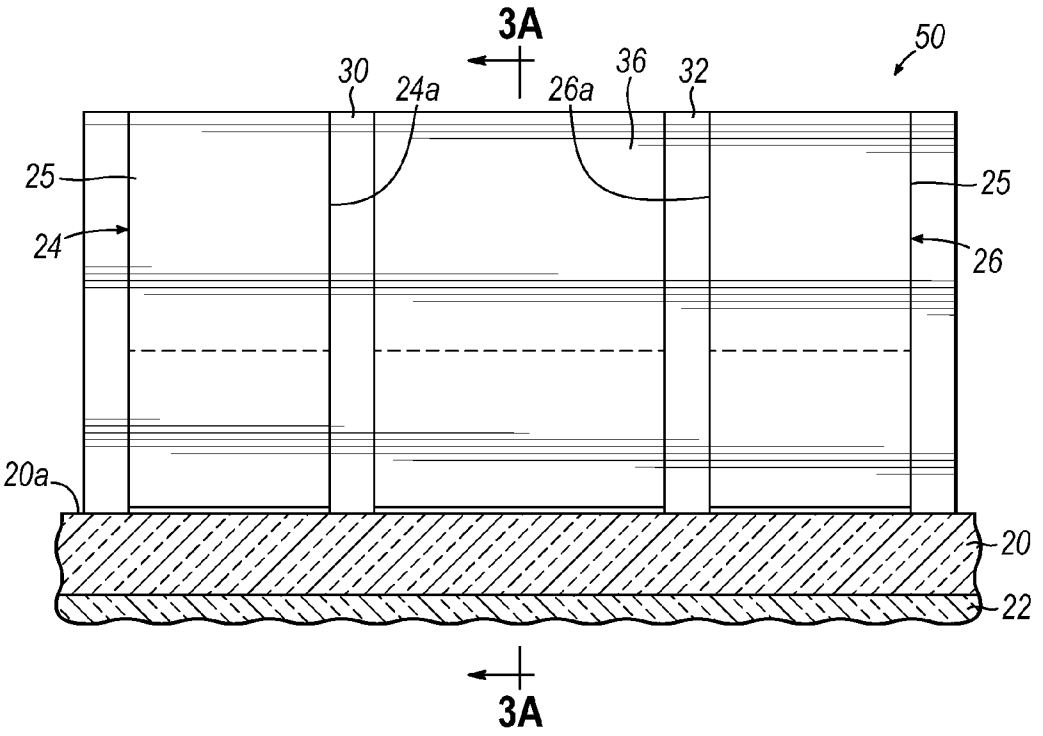

3A
50
30
24a
26a
36
32
25
25
24
26
20a
20
22
3A

FIG. 3

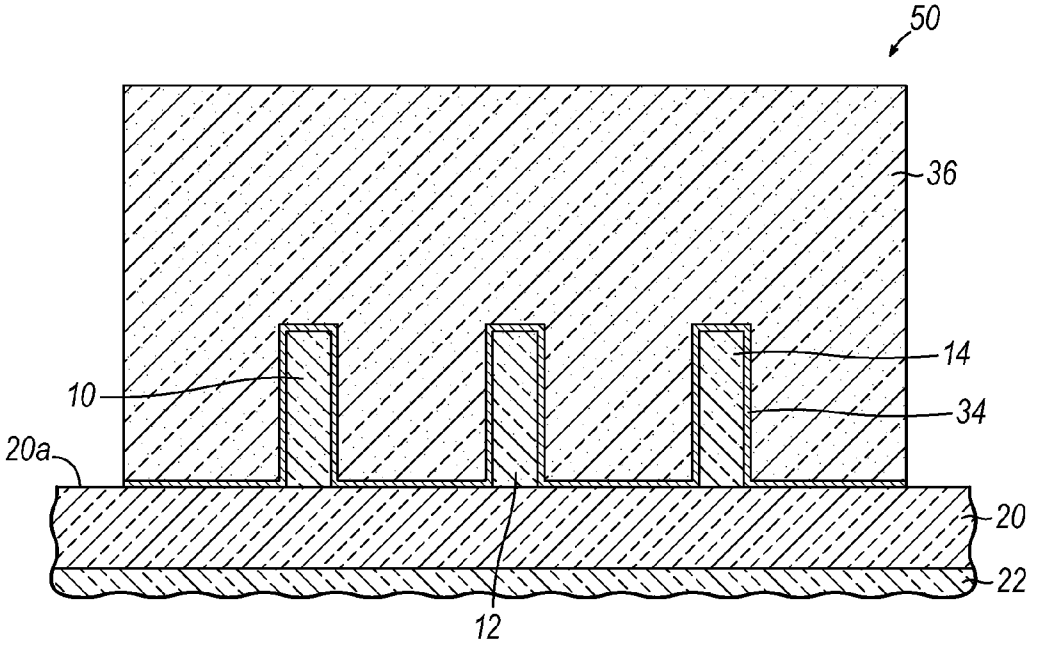

50
36
14
10
34
20a
20
22
12

FIG. 3A

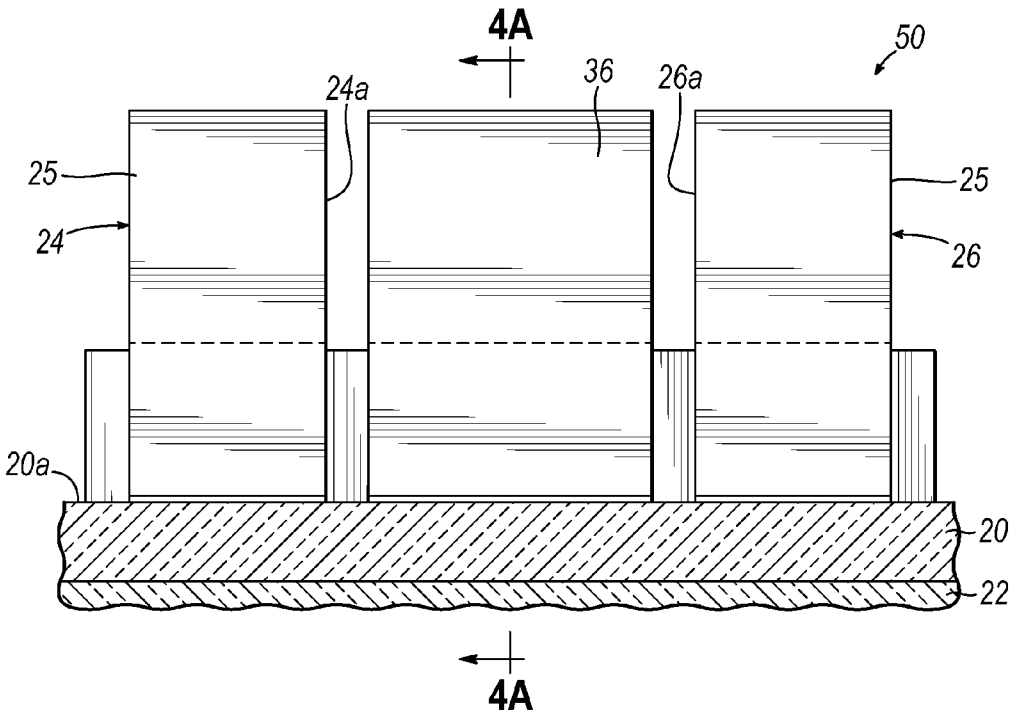


FIG. 4

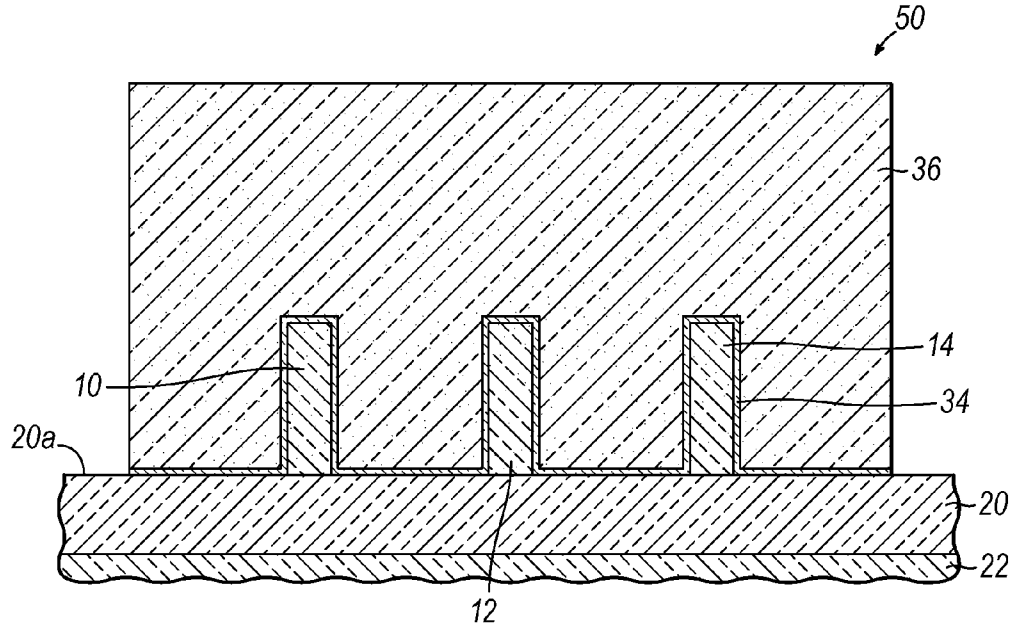


FIG. 4A

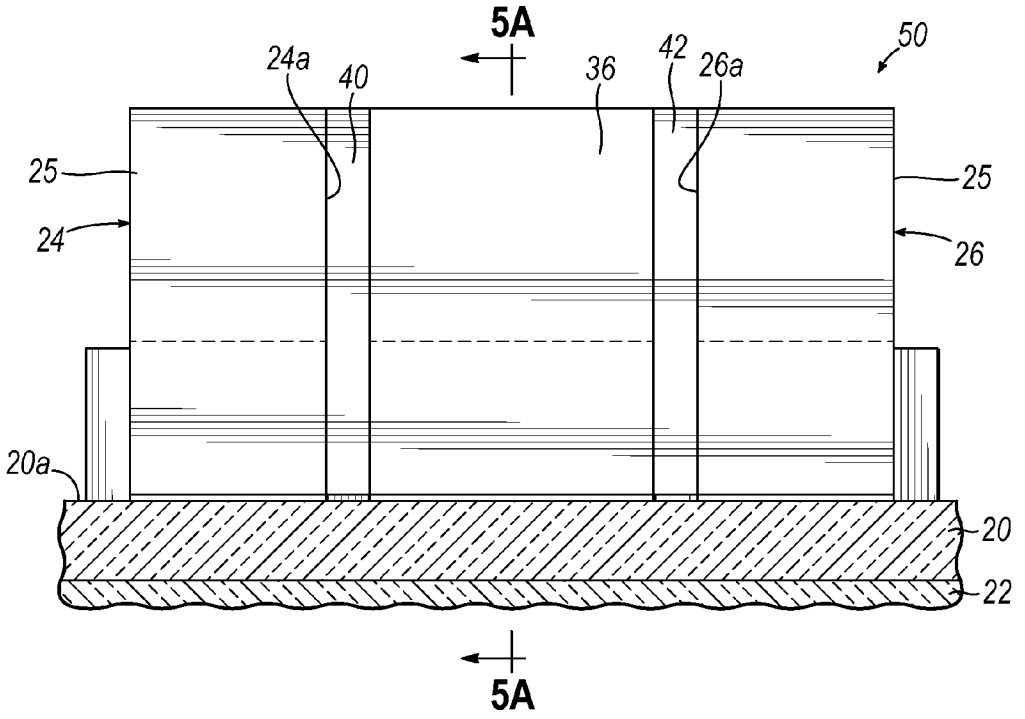

5A
24a
40
36
42
26a
50
25
25
24
26
20a
20
22
5A

FIG. 5

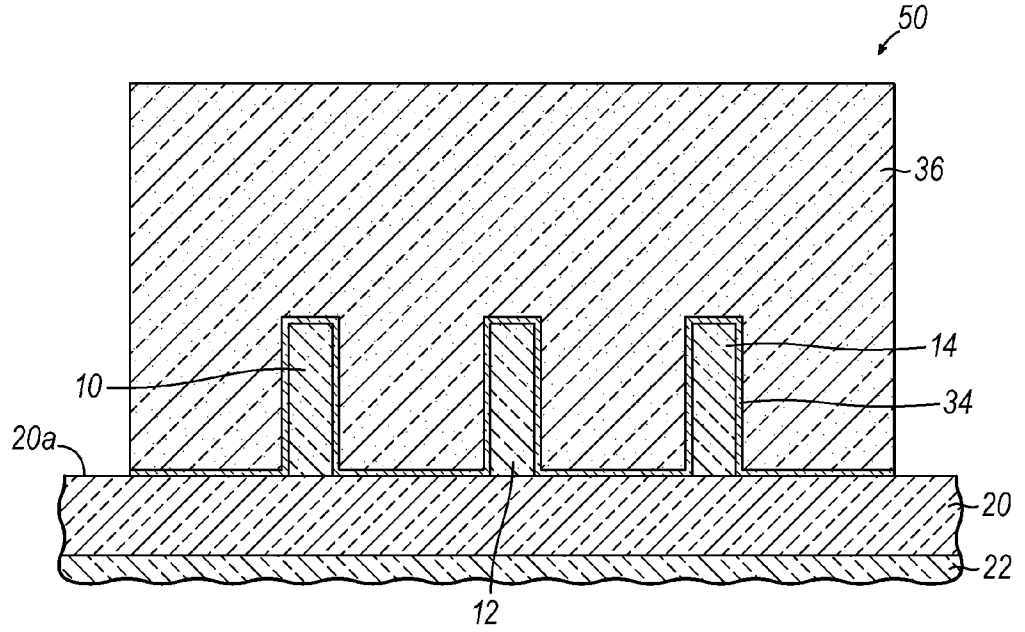

50
36
14
10
34
20a
20
22
12

FIG. 5A

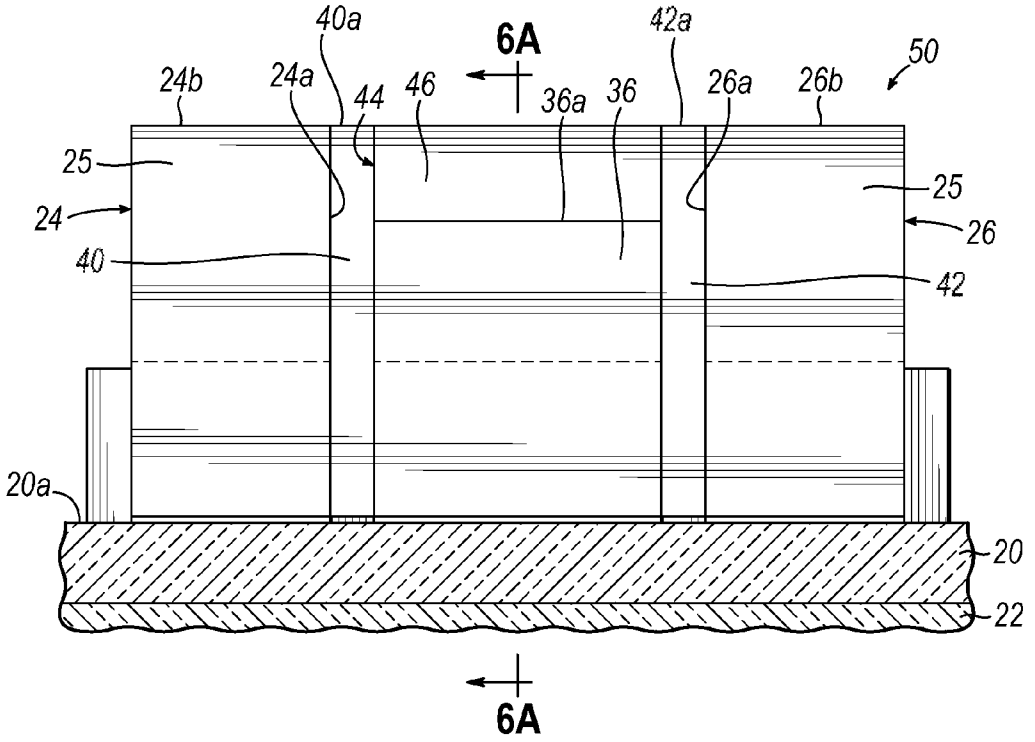

40a
6A
42a
50
24b
24a
44
46
36a
36
26a
26b
25
25
24
26
40
42
20a
20
22
6A

FIG. 6

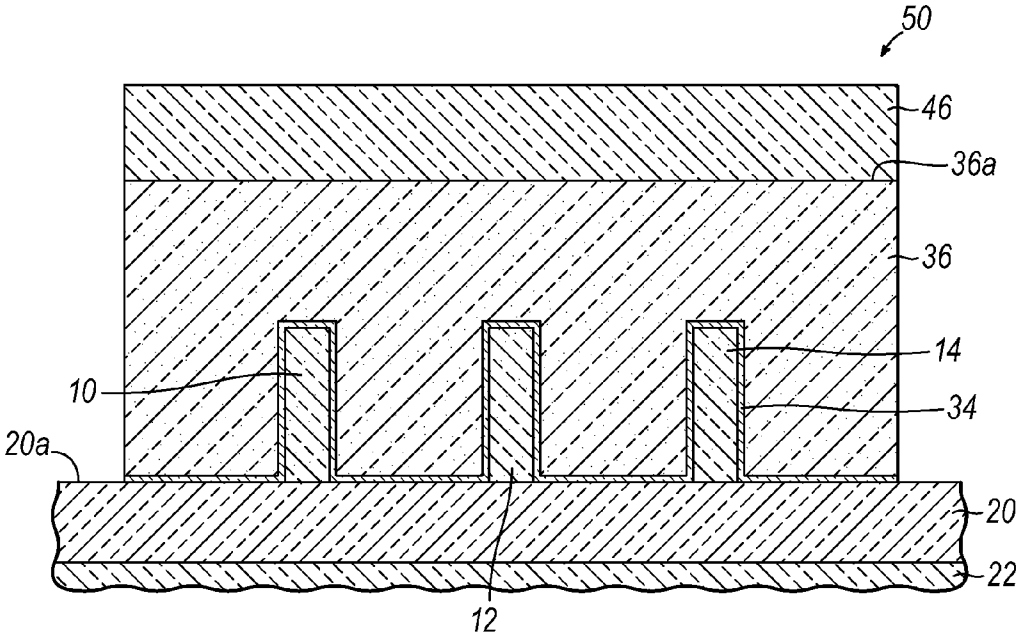

50
46
36a
36
14
10
34
20a
20
22
12

FIG. 6A

CONTACT-FIRST FIELD-EFFECT TRANSISTORS

BACKGROUND

[0001] The present invention relates to semiconductor device fabrication and, more specifically, to device structures for fin-type field-effect transistor (FinFET) integrated circuit technologies, as well as methods of fabricating device structures in FinFET integrated circuit technologies.

[0002] FinFETs are non-planar devices that are capable of being more densely packed in an integrated circuit than planar complementary metal-oxide-semiconductor (CMOS) transistors. In addition to the increase in packing density, FinFETs also offer superior short channel scalability, reduced threshold voltage swing, higher mobility, and the ability to operate at lower supply voltages than traditional planar CMOS transistors. Each FinFET features a narrow vertical fin of semiconductor material and a gate electrode that intersects a central channel of the fin. A thin gate dielectric layer separates the gate electrode from the fin. Heavily-doped source and drain regions are formed at opposite ends of the fin and the central channel is located between the source and drain regions.

[0003] Improved device structures and fabrication methods are needed for FinFET integrated circuit technologies.

SUMMARY

[0004] According to one embodiment of the present invention, a method is provided for forming a device structure. A first contact, a second contact, and a gate electrode are formed on a fin comprised of a semiconductor material. The second contact is spaced along a length of the fin from the first contact. The gate electrode is positioned along the length of the fin between the first contact and the second contact.

[0005] According to another embodiment of the present invention, a device structure includes a first contact on the fin, a second contact on the fin, and a gate electrode on a fin comprised of a semiconductor material. The second contact is spaced along a length of the fin from the first contact. The gate electrode is positioned along the length of the fin between the first contact and the second contact.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] The accompanying drawings, which are incorporated in and constitute a part of this specification, illustrate various embodiments of the invention and, together with a general description of the invention given above and the detailed description of the embodiments given below, serve to explain the embodiments of the invention.

[0007] FIGS. **1-6** are side views of a portion of a substrate at successive fabrication stages of a processing method for forming a device structure from fins in accordance with an embodiment of the invention.

[0008] FIG. **1**A is a cross-sectional view taken generally along line **1**A-**1**A in FIG. **1**.

[0009] FIG. **2**A is a cross-sectional view taken generally along line **2**A-**2**A in FIG. **2**.

[0010] FIG. **3**A is a cross-sectional view taken generally along line **3**A-**3**A in FIG. **3**.

[0011] FIG. **4**A is a cross-sectional view taken generally along line **4**A-**4**A in FIG. **4**.

[0012] FIG. **5**A is a cross-sectional view taken generally along line **5**A-**5**A in FIG. **5**.

[0013] FIG. **6**A is a cross-sectional view taken generally along line **6**A-**6**A in FIG. **6**.

DETAILED DESCRIPTION

[0014] With reference to FIGS. **1**, **1**A and in accordance with an embodiment of the invention, a plurality of fins **10**, **12**, **14** are formed from the device layer **18** of a semiconductor-on-insulator (SOI) substrate **16**. The SOI substrate **16** further includes a buried insulator layer **20** comprised of an electrical insulator and a handle wafer **22**. The device layer **18** is separated from the handle wafer **22** by the intervening buried insulator layer **20** and is in direct contact along a planar interface with a top surface **20***a* of the buried insulator layer **20**. The buried insulator layer **20** electrically isolates the handle wafer **22** from the device layer **18**, which is considerably thinner than the handle wafer **22**. The device layer **18** and the handle wafer **22** may be comprised of a semiconductor material, such as single crystal silicon, and the semiconductor material of the device layer **18** may be device quality. The buried insulator layer **20** may be a buried oxide layer comprised of silicon dioxide (SiO_2).

[0015] Each of fins **10**, **12**, **14** is defined by a three-dimensional body of semiconductor material originating from the device layer **18**. The fins **10**, **12**, **14** are positioned on the top surface **20***a* adjacent to each other, are laterally spaced apart across the top surface **20***a*, and may be aligned parallel with each other with a length L. Each of the fins **10**, **12**, **14** may have a bottom surface that is in direct contact with the top surface **20***a* of the buried insulator layer **20** along the interface between the device layer **18** and the buried insulator layer **20**.

[0016] The fins **10**, **12**, **14** may be formed by photolithography and subtractive etching processes. To that end, the fins **10**, **12**, **14** may be formed, for example, using a sidewall image transfer (SIT) process that promotes dense packing. To that end, a cap layer and a sacrificial layer comprised of, for example, polysilicon may be serially deposited on the top surface of the device layer **18** and the sacrificial layer patterned to define mandrels in the region of the device layer **18** used to form the fins **10**, **12**, **14**. Spacers are then formed on the sidewalls of the mandrels. The mandrels are arranged such that the spacers are formed at the intended locations for the fins **10**, **12**, **14**. The mandrels are then selectively removed relative to the spacers using an etching process, such as RIE. The cap layer and the device layer **18** are patterned with an etching process, such as RIE, using one or more etching chemistries while each spacer operates as an individual etch mask for one of the fins **10**, **12**, **14**. The etching process may stop on a top surface **20***a* of the buried insulator layer **20**. The spacers and cap layer may be removed subsequent to the etching process so that the sidewalls of the fins **10**, **12**, **14** are exposed.

[0017] In an alternative embodiment, the fins **10**, **12**, **14** may be formed from a bulk substrate (i.e., a non-SOI substrate) in a bulk process flow. The subsequent fabrication stages for fins **10**, **12**, **14** formed using the device layer **18** of the SOI substrate **16** apply equally to the bulk substrate in this alternative embodiment.

[0018] Following the formation of the fins **10**, **12**, **14**, contacts **24**, **26** may be formed that partially wrap around the opposite ends of the fins **10**, **12**, **14** and that cover respective portions of their exterior surfaces **10***a*, **12***a*, **14***a*. The con-

tacts **24**, **26** are also in direct contact with the top surface **20***a* of the buried insulator layer **20**. The contacts **24**, **26** are electrically and physically coupled with the fins **10**, **12**, **14**. The gap between the confronting sidewalls or side surfaces **24***a*, **26***a* of the contacts **24**, **26** defines a space in which the gate electrode of the device structure is subsequently formed and defines the physical gate length GL of the device structure. The portions of the fins **10**, **12**, **14** that are contacted by the contacts **24**, **26** comprise source/drain regions **13** of the device structure **50**.

[0019] The contacts **24**, **26** may be comprised of a conductor layer **25** and a liner layer **28**. The liner layer **28** is positioned between the conductor layer **25** and the respective exterior surfaces **10***a*, **12***a*, **14***a* of the fins **10**, **12**, **14**. The conductor layer **25** may be comprised of a metal, such as tungsten (W), that is deposited by, for example, physical vapor deposition (PVD). The liner layer **28** may be comprised of a metal, such as titanium (Ti) or tantalum (Ta), that is deposited by, for example, chemical vapor deposition (CVD).

[0020] The conductor layer **25** and liner layer **28** are subsequently patterned to form contacts **24**, **26**. To that end, a mask layer **29** may be applied on a top surface of the metal layers and patterned with photolithography. The mask layer **29** may comprise a light-sensitive material, such as a photoresist, that is applied by a spin coating process, pre-baked, exposed to light projected through a photomask, baked after exposure, and developed with a chemical developer to define an etch mask. Sections of the mask layer **29** cover the metal layer at the intended locations of the contacts **24**, **26**.

[0021] An etching process is then used, with the mask layer **29** present, to pattern the conductor layer **25** and liner layer **28**. The conductor layer **25** and liner layer **28** may be patterned at a gate pitch when forming the contacts **24**, **26**. The etching process may be selected to remove the material of the conductor layer **25** and liner layer **28** selective to the semiconductor material of the fins **10**, **12**, **14**. As used herein, the term "selective" in reference to a material removal process (e.g., etching) denotes that, with an appropriate etchant choice, the material removal rate for the targeted material is greater than the removal rate for at least another material exposed to the material removal process. The etching process may be conducted in a single etching step or multiple steps, and may rely on one or more etch chemistries.

[0022] The mask layer **29** may be removed following the conclusion of the etching process. If comprised of a photoresist, the mask layer **29** may be removed by ashing or solvent stripping, followed by a cleaning process.

[0023] In an alternative embodiment, the metal forming the contacts **24**, **26** may be doped during deposition in order to provide a solid-state diffusion source for doping the fins **10**, **12**, **14** and/or to improve the contact resistance. The liner layer **28** may function as part of the contacts **24**, **26** to reduce the contact resistance with the fins **10**, **12**, **14**. In an alternative embodiment, the liner layer **28** may be omitted from the construction of the device structure.

[0024] With reference to FIGS. **2**, **2**A in which like reference numerals refer to like features in FIGS. **1**, **1**A and at a subsequent fabrication stage, spacers **30**, **32** are formed on the side surfaces **24***a*, **26***a* of the contacts **24**, **26**. The spacers **30**, **32** may be formed by depositing a conformal layer comprised of an electrical insulator and shaping the conformal layer with an anisotropic etching process, such as a RIE process, that preferentially removes the conformal layer from horizontal surfaces. At the conclusion of the anisotropic etching process, the spacers **30**, **32** constitute residual shapes of electrical insulator residing on the vertical surfaces represented by the side surfaces **24***a*, **26***a*. The spacers **30**, **32** may be comprised of, for example, silicon nitride (Si_3N_4) or silicon dioxide deposited by chemical vapor deposition. The spacers **30**, **32** are separated by gap g_1, which is less than the physical gate length GL of the device structure between the contacts **24**, **26** by the spacer thickness.

[0025] In an alternative embodiment, the spacers **30**, **32** on the side surfaces **24***a*, **26***a* of the contacts **24**, **26** may be comprised of a material, such as a phosphorous-doped silicate glass (PSG), an arsenic-doped silicate glass (ASG), or a boron-doped silicate glass (BSG), that contains a dopant. Dopant originating from the solid-state dopant source represented by the spacers **30**, **32** can be caused to diffuse locally from the spacers **30**, **32** into the fins **10**, **12**, **14** by, for example, a thermal anneal process at a given temperature and over a given duration. These doped portions of the fins **10**, **12**, **14** may function to provide link-up extensions in the constituent semiconductor material between the source/drain regions **13** and channel of the device structure at locations beneath the spacers **30**, **32**.

[0026] With reference to FIGS. **3**, **3**A in which like reference numerals refer to like features in FIGS. **2**, **2**A and at a subsequent fabrication stage, a gate dielectric **34** and a gate electrode **36** are formed on the fins **10**, **12**, **14** over their respective exterior surfaces **10***a*, **12***a*, **14***a*. The gate dielectric **34** and gate electrode **36** are located in the gap g**1** between the spacers **30**, **32**, and cover that respective portion of the exterior surfaces **10***a*, **12***a*, **14***a*. The portion of the fins **10**, **12**, **14** covered by the gate electrode **36** may define a channel of the device structure.

[0027] The gate dielectric **34** may be comprised of an electrical insulator with a dielectric constant (e.g., a permittivity) characteristic of a dielectric material. For example, the gate dielectric **34** may be comprised of silicon dioxide, silicon oxynitride, a high-k dielectric material such as hafnium oxide, or layered combinations of these dielectric materials, deposited by v, atomic layer deposition (ALD), etc. The gate electrode **36** is comprised of a metal, a silicide, polycrystalline silicon (e.g., polysilicon), or a combination of these materials deposited by physical vapor deposition, chemical vapor deposition, etc.

[0028] The gate dielectric **34** and gate electrode **36** may be formed by patterning a deposited layer stack of their constituent materials using photolithography and etching processes. To provide the patterning, a mask layer may be applied on a top surface of the layer stack and patterned with photolithography. The mask layer may comprise a photosensitive material, such as a photoresist, that is applied by spin coating, pre-baked, exposed to light projected through a photomask, baked after exposure, and developed with a chemical developer. A section of the mask layer covers the layer stack at the intended location of the gate electrode **36** and functions as an etch mask. An etching process is used, with the mask layer present, to form the gate dielectric **34** and the gate electrode **36** from the layer stack. The etching process may be selected to remove the materials of the layer stack selective to the respective materials of the fins **10**, **12**, **14** and contacts **24**, **26**. The etching process may be conducted in a single etching step or multiple steps, and may rely on one or more etch chemistries. The mask layer may

be removed following the etching process. If comprised of a photoresist, the mask layer may be removed by ashing or solvent stripping, followed by a cleaning process.

[0029] A planarization process, such as chemical-mechanical polishing (CMP), is employed to planarize the top surfaces of the gate electrode **36** and the contacts **24**, **26**. The gate dielectric **34** is positioned between the gate electrode **36** and a channel in the fins **10**, **12**, **14**, which is itself located between the source/drain regions **13**. The spacers **30**, **32**, which flank the opposite sidewalls of the gate electrode **36**, are positioned between the contacts **24**, **26** and the gate electrode **36** as intervening structures. The gate electrode **36** is formed in a self-aligned manner with the channel as constrained by the presence of the contacts **24**, **26** that are formed before the gate electrode **36** is formed. The contacts **24**, **26** are not dummy structures comprised of a sacrificial material that is removed after the gate electrode **36** is formed and exist as elements in the final device structure **50**.

[0030] The complexity of the processing method producing the device structure **50** is reduced in comparison with the complexity of fabricating conventional device structures. The device structure **50** has the form of a fin-type field effect transistor in which the physical gate length of the device structure **50** is determined by the contact-to-contact spacing between contacts **24**, **26**. Gate lithography is eliminated because the gate electrode **36** is formed between the contacts **24**, **26** in a self-aligned manner. As a result, a positive lithographic step is not needed to establish the channel length of the device structure **50**, which eliminates limitations of on the minimum gate length that is achievable in conventional device structures.

[0031] In the process flow of fabrication stages, the contacts **24**, **26** are formed as metal pillars as an initial step and at earlier fabrication stage in the processing flow than in the fabrication of convention device structures. Another consequence of the process flow is that enabling technologies for low-temperature transistor formation, such as for three-dimensional monolithic integration (nanosecond laser anneal, etc.), may be utilized to form the field-effect transistor after the contacts **24**, **26** are formed.

[0032] The contacts **24**, **26** may provide improved contact metallurgy by eliminating protective liners (generally of lower conductivity) normally used to fill contact holes for prevent interaction of the metal deposition process. The elimination of the protective liners may be effective to reduce the contact resistance. In addition, the device structure **50** can be formed without a contact etch-stop layer on top of the gate electrode, and the contacts **24**, **26** do not have to be etched selectively to maintain self-alignment.

[0033] With reference to FIGS. **4**, **4**A in which like reference numerals refer to like features in FIGS. **3**, **3**A and in accordance with an alternative embodiment, the spacers **30**, **32** may be removed using an etching process that is selective to the materials of the contacts **24**, **26** and the gate electrode **36**. Once removed, the exterior surfaces **10***a*, **12***a*, **14***a* of the fins **10**, **12**, **14** between the side surfaces **24***a*, **26***a* of contacts **24**, **26** and confronting side surfaces of the gate electrode **36** are exposed. Sections of the fins **10**, **12**, **14** are accessible to be doped by, for example, plasma emersion or ion implantation to define link-up extensions. The semiconductor material of the fins **10**, **12**, **14** may be doped by introducing a p-type dopant species selected from Group III of the Periodic Table (e.g., boron) that is effective to impart p-type conductivity. Alternatively, the semiconductor material of the fins **10**, **12**, **14** may be doped by introducing an electrically-active dopant, such as an n-type dopant from Group V of the Periodic Table (e.g., phosphorus (P) or arsenic (As)) that is effective to impart n-type conductivity.

[0034] The spacers **30**, **32** may remain in the gaps between the contacts **24**, **26** and the gate electrode **36**. If not removed and replaced, then the spacers **30**, **32** will be present in the device structure **50** following its fabrication. In an embodiment, the spacers **30**, **32** may not be removed and replaced if dopant is outdiffused from the spacers **30**, **32**, as discussed herein above, to dope sections of the fins **10**, **12**, **14** and thereby provide the link-up extensions.

[0035] With reference to FIGS. **5**, **5**A in which like reference numerals refer to like features in FIGS. **4**, **4**A and at a subsequent fabrication stage, spacers **40**, **42** are formed inside the gaps between the contacts **24**, **26** and gate electrode **36**. The spacers **40**, **42** may be formed from the same dielectric material (e.g., silicon nitride or silicon dioxide) as originally used in spacers **30**, **32** or may be formed using a different dielectric material than original used in spacers **30**, **32**. In an embodiment, the spacers **40**, **42** may be formed from a dielectric material having a lower relative permittivity or dielectric constant than the spacers **30**, **32**. For example, the spacers **40**, **42** may be comprised of a low-k dielectric material characterized by a relative permittivity less than the relative permittivity for silicon dioxide of roughly 3.9. Candidate low-k dielectric materials for spacers **40**, **42** include, but are not limited to, porous and nonporous spun-on inorganic and organic low-k dielectrics (e.g., hydrogen-enriched silicon oxycarbide (SiCOH)). Spacers **40**, **42** may be deposited by any number of techniques including, but not limited to, sputtering, spin-on application, or chemical vapor deposition.

[0036] With reference to FIGS. **6**, **6**A in which like reference numerals refer to like features in FIGS. **5**, **5**A and in accordance with an alternative embodiment, the top surface **36***a* of the gate electrode **36** may be recessed below a plane containing the top surfaces **40***a*, **42***a* of the spacers **40**, **42** if the spacers **30**, **32** are removed and replaced and a plane containing the top surfaces **24***b*, **26***b* of the contacts **24**, **26** to define a cavity **44**. An etching process may be used that removes the material of the gate electrode **36** selective to the materials of the spacers **40**, **42** and contacts **24**, **26**. The etching process may be conducted in a single etching step or multiple steps, and may rely on one or more etch chemistries. If the spacers **30**, **32** are not removed and replaced by spacers **40**, **42**, the top surfaces of the spacers **30**, **32** may provide the reference plane for the recession of the gate electrode **36**.

[0037] The cavity **44** may be filled with a dielectric layer **46** comprised of a dielectric material differing in composition from the conductive material comprising the gate electrode **36**. In one embodiment, the cavity **44** may be filled during middle-of-line (MOL) processing. For example, during middle-of-line processing the cavity **44** may be filled during local interconnect formation with an electrical insulator, such as silicon dioxide (SiO_2), deposited by CVD and subsequently planarized using a chemical mechanical polishing process that eliminates topography. The replacement of a portion of the gate electrode **36** with dielectric material may be effective to reduce the capacitance of the device structure **50**.

[0038] The methods as described above are used in the fabrication of integrated circuit chips. The resulting inte-

grated circuit chips can be distributed by the fabricator in raw wafer form (that is, as a single wafer that has multiple unpackaged chips), as a bare die, or in a packaged form. In the latter case, the chip is mounted in a single chip package (such as a plastic carrier, with leads that are affixed to a motherboard or other higher level carrier) or in a multichip package (such as a ceramic carrier that has either or both surface interconnections or buried interconnections). In any case, the chip is then integrated with other chips, discrete circuit elements, and/or other signal processing devices as part of either (a) an intermediate product, such as a motherboard, or (b) an end product. The end product can be any product that includes integrated circuit chips, ranging from toys and other low-end applications to advanced computer products having a display, a keyboard or other input device, and a central processor.

[0039] References herein to terms such as "vertical", "horizontal", etc. are made by way of example, and not by way of limitation, to establish a frame of reference. The term "horizontal" as used herein is defined as a plane parallel to a conventional plane of a semiconductor substrate, regardless of its actual three-dimensional spatial orientation. The terms "vertical" and "normal" refers to a direction perpendicular to the horizontal, as just defined. The term "lateral" refers to a dimension within the horizontal plane.

[0040] A feature may be "connected" or "coupled" to or with another element may be directly connected or coupled to the other element or, instead, one or more intervening elements may be present. A feature may be "directly connected" or "directly coupled" to another element if intervening elements are absent. A feature may be "indirectly connected" or "indirectly coupled" to another element if at least one intervening element is present.

[0041] The descriptions of the various embodiments of the present invention have been presented for purposes of illustration, but are not intended to be exhaustive or limited to the embodiments disclosed. Many modifications and variations will be apparent to those of ordinary skill in the art without departing from the scope and spirit of the described embodiments. The terminology used herein was chosen to best explain the principles of the embodiments, the practical application or technical improvement over technologies found in the marketplace, or to enable others of ordinary skill in the art to understand the embodiments disclosed herein.

1: A method for forming a device structure, the method comprising:

forming a fin comprised of a semiconductor material;

forming a first contact on the fin;

forming a second contact on the fin and spaced along a length of the fin from the first contact; and

forming a gate electrode on the fin that is positioned along the length of the fin between the first contact and the second contact.

2: The method of claim **1** further comprising:

forming a first dielectric spacer between the first contact and the gate electrode.

3: The method of claim **2** further comprising:

forming a second dielectric spacer between the second contact and the gate electrode.

4: The method of claim **3** wherein the first dielectric spacer and the second dielectric spacer each include a dopant providing a solid-state diffusion source, and comprising:

doping a first portion of the fin with the dopant from the first dielectric spacer to define a first source/drain region; and

doping a second portion of the fin with the dopant from the second dielectric spacer to define a second source/drain region.

5: The method of claim further comprising:

removing the first dielectric spacer; and

forming a second dielectric spacer between the first contact and the gate electrode.

6: The method of claim **5** wherein the first dielectric spacer is comprised of a first dielectric material having a first relative permittivity, and the first dielectric spacer is comprised of a second dielectric material having a second relative permittivity less than the first relative permittivity.

7: The method of claim **1** wherein the first contact and the second contact each include a first layer comprised of a first material and a second layer comprised of a second material.

8: The method of claim **7** wherein the first material comprises a dopant providing a solid-state diffusion source, and comprising:

doping a first portion of the fin with the dopant from the first material of the first contact to define a first source/drain region; and

doping a second portion of the fin with the dopant from the first material of the second contact to define a second source/drain region.

9: The method of claim **1** wherein the first contact has a top surface, and the gate electrode has a top surface that is recessed below the top surface of the gate electrode to define a cavity between the first contact and the second contact.

10: The method of claim **9** further comprising:

forming a dielectric layer in the cavity between the first contact and the second contact.

11: A device structure comprising:

a fin comprised of a semiconductor material;

a first contact that partially wraps around a first end of the fin;

a second contact that partially wraps around a second end of the fin, the second contact spaced along a length of the fin from the first contact, and the first end of the fin is opposite to the second end of the fin; and

a gate electrode on the fin, the gate electrode formed self-aligned between the first contact and the second contact.

12: The device structure of claim **11** further comprising:

a first spacer between the first contact and the gate electrode, the first spacer comprised of a dielectric material.

13: The device structure of claim **12** further comprising:

a second spacer between the second contact and the gate electrode, the second spacer comprised of the dielectric material.

14: The device structure of claim **13** wherein the first spacer and the second spacer include a dopant providing a solid-state diffusion source for doping the fin.

15: The device structure of claim **12** wherein the dielectric material is a low-K dielectric material.

16: The device structure of claim **11** wherein the first contact and the second contact each include a first layer comprised of a first material and a second layer comprised of a second material, a channel length of the device structure is established without a positive lithographic process, and

the first contact and the second contact cover respective portions of an exterior portion of the fin.

17: The device structure of claim **16** wherein the first material of the first layer includes a dopant providing a solid-state diffusion source for doping the fin, and the first contact and the second contact are in direct contact with a top surface of a buried insulator layer of the device structure.

18: The device structure of claim **17** wherein the first layer is positioned between the second layer and the fin.

19: The device structure of claim **11** wherein the first contact has a top surface, and the gate electrode has a top surface that is recessed below the top surface of the gate electrode to define a cavity between the first contact and the second contact.

20: The device structure of claim **19** further comprising:

a dielectric layer in the cavity between the first contact and the second contact.

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