United States Patent

Hesselgren

[15] **3,656,114**

[45] **Apr. 11, 1972**

[54] ELECTRONIC LOCK ARRANGEMENT HAVING PARALLEL CODED INPUT

[72] Inventor: Tore Gottfrid Hesselgren, Borensvagen 1, Johanneshov, Sweden

[22] Filed: **May 1, 1969**

[21] Appl. No.: **820,921**

[30] **Foreign Application Priority Data**

May 7, 1968 Sweden 6113/68

[52] **U.S. Cl.** **340/164,** 340/167, 340/274

[51] **Int. Cl.** **H04g 3/02**

[58] **Field of Search** 340/164, 274, 167

[56] **References Cited**

UNITED STATES PATENTS

3,024,452	3/1962	Leonard	340/274
3,080,547	3/1963	Cooper	340/164
3,327,290	6/1967	Eglish	340/164 X
2,855,588	10/1958	Allen	340/164 UX
3,046,526	7/1962	Scantlin	340/164
3,100,389	8/1963	Noregaard	340/164 UX
3,175,191	3/1965	Cohn	340/164
3,380,024	4/1968	Watkinson	340/164

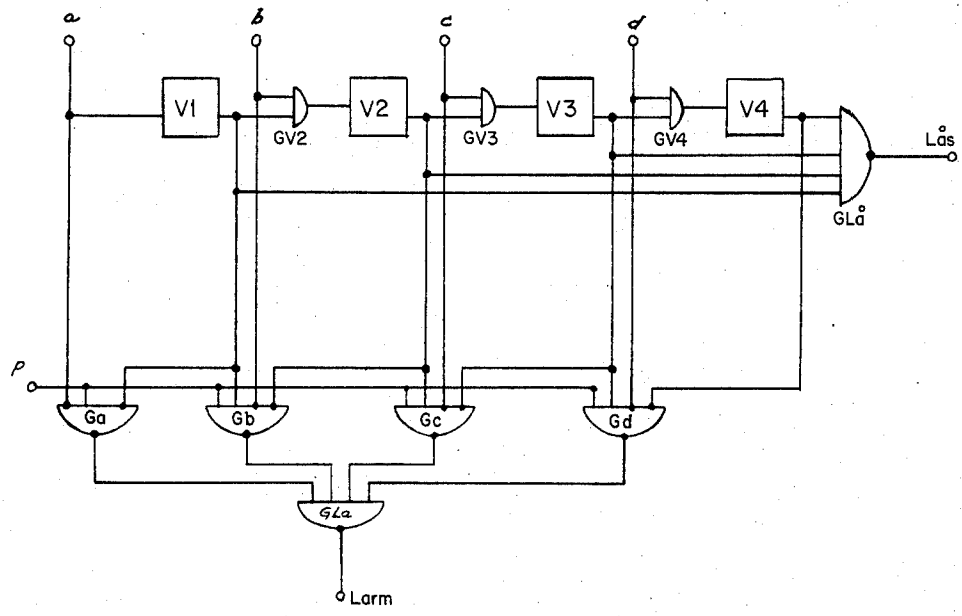
Primary Examiner—Harold I. Pitts

Attorney—Holman & Stern

[57] **ABSTRACT**

An electronic lock arrangement is disclosed, the arrangement comprising a plurality of consecutively disposed code step circuits. Each circuit, when actuated by an input code pulse train, generates a parallel output, which outputs define a lock release output signal when the input code pulse train is received in proper predetermined order.

3 Claims, 3 Drawing Figures



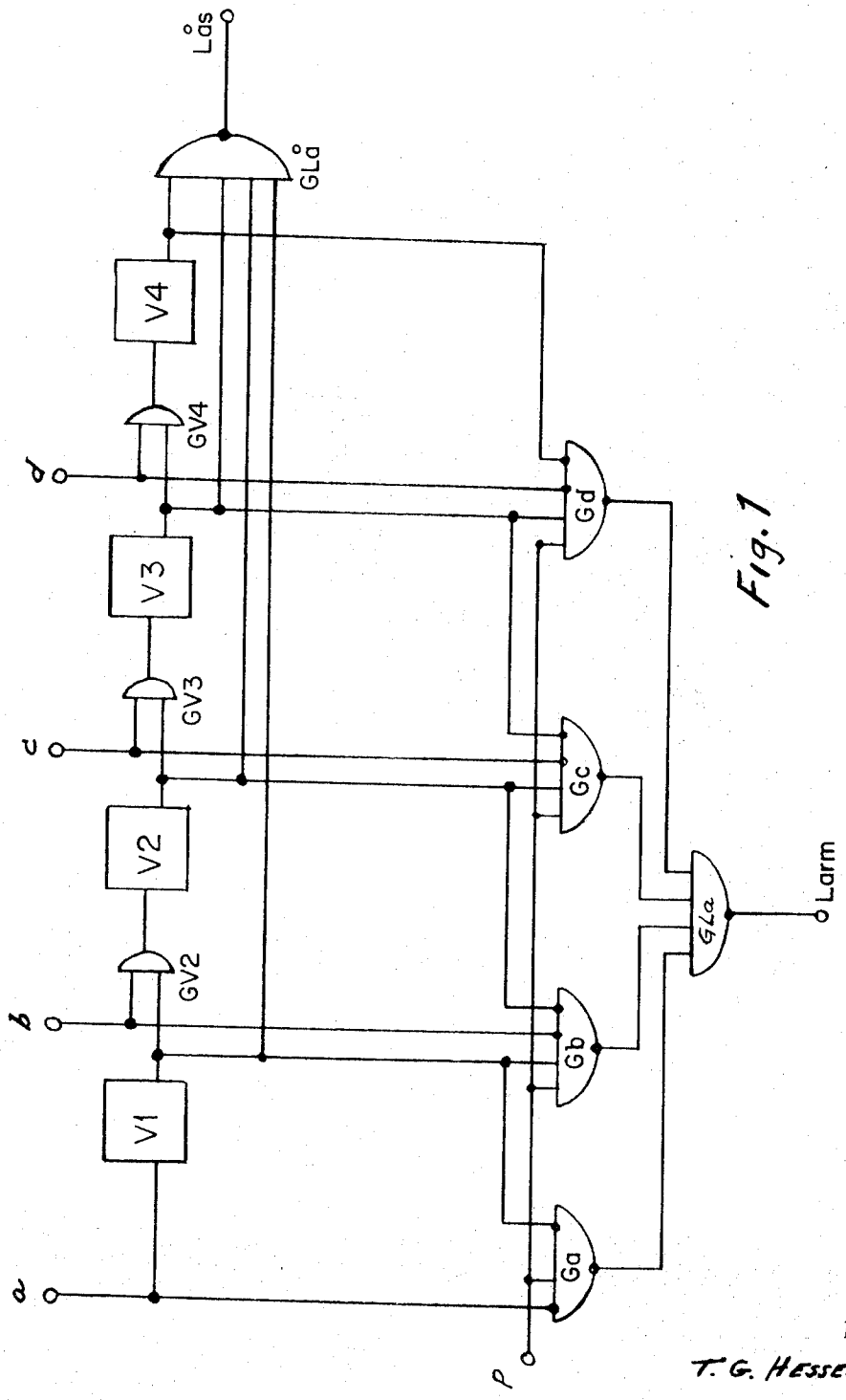


Fig. 1

INVENTOR
T. G. HESSELGREN

BY Holman, Glascock, Downing & Seebold
ATTORNEYS

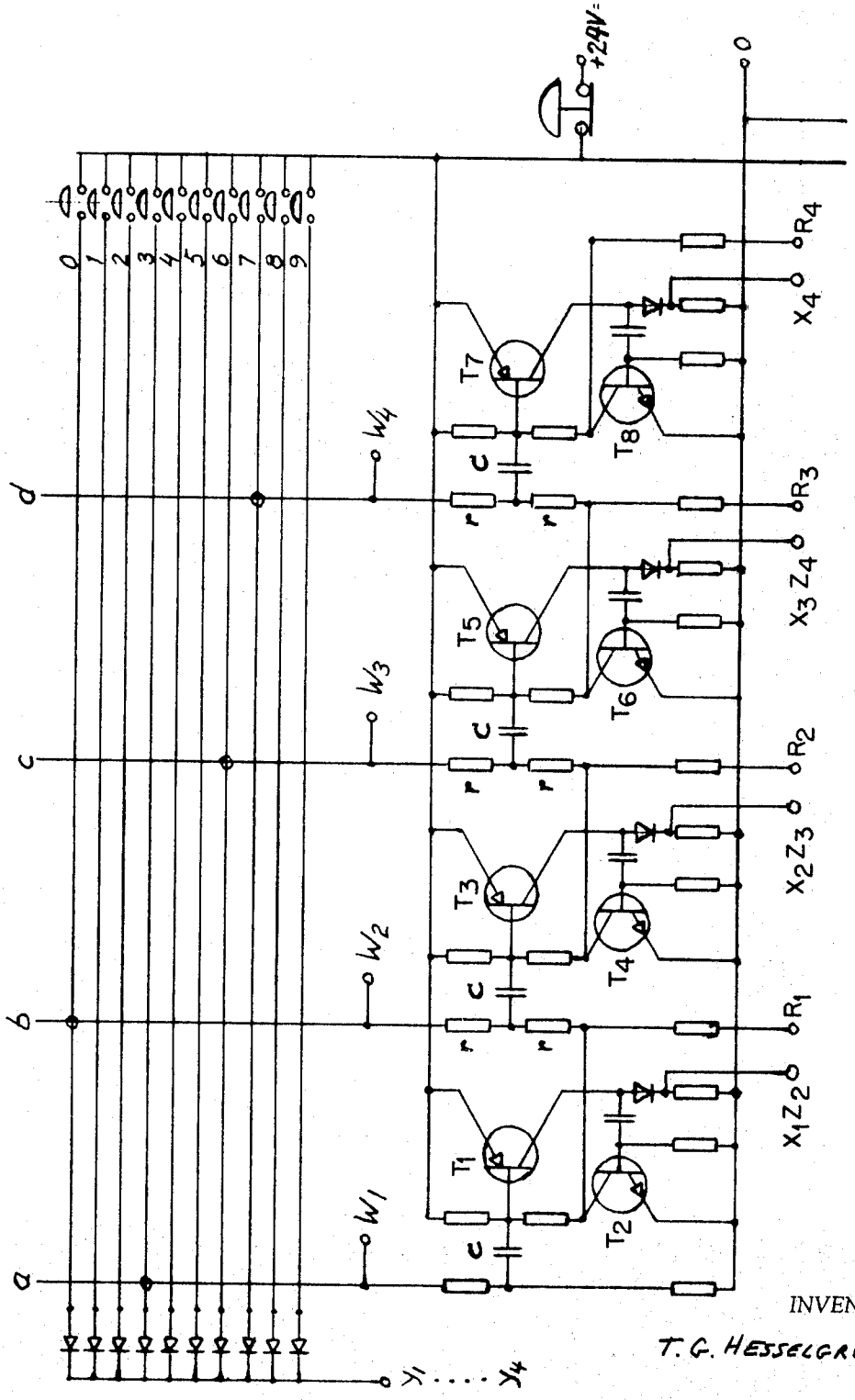


Fig. 2a

INVENTOR

T. G. HESSELGREN

BY Holman, Glascock, Downing & Seifred

ATTORNEYS

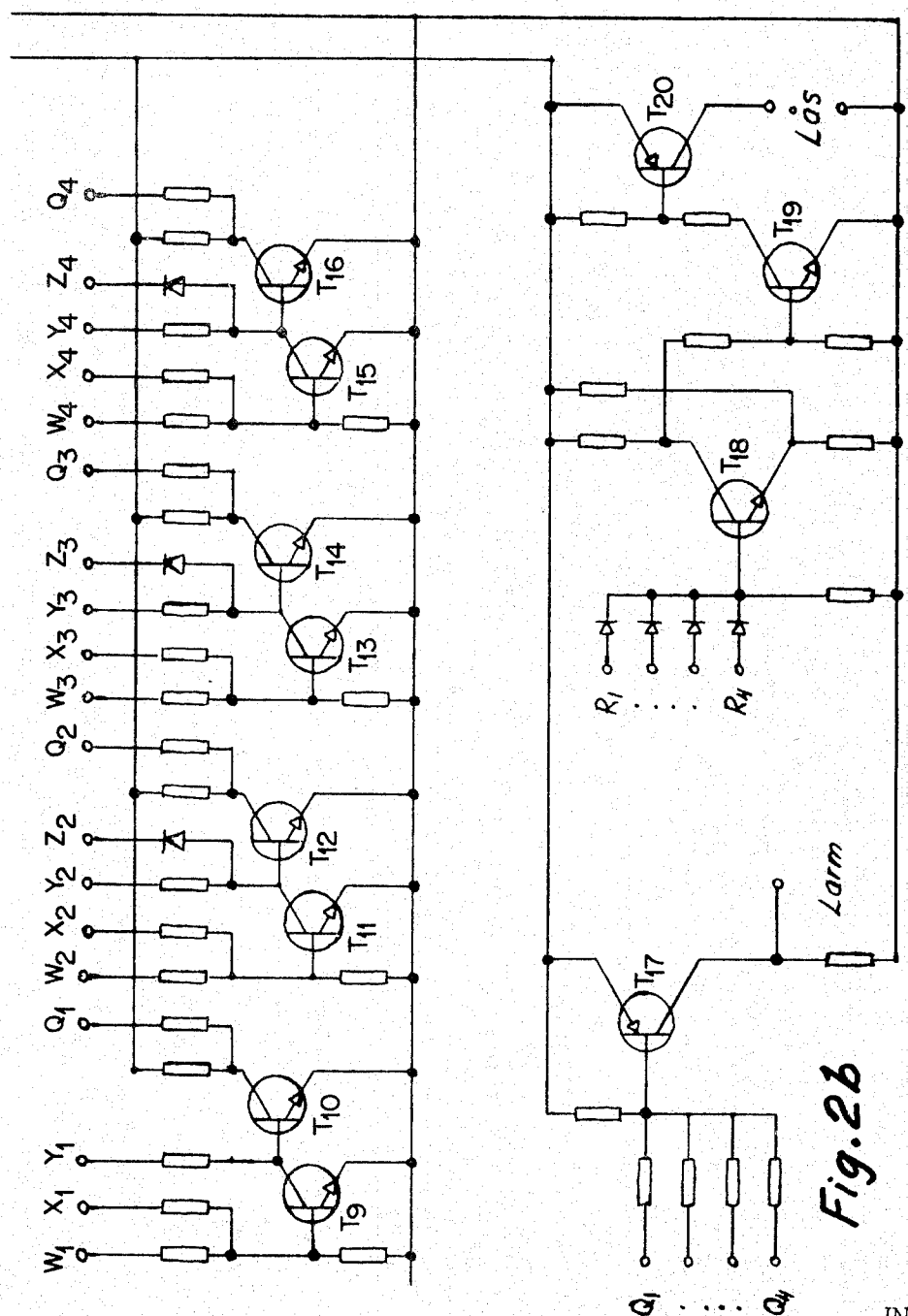


Fig. 2b

INVENTOR
T. G. HESSELGREN

BY Holman, Glascock, Downing & Seibold

ATTORNEYS

ELECTRONIC LOCK ARRANGEMENT HAVING PARALLEL CODED INPUT

DESCRIPTION OF INVENTION

The present invention relates to code locks and especially electronic code locks with very simple and suitable structure and high security against forcing.

Different types of code locks are previously known but they have all been rather complicated and in lack of the desired security. One type uses electro-mechanical step selectors with step-wise feeding in accordance with a predetermined set code, but this means the presence of a number of movable parts, the operations of which can be acoustically localized, thus simplifying a forcing thereof. They are also rather lumbering and not very well suited for automized manufacturing.

Relay chains with mechanical relays have also been suggested for the same or similar purposes, where the relays are to be actuated in a certain order for obtaining the desired result. A change of code setting will in this case be rather complicated as will be a neutralizing of the whole arrangement in connection with wrong handling.

Still another type of electronic code locks is previously known in principle including a number of code steps, which are serially actuated one after the other according to a predetermined code and where the last step when activated generates the control voltage which actuates the lock circuit and releases the lock.

The invention will now be more closely described in connection with the accompanying drawings, which illustrate a practical embodiment of the invention and where

FIG. 1 illustrates the principle design of the invention and

FIGS. 2*a* and 2*b* together show a detailed circuit arrangement.

In FIG. 1 *a* – *d* represent the code pulse inputs and *p* the alarm input. V1 – V4 are flip-flops actuated by incoming code pulses and the actuation of V2 – V4 is accomplished via AND-gates GV2 – GV4. All AND-gates feed directly and AND-gate GLå, which thus requires signals at all inputs for function. There are also a number of gates Ga – Gd which are connected to an OR-circuit, which is activated and causes alarm when output signals are obtained from anyone of the gates Ga–Gd. The inputs of gates Ga – Gd are connected to the code inputs, the alarm input and to the outputs of certain flip-flops.

The lock is so designed that for proper function a code pulse *0* must arrive via cross wire field and proper push button, the gate Ga then maintaining rest condition. Code pulse a also switches the flip-flop V1, the gate Ga then being brought out of function and the first condition for lock release is met simultaneously with the preparation of gate GV2 via code pulse *a*.

As flip-flop V1 is in actuated condition and gate GV2 prepared the gate will pass the succeeding code pulse *b* to flip-flop V2, which then is switched. Code pulse *b* thus can inhibit the alarm pulse in the gate Gb simultaneously with its arrival to gate GV3 then being prepared. The function course is then repeated for consecutive pulses *c* and *d*. However, if a new pulse should appear at *a* after the receipt of pulse *b* alarm is released via gate Gc, wherein no neutralizing of the alarm pulse is obtained in the absence of code pulse *c*.

Thus, the condition for lock release is that all flip-flops V1 – V4 have been switched in proper consecutive order. The lock function is controlled by the AND-circuit GLå, which sends an output signal when all flip-flops have been switched and set in actuated condition. Alternatively the AND-circuit GLå is controlled only by the flip-flop V4, which cannot be switched until all preceeding flip-flops in the chain have been actuated in proper order.

The flip-flops V1 – V4 can be bistable and a time constant for the whole system is then introduced with coordinated resetting. The time constant can suitably be regulated by the alarm pulse *p*.

FIGS. 2*a* and 2*b* illustrate the detailed circuitry of a preferred embodiment of the invention and FIG. 2*b* should be placed below FIG. 2*a* in order to obtain a properly combined arrangement. In order not to overload the drawings unnecessarily with connection wires terminals are shown in both Figures, the principle being that terminals with identical references are interconnected. The drawings include further a large number of coupling elements as resistors, capacitors and diodes, the object of which is to give the various electronic relay circuits proper potential levels at proper times. Most of these elements constitute no part of the invention and such elements have not been referenced and will not be specially mentioned in the following specification, which only refers to elements, active as well as passive, and functions being of importance for the understanding of the invention.

FIG. 2*a* illustrates a cross wire field with a number of horizontal wires and associated push button contacts **0 – 9**, and a number of vertical wires *a* – *d*, each vertical wire being connected to a predetermined horizontal wire, for example at the marked junctions. As the lock can be released only by a consecutive pulse order *a,b,c,d* this means that the illustrated code is 3,0,6,7. This code can of course be easily changed by selecting other junctions. The code pulses are passed via the vertical wires to the flip-flops, here represented by the transistor pairs **T1T2,T3T4,T5T6,T7T8** and transistor combinations **T9T10,T11T12,T13T14,T15T16** in FIG. 2*b* representing the gates Ga – Gd in FIG. 1. The feeding of these gates is made partly via terminals W1 – W4 and partly via terminals Y1 – Y4, the latter corresponding to the alarm input *p* in FIG. 1. The outputs Q1 – Q4 from these gates are connected to transistor T17, which represents the OR-circuit GLa in FIG. 1 causing alarm when actuated. The gate outputs are also connected to the gates **T9T10 . . . T15T16** via terminals X and Z for neutralization, when necessary, of applied alarm pulses and via terminals R to the lock circuit, which has AND-function and here is represented by transistors **T18 – T20**.

The previously mentioned switching of flip-flops T1T2 – T7T8 will now be described more in detail in connection with FIG. 2*a* where it should be noted that switching occurs first at the termination of the applied code pulse.

Switching of the flip-flops is obtained by the presence of a capacitor C in the base circuit of one transistor in each pair. This capacitor is charged by the applied code pulse and the associated base electrode receives the proper potential first at discharge of said capacitor, which happens at the end of the code pulse.

Take for example pulse a which is applied to the first code step including flip-flop T1T2 and through the terminal W1 to gate T9T10 thereby short-circuiting the base of transistor T9 to ground and inhibiting the alarm (alarm pulse arrives simultaneously via terminal Y1). Pulse a actuates the first flip-flop T1T2 so that transistor T1 is made conducting at discharge of capacitor C resulting in a pulse at terminal X1Z2 and this condition is then maintained which means inhibiting function at gate T9T10, i.e. transistor T9 short-circuits the base of transistor T10 thus preventing output signal at the Q1 output of the gate. Output signals at terminals Q are always negative in the selected example.

At arrival of code pulse a the base of transistor T1 goes negative thus making T1 conducting and as a result thereof also making T2 conducting. A special potential condition is then established by aid of resistors *r* which constitute a potential divider and correspond to the AND-gates GV2 – GV4 in FIG. 1. This established potential condition makes then the proper function possible at arrival of the next code pulse *b*.

When code pulse *b* is applied to next flip-flop the condition thereof will be influenced first at the termination of the pulse when a discharge occurs via the lower resistor *r* and transistor T2 to ground. Then transistor T3 will be made conducting and the same course as previously described in connection with the first code pulse will be repeated. Similar courses will be obtained for the following code steps.

Alarm is released as soon as a negative pulse is obtained at anyone of the inputs Q1 – Q4 of transistor T17. This transistor will then be conducting and alarm is released. Negative poten-

tial on terminals Q1 – Q4 is obtained when one or more of transistors T10,T12, T14 or T16 are made conducting and this happens only in connection with improper handling of the lock, i.e. wrong order between the input code pulses.

I claim:

1. An electronic code lock device comprising:

lock release means comprising a plurality of multi-stable serially connected elements each element having a parallel input and a parallel output, said lock release means only being responsive to the application of code pulses to said parallel input in a predetermined sequential manner to generate a signal on each of the parallel outputs, each signal defining the state of a respective multi-state element, and said plurality of signals defining a lock release signal; and

alarm actuating means having a plurality of parallel monitoring inputs each respectively coupled to said parallel outputs of each multi-stable element and sensing the state thereof, said alarm actuating means generating an alarm signal only in response to states of said multi-state elements indicative of the application of code pulses to said multi-stable element parallel inputs in a manner other than in said predetermined manner.

2. The device of claim 1, further including a lock release mechanism, said lock release mechanism being coupled to each of said parallel outputs of said multi-stable element, said lock release mechanism being responsive to said lock release signal.

3. The device of claim 1, wherein said alarm actuating means includes a plurality of sampling gates having inputs coupled to selected parallel outputs of said multi-stable elements, each sampling gate further being coupled to a common alarm interrogation input, the coexistence at any sampling gate of an alarm interrogation signal and a state of a multi-stable element parallel output indicative of code pulse application in a manner other than in said predetermined manner effecting actuation of said sampling gate and generation of said alarm signal.

* * * * *

UNITED STATES PATENT OFFICE

CERTIFICATE OF CORRECTION

Patent No. 3 656,114 Dated April 11, 1972

Inventor(s) Tore Gottfrid Hesselgren

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

In the grant (only) insert the attached sheet:

Signed and sealed this 6th day of March 1973.

(SEAL)
Attest:

EDWARD M.FLETCHER,JR.
Attesting Officer

ROBERT GOTTSCHALK
Commissioner of Patents

FORM PO-1050 (10-69)

USCOMM-DC 60376-P69
* U.S. GOVERNMENT PRINTING OFFICE : 1969 O—366-334.