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(71) Applicant: **HEWLETT-PACKARD DEVELOPMENT COMPANY, L.P.** [US/US]; 10300 Energy Drive, Spring, Texas 77389 (US).

(72) Inventors: **HUANG, Chun-Hua**; No. 66 Jing Mao 2 Road, 10F-2, NanGang District, Taipei City, 11568 (TW). **CHEN, Hsin-Yu**; IF., No. 11, Aly. 1, Ln. 192, Sec. 2, Nanya W. Rd., Banqiao District, Taipei City, 220 (TW). **LIAO,**

Sheng-Lung; No. 66 Jing Mao 2 Road, 10F-2, NanGang District, Taipei City, 11568 (TW).

(74) Agent: **GORDON, Erica** et al.; HP Inc., 3390 E. Harmony Road, Mail Stop 35, Fort Collins, Colorado 80528-9544 (US).

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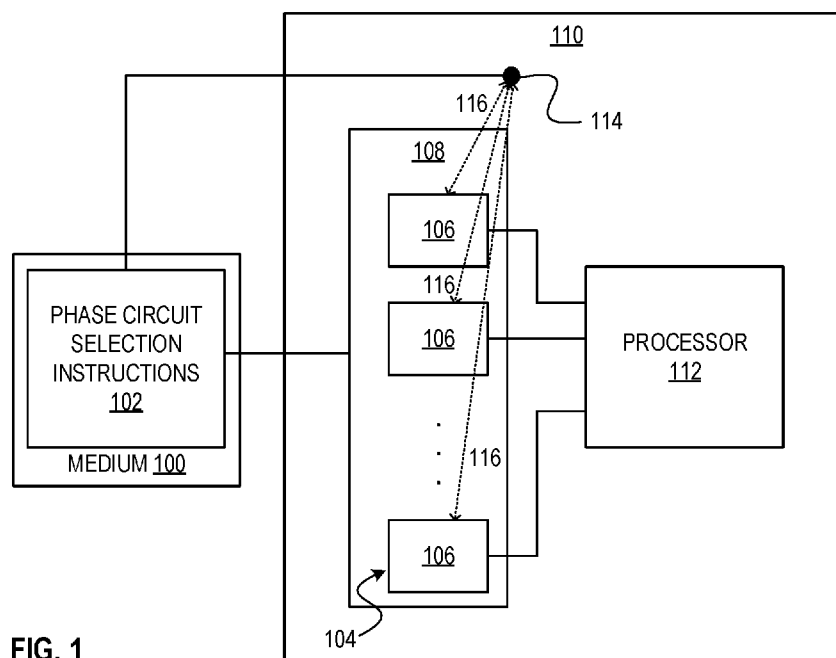


FIG. 1

(57) Abstract: An example non-transitory machine-readable medium includes instructions to determine that an active phase circuit of an array of phase circuits of a voltage regulator is to be disabled based on a reduction in a load of a processor. The voltage regulator and the processor are disposed in a circuit. The voltage regulator provides multi-phase voltages to the processor. The instructions further determine by a temperature sensor a temperature at a position at the circuit, and select the active phase circuit to disable from the array of phase circuits based on the temperature and a predetermined orientation of the array of phase circuits with respect to the position of the temperature.

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CONTROL OF VOLTAGE REGULATOR PHASE CIRCUITS USING TEMPERATURES

BACKGROUND

[0001] A computing device may include a voltage regulator or voltage regulator module (VRM) to provide a central processing unit (CPU) with a stable voltage level. A typical VRM may provide power to various CPU cores and other components of the CPU, such as integrated graphics circuitry. The VRM may be provided on a mainboard that also carries the CPU and other components of a computing device. Pulse-width modulation (PWM) may be used to deliver a stable operating voltage.

[0002] A multi-phase VRM may include parallel phase circuits to provide a plurality of power phases. Each phase may carry a portion of the total power delivered. Phases may be overlapped to provide a stable average voltage to the CPU.

BRIEF DESCRIPTION OF THE DRAWINGS

[0003] FIG. 1 is a block diagram of an example non-transitory machine-readable medium that includes instructions to selectively control an array of phase circuits.

[0004] FIG. 2 is a flowchart of an example method to select a phase circuit to enable or disable based on a temperature.

[0005] FIG. 3 is a block diagram of a device to select a phase circuit to enable or disable based on a temperature.

[0006] FIG. 4A is a schematic diagram of example relationships among phase circuits and temperature sensing locations.

[0007] FIG. 4B is a table of example sequences in which to disable or enable phase circuits based on proximate temperatures as shown in the relationship of FIG. 4A.

[0008] FIG. 5 is a flowchart of an example method to select a phase circuit to enable or disable based on a temperature gradient.

[0009] FIG. 6A is a schematic diagram of an example arrangement of phase circuits and temperature sensing locations.

[0010] FIG. 6B is a schematic diagram of another example arrangement of phase circuits and temperature sensing locations.

[0011] FIG. 7 is a plot of an example thermal gradient with locations of temperature sensors and phase circuits.

DETAILED DESCRIPTION

[0012] VRM phase circuits may be enabled or disabled based on processor load. When computations are reduced, power demand decreases, and a phase circuit may be disabled.

[0013] Phase circuits generate heat. An example phase circuit includes a metal-oxide-semiconductor field-effect transistor (MOSFET) that may contribute significant heat to the overall heat output of a computing device.

[0014] It is often the case that a phase circuit is disabled due to reduced processor load according to an arbitrary predetermined logic. Each phase circuit in an array of phase circuits may be assigned an identifier and may be disabled and enabled based on identifier. For example, phase circuits designated with identifiers 1 to 8 may be disabled starting from the phase circuits with identifiers 7 and 8, then 5 and 6, and so on. This type of logic does not consider heat generation or the thermal balance of the larger circuit or device as a whole.

[0015] A temperature near the phase circuits may be determined and the phase circuits to disable may be selected based on this temperature, so as to control hot spots and improve or maintain thermal balance. For example, rather than arbitrarily selecting a phase circuit to disable, a phase circuit near a hot spot may be disabled, so as to promote the cooling of the hot spot and increase thermal balance. A similar approach may be taken when enabling phase circuits. For example, a phase circuit further from a hot spot may be enabled when processor load demands it.

[0016] FIG. 1 shows an example non-transitory machine-readable medium 100 that includes instructions 102 to selectively control an array 104 of phase circuits 106 of a voltage regulator or VRM 108. A particular phase circuit 106 may be selected to be disabled or enabled based on processor load and determined temperature proximate the array 104. For example, since active phase circuits 106 generate heat, an active phase circuit 106 near a hot zone may be disabled instead of disabling an active phase circuit 106 further from the hot zone. This may increase the thermal balance of a larger circuit 110 that the array 104 of phase circuits 106 supports.

[0017] The voltage regulator supports a processor 112, such as a central processing unit CPU, field-programmable gate array (FPGA), or application-specific integrated circuit (ASIC). The processor 112 may be the CPU of a computing device, such as a notebook computer, desktop computer, server, all-in-one (AIO) computer, or similar.

[0018] The voltage regulator 108 and the processor 112 may be disposed in the 110 circuit, which may be carried by a computing device mainboard. The voltage regulator 108 provides multi-phase voltages to the processor 112.

[0019] The array 104 of phase circuits 106 may be arranged in a predetermined orientation decided at time of design. The orientation may be limited by available space, manufacturing concerns, or similar factors. The depicted linear arrangement is but one example.

[0020] The non-transitory machine-readable medium 100 may include an electronic, magnetic, optical, or other physical storage device that encodes the instructions 102. The medium 100 may include, for example, random access memory (RAM), read-only memory (ROM), electrically-erasable programmable read-only memory (EEPROM), flash memory, a storage drive, an optical device, or similar.

[0021] The medium 100 may cooperate with a controller that may include a microcontroller, a microprocessor, an FPGA, an ASIC, or a similar device capable of executing the instructions. The controller may be separate and distinct from the processor 112. The controller may be a Super I/O controller. In other examples, controller may be the processor 112 or a sub-circuit of the processor 112.

[0022] A temperature sensor 114 may be provided to the circuit 110 to provide a sensed temperature to the instructions 102. The temperature sensor 114 may be positioned in the circuit 110 to sense a temperature at a location in the circuit 110, as decided at time of design. The position of the sensed temperature therefore has a predetermined spatial relationship with the orientation of the array 104 of phase circuits 106. This spatial relationship defines a thermal relationship based on the thermal conductivities of materials that form the circuit 110, active cooling (*e.g.*, a fan, heat pipe, *etc.*), and similar. For example, two components that are separated by a distance on the same circuit board may have a large number of metal traces connecting them. Therefore, these two components may have a closer thermal proximity than two other components separated by the same physical distance but connected with fewer metal traces. In another example, two components separated by a small air gap may be thermally distant as compared to two components positioned on the same circuit board but separated by a large physical distance. Accordingly, each phase circuit 106 has a thermal proximity 116 to the location of the temperature sensor 114.

[0023] The phase circuit selection instructions 102 determine that an active phase circuit 106 of an array 104 is to be disabled, where disabling a phase circuit 106 may be responsive to reduced load at the processor 112.

[0024] The decision to disable an active phase circuit 106 based on processor load may be made by the phase circuit selection instructions 102, by other instructions, or by another controller. Such a decision may be made based on the load of the processor 112. When the load of the processor 112 is reduced, such as by a user process ending or an application being terminated, it may be possible to disable a phase circuit 106 to save power. Once it has been determined that an active phase circuit 106 is to be disabled, the phase circuit selection instructions 102 select the particular active phase circuit 106 to disable.

[0025] The phase circuit selection instructions 102 determine a temperature as sensed by the temperature sensor 114 at the sensor's position in the circuit 110. Other instructions or another controller may continually obtain the temperature and the phase circuit selection instructions 102 may query the relevant portion of memory where such temperature is stored. In other examples, the phase circuit selection instructions 102 directly monitor the temperature sensor 114.

[0026] The phase circuit selection instructions 102 select the active phase circuit 106 to disable based on the sensed temperature and the predetermined orientation of the array 104 of phase circuits 106 with respect to the position of the temperature sensor 114. That is, the active phase circuit 106 to disable is selected with regard to the temperature and the active phase circuit's thermal proximity 116 to the temperature. As such, an active phase circuit 106 that is close to a high temperature may be shut off, so as to promote the reduction of the high temperature.

[0027] The phase circuit selection instructions 102 may compare the sensed temperature to an expected temperature. The expected temperature may be a temperature or temperature range that normally occurs at the circuit 110. The

expected temperature may be predetermined to be a temperature that provides suitable thermal balance to the circuit 110. In other examples, the expected temperature may be another sensed temperature that is determined with another temperature sensor at a different position in the circuit 110. Comparison of two sensed temperatures may thus establish a thermal gradient that may inform the control of the phase circuits 106. That is, if the temperature at a first position exceeds the temperature at a second position, then a high-to-low thermal gradient extends from the first position to the second position. Likewise, if the temperature at the first position is lower than the temperature at the second position, then a low-to-high thermal gradient extends from the first position to the second position.

[0028] The phase circuit selection instructions 102 may determine that the sensed temperature is higher than an expected temperature and, in response, select the active phase circuit 106 nearest the position of the temperature as the phase circuit 106 to be disabled. That is, if the sensed temperature is high, then the phase circuit 106 with the smallest thermal proximity 116 may be disabled to reduce the phase circuit's contribution to the high temperature. The phase circuit selection instructions 102 may determine that the sensed temperature is lower than an expected temperature and, in response, select an active phase circuit 106 to be disabled irrespective of thermal proximity 116.

[0029] After selecting an active phase circuit 106 to disable, the instructions 102 may disable the active phase circuit 106. This may include outputting a signal to the voltage regulator 108. In other examples, the instructions 102 provide an indication of the phase circuit 106 to disable to other instructions or another controller that carries out the disabling of the phase circuit 106.

[0030] The phase circuit selection instructions 102 may select a disabled phase circuit 106 to enable based on the converse of the above-described logic. The instructions 102 may determine that a disabled phase circuit 106 is to be enabled based on an increase in the load of the processor 112.

[0031] The decision to enable a disabled phase circuit 106 may be made by the phase circuit selection instructions 102, by other instructions, or by another controller. When the load of the processor 112 is increased, such as by an application being launched or by the starting of an intensive computation, a disabled phase circuit 106 may be enabled to provide additional power to the processor 112. Once it has been determined that a disabled phase circuit 106 is to be enabled, the phase circuit selection instructions 102 select the particular disabled phase circuit 106 to enable.

[0032] The instructions 102 may select the disabled phase circuit 106 to enable based on a temperature determined by the temperature sensor 114 and the predetermined orientation of the array 104 of phase circuits 106 with respect to the position of the temperature sensor 114. That is, the phase circuit 106 to enable is selected with regard to the temperature and the active phase circuit's thermal proximity 116 to the temperature. As such, a disabled phase circuit 106 that is thermally distant from a high temperature may be turned on, so as to avoid undue increase to the high temperature.

[0033] When selecting a phase circuit 106 to enable, the phase circuit selection instructions 102 may compare the sensed temperature to an expected temperature, as discussed above. The phase circuit selection instructions 102 may determine that the sensed temperature is higher than an expected temperature and, in response, activate a phase circuit 106 that is furthest from the sensed temperature. The phase circuit selection instructions 102 may determine that the sensed temperature is lower than an expected temperature and, in response, activate a phase circuit 106 irrespective of thermal proximity 116.

[0034] As such, the phase circuit selection instructions 102 allow for a thermally informed logic in disabling and enabling VRM phase circuits 106 in response to changes in processor loading. Hot spots in the circuit 110 may be reduced by selection appropriate phase circuits 106 to disable or enable and overall thermal balance may be improved.

[0035] FIG. 2 shows an example method 200 to select a phase circuit to enable or disable based on a temperature. The method 200 may be implemented with instructions that may be stored in non-transitory machine-readable media and executed by a controller. Detail concerning elements of the method 200 described elsewhere herein will not be repeated at length below; the relevant description provided elsewhere herein may be referenced for elements identified by like terminology or reference numerals.

[0036] At block 202, it is determined that a phase circuit of a voltage regulator is to be enabled or disabled based on a change in a load of a processor, such as a CPU of a computing device. The voltage regulator includes an array of phase circuits, which are arranged in an established pattern. A reduced computational demand may require less power and therefore a presently active phase circuit may be disabled. An increased computational demand may require more power and therefore a presently inactive phase circuit may be enabled.

[0037] At block 204, a temperature sensor is used to sense a temperature at a position in thermal proximity to the voltage regulator. The thermal proximity of each phase circuit to the location of the sensed temperature is constrained by the physical layout of the phase circuits. As such, the phase circuits may be ranked from closest to furthest from the location of the sensed temperature.

[0038] Blocks 202, 204 may be performed in any sequence and may be performed asynchronously at the same or different frequencies.

[0039] At block 206, a suitable phase circuit is selected based on the sensed temperature and the thermal proximity of the phase circuit to the position of the sensed temperature. For example, the phase circuit may be selected based on the magnitude of the sensed temperature and whether the phase circuit is to be enabled or disabled.

[0040] For example, if a phase circuit is to be enabled to respond to increased processing load and the sensed temperature exceeds an expected

temperature, then a phase circuit with a large thermal distance from the location of the sensed temperature may be selected for activation. This may reduce or minimize the effect of heat generated by the newly enabled phase circuit on the already high temperature. If a phase circuit is to be disabled to respond to decreased processing load and the sensed temperature exceeds an expected temperature, then a phase circuit with a small thermal distance from the location of the sensed temperature may be selected for activation. This may help promote cooling of the high temperature by ending the heat contribution of a nearby phase circuit.

[0041] At block 204, more than one temperature may be sensed at more than one position. As such, a thermal gradient may be determined and, at block 206, the phase circuit to disable or enable may be selected based on the orientation of the phase circuits in the thermal gradient. For example, if a phase circuit is to be disabled, then a currently active phase circuit at or near a high end of the thermal gradient may be selected to be disabled. Similarly, if a phase circuit is to be enabled, then a currently inactive phase circuit at or near a low end of the thermal gradient may be selected to be enabled.

[0042] The method 200 may be repeated continually as the computing device operates.

[0043] FIG. 3 shows an example device 300 to select a phase circuit to enable or disable based on circuit temperatures. Detail concerning elements of the device 300 described elsewhere herein will not be repeated at length below; the relevant description provided elsewhere herein may be referenced for elements identified by like terminology or reference numerals.

[0044] The device 300 includes a processor 112, a first circuit 302, and a second circuit 304. The processor 112 and circuits 302, 304 may be disposed on a circuit board 306. The device 300 may be a computing device, such as a notebook computer, desktop computer, server, AIO computer, or similar.

[0045] Examples of a processor 112, such as CPU, have been given above.

[0046] Each of the first and second circuits 302, 304 may include an integrated circuit or chip that acts as a localized heat source. For example, the circuit 302, 304 may include a graphics processing module (GPU), Input/Output (I/O) circuit, or memory. The circuit 302, 304 may have a maximum temperature limit for safe operation. In other examples, the circuit 302, 304 may include a plurality of discrete components that generate heat.

[0047] A temperature of the first circuit 302 may be obtained by a first temperature sensor 308 at or near the first circuit 302. The first circuit 302 may include an integral temperature sensor. Similarly, a temperature of the second circuit 304 may be obtained by a second temperature sensor 310 at or near the second circuit 304. The second circuit 304 may include an integral temperature sensor.

[0048] The device 300 further includes a voltage regulator module 312 or VRM including an array of phase circuits 106. Each phase circuit 106 may include a capacitor, a choke, and a MOSFET. The VRM 312 may further include a VRM controller 314 to control PWM signals generated by the phase circuits 106. The voltage regulator module 312 is electrically connected to the processor 112 to provide a suitable amount of power at a stable voltage.

[0049] The VRM 312 is in thermal proximity to the first and second circuits 302, 304, such that heat generated by the VRM 312 may affect temperatures experienced at the first and second circuits 302, 304. The array of phase circuits 106 has an orientation with respect to the first and second circuits 302, 304, such that individual phase circuits 106 may have different effects on the temperatures experienced at or near the first and second circuits 302, 304. That is, each phase circuit 106 has an independent thermal proximity to each of the first and second circuits 302, 304. Examples of first and second thermal proximities 316, 318 are shown for one example phase circuit 106. The VRM 312 and its phase circuits 106 may be oriented with respect to the positioned of the first and second circuits 302, 304 in various different ways. A specific orientation is established at time of design and manufacture.

[0050] The VRM controller 314 is to control the array of phase circuits 106 to enable or disable particular phase circuits 106 depending on load at the processor and the temperatures of the first and second circuits 302, 304. The VRM controller 314 may disable or enable a phase circuit 106 based on a received signal 326.

[0051] The device 300 may further include a controller 320, such as a Super I/O controller, that is connected to the VRM controller 314 and the temperature sensors 308, 310 at the first and second circuits 302, 304. The controller 320 may sense first and second temperatures 322, 324 of the first and second circuits 302, 304, select the phase circuit 106 to be disabled or enabled based on the first and second temperatures 322, 324, and send a signal 326 to the VRM controller 314 to control the VRM 312 to disable or enable the selected phase circuit 106.

[0052] If load on the processor 112 decreases, then an active phase circuit 106 may be disabled. Accordingly, the specific phase circuit 106 to disable may be selected based on a first temperature 322 at the first circuit 302 and a second temperature 324 at the second circuit 304, with regard to the thermal proximity 316, 318 of the phase circuit 106 to the first and second circuits 302, 304. For example, if the first temperature 322 exceeds the second temperature 324, then a phase circuit 106 that is relatively thermally proximate the first circuit 302 may be disabled. The phase circuit 106 to be disabled may be the active one that is nearest the first circuit 302 (*i.e.*, with lowest first thermal proximity 316). Conversely, if the second temperature 324 exceeds the first temperature 322, then a phase circuit 106 that is relatively thermally proximate the second circuit 304 may be disabled. That is, the phase circuit 106 to be disabled may be the active one that is nearest the second circuit 304 (*i.e.*, with lowest second thermal proximity 318).

[0053] If load on the processor 112 increases, then an inactive phase circuit 106 may be enabled. Accordingly, the specific phase circuit 106 to enable may be selected based on a first temperature 322 at the first circuit 302 and a

second temperature 324 at the second circuit 304, with regard to the thermal proximity 316, 318 of the phase circuit 106 to the first and second circuits 302, 304. For example, if the first temperature 322 exceeds the second temperature 324, then a phase circuit 106 that is relatively thermally distant from the first circuit 302 may be enabled. The phase circuit 106 to be enabled may be the inactive one that is furthest from the first circuit 302 (*i.e.*, with highest first thermal proximity 316). Conversely, if the second temperature 324 exceeds the first temperature 322, then a phase circuit 106 that is relatively thermally distant from the second circuit 304 may be enabled. That is, the phase circuit 106 to be enabled may be the inactive one that is furthest from the second circuit 304 (*i.e.*, with highest second thermal proximity 318).

[0054] The first and second temperatures 322, 324 may be compared in absolute terms, such as degrees Celsius or temperature sensor voltage. As such, the higher temperature is readily apparent.

[0055] In other examples, the first and second temperatures 322, 324 may be compared proportionally. That is, each temperature may be have a reference, such as a maximum allowable safe temperature. A measured temperature of 60 degrees at a chip that can safely handle 100 degrees is less of a concern than the same measured temperature on a chip that can safely handle 80 degrees. A measured temperature 322, 324 may be converted to a proportional value with respect to its reference, and proportional values may be compared to determine which phase circuit 106 to disable or enable. For example, assuming a datum temperature of 20 degrees, the above numerical examples provide proportions of 0.50 (*i.e.*, $[60 - 20] / [100 - 20]$) and 0.67 (*i.e.*, $[60 - 20] / [80 - 20]$).

[0056] Hence, when the first temperature in proportion to the first reference is greater than the second temperature in proportion to the second reference, the phase circuit 106 to disable is selected as an active phase circuit nearer the location of the first temperature.

[0057] The controller 320 may include or have access to memory 328 to store instructions to carry out the above discussed functionality.

[0058] The memory 328 may store data 330 indicative of the orientation of the array of phase circuits relative to the first and second circuits. FIGs. 4A and 4B show an example of such data 330.

[0059] FIG. 4A shows an example thermal arrangement of sensed temperatures T1, T2 to locations of phase circuits, identified as PC#1, PC#2, *etc.* In this example PC#1 is thermally closest to temperature T1, PC#2 is next closest, and so on. FIG. 4B shows example sequences in which to disable or enable phase circuits of FIG. 4A based on relative magnitudes or proportions of temperatures T1 and T2. Each sequence expresses the predetermined orientation of the array of phase circuits relative to the first and second circuits with consideration of the individual thermal proximity of each phase circuit to the first and second circuits. The numbers 1, 2, 3, *etc.* are the phase circuit ranks for a given set of conditions and show the order in which the phase circuits should be enabled or disabled. For example, if a phase circuit is to be disabled and $T1 > T2$, then phase circuit PS#2 is the second phase circuit to disable. In another example, if a phase circuit is to be enabled and $T2 > T1$, then phase circuit PS#3 is the third phase circuit to enable.

[0060] FIG. 5 shows an example method 500 to select a phase circuit to enable or disable based on a temperature gradient. The method 500 may be implemented with instructions that may be stored in non-transitory machine-readable media and executed by a controller. Detail concerning elements of the method 200 described elsewhere herein will not be repeated at length below; the relevant description provided elsewhere herein may be referenced for elements identified by like terminology or reference numerals.

[0061] At block 502 it is determined whether a phase circuit of a VRM is to be disabled or enabled. The decision of whether to disable or enable a phase circuit may be based on a respective decrease or increase in a load to a processor.

[0062] If a phase circuit is to be disabled, at block 504, a phase circuit close to a higher end of a thermal gradient is selected. A thermal gradient may be determined by sensing a plurality of temperatures in a device that contains the VRM.

[0063] At block 506, the selected phase circuit is disabled. The contribution of the selected phase circuit to the thermal gradient is thus reduced or eliminated and the thermal gradient may thus become more balanced (*i.e.*, the gradient's slope is reduced).

[0064] If a phase circuit is to be enabled, at block 508, a phase circuit close to a lower end of the thermal gradient is selected.

[0065] At block 510, the selected phase circuit is enabled. The newly enabled phase circuit then heats and contributes to the thermal gradient, which is thus made more balanced.

[0066] In various examples, as shown in FIGs. 6A and 6B, other arrangements of arrays of phase circuits may be provided with any suitable number of temperature sensors to determine a temperature gradient, which may be in one, two, or three spatial dimensions. The influence of each phase circuit on the temperature gradient is readily quantifiable, whether empirically or by calculation. Hence, various sequences to disable and enable phase circuits may be established for various measured temperature gradients by applying the teachings described herein.

[0067] FIG. 7 shows an example thermal gradient of temperature, T , vs. position on an X , Y , and/or Z axis, as may be established within a computing device. Temperatures at various sensors (TS) at various positions may be measured and referenced to define the gradient. The locations of phase circuits (PC) with reference to the temperature gradient may be referenced when enabling or disabling a phase circuit due to a change in processing load. An active phase circuit with a high temperature gradient value may be selected

when disabling a phase circuit, and a disabled phase circuit with a low temperature gradient value may be selected when enabling a phase circuit.

[0068] In view of the above, a phase circuit to disable due to decreased CPU load may be selected based on temperature in the vicinity of the phase circuits. Likewise, a phase circuit to enable due to increased CPU load may be selected based on temperature. A thermal gradient may be determined and the positions of the phase circuits in the thermal gradient may be referenced to select a phase circuit to disable or enable.

[0069] It should be recognized that features and aspects of the various examples provided above can be combined into further examples that also fall within the scope of the present disclosure. In addition, the figures are not to scale and may have size and shape exaggerated for illustrative purposes.

CLAIMS

1. A non-transitory machine-readable medium comprising instructions to:

determine that an active phase circuit of an array of phase circuits of a voltage regulator is to be disabled based on a reduction in a load of a processor, wherein the voltage regulator and the processor are disposed in a circuit, and wherein the voltage regulator provides multi-phase voltages to the processor;

determine by a temperature sensor a temperature at a position at the circuit; and

select the active phase circuit to disable from the array of phase circuits based on the temperature and a predetermined orientation of the array of phase circuits with respect to the position of the temperature.

2. The non-transitory machine-readable medium of claim 1, wherein the instructions are further to disable the active phase circuit.

3. The non-transitory machine-readable medium of claim 1, wherein the instructions are further to:

determine that the temperature is higher than an expected temperature and, in response, select the active phase circuit nearest the position of the temperature.

4. The non-transitory machine-readable medium of claim 1, wherein the instructions are further to:

determine that the temperature is lower than an expected temperature and, in response, select the active phase circuit irrespective of the position of the temperature.

5. The non-transitory machine-readable medium of claim 1, wherein the temperature is a first temperature and the position is a first position, and wherein the instructions are further to:

sense a second temperature at a second position; and

select the phase circuit to disable based on the first temperature, the second temperature, and the predetermined orientation of the array of phase circuits with respect to the first and second positions.

6. The non-transitory machine-readable medium of claim 1, wherein the instructions are further to:

determine that a disabled phase circuit of the array of phase circuits is to be enabled based on an increase in the load of the processor;

select the disabled phase circuit to enable based on the temperature and the predetermined orientation of the array of phase circuits with respect to the position of the temperature.

7. A device comprising:

a processor;

a first circuit;

a second circuit; and

a voltage regulator module including an array of phase circuits, the voltage regulator module electrically connected to the processor, the voltage regulator module in thermal proximity to the first circuit and the second circuit;

wherein the voltage regulator module is to disable a phase circuit of the array of phase circuits in response to a reduced load at the processor, wherein the phase circuit is selected from the array of phase circuits based on a first temperature of the first circuit and a second temperature of the second circuit.

8. The device of claim 7, wherein, when the first temperature exceeds the second temperature, the phase circuit to disable is selected as an active phase circuit that has a first thermal proximity to the first circuit and that has a second

thermal proximity to the second circuit, wherein the first thermal proximity is smaller than the second thermal proximity.

9. The device of claim 7, wherein, when the first temperature in proportion to a first reference is greater than the second temperature in proportion to a second reference, the phase circuit to disable is selected as an active phase circuit that has a first thermal proximity to the first circuit and that has a second thermal proximity to the second circuit, wherein the first thermal proximity is smaller than the second thermal proximity.

10. The device of claim 7, further comprising a controller to:

sense the first temperature and the second temperature; and

select the phase circuit to be disabled based on the first temperature and the second temperature; and

control the voltage regulator module to disable the phase circuit.

11. The device of claim 7, wherein the voltage regulator module is to enable a disabled phase circuit of the array of phase circuits in response to an increased load at the processor, wherein the disabled phase circuit is selected from the array of phase circuits based on the first temperature and the second temperature.

12. A method comprising:

determining that a phase circuit of a voltage regulator is to be enabled or disabled based on a change in a load of a processor;

using a temperature sensor to sense a temperature at a position in thermal proximity to the voltage regulator; and

selecting the phase circuit from a plurality of phase circuits of the voltage regulator, the selecting being based on the temperature and a thermal proximity of the phase circuit to the position of the temperature.

13. The method of claim 12, further comprising:

determining that a disabled phase circuit of the plurality of phase circuits is to be enabled; and

selecting the disabled phase circuit from the plurality of phase circuits of the voltage regulator, the selecting being based on the temperature and a thermal proximity of the disabled phase circuit to the position of the temperature.

14. The method of claim 13, further comprising determining a temperature gradient, wherein the selecting is based on locations of the plurality of phase circuits in the temperature gradient.

15. The method of claim 13, further comprising disabling the phase circuit.

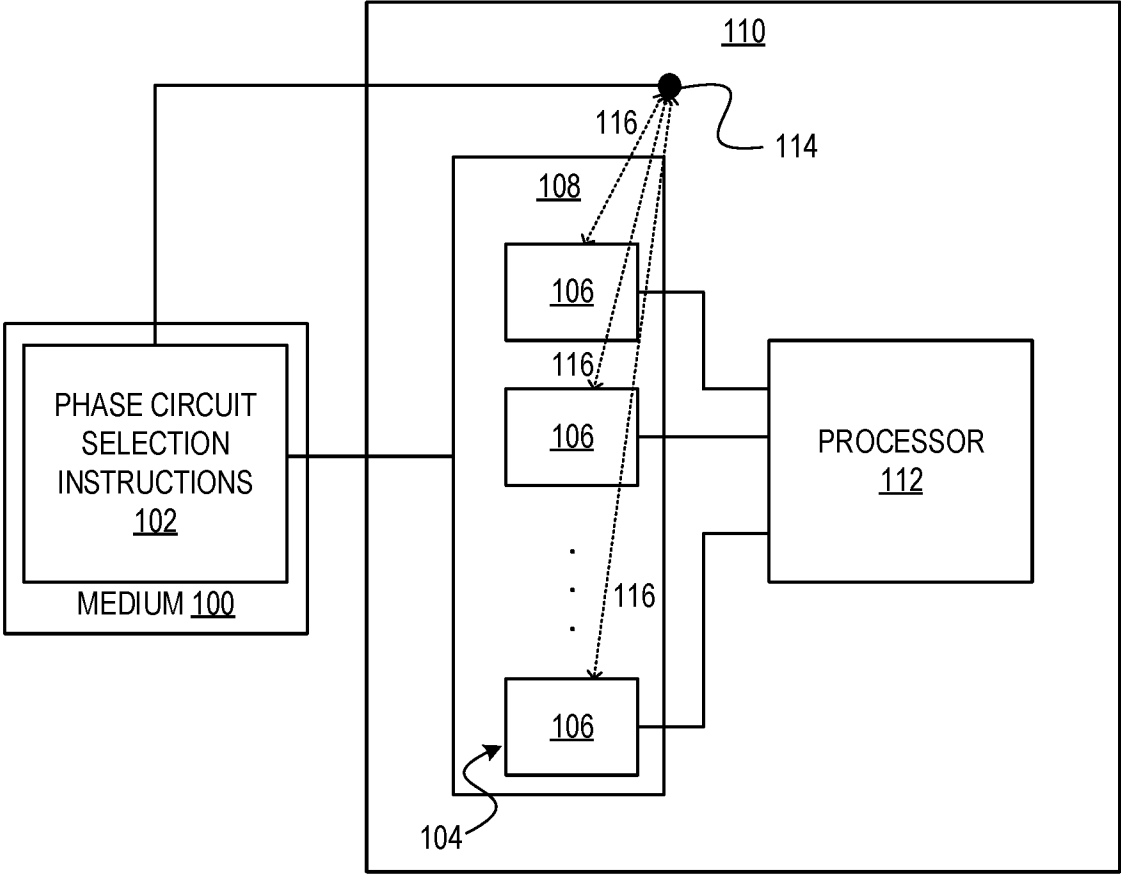


FIG. 1

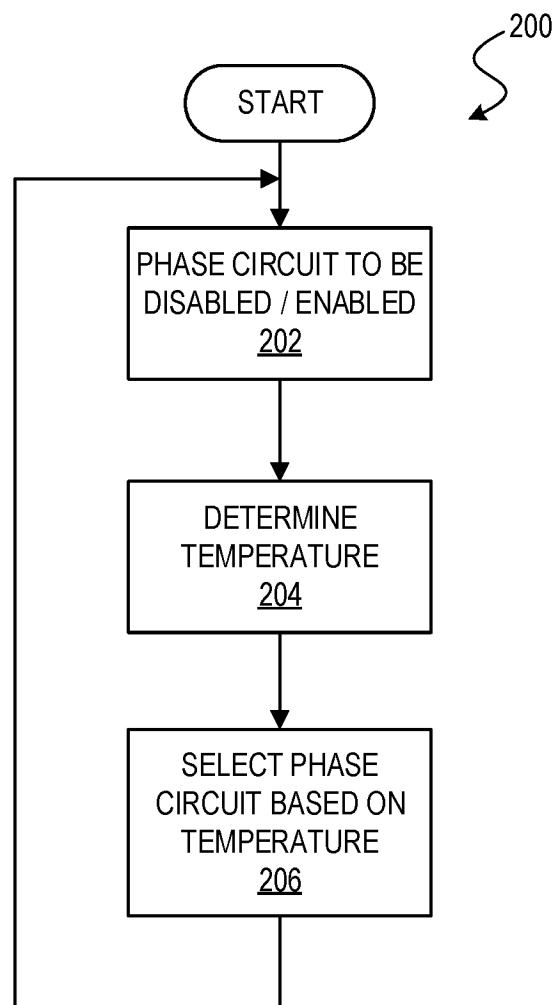


FIG. 2

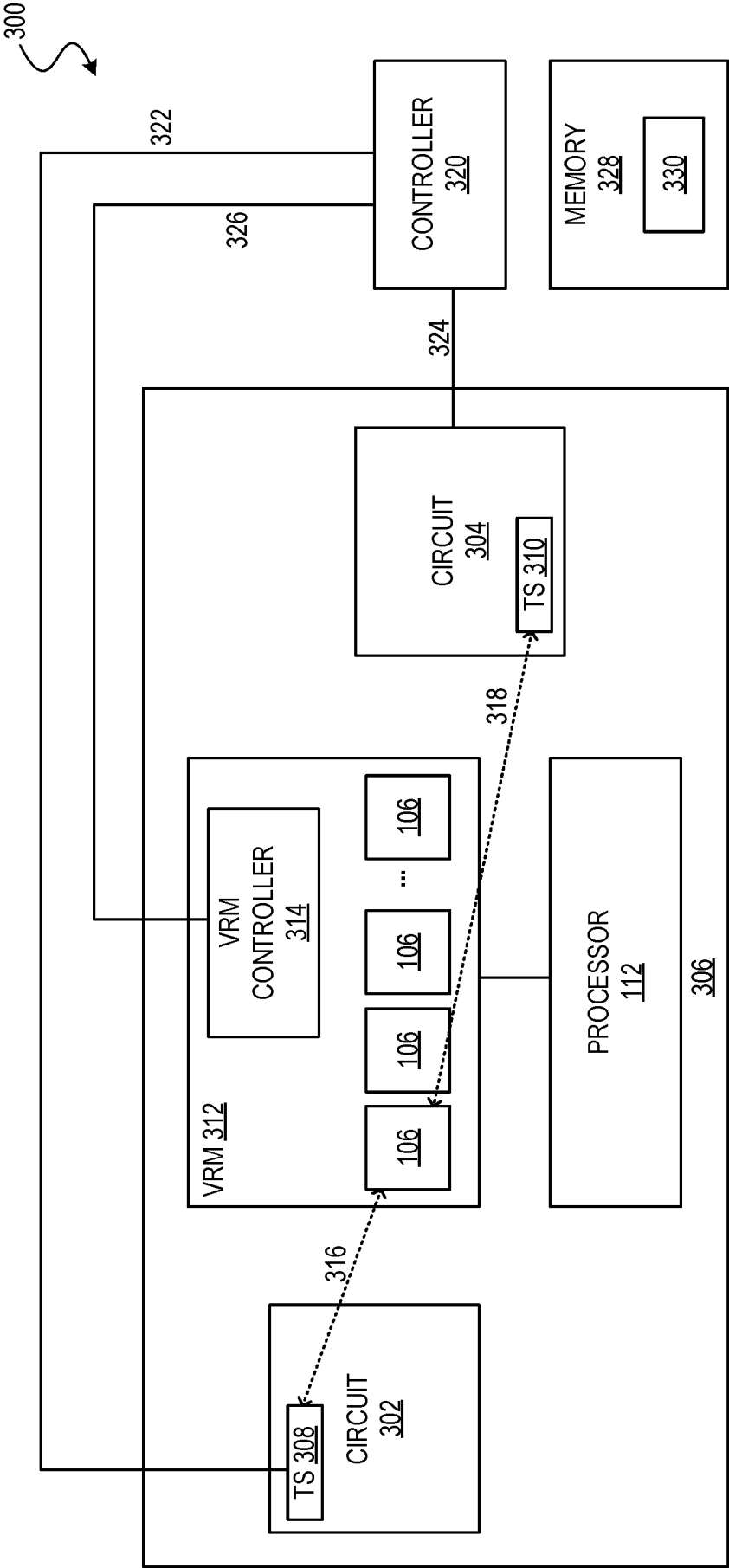


FIG. 3

T1	PC#1	PC#2	PC#3	PC#4	PC#5	PC#6	PC#7	PC#8	T2
----	------	------	------	------	------	------	------	------	----

FIG. 4A

PHASE CIRCUITS	DISABLE		ENABLE	
	T1>T2	T2>T1	T1>T2	T2>T1
PC#1	1	8	8	1
PC#2	2	7	7	2
PC#3	3	6	6	3
PC#4	4	5	5	4
PC#5	5	4	4	5
PC#6	6	3	3	6
PC#7	7	2	2	7
PC#8	8	1	1	8

FIG. 4B

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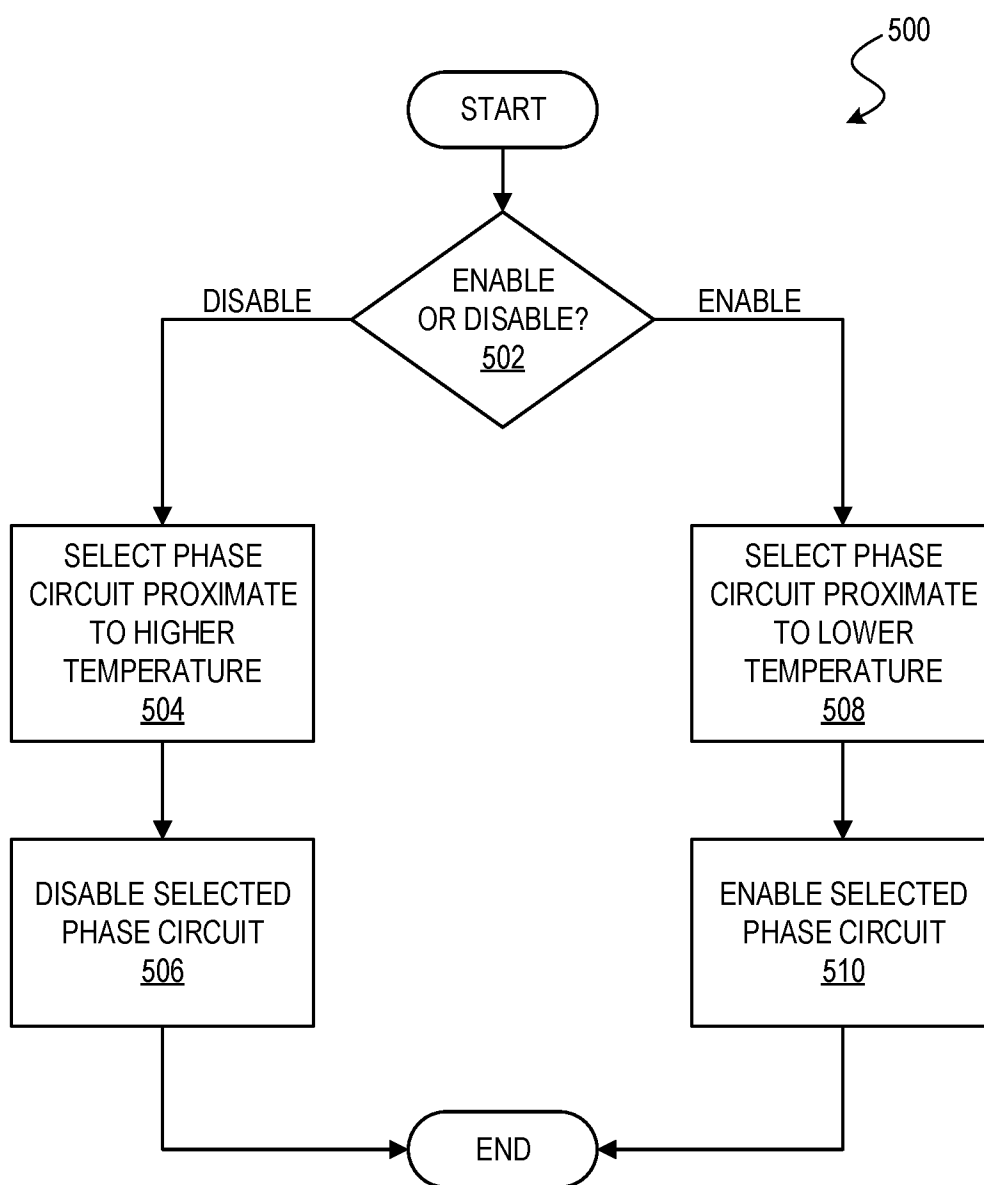


FIG. 5

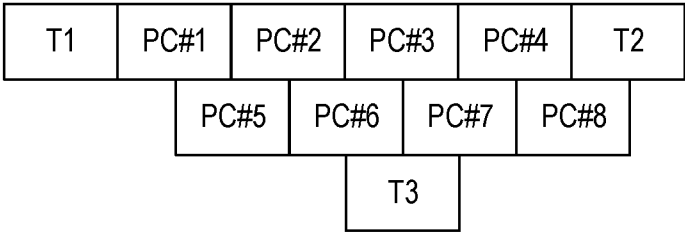


FIG. 6A

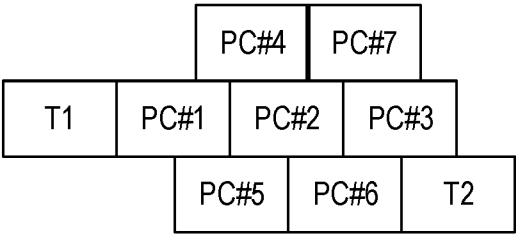


FIG. 6B

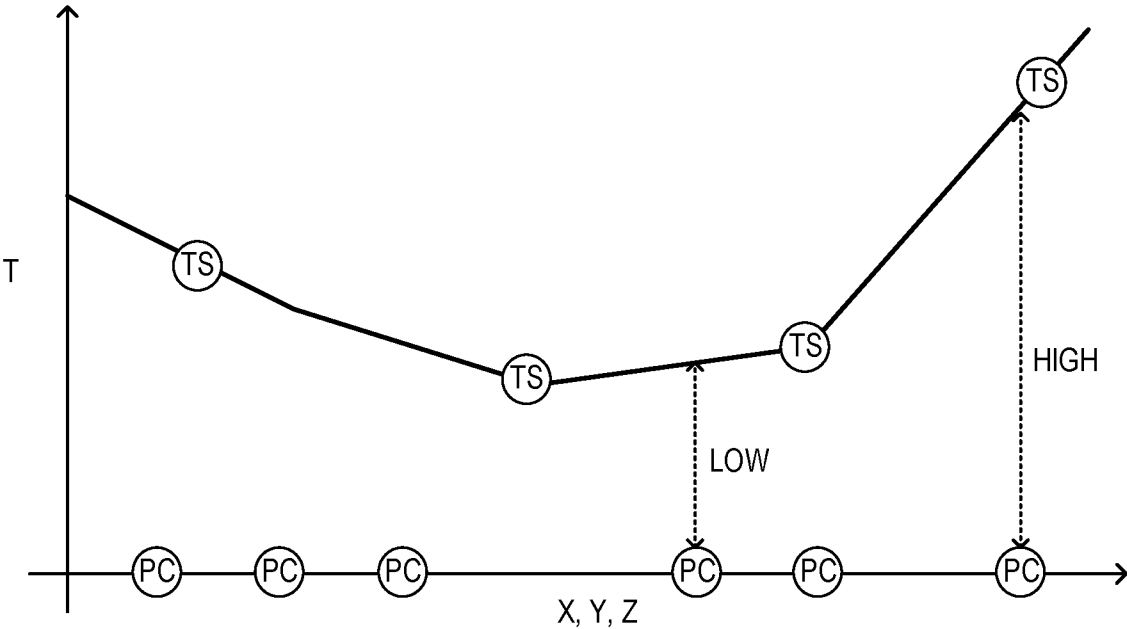


FIG. 7

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 2020/048686

A. CLASSIFICATION OF SUBJECT MATTER		
G06F 1/3296 (2019.01) G06F 1/3206 (2019.01) G06F 1/26 (2006.01)		
According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED		
Minimum documentation searched (classification system followed by classification symbols)		
G06F 1/00, 1/32, 1/3203, 1/3206, 1/3234, 1/3296		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched		
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)		
PatSearch (RUPTO internal), USPTO, PAJ, Esp@cenet, DWPI, EAPATIS, PATENTSCOPE		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2019/0121411 A1 (INTEL CORPORATION) 25.04.2019, [0032]-[0034], [0046], [0047], [0136]	1-15
A	US 2016/0225562 A1 (UNILECTRIC, LLC) 04.08.2016	1-15
A	WO 2014/107197 A1 (INTEL CORPORATION) 10.07.2014	1-15
☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.		
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"P" document published prior to the international filing date but later than the priority date claimed		
Date of the actual completion of the international search	Date of mailing of the international search report	
13 May 2021 (13.05.2021)	20 May 2021 (20.05.2021)	
Name and mailing address of the ISA/RU: Federal Institute of Industrial Property, Berezhkovskaya nab., 30-1, Moscow, G-59, GSP-3, Russia, 125993 Facsimile No: (8-495) 531-63-18, (8-499) 243-33-37	Authorized officer V. Volodin Telephone No. 8 499 240 25 91	