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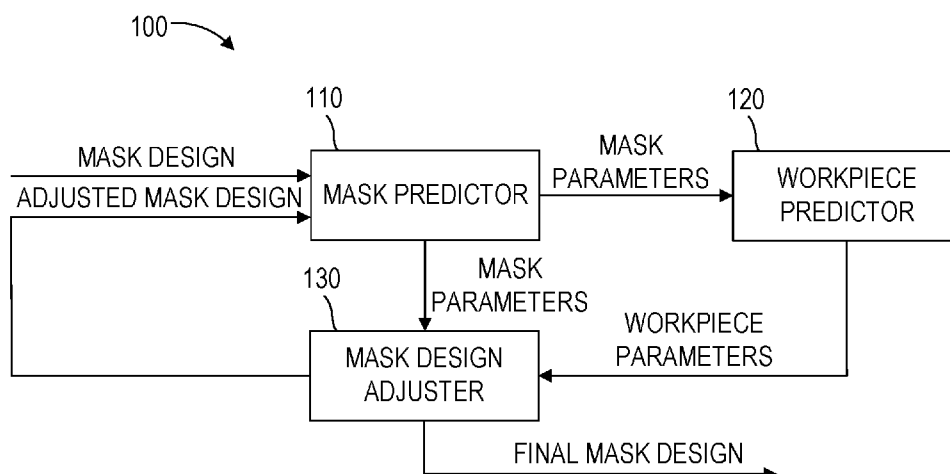


FIG. 1

(57) **Abstract:** Accounting for predicted mask infidelities is disclosed. A computer-readable medium includes computer-readable instructions configured to instruct a processor to predict mask infidelities and workpiece infidelities resulting from the predicted mask infidelities, and produce a compensated mask design to compensate for the predicted mask and workpiece infidelities. A method includes providing a preliminary mask design, determining mask infidelities responsive to the preliminary mask design, determining workpiece infidelities responsive to the mask infidelities, and adjusting the preliminary mask design to compensate for the determined manufacturing infidelities and the determined workpiece infidelities.

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ACCOUNTING FOR MASK MANUFACTURING INFIDELITIES IN SEMICONDUCTOR DEVICES

Technical Field

[0001] The disclosure relates generally to compensating mask designs for predicted manufacturing infidelities in masks used for manufacturing workpieces. More specifically, the disclosure relates to compensating mask designs for use in manufacturing semiconductor devices (e.g., semiconductor wafers).

Background

[0002] Demand for compact semiconductor devices has driven production of semiconductor devices with smaller and smaller features as time progresses. As a result, mask design for producing these smaller features is no longer a trivial task. For example, in decades past, when features were larger, features in masks designed to produce the features in the semiconductor device had similar shapes as the features in the semiconductor device. In contrast, features in masks for producing today's much smaller features in semiconductor devices may not be recognizable to a human observer as corresponding to the features in the semiconductor device.

[0003] Software tools are often used to aid in the design of masks for producing very small features in semiconductor devices. Sometimes mask features designed with the aid of these software tools are at or near manufacturing tolerances for mask manufacturing (e.g., tolerances in dimensions). As a result, infidelities in manufactured masks sometimes occur, particularly in features at or near manufacturing tolerances. Infidelities in masks can lead to infidelities in the features of semiconductor devices manufactured with the masks. Some of these infidelities in the features of the semiconductor devices may prevent the semiconductor devices from functioning properly.

Brief Description of the Drawings

[0004] FIG. 1 is a simplified block diagram of a mask design system, according to some embodiments.

[0005] FIG. 2 is a simplified plan view of a portion of a mask design for illustrating an example of the impact mode, according to some embodiments.

[0006] FIG. 3 is a simplified plan view of a portion of a mask design for illustrating an example of the sensitivity mode, according to some embodiments.

[0007] FIG. 4 is a simplified flowchart illustrating a method of designing a mask for manufacturing a workpiece.

[0008] FIG. 5 is a simplified flowchart illustrating a method of manufacturing a semiconductor device.

[0009] FIG. 6 is a simplified block diagram of a computing system, according to some embodiments.

Detailed Description

[0010] In the following description, various aspects of the illustrative implementations will be described using terms commonly employed by those skilled in the art to convey the substance of their work to others skilled in the art. However, it will be apparent to those skilled in the art that the disclosure may be practiced with only some of the described aspects. For purposes of explanation, specific numbers, materials and configurations are set forth in order to provide a thorough understanding of the illustrative implementations. It will be apparent to one skilled in the art, however, that the disclosure may be practiced without the specific details. In other instances, well-known features are omitted or simplified in order not to obscure the illustrative implementations.

[0011] Various operations will be described as multiple discrete operations, in turn, in a manner that is helpful in understanding the disclosure. The order in which the operations are presented in the description, however, should not be construed to imply that these operations are necessarily order dependent. In particular, these operations need not be performed in the order of presentation. Rather, in some embodiments, the order may be modified.

[0012] Accounting for mask infidelities is disclosed herein. In particular, disclosed is compensation for mask infidelities of masks to be used in manufacturing semiconductor devices (e.g., lithography). Although the mask design principles discussed herein are applicable to semiconductor device manufacturing, principles disclosed herein may also be applicable to mask design for other industries. Through use of principles disclosed herein, improved mask fidelity may be achieved, resource waste (e.g., materials, engineering time, computing time, etc.) may be avoided, mask rule constraints may be improved.

[0013] As used herein, the term “workpiece” refers to an apparatus that a mask is intended to pattern features onto (e.g., by using lithography). By way of non-limiting example, a workpiece may include a semiconductor wafer (sometimes referred to

herein as “wafer”) or semiconductor device. As used herein, the term “semiconductor wafer” refers to wafers or chips of semiconductor material (e.g., silicon, III-V semiconductor material, II-VI semiconductor material, other semiconductor materials, or combinations thereof). It should be noted that a semiconductor wafer may include a semiconductor material substrate alone or with other materials and/or features formed therein or thereon. Also, a semiconductor wafer may include a silicon on insulator (SOI) substrate (e.g., a silicon on glass substrate, a silicon on sapphire substrate, etc.). In some instances the term “semiconductor wafer” may refer to an apparatus formed on or in a semiconductor substrate but that has had part or all of the semiconductor substrate removed therefrom.

[0014] It will be appreciated by those of ordinary skill in the art that one or more masks may be used at various different stages of manufacturing of a semiconductor device. The mask design principles disclosed herein may be applied to the design of any one or more of these masks used at any of the various different stages.

[0015] FIG. 1 is a simplified block diagram of a mask design system 100, according to some embodiments. The mask design system 100 includes a mask predictor 110, a workpiece predictor 120, and a mask design adjuster 130. The mask predictor 110 is configured to predict mask parameters of a manufactured mask based on a mask design inputted into the mask predictor 110 if manufactured according to the mask design. The workpiece predictor 120 is configured to predict workpiece parameters of a manufactured workpiece based on the mask parameters from the mask predictor 110. The mask design adjuster 130 is configured to generate an adjusted mask design based on the workpiece parameters from the workpiece predictor 120. The adjusted mask design may be inputted into the mask predictor 110, and the mask design system 100 may repeat operations of the mask predictor 110, the workpiece predictor 120, and the mask design adjuster 130 until it is determined, based on the workpiece parameters from the workpiece predictor 120, that the adjusted mask design is suitable to be outputted as a final mask design.

[0016] The mask design adjuster 130 identifies geometries of predicted workpieces (e.g., predicted by the workpiece predictor 120) that are patterning liabilities (e.g., lithographic patterning liabilities) as a result of predicted mask infidelities (e.g., predicted by the mask predictor 110 and identified in the mask parameters). This information can be used to refine, revise, or both refine and revise

the mask design and/or Mask Rule Constraints (MRCs) applied to optical proximity correction (OPC) layouts (e.g., an OPC of the workpiece predictor 120), or combinations thereof. This information can also supplement a mask defect inspection process.

[0017] The mask predictor 110 is configured to receive a mask design as an input, and generate mask parameters of a predicted manufactured mask resulting therefrom as an output. In some embodiments, the inputted mask design may be generated by a software tool configured to generate the mask design based on a desired workpiece design. The outputted mask parameters may include data indicating a geometry of the predicted manufactured mask, predicted mask patterning infidelities (also referred to herein as “mask infidelities”), other predicted mask parameters, or combinations thereof. In some embodiments, the mask predictor 110 may include a mask-error-correction (MEC) software tool.

[0018] As used herein, the term “infidelities” refers to deviations from a desired geometry or design. For example, mask infidelities include differences between a desired mask (e.g., a mask indicated by a mask design) and a manufactured or prediction of a manufactured mask. Mask infidelities can translate to workpiece (e.g., a semiconductor wafer) patterning infidelities (also referred to herein as “workpiece infidelities”). Workpiece infidelities include differences between a desired workpiece (e.g., a desired workpiece design used to generate a mask design) and a manufactured or prediction of a manufactured workpiece (e.g., geometric differences, wafer intensity differences, etc.).

[0019] The workpiece predictor 120 is configured to receive the mask parameters from the mask predictor 110, and generate workpiece parameters of a predicted workpiece resulting from manufacturing using a mask following the mask parameters. By way of non-limiting example, the workpiece predictor 120 may include one or more OPC software tools. The workpiece predictor 120 (e.g., including one or more OPC models) provides a quantitative method for assessing how mask infidelities will impact a workpiece’s (e.g., wafer’s) health, patterning, other workpiece parameters, or combinations thereof. By way of non-limiting example, the workpiece predictor 120 may be configured to provide a maximum wafer aerial image intensity, a wafer critical dimension delta at locations where the mask deviates from a target geometry (e.g., mask infidelity), other parameters, or combinations thereof.

[0020] Rather than evaluating the mask design with an OPC software tool (which conventionally receives a perfect mask design without mask infidelities as an input) and an MEC software tool separately and independently to assess mask infidelities, the mask design system 100 of FIG. 1 leverages the knowledge of predicted mask infidelities when predicting workpiece parameters. Since manufactured masks rarely perfectly match the mask design used to generate the manufactured masks, the mask design system 100 of FIG. 1 may provide more accurate workpiece parameter predictions than conventional systems. In order to achieve these improved results over conventional systems, mask infidelity information is provided to the workpiece predictor 120.

[0021] The mask design adjuster 130 uses the results from the mask predictor 110 to modify the mask design to produce an adjusted mask design, and ultimately a final mask design. As a result, a mask manufactured using the final mask design may, in some instances, more closely match the original mask design than a mask manufactured using the original mask design itself. The mask design adjuster 130 uses the results of the mask predictor 110 and the workpiece predictor 120 to assess the workpiece patterning impact resulting from the adjusted mask design. Accordingly, the mask design system 100 enables the evaluation of predicted workpiece infidelities as a function of predicted mask infidelities.

[0022] In some embodiments, the workpiece predictor 120 may be configured to evaluate the entire mask indicated by the mask parameters from the mask predictor 110. Such computation may be cumbersome, however, especially when assessing extremely large numbers of features that may exist in a mask for manufacturing devices such as processors, large memory arrays, and the like. Accordingly, in some embodiments, the workpiece predictor 120 may be configured to only evaluate specific sites of a workpiece. For example, the workpiece predictor 120 may be configured to evaluate features of the workpiece corresponding to mask features that are at or near mask manufacturing tolerances.

[0023] As another example, the workpiece predictor 120 may be configured to only evaluate features of the workpiece corresponding to specific predicted mask infidelities that amount to violations of a predetermined set of rules (e.g., deviation or bridge/pinch mask infidelity violations). In such embodiments, the workpiece predictor 120 may perform predictions for workpiece parameters on a violation site-by-site basis (e.g., sites of the workpiece that correspond to sites of the predicted

mask that exhibit specific infidelities). The mask design adjuster 130 may use different measurement modes (the term “measurement” referring to conceptual measurements of a predicted mask) for evaluating the mask design on this site-by-site basis. Two of these measurement modes may include an impact mode and a sensitivity mode.

[0024] In the impact mode, the mask predictor 110 may provide mask parameters that match what is predicted to be patterned on a mask manufactured by a mask manufacturer responsive to the original mask design. The workpiece predictor 120 may predict a maximum wafer intensity and a maximum contour delta of specific features of a workpiece predicted to be manufactured using the mask provided by the mask manufacturer responsive to the mask parameters from the mask predictor 110. FIG. 2 illustrates an example of functionality of the impact mode.

[0025] FIG. 2 is a simplified plan view of a portion 200 of a mask design for illustrating an example of the impact mode, according to some embodiments. Referring to FIGS. 1 and 2 together, the portion 200 illustrated in FIG. 2 is merely a conceptual portion 200 of a desired mask indicated by the mask design, as the mask design system 100 of FIG. 1 merely processes the mask design as data indicating the desired mask. Accordingly, although FIG. 2 is discussed in terms of the conceptual portion 200, it should be understood that, in contrast, the mask design system 100 performs functions that parallel those discussed with reference to FIG. 2 using the data of the mask design.

[0026] The portion 200 includes a feature 240 of the mask design, illustrated in solid lines. When the mask predictor 110 generates the mask parameters, a predicted feature 250 (illustrated in broken lines) of the manufactured mask that corresponds to the feature 240 may be determined. The predicted feature 250 may deviate from the feature 240. For example, an end of the predicted feature 250 may extend past an end of the feature 240 by a length A. If the length A is larger than a predetermined tolerance defined in violations parameters, the mask design adjuster 130 may flag the feature 240 for analysis with the workpiece predictor 120 to determine an impact of the mask infidelity on a workpiece.

[0027] The workpiece predictor 120 may predict a workpiece feature corresponding to the predicted feature 250 of the mask, and provide workpiece parameters (e.g., a maximum wafer intensity and a maximum contour delta) indicating information regarding the workpiece feature to the mask design adjuster

130. The mask design adjuster 130 may determine whether it is believed that the workpiece will function as intended based on the predicted workpiece feature. If the mask design adjuster 130 determines that the workpiece feature will not function as intended (e.g., a catastrophic failure), the mask design adjuster 130 may adjust the mask design to compensate for the mask infidelity. If, however, the mask design adjuster 130 determines that the workpiece feature will function as intended despite the mask infidelity, the mask design adjuster 130 may not adjust the mask design to compensate for the mask infidelity.

[0028] The mask design adjuster 130 may use the mask predictor 110 to flag other mask infidelities, and the workpiece predictor 120 to analyze the impact of these mask infidelities on the workpiece. The mask design adjuster 130 may adjust the mask design accordingly, and provide a final mask design including the adjusted mask (if any adjustments are made; otherwise the final mask may include the original mask design). The final mask design may be provided to a mask manufacturer to manufacture a mask according to the final mask design.

[0029] Referring once again to FIG. 1, in the sensitivity mode, the mask predictor 110 may provide mask parameters that match what is predicted to be patterned in a mask manufactured by a mask manufacturer responsive to the original mask design. Similarly as discussed above with reference to the impact mode, the workpiece predictor 120 may predict a maximum wafer intensity and a maximum contour delta of a workpiece manufactured using the mask provided by the mask manufacturer responsive to the mask parameters from the mask predictor 110. In addition, however, in the sensitivity mode the mask design is varied (perturbed) incrementally. The workpiece predictor 120 may predict a maximum wafer intensity and a maximum contour delta for the mask design for each of the different perturbations.

[0030] The variation/perturbation is intended to mimic mask patterning process variability. Accordingly, analyzing the workpiece parameters for each of the different variations/perturbations enables the mask design adjuster 130 to approximate a worst possible workpiece impact that may be observed using masks having a range of different infidelities. As a result, in the sensitivity mode, the mask design adjuster 130 may vary the mask design to minimize the worst possible workpiece impact (e.g., as measured in maximum wafer intensity and maximum contour delta).

[0031] FIG. 3 is a simplified plan view of a portion 300 of a mask design for illustrating an example of the sensitivity mode, according to some embodiments.

Referring to FIGS. 1 and 3 together, the portion 300 illustrated in FIG. 3 is merely a conceptual portion 300 of a desired mask indicated by the mask design, as the mask design system 100 of FIG. 1 merely processes the mask design as data indicating the desired mask. Accordingly, although FIG. 3 is discussed in terms of the conceptual portion 300, it should be understood that, in contrast, the mask design system 100 performs functions that parallel those discussed with reference to FIG. 3 using the data of the mask design.

[0032] The portion 300 includes a feature 340 of the mask design, illustrated in solid lines. When the mask predictor 110 generates the mask parameters, a predicted feature 350 (illustrated in dashed lines) of the manufactured mask that corresponds to the feature 340 may be determined. The predicted feature 350 may deviate from the feature 340. For example, an end of the predicted feature 350 may extend past an end of the feature 340 by a length A. If the length A is larger than a predetermined tolerance defined in violations parameters, the mask design adjuster 130 may flag the feature 340 for analysis with the workpiece predictor 120 to determine an impact of the mask infidelity on a workpiece.

[0033] The workpiece predictor 120 may predict a workpiece feature corresponding to the predicted feature 350 of the mask, and provide workpiece parameters (e.g., a maximum wafer intensity and a maximum contour delta) indicating information regarding the workpiece feature to the mask design adjuster 130. The mask design adjuster 130 may determine whether it is believed that the workpiece will function as intended based on the predicted workpiece feature. If the mask design adjuster 130 determines that the workpiece feature will not function as intended (e.g., a catastrophic failure), the mask design adjuster 130 may adjust the mask design to compensate for the mask infidelity.

[0034] The mask design adjuster 130 may adjust the feature 340 of the mask design to one or more different variations. For example, FIG. 3 illustrates feature variations 342, 344, 346, and 348, illustrated with dotted lines. The mask predictor 110 may provide mask parameters responsive to each of these feature variations 342, 344, 346, 348, and the workpiece predictor 120 may provide workpiece parameters responsive to each of the different sets of mask parameters. Using these workpiece parameters, the mask design adjuster 130 may select one of the feature variation 342, 344, 346, 348, or the feature 340 that is predicted to result in a best corresponding workpiece feature. The mask design adjuster 130 may adjust

the mask design to reflect the selected one of the feature variations 342, 344, 346, 348 if the selected feature is not the feature 340 of the original design.

[0035] If, however, the mask design adjuster 130 determines that the workpiece feature will function as intended despite the mask infidelity, the mask design adjuster 130 may not adjust the mask design to compensate for the mask infidelity. The mask design adjuster 130 may use the mask predictor 110 to flag other mask infidelities, and the workpiece predictor 120 to analyze these mask infidelities on the workpiece according to the sensitivity mode, as discussed above. The mask design adjuster 130 may adjust the mask design accordingly, and provide a final mask design including the adjusted mask (if any adjustments are made; otherwise the final mask design may include the original mask design). The final mask design may be provided to a mask manufacturer to manufacture a mask using the final mask design.

[0036] Referring again to FIG. 1, the mask design system 100 has the flexibility to comprehend different OPC model wafer patterning failure metrics. The mask design system 100 also has the capability of making simultaneous measurements using different OPC models and process conditions. Mask layers often use multiple OPC model metrics to assess wafer patterning health. The mask design system 100 integrates the use of OPC and MEC models in a single module for assessing workpiece (e.g., wafer) patterning liabilities that result from mask infidelities. Accordingly, the application of the OPC model comes after the application of MEC model.

[0037] The mask design system 100 can be used to better utilize the mask area, creating an improved mask design to reduce workpiece variability and increase workpiece fidelity to a design target. Mask Rule Constraints (MRCs) can be optimized and/or made more complex to allow smaller mask features or even mask failures in regions where negligible workpiece impact is observed. MRCs can also be optimized and/or made more complex to require larger mask features in regions where mask variation has a big impact on the workpiece. By actively avoiding mask geometries that can have a large impact on the workpiece, the overall workpiece fidelity, and potentially, workpiece and mask yield, can be improved. Moreover, the mask design system 100 may not waste time and resources compensating for mask infidelities that have negligible impact on wafer patterning, thus speeding up the tapeout process and saving engineering and compute time.

[0038] FIG. 4 is a simplified flowchart illustrating a method 400 of designing a mask for manufacturing a workpiece. The method 400 includes providing 410 a preliminary mask design for producing a desired pattern on or in a semiconductor device by analyzing the desired pattern for the semiconductor device.

[0039] The method 400 also includes determining 420 manufacturing infidelities in at least one simulated mask that may occur while manufacturing a mask based on the preliminary mask design. In some embodiments, determining 420 manufacturing infidelities includes determining 420 manufacturing infidelities of a plurality of different simulated masks.

[0040] The method 400 further includes determining 430 pattern infidelities that may occur in the semiconductor device if manufactured with the at least one simulated mask. In some embodiments, determining 430 pattern infidelities includes analyzing determined maximum wafer intensity and determined contour delta. In some embodiments, determining 430 pattern infidelities includes estimating worst possible wafer impact. In some embodiments, determining 430 pattern infidelities includes only determining pattern infidelities that correspond to features of the mask design that are at or near mask manufacturing tolerances.

[0041] The method 400 also includes generating 440 a final mask design for producing the desired pattern on or in the semiconductor device by adjusting the preliminary mask design to compensate for the determined manufacturing infidelities and the determined pattern infidelities. In some embodiments, generating 440 a final mask design includes modifying the preliminary mask design such that the semiconductor device will be operable even if the estimated worst possible wafer impact is realized during manufacturing of the semiconductor device. In some embodiments, adjusting the preliminary mask design to compensate for the determined manufacturing infidelities and the determined pattern infidelities includes only adjusting portions of the preliminary mask design that correspond to pattern infidelities that are predicted to prevent the semiconductor device from functioning properly. In some embodiments, adjusting the preliminary mask design to compensate for the determined manufacturing infidelities and the determined pattern infidelities includes only adjusting portions of the preliminary mask design that correspond to mask infidelities that violate at least one predetermined tolerance parameter.

[0042] In some embodiments, the determining 420 of the manufacturing infidelities and the determining 430 of the pattern infidelities may be repeated to generate at least one intervening mask design. In such embodiments, the preliminary mask design may be adjusted to compensate for the determined manufacturing infidelities and the determined pattern infidelities by incrementally adjusting the at least one intervening mask design to generate the final mask design. In some embodiments, the repeating of the determining 430 of the pattern infidelities may include determining the pattern infidelities corresponding to each of the at least one intervening mask design.

[0043] In addition, the method 400 includes manufacturing 450 a mask using the final mask design.

[0044] FIG. 5 is a simplified flowchart illustrating a method 500 of manufacturing a semiconductor device. The method 500 includes generating 510 preliminary mask design data indicating a preliminary mask design from desired wafer pattern data indicating a desired wafer pattern of the semiconductor device. In some embodiments, generating 510 preliminary mask design data includes automatically generating the preliminary mask design data from the desired wafer pattern data using a software program. The method 500 also includes storing 520 the preliminary mask design data on a data storage device.

[0045] The method 500 also includes predicting 530 mask infidelities relative to the preliminary mask design that are predicted to result from manufacturing the mask using the preliminary mask design to generate mask infidelity data indicating the mask infidelities. In some embodiments, predicting 530 mask infidelities comprises only predicting mask infidelities corresponding to a portion of features of the preliminary mask design. By way of non-limiting example, only the mask infidelities corresponding to features of the preliminary mask design that are at or near mask manufacturing tolerances may be predicted. In some embodiments, all of the mask infidelities may be predicted.

[0046] The method 500 further includes predicting 540 wafer infidelities relative to a desired wafer design to generate wafer infidelity data indicating the wafer infidelities responsive to the predicted mask infidelities. In some embodiments, predicting 540 wafer infidelities may only be performed for wafer features corresponding to a subset of the mask infidelities. By way of non-limiting example,

only wafer infidelities corresponding to mask infidelities that violate predetermined tolerances may be predicted.

[0047] The method 500 also includes identifying 550 a portion of the wafer infidelities and the mask infidelities for which to compensate the preliminary mask design. In some embodiments, the portion of the wafer infidelities may include all of the predicted wafer infidelities. In some embodiments, the portion of wafer infidelities may include only those of the wafer infidelities that would prevent the semiconductor device from functioning properly (e.g., that would cause catastrophic failures), or that would otherwise violate design standards.

[0048] The method 500 further includes adjusting 560 the preliminary mask design to compensate for the identified portion of the mask and wafer infidelities. The method 500 also includes manufacturing 570 a manufactured mask based on the adjusted preliminary design. The method 500 further includes manufacturing 580 the semiconductor device using the manufactured mask.

[0049] FIG. 6 is a simplified block diagram of a computing system 600, according to some embodiments. The computing system 600 includes at least one data storage device 610 (also referred to herein simply as “storage” 610) operably coupled to at least one processor 620 (also referred to herein simply as “processor” 620). The storage 610 includes at least one database 612 (also referred to herein simply as “database” 612) and computer-readable instructions 614 stored thereon. The database 612 is configured to store data that is used by the mask design system 100 of FIG. 1, and/or data identified in the methods 400, 500 of FIGS. 5 and 6. For example, the database 612 may be configured to store data indicating desired workpiece designs, desired wafer designs, mask designs (e.g., original mask designs, adjusted mask designs, final mask designs, preliminary mask designs, intervening mask designs, etc.), predicted mask parameters (e.g., mask infidelities, simulated masks, etc.), predicted workpiece parameters (e.g., simulated workpieces, simulated wafers, predicted workpiece features, maximum wafer intensities, contour deltas, etc.), other data indicating parameters discussed above with reference to FIGS. 1-5, or combinations thereof.

[0050] The computer-readable instructions 614 are configured to instruct the processor 620 to perform at least a portion of the operations disclosed herein. By way of non-limiting example, the computer-readable instructions 614 may be configured to instruct the processor 620 to perform at least a portion of the

operations discussed herein with reference to the mask predictor 110, the workpiece predictor 120, the mask design adjuster 130, and the mask design system 100 in general. Also by way of non-limiting example, the computer-readable instructions 614 may be configured to instruct the processor 620 to perform at least a portion of the operations discussed herein with reference to the impact mode (FIG. 2), the sensitivity mode (FIG. 3), the method 400 of FIG. 4, the method 500 of FIG. 5, the Examples enumerated in the Examples section below, or combinations thereof.

[0051] The storage 610 may include any device or devices configured to store information. By way of non-limiting example, the storage 610 may include volatile data storage devices (e.g., random access memory (RAM)), non-volatile data storage devices (e.g., Flash memory, a hard drive, electrically programmable read only memory (EPROM), optical storage media, memory cards, etc.), or combinations thereof.

[0052] The processor 620 is configured to execute the computer-readable instructions 614 stored by the storage 610. The processor 620 may include any device capable of reading and executing computer-readable instructions. By way of non-limiting example, the processor 620 may include any one or more of a central processing unit (CPU), a microcontroller, a programmable logic controller (PLC), other programmable devices, or combinations thereof.

[0053] In some embodiments, the computing system 600 may also include hardware elements 630 configured to perform at least a portion of the operations disclosed herein. By way of non-limiting example, the hardware elements 630 may include any one or more of a system on chip (SOC), an integrated circuit, a logic circuit, an array of logic circuit elements programmable to perform operations disclosed herein (e.g., a field programmable gate array (FPGA)), other hardware elements, or combinations thereof.

[0054] It will be apparent to those of ordinary skill in the art that any functionality that can be programmed into a storage device for instructing a processor to perform operational acts may also be hardwired into a logic circuit, programmed into an FPGA, or otherwise implemented using discrete or integrated circuit components to accomplish the same or similar operational acts. Accordingly, the present disclosure contemplates that some or all of the functionality disclosed herein may be executed by the processor 620 operably coupled to the storage 610, by the hardware elements 630, or by a combination thereof.

Examples

[0055] The following is a list of example embodiments that fall within the scope of the disclosure. In order to avoid complexity in providing the disclosure, not all of the examples listed below are separately and explicitly disclosed as having been contemplated herein as combinable with all of the others of the examples listed below and other embodiments disclosed hereinabove. Unless one of ordinary skill in the art would understand that these examples listed below, and the above disclosed embodiments, are not combinable, it is contemplated within the scope of the disclosure that such examples and embodiments are combinable.

[0056] Example 1: A computer-readable storage medium having computer-readable instructions stored thereon, the computer-readable instructions configured to instruct one or more processors to: predict possible infidelities that may occur in a manufactured mask when manufacturing the manufactured mask responsive to a mask design, the mask design including data indicating desired parameters of the manufactured mask; predict possible infidelities that may occur in a workpiece manufactured using the manufactured mask responsive to the mask design and the predicted possible infidelities that may occur in the manufactured mask; determine a portion of the predicted possible infidelities in the workpiece that would result in failure of the workpiece to operate as intended; and produce a compensated mask design by adjusting features of the mask design to compensate for the determined portion of the predicted possible infidelities in the workpiece that would result in failure of the workpiece.

[0057] Example 2: The computer-readable storage medium of Example 1, wherein the computer-readable instructions are further configured to instruct the one or more processors to generate the mask design responsive to a workpiece design, the workpiece design including data indicating a desired design of the workpiece and data indicating Mask Rule Constraints (MRCs) for manufacturing the manufactured mask.

[0058] Example 3: The computer-readable storage medium of Example 2, wherein a portion of the computer-readable instructions configured to instruct the one or more processors to generate the mask design responsive to the workpiece design includes an Optical Proximity Correction (OPC) software program.

[0059] Example 4: The computer-readable storage medium according to any one of Examples 1-3, wherein the computer-readable instructions are configured to

instruct the one or more processors to predict the possible infidelities that may occur in the manufactured mask by predicting a range of dimensional error of at least one feature of the manufactured mask.

[0060] Example 5: The computer-readable storage medium of Example 4, wherein the computer-readable instructions are configured to instruct the one or more processors to predict the possible infidelities that may occur in the workpiece manufactured using the manufactured mask by predicting the possible infidelities that may occur in the workpiece responsive to each of a plurality of different errors within the range of dimensional error of the at least one feature of the manufactured mask.

[0061] Example 6: The computer-readable storage medium according to any one of Examples 1-5, wherein the computer-readable instructions are configured to instruct the one or more processors to predict the possible infidelities that may occur in the workpiece by analyzing a predicted maximum wafer intensity and a predicted contour delta of desired features of the workpiece.

[0062] Example 7: The computer-readable storage medium according to any one of Examples 1-6, wherein the computer-readable instructions are configured to instruct the one or more processors to determine the portion of the predicted possible infidelities in the workpiece that would result in failure of the workpiece to operate as intended by selecting portions of the workpiece that correspond to features of the mask design that are at or near a critical dimension delta of the manufactured mask.

[0063] Example 8: A method of designing a mask for use in semiconductor processing, the method comprising: providing a preliminary mask design for producing a desired pattern on or in a semiconductor device by analyzing the desired pattern for the semiconductor device; determining manufacturing infidelities of at least one simulated mask that may occur while manufacturing a mask based on the preliminary mask design; determining pattern infidelities that may occur in the semiconductor device responsive to the manufacturing infidelities; and generating a final mask design for producing the desired pattern on or in the semiconductor device by adjusting the preliminary mask design to compensate for the determined manufacturing infidelities and the determined pattern infidelities.

[0064] Example 9: The method of Example 8, further comprising manufacturing a mask using the final mask design.

[0065] Example 10: The method according to any one of Examples 8 and 9, wherein determining manufacturing infidelities of at least one simulated mask comprises determining manufacturing infidelities of a plurality of different simulated masks.

[0066] Example 11: The method according to any one of Examples 8-10, further comprising repeating the determining of the manufacturing infidelities and the determining of the pattern infidelities to generate at least one intervening mask design, wherein adjusting the preliminary mask design to compensate for the determined manufacturing infidelities and the determined pattern infidelities comprises incrementally adjusting the at least one intervening mask design to generate the final mask design.

[0067] Example 12: The method of Example 11, wherein repeating the determining of the pattern infidelities comprises determining the pattern infidelities corresponding to each of the at least one intervening mask design.

[0068] Example 13: The method according to any one of Examples 8-12, wherein determining pattern infidelities that may occur in the semiconductor device comprises analyzing determined maximum wafer intensity and determined contour delta.

[0069] Example 14: The method according to any one of Examples 8-13, wherein determining pattern infidelities that may occur in the semiconductor device comprises estimating worst possible wafer impact.

[0070] Example 15: The method of Example 14, wherein generating a final mask design comprises modifying the preliminary mask design such that the semiconductor device will be operable even if the estimated worst possible wafer impact is realized during manufacturing of the semiconductor device.

[0071] Example 16: The method according to any one of Examples 8-15, wherein adjusting the preliminary mask design to compensate for the determined manufacturing infidelities and the determined pattern infidelities comprises only adjusting portions of the preliminary mask design that correspond to pattern infidelities that are predicted to prevent the semiconductor device from functioning properly.

[0072] Example 17: The method according to any one of Examples 8-16, wherein adjusting the preliminary mask design to compensate for the determined manufacturing infidelities and the determined pattern infidelities comprises only

adjusting portions of the preliminary mask design that correspond to mask infidelities that violate at least one predetermined tolerance parameter.

[0073] Example 18: The method according to any one of Examples 8-17, wherein determining pattern infidelities that may occur in the semiconductor device responsive to the manufacturing infidelities comprises only determining the pattern infidelities that correspond to features of the mask design that are at or near mask manufacturing tolerances.

[0074] Example 19: A method of manufacturing a semiconductor device, the method comprising: storing preliminary mask design data on a data storage device, the preliminary mask design data indicating a preliminary design for a mask; predicting mask infidelities relative to the preliminary mask design that are predicted to result from manufacturing the mask using the preliminary mask design to generate mask infidelity data indicating the mask infidelities; predicting wafer infidelities relative to a desired wafer design to generate wafer infidelity data indicating the wafer infidelities; identifying a portion of the wafer infidelities and the mask infidelities for which to compensate the preliminary mask design; adjusting the preliminary mask design to compensate for the identified portion of the wafer infidelities; and manufacturing the semiconductor device using a manufactured mask manufactured based on the adjusted preliminary mask design.

[0075] Example 20: The method of Example 19, further comprising using a software program to automatically generate the preliminary mask design data from desired wafer pattern data indicating the desired wafer design.

[0076] Example 21: The method according to any one of Examples 19 and 20, further comprising manufacturing the manufactured mask based on the adjusted preliminary mask design.

[0077] Example 22: A method of generating a compensated mask design, the method comprising: predicting possible infidelities that may occur in a manufactured mask when manufacturing the manufactured mask responsive to a mask design, the mask design including data indicating desired parameters of the manufactured mask; predicting possible infidelities that may occur in a workpiece manufactured using the manufactured mask responsive to the mask design and the predicted possible infidelities that may occur in the manufactured mask; determining a portion of the predicted possible infidelities in the workpiece that would result in failure of the workpiece to operate as intended; and producing a compensated mask design by

adjusting features of the mask design to compensate for the determined portion of the predicted possible infidelities in the workpiece that would result in failure of the workpiece.

[0078] Example 23: The method of Example 22, wherein the computer-readable instructions are further configured to instruct the one or more processors to generate the mask design responsive to a workpiece design, the workpiece design including data indicating a desired design of the workpiece and data indicating Mask Rule Constraints (MRCs) for manufacturing the manufactured mask.

[0079] Example 24: The method of Example 23, wherein a portion of the computer-readable instructions configured to instruct the one or more processors to generate the mask design responsive to the workpiece design includes an Optical Proximity Correction (OPC) software program.

[0080] Example 25: The method according to any one of Examples 22-24, wherein the computer-readable instructions are configured to instruct the one or more processors to predict the possible infidelities that may occur in the manufactured mask by predicting a range of dimensional error of at least one feature of the manufactured mask.

[0081] Example 26: The method of Example 25, wherein the computer-readable instructions are configured to instruct the one or more processors to predict the possible infidelities that may occur in the workpiece manufactured using the manufactured mask by predicting the possible infidelities that may occur in the workpiece responsive to each of a plurality of different errors within the range of dimensional error of the at least one feature of the manufactured mask.

[0082] Example 27: The method according to any one of Examples 22-26, wherein the computer-readable instructions are configured to instruct the one or more processors to predict the possible infidelities that may occur in the workpiece by analyzing a predicted maximum wafer intensity and a predicted contour delta of desired features of the workpiece.

[0083] Example 28: The method according to any one of Examples 22-27, wherein the computer-readable instructions are configured to instruct the one or more processors to determine the portion of the predicted possible infidelities in the workpiece that would result in failure of the workpiece to operate as intended by selecting portions of the workpiece that correspond to features of the mask design that are at or near a critical dimension delta of the manufactured mask.

[0084] Example 29: At least one computer-readable storage medium including computer-readable instructions stored therein, the computer-readable instructions configured to instruct at least one processor to: provide a preliminary mask design for producing a desired pattern on or in a semiconductor device by analyzing the desired pattern for the semiconductor device; determine manufacturing infidelities of at least one simulated mask that may occur while manufacturing a mask based on the preliminary mask design; determine pattern infidelities that may occur in the semiconductor device responsive to the manufacturing infidelities; and generate a final mask design for producing the desired pattern on or in the semiconductor device by adjusting the preliminary mask design to compensate for the determined manufacturing infidelities and the determined pattern infidelities.

[0085] Example 30: The at least one computer-readable storage medium of Example 29, wherein the computer-readable instructions are further configured to instruct the at least one processor to cause a mask to be manufactured using the final mask design.

[0086] Example 31: The at least one computer-readable storage medium according to any one of Examples 29 and 30, wherein the computer-readable instructions are further configured to instruct the at least one processor to determine manufacturing infidelities of a plurality of different simulated masks.

[0087] Example 32: The at least one computer-readable storage medium according to any one of Examples 29-31, wherein the computer-readable instructions are further configured to instruct the at least one processor to: repeat the determining of the manufacturing infidelities and the determining of the pattern infidelities to generate at least one intervening mask design; and incrementally adjust the at least one intervening mask design to generate the final mask design.

[0088] Example 33: The at least one computer-readable storage medium of Example 32, wherein the computer-readable instructions are further configured to instruct the at least one processor to determine the pattern infidelities corresponding to each of the at least one intervening mask design.

[0089] Example 34: The at least one computer-readable storage medium according to any one of Examples 29-33, wherein the computer-readable instructions are further configured to instruct the at least one processor to analyze determined maximum wafer intensity and determined contour delta.

[0090] Example 35: The at least one computer-readable storage medium according to any one of Examples 29-34, wherein the computer-readable instructions are further configured to instruct the at least one processor to estimate worst possible wafer impact.

[0091] Example 36: The at least one computer-readable storage medium of Example 35, wherein the computer-readable instructions are further configured to instruct the at least one processor to modify the preliminary mask design such that the semiconductor device will be operable even if the estimated worst possible wafer impact is realized during manufacturing of the semiconductor device.

[0092] Example 37: The at least one computer-readable storage medium according to any one of Examples 29-36, wherein the computer-readable instructions are further configured to instruct the at least one processor to adjust only portions of the preliminary mask design that correspond to pattern infidelities that are predicted to prevent the semiconductor device from functioning properly.

[0093] Example 38: The at least one computer-readable storage medium according to any one of Examples 29-37, wherein the computer-readable instructions are further configured to instruct the at least one processor to adjust only portions of the preliminary mask design that correspond to mask infidelities that violate at least one predetermined tolerance parameter.

[0094] Example 39: The at least one computer-readable storage medium according to any one of Examples 29-38, wherein the computer-readable instructions are further configured to instruct the at least one processor to determine only the pattern infidelities that correspond to features of the mask design that are at or near mask manufacturing tolerances.

[0095] Example 40: A semiconductor device comprising features produced, at least in part, by: storing preliminary mask design data on a data storage device, the preliminary mask design data indicating a preliminary design for a mask; predicting mask infidelities relative to the preliminary mask design that are predicted to result from manufacturing the mask using the preliminary mask design to generate mask infidelity data indicating the mask infidelities; predicting wafer infidelities relative to a desired wafer design to generate wafer infidelity data indicating the wafer infidelities; identifying a portion of the wafer infidelities and the mask infidelities for which to compensate the preliminary mask design; adjusting the preliminary mask design to compensate for the identified portion of the wafer infidelities; and manufacturing the

semiconductor device using a manufactured mask manufactured based on the adjusted preliminary mask design.

[0096] Example 41: The semiconductor device of Example 40, wherein the features are further produced by using a software program to automatically generate the preliminary mask design data from desired wafer pattern data indicating the desired wafer design.

[0097] Example 42: The semiconductor device according to any one of Examples 40 and 41, wherein the features are further produced by manufacturing the manufactured mask based on the adjusted preliminary mask design.

[0098] Example 43: A non-transitory computer-readable storage medium comprising computer-readable instructions stored thereon, the computer-readable instructions configured to instruct a processor to perform at least a portion of the method according to any one of Examples 8-28.

[0099] Example 44: A means for performing at least a portion of the method according to any one of Examples 8-28.

[00100] It will be apparent to those having skill in the art that many changes may be made to the details of the above-described embodiments without departing from the underlying principles of the invention. The scope of the present invention should, therefore, be determined only by the following claims.

Claims

1. A computer-readable storage medium having computer-readable instructions stored thereon, the computer-readable instructions configured to instruct one or more processors to:

predict possible infidelities that may occur in a manufactured mask when manufacturing the manufactured mask responsive to a mask design, the mask design including data indicating desired parameters of the manufactured mask;

predict possible infidelities that may occur in a workpiece manufactured using the manufactured mask responsive to the mask design and the predicted possible infidelities that may occur in the manufactured mask;

determine a portion of the predicted possible infidelities in the workpiece that would result in failure of the workpiece to operate as intended; and

produce a compensated mask design by adjusting features of the mask design to compensate for the determined portion of the predicted possible infidelities in the workpiece that would result in failure of the workpiece.

2. The computer-readable storage medium of claim 1, wherein the computer-readable instructions are further configured to instruct the one or more processors to generate the mask design responsive to a workpiece design, the workpiece design including data indicating a desired design of the workpiece and data indicating Mask Rule Constraints (MRCs) for manufacturing the manufactured mask.

3. The computer-readable storage medium of claim 2, wherein a portion of the computer-readable instructions configured to instruct the one or more processors to generate the mask design responsive to the workpiece design includes an Optical Proximity Correction (OPC) software program.

4. The computer-readable storage medium of claim 1, wherein the computer-readable instructions are configured to instruct the one or more processors to predict the possible infidelities that may occur in the manufactured mask by predicting a range of dimensional error of at least one feature of the manufactured mask.

5. The computer-readable storage medium of claim 4, wherein the computer-readable instructions are configured to instruct the one or more processors to predict the possible infidelities that may occur in the workpiece manufactured using the manufactured mask by predicting the possible infidelities that may occur in

the workpiece responsive to each of a plurality of different errors within the range of dimensional error of the at least one feature of the manufactured mask.

6. The computer-readable storage medium according to any one of claims 1-5, wherein the computer-readable instructions are configured to instruct the one or more processors to predict the possible infidelities that may occur in the workpiece by analyzing a predicted maximum wafer intensity and a predicted contour delta of desired features of the workpiece.

7. The computer-readable storage medium according to any one of claims 1-5, wherein the computer-readable instructions are configured to instruct the one or more processors to determine the portion of the predicted possible infidelities in the workpiece that would result in failure of the workpiece to operate as intended by selecting portions of the workpiece that correspond to features of the mask design that are at or near a critical dimension delta of the manufactured mask.

8. A method of designing a mask for use in semiconductor processing, the method comprising:

providing a preliminary mask design for producing a desired pattern on or in a semiconductor device by analyzing the desired pattern for the semiconductor device;

determining manufacturing infidelities of at least one simulated mask that may occur while manufacturing a mask based on the preliminary mask design;

determining pattern infidelities that may occur in the semiconductor device responsive to the manufacturing infidelities; and

generating a final mask design for producing the desired pattern on or in the semiconductor device by adjusting the preliminary mask design to compensate for the determined manufacturing infidelities and the determined pattern infidelities.

9. The method of claim 8, further comprising manufacturing a mask using the final mask design.

10. The method of claim 8, wherein determining manufacturing infidelities of at least one simulated mask comprises determining manufacturing infidelities of a plurality of different simulated masks.

11. The method of claim 8, further comprising repeating the determining of the manufacturing infidelities and the determining of the pattern infidelities to generate at least one intervening mask design, wherein adjusting the preliminary mask design to compensate for the determined manufacturing infidelities and the

determined pattern infidelities comprises incrementally adjusting the at least one intervening mask design to generate the final mask design.

12. The method of claim 11, wherein repeating the determining of the pattern infidelities comprises determining the pattern infidelities corresponding to each of the at least one intervening mask design.

13. The method of claim 8, wherein determining pattern infidelities that may occur in the semiconductor device comprises analyzing determined maximum wafer intensity and determined contour delta.

14. The method of claim 8, wherein determining pattern infidelities that may occur in the semiconductor device comprises estimating worst possible wafer impact.

15. The method of claim 14, wherein generating a final mask design comprises modifying the preliminary mask design such that the semiconductor device will be operable even if the estimated worst possible wafer impact is realized during manufacturing of the semiconductor device.

16. The method of claim 8, wherein adjusting the preliminary mask design to compensate for the determined manufacturing infidelities and the determined pattern infidelities comprises only adjusting portions of the preliminary mask design that correspond to pattern infidelities that are predicted to prevent the semiconductor device from functioning properly.

17. The method of claim 8, wherein adjusting the preliminary mask design to compensate for the determined manufacturing infidelities and the determined pattern infidelities comprises only adjusting portions of the preliminary mask design that correspond to mask infidelities that violate at least one predetermined tolerance parameter.

18. The method of claim 8, wherein determining pattern infidelities that may occur in the semiconductor device responsive to the manufacturing infidelities comprises only determining the pattern infidelities that correspond to features of the mask design that are at or near mask manufacturing tolerances.

19. A method of manufacturing a semiconductor device, the method comprising:

storing preliminary mask design data on a data storage device, the preliminary mask design data indicating a preliminary design for a mask;

predicting mask infidelities relative to the preliminary mask design that are predicted to result from manufacturing the mask using the preliminary mask design to generate mask infidelity data indicating the mask infidelities;

predicting wafer infidelities relative to a desired wafer design to generate wafer infidelity data indicating the wafer infidelities;

identifying a portion of the wafer infidelities and the mask infidelities for which to compensate the preliminary mask design;

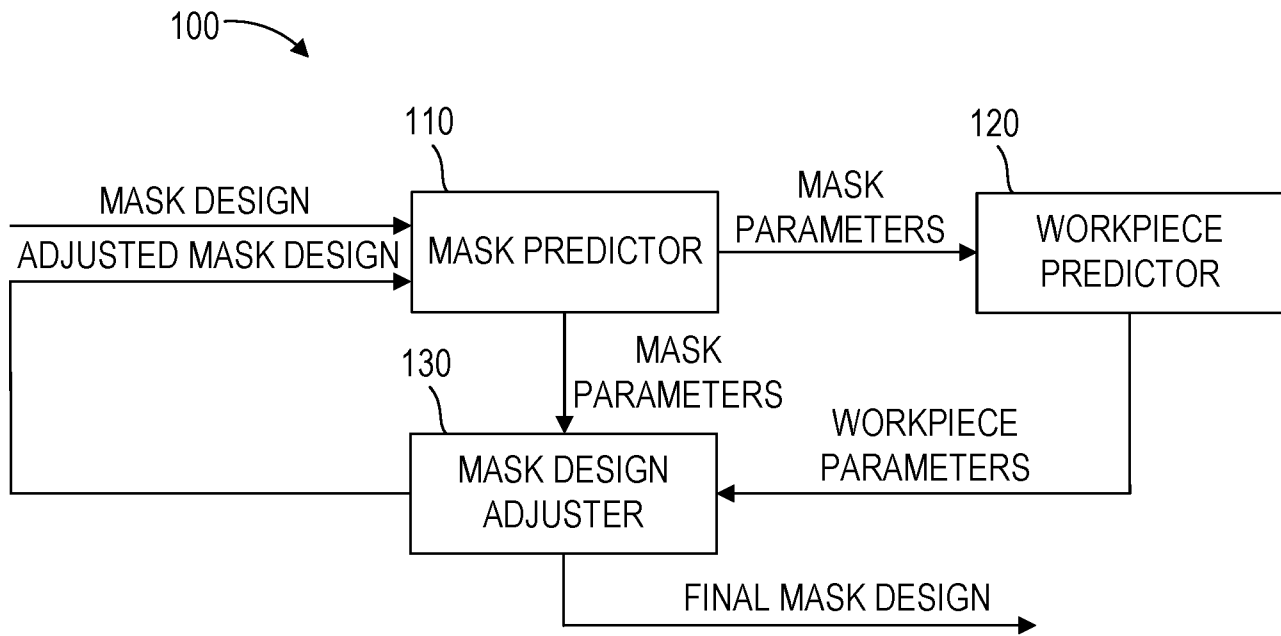
adjusting the preliminary mask design to compensate for the identified portion of the wafer infidelities; and

manufacturing the semiconductor device using a manufactured mask manufactured based on the adjusted preliminary mask design.

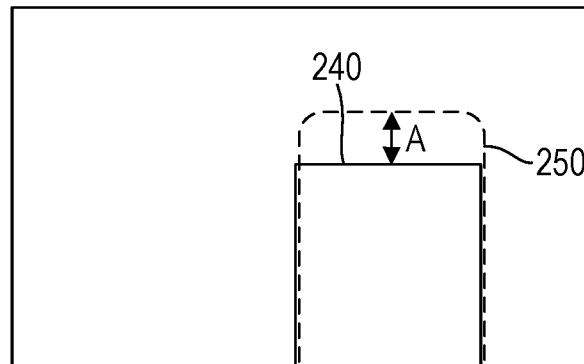
20. The method of claim 19, further comprising using a software program to automatically generate the preliminary mask design data from desired wafer pattern data indicating the desired wafer design.

21. The method of claim 19, further comprising manufacturing the manufactured mask based on the adjusted preliminary mask design.

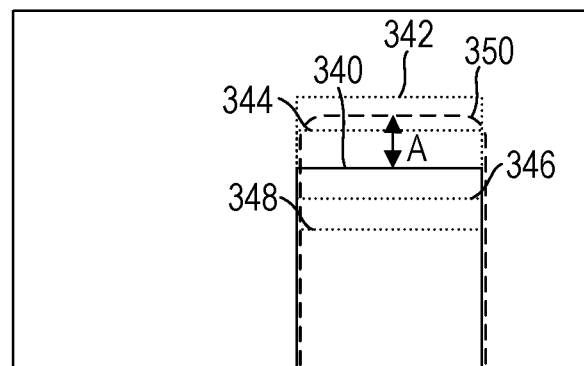
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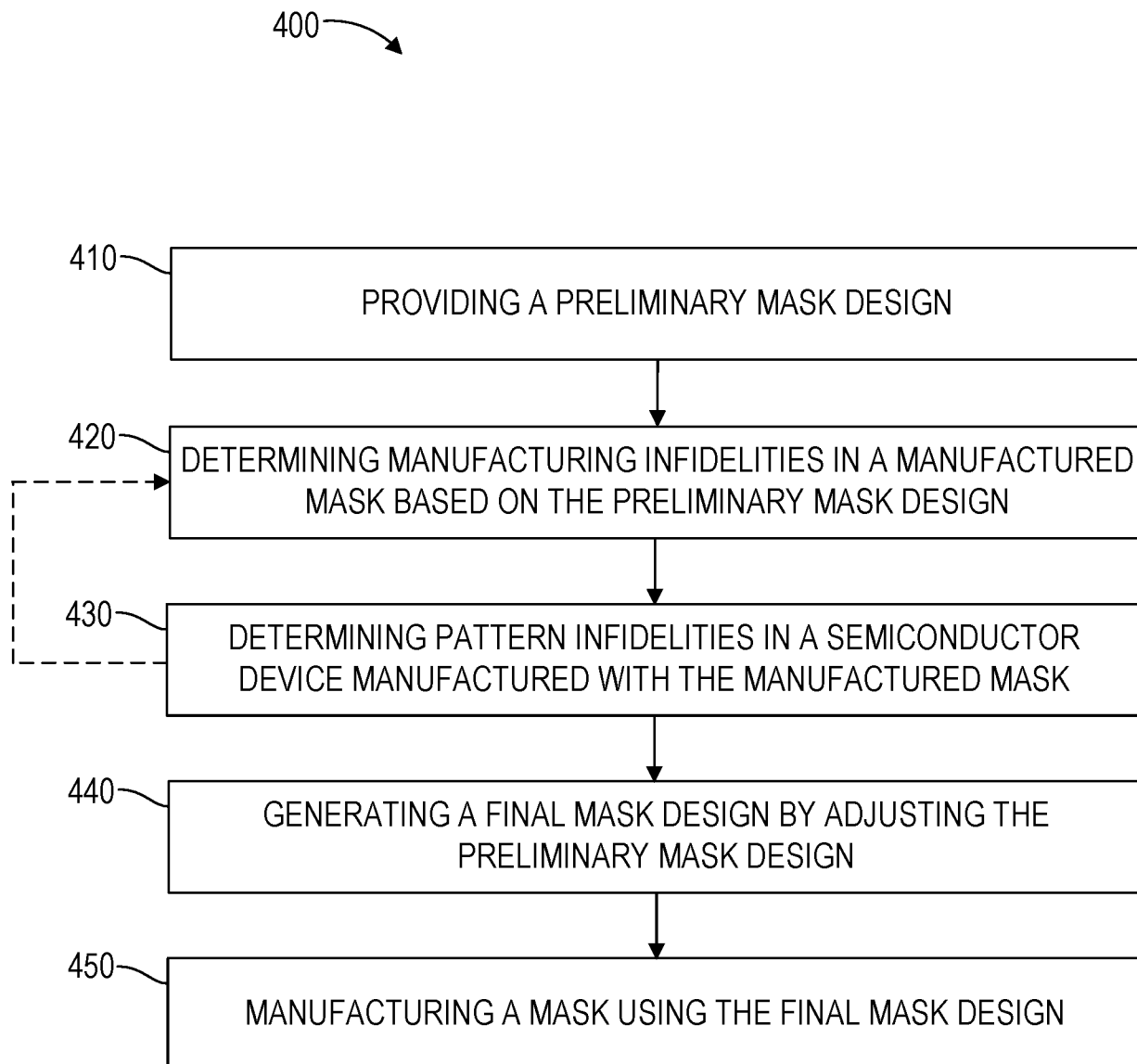
**FIG. 1**

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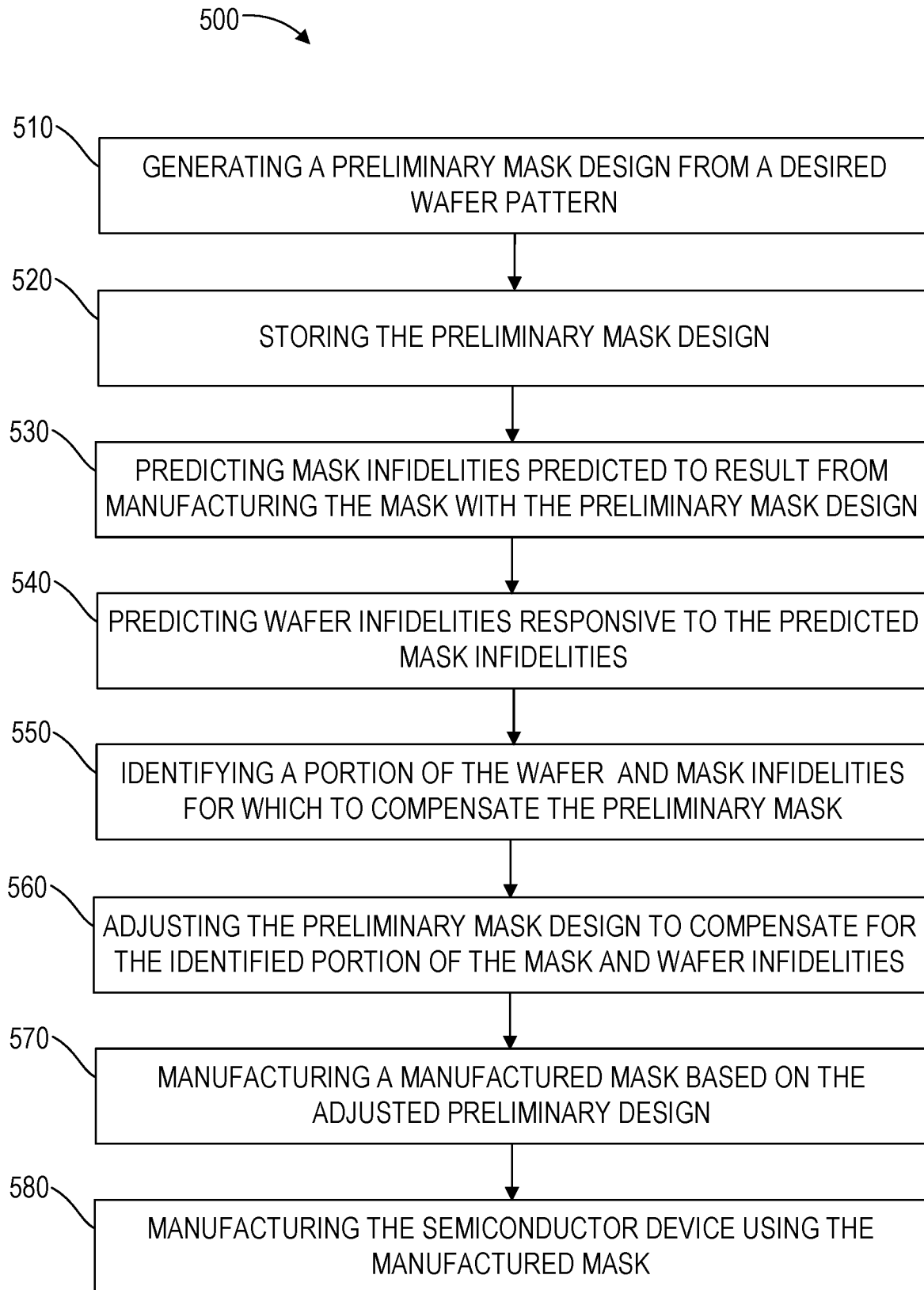
**FIG. 2**

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**FIG. 3**

**FIG. 4**

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**FIG. 5**

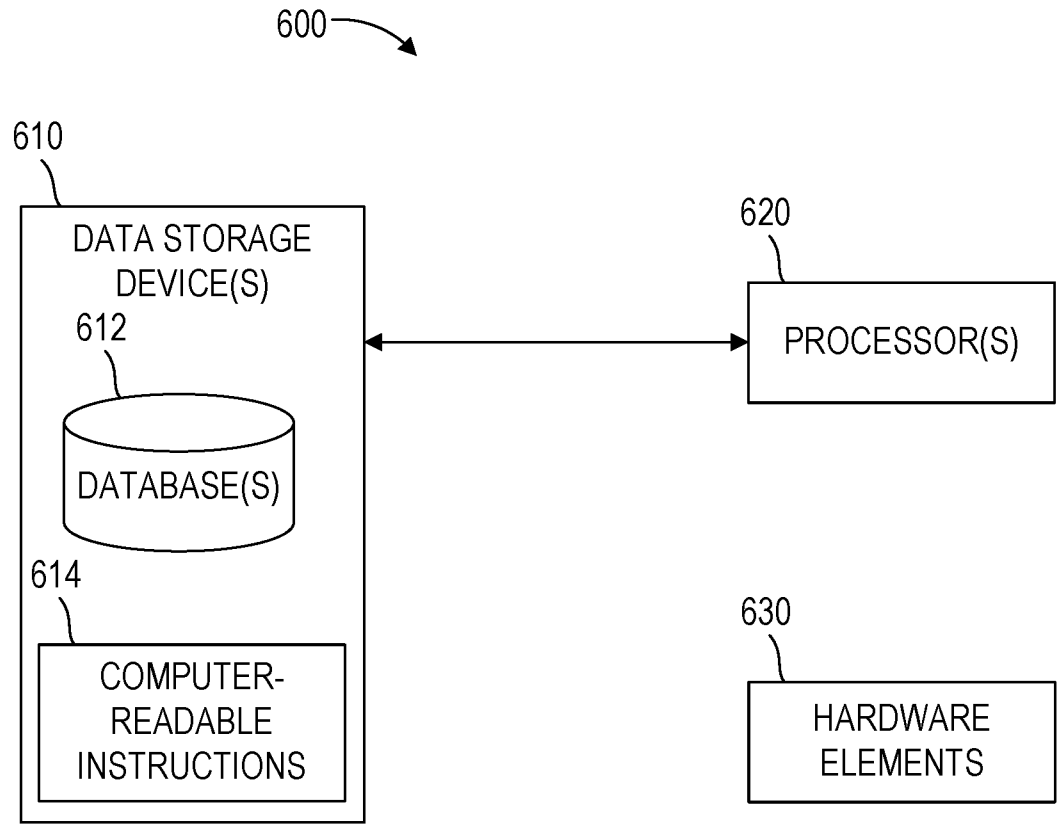


FIG. 6

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2016/069103

A. CLASSIFICATION OF SUBJECT MATTER G03F 1/36(2012.01)i, G03F 1/72(2012.01)i, G03F 1/70(2012.01)i, G03F 7/20(2006.01)i		
According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED		
Minimum documentation searched (classification system followed by classification symbols) G03F 1/36; G06F 17/50; G03F 1/00; G03F 1/14; G06F 9/45; G03F 1/72; G03F 1/70; G03F 7/20		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched Korean utility models and applications for utility models Japanese utility models and applications for utility models		
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used) eKOMPASS(KIPO internal) & keywords: computer-readable storage medium, computer-readable instructions, processors, possible infidelities, manufactured mask, mask design, desired parameters, workpiece, adjust, compensate, semiconductor device		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 9292627 B2 (CADENCE DESIGN SYSTEMS, INC.) 22 March 2016 See abstract; column 4, lines 35-55; and claims 1, 13.	1-21
A	US 2002-0133801 A1 (GRANIK, Y. et al.) 19 September 2002 See claims 1, 5, 8, 12, 15, 20.	1-21
A	EP 1290496 B1 (ADVANCED MICRO DEVICES INC.) 10 December 2003 See claims 1, 8, 10.	1-21
A	US 2008-0010628 A1 (JUNG, S.-G. et al.) 10 January 2008 See claims 1, 9, 17.	1-21
A	US 2004-0225488 A1 (WANG, W.-C. et al.) 11 November 2004 See claims 1, 6, 12, 18.	1-21
☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.		
* Special categories of cited documents: "A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier application or patent but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art "&" document member of the same patent family	
Date of the actual completion of the international search 25 September 2017 (25.09.2017)	Date of mailing of the international search report 25 September 2017 (25.09.2017)	
Name and mailing address of the ISA/KR  International Application Division Korean Intellectual Property Office 189 Cheongsu-ro, Seo-gu, Daejeon, 35208, Republic of Korea Facsimile No. +82-42-481-8578	Authorized officer LEE, Ki Cheul  Telephone No. +82-42-481-3353	

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

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