United States Patent

Starr et al.

[15] **3,670,269**

[45] **June 13, 1972**

[54] AUTOMATIC TRANSVERSAL EQUALIZER

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[21] Appl. No.: **87,546**

[30] **Foreign Application Priority Data**

April 21, 1970 Great Britain 19,039/70

[52] **U.S. Cl.** ..... **333/18**, 325/65, 333/28 R

[51] **Int. Cl.** **H04b 3/04**

[58] **Field of Search** ..... 333/18, 28, 70 T, 16; 179/1 P; 325/42, 65

[56] **References Cited**

UNITED STATES PATENTS

3,011,135	11/1961	Stump et al.	333/18 X
3,017,508	1/1962	Kious	333/18 X
3,292,116	12/1966	Walker et al.	333/18
3,292,110	12/1966	Becker et al.	333/18

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[57] **ABSTRACT**

An equalizing circuit, intended to be inserted between the transmission link and the receiver of an electrical information transmission system, the equalizer being arranged to have, within a preselected bandwidth of audio frequencies, an amplitude frequency response in the form of a family of similar curves, the equalizer including comparison means which is responsive to the difference between the outputs of the equalizer at two different frequencies of which at least one is within the said bandwidth to thereby automatically select a predetermined one of the said curves.

10 Claims, 13 Drawing Figures

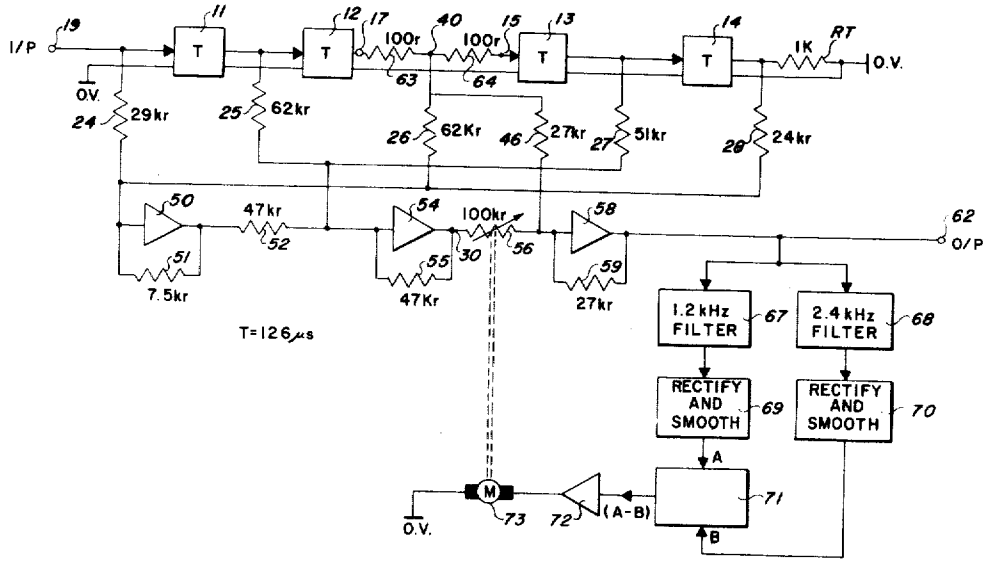

FIG. 1

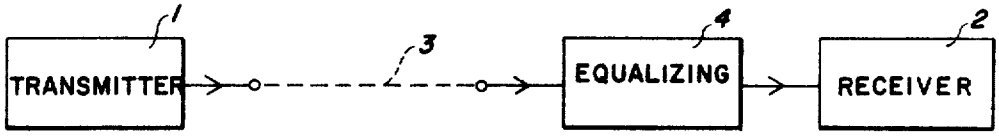

FIG. 3

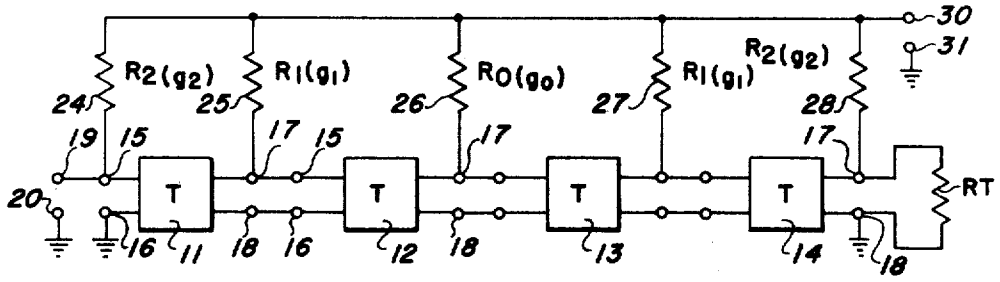

FIG. 4

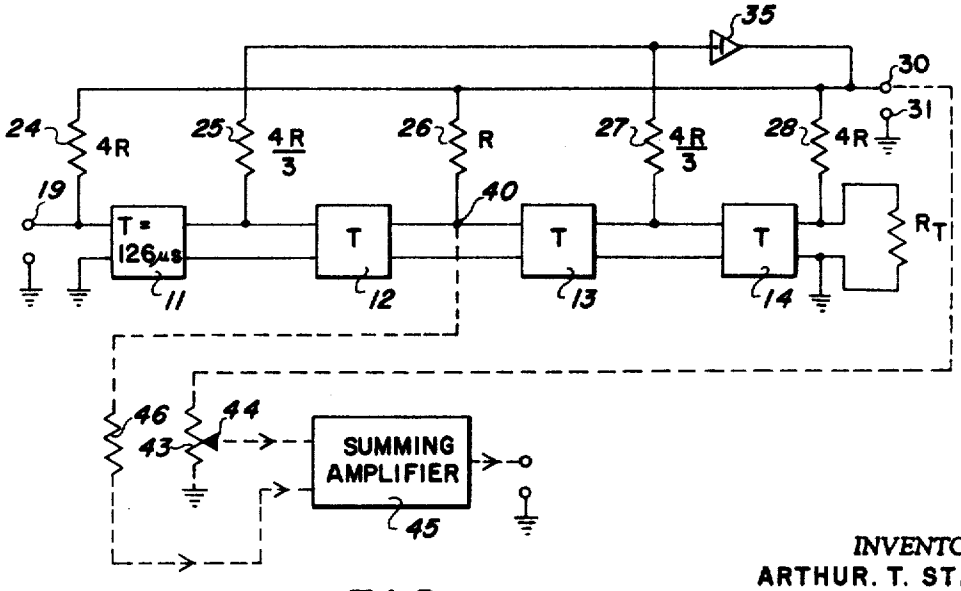

FIG. 6

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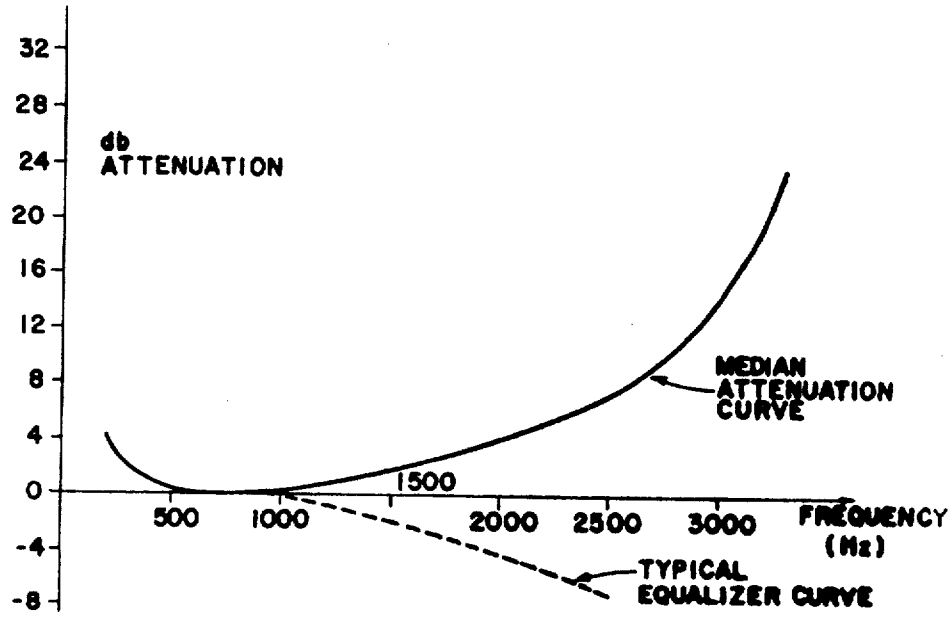

32
28
24
20
16
12
8
4
0
-4
-8
db
ATTENUATION
MEDIAN
ATTENUATION
CURVE
1500
500
1000
2000
2500
3000
FREQUENCY
(Hz)
TYPICAL
EQUALIZER CURVE

FIG. 2

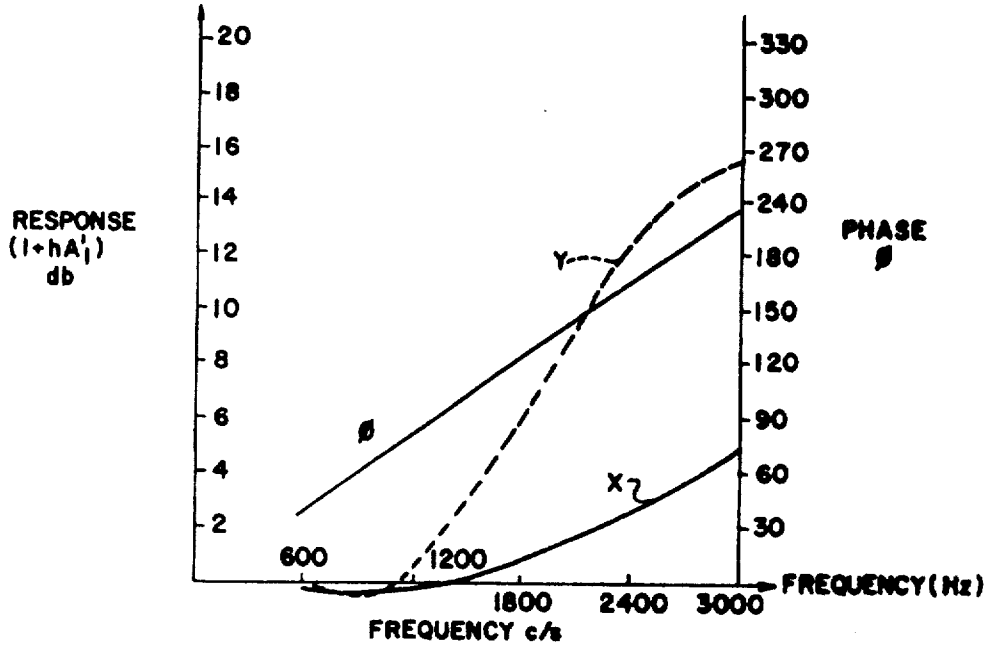

RESPONSE
(1+hA'1)
db
20
18
16
14
12
10
8
6
4
2
330
300
270
240
180
150
120
90
60
30
PHASE
Y
X
600
1200
1800
2400
3000
FREQUENCY c/s
FREQUENCY(Hz)

FIG. 7

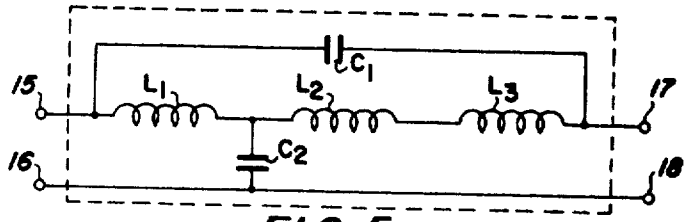

C1
L1
L2
L3
15
17
16
18
C2

FIG. 5

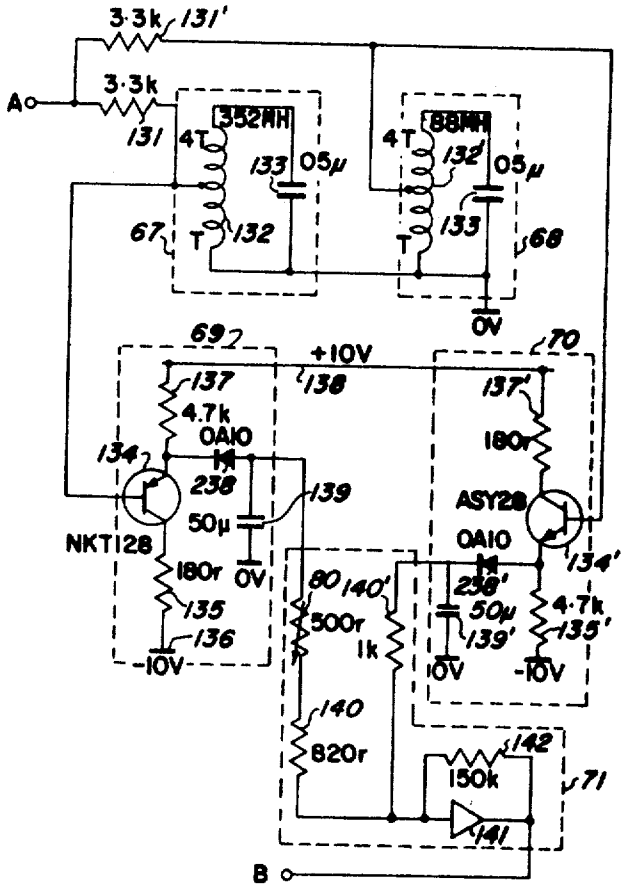

3·3k
131'
A
3·3k
131
352MH
4T
133
05μ
67
T
132
88MH
4T
132'
05μ
133
T
68
0V
69
+10V
70
137
138
137'
4·7k
OA10
180r
134
238
139
ASY28
50μ
OA10
NKT128
180r
0V
134'
238'
80
140'
4·7k
135'
135
136
500r
50μ
139'
1k
0V
-10V
-10V
140
820r
142
150k
71
141
B

FIG. 9B

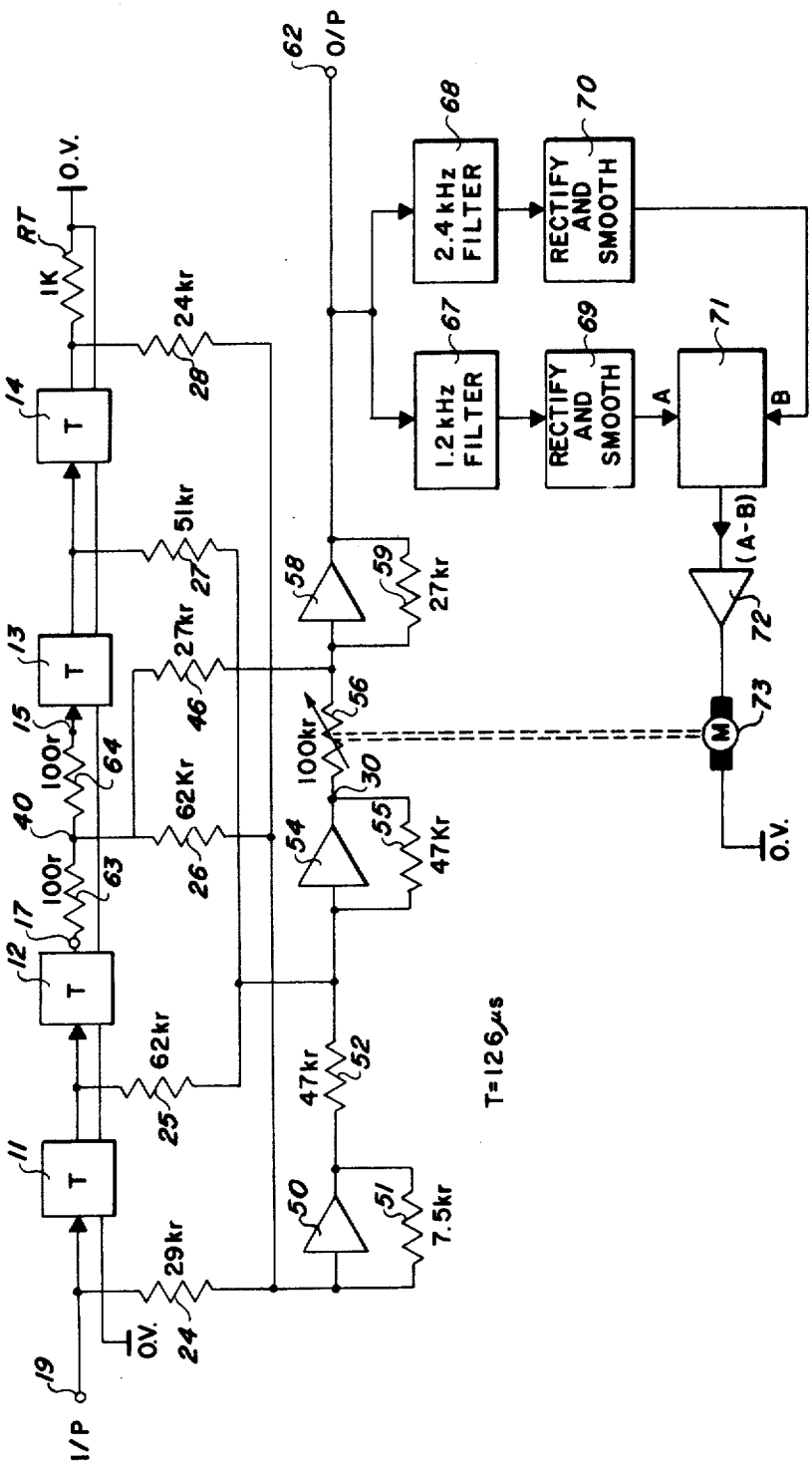

62
O/P
68
2.4 kHz FILTER
70
RECTIFY AND SMOOTH
67
1.2 kHz FILTER
69
RECTIFY AND SMOOTH
71
A
B
(A-B)
72
73
M
O.V.
RT
1K
O.V.
24kr
28
14
T
51kr
27
13
T
27kr
46
15
100r
64
40
100r
63
17
12
T
62kr
26
62Kr
25
11
T
29kr
24
O.V.
19
I/P
58
59
27kr
56
100kr
30
54
55
47Kr
47kr
52
50
51
7.5kr
T=126μs

FIG. 8

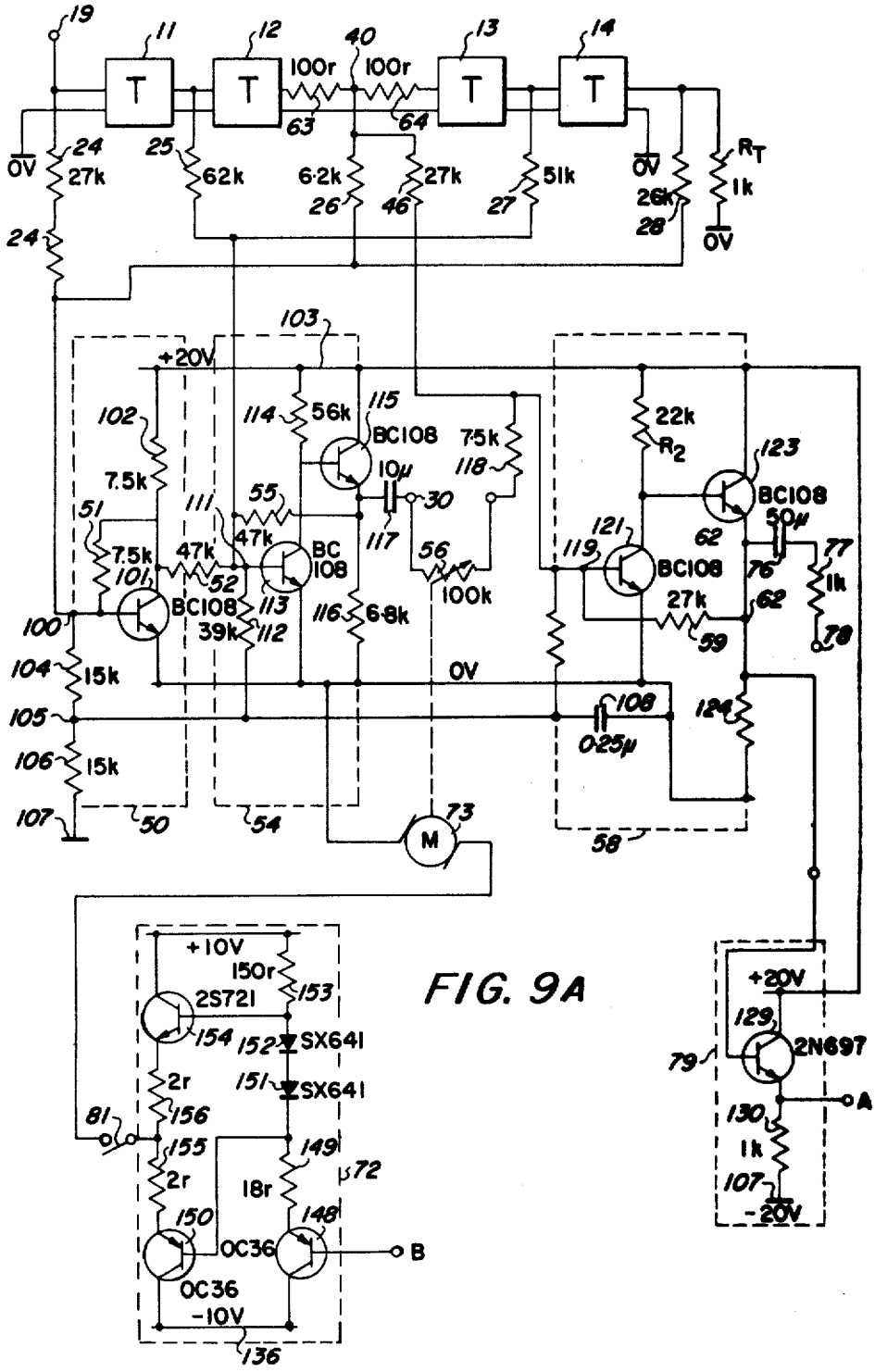

T
T
T
T
100r
100r
62k
6·2k
27k
51k
27k
1k
+20V
7·5k
56k
BC108
10μ
47k
BC 108
100k
6·8k
39k
15k
15k
0V
22k
R2
BC108
50μ
27k
1k
0·25μ
M
+10V
150r
2S721
SX641
SX641
2r
2r
18r
OC36
OC36
-10V
+20V
2N697
1k
-20V
A
B

FIG. 9A

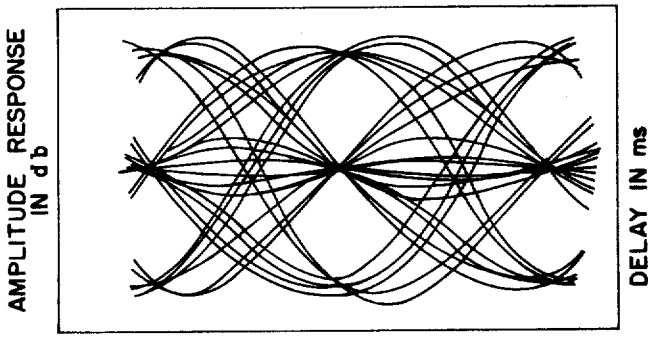


FIG. 10

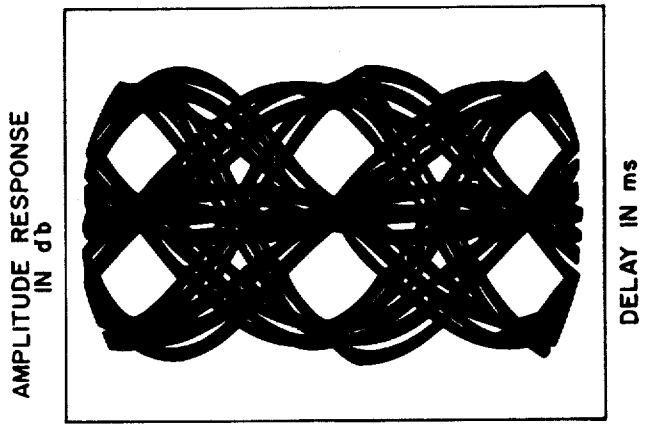
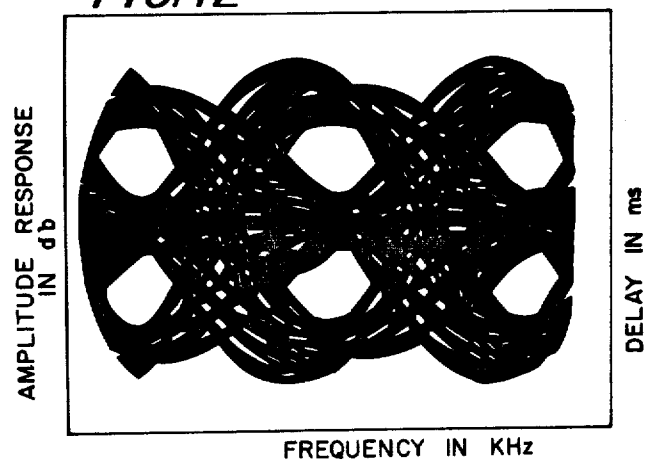


FIG. 11

FIG. 12



AUTOMATIC TRANSVERSAL EQUALIZER

This invention is concerned with improvements in or relating to electrical information transmission systems of the type (hereinafter referred to for convenience as "the type specified") wherein the system includes a transmitter of audio-frequency signals and a receiver of those signals, the system being of the kind wherein the signals are conveyed from the transmitter to the receiver by establishing an interconnection therebetween by means of a given one, or one at a time, of typically available audio-frequency transmission links.

One example of such a case is where the transmitter and the receiver of the data-transmission system of our co-pending U.S. Pat. application, Ser. No. 87,545 filed on Nov. 6, 1970 are intermittently interconnected, for the transmission of the data, by way of a commercial telephone or telegraph transmission link which is established, as and when required, between the locations of the transmitter and of the receiver.

According to one aspect of the invention there is provided an equalizing circuit, intended to be inserted between the transmission link and the receiver of an electrical information transmission system of the type specified, the equalizer being arranged to have, within a preselected bandwidth of the said audio-frequencies, an amplitude-frequency response in the form of a family of similar curves, the equalizer including comparison means which is responsive to the difference between the outputs of the equalizer at two different frequencies of which at least one is within the said bandwidth to thereby automatically select a predetermined one of the said curves.

Conveniently, the circuit includes a transversal network of the kind comprising at least two time-delay network circuits each having an input and an output and connected together in series so as to form a chain having an input, which constitutes the network input, and an output and a number of intermediate junctions each formed where the output of one said circuit is connected to the input of the next succeeding circuit in the chain, the network also including a separate corresponding pick-off resistance associated with and connected to each of the said chain input, the said chain output and the said intermediate junctions so as to provide, in response to an input signal appearing at the network input, a number of pick-off signals equal in number to the number of the resistances, and the network also including first combining means for combining the pick-off signals in predetermined relationship to produce a first network output signal, the network also including at least one further pick-off resistance associated with and connected to one of the said intermediate junctions so as to provide, in response to the said input signal appearing at the network input, a further pick-off signal constituting a second network output signal, the network also including second combining means for combining the first and the second network output signals in variable relationship to thereby provide the said family of curves.

Conveniently, there is an even number of the time-delay circuits arranged in pairs, the circuits of each pair having equal time-delays and being symmetrically located at opposite sides of that one said intermediate junction which is at the center of the chain, the first-mentioned pick-off resistances being so selected that the corresponding pick-off signals comprise a single pick-off signal from the said central one intermediate junction and a number of pairs of pick-off signals for each of which pairs the two signals are similar except in that one is time-delayed relatively to the other.

Conveniently, there is one said further pick-off resistance, which resistance is associated with and connected to the said one intermediate junction which is at the center of the chain.

There may be four of the time-delay circuits.

Conveniently, the time-delay circuits have each the same time-delay.

The first combining means may comprise, at least in part, the connection of at least two of the first-mentioned pick-off signals to a common point, and/or may comprise, at least in part, an inverting amplifier for reversing the polarity of at least one of the first-mentioned pick-off signals.

Conveniently, the second combining means includes a variable resistance which is variable to provide the said variable relationship.

Conveniently, the comparison means includes an electric motor which is arranged to control the variable resistance in response to the said difference between the outputs of the equalizer.

According to a second aspect of the invention there is provided an electrical information transmission system of the type specified, the system having an equalizer according to the invention inserted between the transmission link and the receiver, and the system being arranged for the transmission, from the transmitter to the receiver, of two signals respectively of two different audio-frequencies, the comparison means of the equalizer being arranged to respond to the difference between the outputs of the equalizer at those two frequencies.

An example of the invention will now be described with reference to the accompanying drawings in which:

FIGS. 1 and 3 are block diagrams illustrating systems of the type to which the invention is applicable;

FIG. 2 is a curve of attenuation plotted against frequency;

FIG. 4 is a part-schematic circuit diagram of one form of transversal network;

FIG. 5 is a circuit diagram of a time-delay network for use in the network of FIG. 4;

FIG. 6 is a part-schematic circuit diagram showing, in full lines, one form of the transversal network of FIG. 4 and, in broken lines, a form of modification of the network;

FIG. 7 is a graph illustrating the frequency response of the modified network of FIG. 6;

FIG. 8 is a part-schematic circuit diagram of an automatic equalizer circuit according to the invention;

FIG. 9A and 9B in combination show a circuit diagram showing more details of the apparatus of FIG. 8, and

FIGS. 10, 11 and 12 show eye patterns.

Referring to FIG. 1, consider an electrical information transmission system which includes a transmitter 1 of audio-frequency signals and a receiver 2 of those signals, the receiver being located remotely from the transmitter, and the system being of the kind wherein the signals are conveyed from the transmitter to the receiver by establishing an interconnection therebetween by means of one at a time of typically available audio-frequency transmission links such as that indicated by the broken line 3.

According to workers who examined and compared the audio-frequency responses of many such links, the median attenuation of those links had the form of the full-line curve of FIG. 2, and the attenuation of many of those links rose approximately linearly (in decibels) within the frequency bandwidth of about 1,200 Hz to 2,800 Hz.

The present invention proposes that this approximately linear rise in attenuation should be automatically approximately neutralized, for systems of the type of FIG. 1, by inserting, between the transmission link 3 and the receiver 2, a suitable automatic equalizing circuit 4 (FIG. 3) which is designed to automatically balance the said linear rise in attenuation by providing an appropriately rising amplitude response.

The equalizing circuit makes use of a transversal network of a particular kind (of which an example is shown in FIG. 4). In the case of FIG. 4, the transversal network comprises four identical delay networks 11, 12, 13 and 14 each having input terminals 15, 16 and output terminals 17, 18, the networks 11-14 being connected together in series, output to input, to form a chain.

Each of the networks 11–14 of FIG. 4 has the same time-delay T, so that if a wave represented by $e^{j\omega t}$ is supplied to the input of one of those networks, there emerges at the output of the network a corresponding wave represented by $e^{j\omega(t-T)}$, i.e. each of the networks has a response factor $e^{-j\omega T}$.

FIG. 5 shows one suitable form of delay network. The terminal 15 is connected to the terminal 17 by way of three series-connected inductances L_1, L_2 and L_3, the inductances L_1 and L_2 being intercoupled and the three inductances being

bridged by a capacitance C_1. The terminals **16** and **18** are directly interconnected by a line which is connected, by way of a capacitance C_2, to the common point of the inductances L_1 and L_2.

In FIG. **4**, the input terminal **16** of the network **11**, and the output terminal **18** of the network **14**, are connected to earth. The chain of networks may thus be regarded as having an input (afforded by the terminal **15** of the network **11**, which terminal is connected to the input terminal **19** of the complete transversal network), an output (afforded by the terminal **17** of the network **14**), and three intermediate junctions each formed where the output of one of the networks **11–13** is connected to the input of the next succeeding network in the chain, the three intermediate junctions being in this case afforded by the terminals **17** of the respective networks **11–13**.

The transversal network also includes a separate corresponding pick-off resistance associated with and connected to each of the said chain input, the said chain output and the said intermediate junctions so as to provide, in response to an input signal appearing at the network input (terminal **19**), a number of pick-off signals equal in number to the number of the resistances. In the case of FIG. **4**, these resistances are constituted respectively by the resistances **24**, **28**, and **25**, **26**, **27**, the remote ends of the resistances being shown as commoned by connection to the output terminal **30** of the transversal network. In the simple case of FIG. **4**, the resistance **26** is of magnitude R_0, the resistances **25** and **27** are of identical magnitude R_1, and the resistances **24** and **28** are of identical magnitude R_2, the resistances R_0, R_1 and R_2 corresponding respectively to conductances g_0, g_1 and g_2.

A suitable terminal impedance, in the form of a resistance R_T, is connected in known manner between the terminals **17** and **18** of the network **14**.

Thus, in FIG. **4**, the output current wave (at the terminal **30**, when **30** is connected to a very low impedance,) for unit input wave (at the terminal **19**) is the sum of the five pick-off signals obtained respectively via the five resistances **24–28**, and is given by

$$g_2 + g_1 e^{-j\omega T} + g_0 e^{-j\omega 2T} + g_1 e^{-j\omega 3T} + g_2 e^{-j\omega 4T} = e^{-j\omega 2T}(g_0 + 2g_1 \cos \omega T + 2g_2 \cos 2\omega T)$$

it being noted that this result is obtained by combining four of the five pick-off signals in pairs (e.g., $g_1 e^{-j\omega t}$ and $g_1 e^{-j\omega 3T}$) of which the two signals are of equal amplitude (g_1) but differ in that one is delayed relatively to the other.

In calculating the response of the transversal network, the factor $e^{-j\ 2T}$ may be ignored, since it represents only a distortionless delay of 2T. Then the transversal network of FIG. **4** has the response

$$A_1(\omega) = g_0 + 2g_1 \cos \omega T + 2g_2 \cos 2\omega T.$$

Denoting (ωT) by θ, and noting that $A_1(\omega)$ is symmetrical about $\theta = \pi$, we choose g_0, g_1 and g_2 such that $A_1(\omega)$ has the values 0, 0, ½ and 1 respectively for θ equal to 0, $\pi/3$, $2\pi/3$ and π. This gives $g_0 = \frac{1}{3}$, $g_1 = -\frac{1}{4}$, and $g_2 = 1/12$, whence

$$A_1(\omega) = \tfrac{1}{3}\,[\ 1 - 3/2 \cos \omega BT + \tfrac{1}{2} \cos 2\omega T\ ],$$

which approximates closely to a full, raised cosine curve and has the following values:

$\omega T =$	0°	30°	60°	90°	120°	150°	180°
$A_1(\omega) =$	0	−0.02	0	0.166	0.50	0.85	1.00

The ratio of the resistances $R_0 : R_1 : R_2$ is given by the ratio

$(1/g_0)$	$: (1/g_1)$	$: (1/g_2)$
= 3	: (−4)	: 12
= 1	: (−(4/3))	: 4

the negative signal indicating that those pick-off signals which are obtained via the resistances **25** and **27** (of resistance R_1) need to be inverted relatively to the remaining pick-off signals.

We find that, if we choose (T) such that $\theta = 60°$ at a frequency ($\omega/2\pi$) equal to 1,323 Hz, then T = 126 microseconds.

The transversal network then has the basic form indicated in solid lines in FIG. **6**, wherein R represents the magnitude of a basic resistance and **35** represents an amplifier of current gain equal to (−1) of very low input impedance, and of high output inpedance.

If the response of the transversal network of FIG. **6** is denoted by $A_1'(\omega)$, i.e. a particular example of $A_1(\omega)$, then we find that if that transversal network is so placed upon a unit pedestal that the overall response of the resulting arrangement is $[\ 1 + h \cdot A_1'(\omega)\ ]$, where ($h$) is a fraction of which the magnitude is adjustable as required, then that overall response is of the kind desired for the equalizing circuit **4** of FIG. **3**.

Thus, in FIG. **7**, the curves X and Y show respectively the said overall response of such an arrangement, for the particular two cases of $(1 + hA_1') = 4$ db at a frequency of 2,850 Hz and $(1 + hA_1') = 16$ db at the same frequency. The curves X and Y are representative of a family of curves, corresponding to different values of the fraction (h), these curves providing good approximate compensations for the said approximately linear rise in attenuation of many audio-frequency transmission links.

It will be noted, from FIG. **7**, wherein the straight-line curve ϕ represents the phase associated with the response $(1 + hA_1')$, that the introduction of the arrangement into the system, in the manner of FIG. **3**, does not introduce a variation of time-delay over the audiofrequency band.

The expression "placed upon a unit pedestal" employed above, is intended to indicate that the basic circuit of FIG. **6**, as shown in the full lines and having the response A_1', is so modified that the resultant response is equal to the sum of unity and the fraction (h) of the response A_1'.

A general manner of attaining such a result is indicated by the broken-line portion of FIG. **6**, wherein the output at the output terminal **30** of the basic transversal network is supplied to a potentiometer **43** of which the tapping **44** is arranged to derive the required variable fraction (h) of that output and to supply that fraction to one input of a summing amplifier **45** of which the other input is supplied, from the basic transversal network, with a signal representing the unity just referred to. In FIG. **6**, this latter signal is shown as obtained, via a resistance **46**, from that one said intermediate junction **40** which is at the center of the chain: the reason for taking this further pick-off signal from the terminal **40** is to allow for the said distortionless delay of 2T associated with that factor $e^{-j\omega 2T}$ which was ignored above, in deriving the expression for $A_1(\omega)$.

It is to be understood that the circuit of FIG. **6** is of simple form, in regard to the manner in which the said five pick-off signals and the said further pick-off signal are derived from the chain and subsequently combined as required.

FIG. **8** is a part-schematic circuit diagram of an automatic equalizing circuit according to the invention and making use of the general principles discussed above. The circuit gives a range of adjustment of response from (at 2,850 Hz) 3.5 db to 17.5 db, relative to the response up to about 1,200 Hz.

The circuit includes a modified transversal network of the general form of that described with reference to FIG. **6**. Thus, the pick-off resistances **24**, **26** and **28** provide three of the five pick-off signals in the form of currents which are effectively summed and inverted by a first amplifying stage of the virtual-earth-input type and having unit gain, the stage comprising a high-gain inverting amplifier **50** having a feed-back resistance **51** connected between its output and input and arranged to deliver its current output via resistance **52** to the input of a second amplifying stage.

The pick-off resistances **25** and **27** similarly provide the remaining two pick-off signals in the form of currents which are also delivered to the input of the second amplifying stage. The second amplifying stage effectively sums and inverts the current signals thus delivered to its input, the stage comprising a high-gain amplifier **54** having a feedback resistance **55** connected between its output and input and arranged to deliver its current output via a variable resistance **56** (corresponding to the potentiometer **43**, FIG. **6**) to the input of a third amplifying stage.

The said further pick-off signal is obtained, in the form of a current and via the further pick-off resistance **46**, from that said intermediate junction **40** which is at the center of the chain, the current signal being also delivered to the input of the third amplifying stage.

The third amplifying stage effectively sums the currents thus delivered to its input, the stage comprising a high-gain amplifier **58** having a feedback resistance **59** connected between its output and input and arranged to deliver its output to the output terminal **62** of the equalizing circuit of which the input terminal is constituted by the terminal **19**.

It will be noted that the magnitudes of the resistances **24–28** depart somewhat from the ratios indicated in the simple circuit of FIG. **6**. The reason for this is that, whereas the above theory assumes that, for each of the delay networks **11–14**, the associated pick-off resistances can be so chosen as not to significantly affect the values of the load and source impedances presented to those networks, in practice however, convenient values of those resistances do not always meet this condition. Thus, the theoretically derived simple arrangement may in practice, in certain cases, have to be modified somewhat, in generally known manner and by simple experiment, in order to obtain the required result. In the case of FIG. **8**, the pick-off resistances **26** and **46** would significantly affect the delay-network impedance (of 1 Kilohm) in this case), were the effect not overcome by insertion of the resistances **63** and **64**. The attenuation changes associated with the introduction of the resistances **63**, and **64** necessitated modification of the magnitudes of the pick-off resistances **26,46, 27** and **28**.

When an equalizing circuit of the form of FIG. **8** is inserted into an electrical information transmission system in the manner of FIG. **3**, the transmitter **1** of that system is arranged to transmit, over the transmission link **3**, two control signals respectively of two different frequencies of which at least one is within the frequency bandwidth over which the response ($1 + hA_1'$) is arranged to be variable by adjustment of the fraction (h). These control signals need not be continuously transmitted during the whole of the time for which the transmitter **1** is connected to the receiver **2** by way of one particular transmission link **3** but may conveniently be transmitted only for a limited time immediately following the establishment of that connection by way of one particular transmission link **3**. Thus, for example, in the case where the system is the data-transmission system of our co-pending U.S. Pat. application Ser. No. 87,545 filed on Nov. 6, 1970 the two control signals would conveniently be provided by, firstly, the continuously transmitted quadrature carrier of frequency 2,400 Hz, and, secondly, by causing the transmitter to commence transmission to the receiver with a sufficiently long series of binary ones, for such a series has a fundamental of 1,200 Hz with no second harmonic.

The two control signals do not have to be of equal amplitude at transmission from the transmitter, but their relative amplitude must be predetermined and (see below) the comparison circuit of the equalizer set accordingly.

Returning to FIG. **8**, assuming that those control signals are respectively of frequency 1,200 Hz and 2,400 Hz, the signals of these frequencies which appear at the terminal **62** are respectively selected by means of filters **67** and **68** of which the outputs are respectively both rectified and smoothed by circuits **69** and **70**. The resulting two signals are supplied to the two inputs of a difference circuit **71** of which the output is amplified by the amplifier **72** of which the output is arranged to drive an electric motor **73** arranged in known manner to control the magnitude of the resistance **56** by varying the position of the slider of that resistance. It will be understood that variation of the magnitude of the resistance **56** effectively varies the magnitude of the fraction (h) referred to above.

It is to be understood that, instead of the motor **73** controlling the magnitude of the resistance **56**, any other suitable means may be employed to combine the said further pick-off signal with the said five pick-off signals in suitable variable relationship.

FIGS. **9A** and **9B** in combination show is a circuit diagram showing more details of the circuit of FIG. **8**, corresponding elements having been marked with the same reference numerals. FIG. **9B** can be combined with FIG. **9A** by connecting the terminals designated A and B in the former to those similarly designated in the latter. It will be noted that the output terminal **62** is capacitance-coupled via a capacitor **76** and a 1-kilohm resistor **77** to a terminal **78** for connection to the receiver **2** (FIG. **3**). In a modification, a direct output of low impedance, with a standing direct voltage of about 8 volts, may be employed instead. The terminal **62** is also connected, via a transistor amplifier stage **79**, to the filters **67** and **68**. The current outputs of the rectifying and smoothing circuits **69** and **70** are differenced in the amplifying stage **71**, the variable resistance permitting the ratio of the two currents to be adjusted to suit the predetermined relative amplitudes of the two control signals at transmission from the transmitter. The on-off switch **81** can be used to disconnect the output of the amplifier **72** from the motor **73**, thereby interrupting the automatic operation of the circuit. The input impedance of the arrangement, at the terminal **19**, is 1 kilohm, and attention must be paid to impedance matching at this point. The maximum output of the arrangement is 5 volts peak-to-peak, when the input at 600 Hz is 5 volts peak-to-peak.

Referring to FIG. **9A** in detail, the transversal network at the top left-hand corner is identical with that of FIG. **8**. The input to the amplifier **50** (FIGS. **8, 9**) appears at the terminal **100** which is connected to the base of a transistor **101** of which the emitter is connected to earth and the collector is connected, firstly, via the resistance **51** to the base, and, secondly, via a resistance **102** to a positive supply line **103**. The terminal **100** is also connected via a resistance **104** to a common point **105** which is connected, firstly, via a resistance **106** to a negative supply line **107**, and, secondly, via a capacitance **108** to earth.

The collector of transistor **101** is also connected via the resistance **52** to a common point **111** which constitutes the input of the amplifier **54** (FIGS. **8, 9**). The common point **111** is connected, firstly, via a resistance **112** to the common point **105**, and, secondly, to the base of a transistor **113** of which the emitter is connected to earth and the collector is connected, firstly, via a resistance **114** to the line **103**, and, secondly, to the base of a transistor **115**. The collector of this transistor is connected to the supply line **103**, and the emitter is connected, firstly, via the resistance **55** to the common point **111**, and, secondly, via a resistance **116** to earth, and, thirdly, via a capacitance **117** to the terminal **30**.

The terminal **30** is connected, via the variable resistance **56** and a supplementary resistance **118**, to the common point **119** which constitutes the input of the amplifier **58** (FIGS. **8,9**). THe common point **119** is connected, firstly, via a resistance **120** to the common point **105**, and, secondly, to the base of a transistor **121** of which the emitter is connected to earth and the collector is connected, firstly, via a resistance **122** to the supply line **103**, and, secondly, to the base of a transistor **123** of which the collector is also connected to the line **103**.

The emitter of the transistor **123** is connected, to the terminal **62** which is connected, firstly, via the resistance **59** to the common point **119**, and, secondly, via a resistance **124** to earth, and, thirdly, via the capacitance **76** and the series resistance **77** to the terminal **78**, and, fourthly, to the base of a transistor **129** of the amplifying stage **79**.

The collector of the transistor **129** is connected to the supply line **103**, and the emitter is connected via a resistance **130** to the negative supply line **107**.

The emitter is also connected, via a resistance **131**, (FIG. **9B**) to the tapping (at T turns from one end) of an inductance **132** (having $5T$ turns) bridged by a capacitance **133**, the said one end of the inductance being earthed.

The emitter is also connected, via a resistance **131'**, to the tapping (at T turns from one end) of an inductance **132'** (having $5T$ turns) bridged by a capacitance **133'**, the said one end of the inductance **132'** being also earthed.

The tapping of the inductance **132** is connected to the base of a transistor **134** of which the collector is connected, via a resistance **135**, to a negative supply line **136** and of which the emitter is connected, firstly, via a resistance **137** to a positive supply line **138**, and, secondly, to the cathode of a diode rectifier **238** of which the anode is connected, firstly, via a capacitance **139** to earth, and, secondly, via the variable resistance **80** and a fixed series resistance **140**, to the input of a high-gain inverting amplifier **141** having a feedback resistance **142** connected between its output and its input.

The tapping of the inductance **132'** is connected to the base of a transistor **134'** of which the collector is connected, via a resistance **137'**, to the supply line **138** and of which the emitter is connected, firstly, via a resistance **135'** to the negative supply line **136**, and, secondly, to the anode of a diode rectifier **238'** of which the cathode is connected, firstly, via a capacitance **139'** to earth, and, secondly, via a resistance **140'** to the input of the amplifier **141** (FIG. **9B**).

The output of the amplifier **141** (FIG. **9A**) is connected to the base of a transistor **148** of which the collector is connected to the negative supply line **136** and the emitter is connected, via a resistance **149**, to the base of a transistor **150** of which the collector is connected to the line **136**.

The base of the transistor **150** is connected to the cathode of a diode rectifier **151** of which the anode is connected to the cathode of a further diode rectifier **152** of which the anode is connected, firstly, via a resistance **153** to the positive supply line **138**, and, secondly, to the base of a transistor **154** of which the collector is connected to the line **138**.

The emitter of transistor **150** is connected, via a resistance **155**, to one contact of the on-off switch **81**, which contact is also connected, via a resistance **156**, to the emitter of transistor **154**. The other contact of the switch **81** is connected, via the motor **73**, to earth.

The broken line of FIG. **2** illustrates how the equalizer is employed to balance the said approximately linear rise in attenuation of a transmission link **3** (FIG. **3**) by providing an appropriately rising response.

The remaining FIGS. **10–12** show the response characteristics of the transmission systems in the form of the amplitude response and delay characteristics in terms of decibels and milliseconds as a function of the frequency variation of the signal in the usual form of eye patterns. FIG. **10** shows the eye pattern of a bipolar system in which there is no line distortion. FIG. **11** shows a severely degraded eye pattern in which there are median attenuation and time-delay distortions as found in certain transmission links. FIG. **12** shows an improved eye pattern obtained with the present equalizer in conjunction with the a transmission line which had median attenuation and time-delay distortions.

What we claim is:

1. An automatic equalizer to be inserted in a transmission system between its transmission link and receiver for correcting the frequency-dependent distortions in the signal introduced by said transmission link, said equalizer including a transversal network comprising:

at least two time-delay circuits each having an input and an output and connected together in series so as to form a chain having an input and an output, which constitutes the transversal network input and output, and at least one intermediate junction formed where the output of one of said time-delay circuit is connected to the input of the next succeeding time-delay circuit in the chain, the network also including,

a separate corresponding pick-off means associated with and connected to each of the input and output of said transversal network and the intermediate junction so as to provide, in response to the input signal appearing at the network input, a number of pick-off signals equal in number to the number of the pick-off means, and the network also including,

first combining means for combining the pick-off signals in predetermined relationship to produce a first network output signal, the network also including,

at least one further pick-off means associated with and connected to said at least one intermediate junction so as to provide, in response to the input signal appearing at the network input, a further pick-off signal constituting a second network output signal, and the network also including,

second combining means for combining the first and the second network output signals in variable relationship to thereby correct the frequency-dependent distortions.

The equalizer according to claim **1**, wherein there is an even number of the time-delay circuits arranged in pairs, the circuits of each pair having equal time-delays and being symmetrically located at opposite sides of that one said intermediate junction which is at the center of the chain, the first-mentioned pick-off means being so selected that the corresponding pick-off signals comprise a single pick-off signal from the said central one intermediate junction and a number of pairs of pick-off signals for each of which pairs the two signals are similar except that one is time-delayed relative to the other.

3. The equalizer according to claim **2**, wherein said further pick-off means, is associated with and connected to the said one intermediate junction which is at the center of the chain.

4. The equalizer according to claim **3**, wherein there are four of the time-delay circuits.

5. The equalizer according to claim **4**, wherein the time-delay circuits have each the same time-delay.

6. The equalizer according to claim **5**, wherein the first combining means comprises, at least in part, the connection of at least two of the first-mentioned pick-off signals to a common point.

7. The equalizer according to claim **6**, wherein the first combining means comprises, at least in part, an inverting amplifier connected to said common point for reversing the polarity of at least one of the first-mentioned pick-off signals.

8. The equalizer according to claim **7** wherein the second combining means includes a variable resistance which is variable to provide the said variable relationship.

9. The equalizer according to claim **8** having an amplitude-frequency response in the form of a family of curves and including comparison means for comparing the outputs of said transversal delay network at two different frequencies of which at least one is within a preselected audio frequency bandwidth to select a predetermined one of the said family of curves.

10. The equalizer according to claim **9** wherein said comparison means includes an electric motor which is arranged to control said variable resistance in response to the said difference between the two outputs of said transversal delay network.

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