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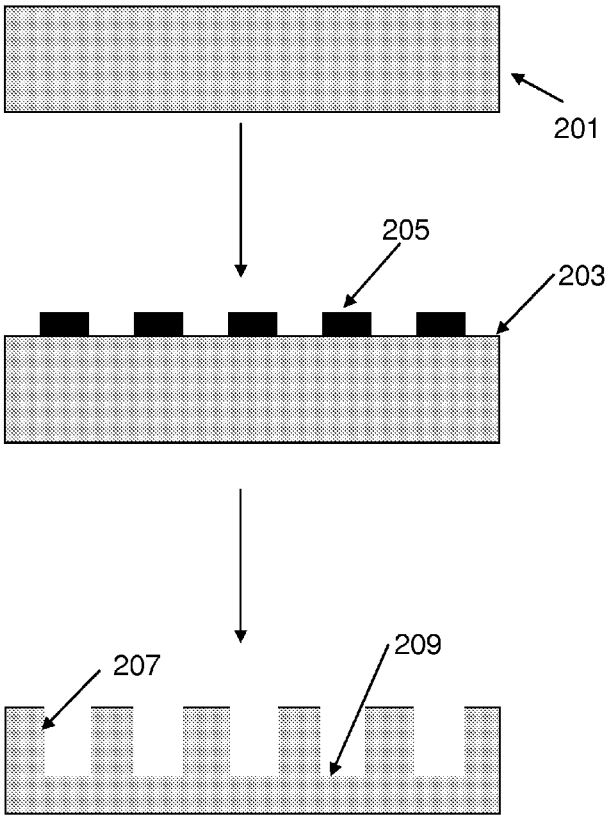
[Continued on next page]

(54) Title: ETCHED SILICON STRUCTURES, METHOD OF FORMING ETCHED SILICON STRUCTURES AND USES THEREOF

FIGURE 2A



(57) Abstract: A method of etching silicon, the method comprising the steps of: partially covering at least one silicon surface of a material to be etched with copper metal; and exposing the at least one surface to an aqueous etching composition comprising an oxidant and a source of fluoride ions.

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Etched Silicon Structures, Method of Forming Etched Silicon Structures and Uses Thereof

Field of the Invention

The present invention relates to methods of etching silicon, etched silicon structures, electrodes containing etched silicon structures and devices including etched silicon structures.

Background of the Invention

Rechargeable lithium-ion batteries are extensively used in portable electronic devices such as mobile telephones and laptops, and are finding increasing application in electric or hybrid electric vehicles. However, there is an ongoing need to provide batteries that store more energy per unit mass and / or per unit volume.

The structure of a conventional lithium-ion rechargeable battery cell is shown in Fig. 1. The battery cell includes a single cell but may also include more than one cell. Batteries of other metal ions are also known, for example sodium ion and magnesium ion batteries, and have essentially the same cell structure.

The battery cell comprises a current collector for the anode 10, for example copper, and a current collector for the cathode 12, for example aluminium, which are both externally connectable to a load or to a recharging source as appropriate. A composite anode layer 14 overlays the current collector 10 and a lithium containing metal oxide-based composite cathode layer 16 overlays the current collector 12 (for the avoidance of any doubt, the terms "anode" and "cathode" as used herein are used in the sense that the battery is placed across a load – in this sense the negative electrode is referred to as the anode and the positive electrode is referred to as the cathode).

The cathode comprises a material capable of releasing and reabsorbing lithium ions for example a lithium-based metal oxide or phosphate, $LiCoO_2$, $LiNi_{0.8}Co_{0.15}Al_{0.05}O_2$, $LiMn_xNi_xCo_{1-2x}O_2$ or $LiFePO_4$.

A porous plastic spacer or separator 20 is provided between the graphite-based composite anode layer 14 and the lithium containing metal oxide-based composite cathode layer 16. A liquid electrolyte material is dispersed within the porous plastic spacer or separator 20, the composite anode layer 14 and the composite cathode layer 16. In some cases, the porous plastic spacer or separator 20 may be replaced by a polymer electrolyte material and in such cases the polymer electrolyte material is present within both the composite anode layer 14 and the composite cathode layer 16. The polymer electrolyte material can be a solid polymer electrolyte or a gel-type polymer electrolyte and can incorporate a separator.

When the battery cell is fully charged, lithium has been transported from the lithium containing metal oxide cathode layer 16 via the electrolyte into the anode layer 14. In the case of a graphite-based anode layer, the lithium reacts with the graphite to create the compound, LiC_6. The graphite, being the electrochemically active material in the composite anode layer, has a maximum capacity of 372 mAh/g. ("active material" or "electroactive material" as used herein means a material which is able to insert into its structure, and release therefrom, metal ions such as lithium, sodium, potassium, calcium or magnesium during the respective charging phase and discharging phase of a battery. Preferably the material is able to insert and release lithium.)

The use of a silicon-based active anode material is also known in the art. Silicon has a substantially higher maximum capacity than graphite. However, unlike active graphite which remains substantially unchanged during insertion and release of metal ions, the process of insertion of metal ions into silicon results in substantial structural changes, accompanied by substantial expansion. For example, insertion of lithium ions into silicon results in formation of a Si-Li alloy. The effect of Li ion insertion on the anode material is described in, for example, "Insertion Electrode Materials for Rechargeable Lithium Batteries", Winter et al, Adv. Mater. 1988, 10, No. 10, pages 725-763.

US 7402829 discloses etching of a silicon substrate to form an array of silicon pillars extending from the silicon substrate.

Peng et al, "Dendrite-Assisted Growth of Silicon Nanowires in Electroless Metal Deposition", Adv. Funct. Mater. 2003, 13(2), 127-132 discloses that electroless deposition of Pt and Cu in HF solutions tends to result in formation of continuous grain films on silicon that result in uniform etching of the underlying silicon whereas silver forms nanoclusters that may be etched to form nanowires.

WO2009/010758 discloses the etching of silicon powder in order to make silicon material for use in lithium ion batteries. The resulting etched particles contain pillars on their surface.

US 2010/0301276 discloses a method of preparing a porous silicon nanorod structure by adding silicon to a solution of aqueous hydrogen fluoride and a metal precursor.

US 2008/0268652 discloses a method of forming porous silicon by putting silicon in contact with a solution of hydrofluoric acid, an alcohol and a metallic salt. Copper, silver, platinum and gold salts are disclosed. The pores have a depth lying in the range 150 – 250 nm and a diameter lying in the range 15 – 30 nm.

WO2011073666 discloses a method of making mesoporous particulate silicon using an aqueous chemical etchant comprising hydrofluoric acid and a dissolved metal salt.

US6399177 discloses a composite structure comprising a porous silicon-based film comprising a plurality of amorphous or polycrystalline rod-like elements extending from a substrate, made using high density plasma deposition.

US7402829 discloses an energy storage device comprising an anode comprising an array of sub-micron silicon structures supported on a silicon substrate, made by etching the silicon substrate.

WO2007083152 discloses a method of etching a silicon substrate comprising contacting the silicon substrate with an aqueous solution of a fluoride acid or a fluoride salt, a metal salt capable of electroless deposition of the metal on the silicon in the presence of fluoride ions and an alcohol.

US 2011/215441 discloses etching a silicon substrate under metal nanostructures on the silicon substrate; side-etching the silicon; and removing the metal nanostructures.

Huang et al, "Metal-Assisted Chemical Etching of Silicon: A Review", Advanced Materials 2010, 1-24, discloses that electroless deposition of Pt and Cu tends to result in formation of a dense metal film that cannot be used to etch Si into wires or pores.

Huang et al, "Metal-assisted electrochemical etching of silicon", Nanotechnology 21 (2010), 465301 discloses use of Ag and Cu in electrochemical etching of Si.

It is an object of the invention to provide a controllable method for etching silicon, in particular anisotropic etching of silicon.

It is a further object of the invention to provide structured silicon formed by deep etching of a silicon starting material, for example to produce an etched silicon surface having pillars extending outwardly from the etched surface, or macroporous silicon.

It is a yet further object of the invention to provide a low-cost method for etching silicon.

Summary of the Invention

In a first aspect the invention provides a method of etching silicon, the method comprising the steps of: partially covering at least one silicon surface of a material to be etched with copper metal; and exposing the at least one surface to an aqueous etching composition comprising an oxidant and a source of fluoride ions.

The material to be etched may consist essentially of silicon and may be, for example, undoped, n-doped or p-doped silicon, or it may be a material containing silicon and one or more further materials, for example a material having at least one silicon surface, such as a material having a non-silicon core and a silicon shell.

Optionally, at least some of the copper metal is formed on the at least one surface of the material to be etched by an electroless deposition process.

Optionally, the electroless deposition process comprises exposing the at least one surface of the material to be etched to an aqueous deposition composition comprising a copper salt and a source of fluoride ions.

Optionally, the oxidant is selected from the group consisting of O_2; O_3; and the acid or salt of NO_3^-, $S_2O_8^{2-}$, NO_2^-, $B_4O_7^{2-}$ or ClO_4^- or a mixture thereof.

Optionally, the oxidant is selected from the group consisting of alkali metal nitrates, ammonium nitrate and mixtures thereof.

Optionally, the aqueous etching composition is substantially free of copper ions.

Optionally, the aqueous etching composition is formed by adding the oxidant and, optionally, further fluoride ions to the aqueous deposition composition.

Optionally, the oxidant and optional further fluoride ions are added in aqueous form, and wherein the concentration of copper ions is diluted by addition of the aqueous oxidant and optional further fluoride.

Optionally, the concentration of copper ions is diluted by addition of the aqueous oxidant and optional further fluoride to substantially stop further electroless deposition of copper once the electrolessly deposited copper has formed of a plurality of isolated islands of copper, the isolated islands optionally having a diameter in the range of 50-200 nm, optionally 50-100 nm.

Optionally, the concentration of copper ions is diluted by addition of the aqueous oxidant and optional further fluoride to substantially stop further electroless deposition of copper once the electrolessly deposited copper has formed a monolayer of copper.

Optionally, the material to be etched is removed from the aqueous deposition composition following electroless deposition and before being exposed to the aqueous etching composition.

Optionally, the electrolessly deposited copper forms of a plurality of isolated islands of copper, and wherein the material to be etched is removed from the first aqueous

composition to provide the plurality of isolated islands of copper on the at least one silicon surface, the isolated islands optionally having a diameter in the range of 50-200 nm.

Optionally, the electrolessly deposited copper forms a monolayer of copper, and wherein the material to be etched is removed from the first aqueous composition to provide the monolayer of copper on the at least one silicon surface.

Optionally, the at least one surface is etched to form silicon pillars extending from an etched silicon surface formed by etching of the at least one surface. Optionally, the method comprises the further step of detaching the silicon pillars from the etched silicon surface.

Optionally, the source of fluoride ions in the aqueous etching composition is hydrogen fluoride.

Optionally, the source of fluoride ions in the aqueous deposition composition is hydrogen fluoride.

Optionally, the concentration of hydrogen fluoride in the aqueous deposition composition and in the aqueous etching composition is independently in the range of 1 to 10 M.

Optionally, the concentration of the copper salt in the aqueous deposition composition is in the range of 0.001 to 5 M.

Optionally, the aqueous etching composition is substantially free of alcohols.

Optionally, the at least one surface is exposed to the aqueous deposition composition for less than 2 minutes, optionally no more than 1 minute.

Optionally, the silicon has a resistivity of at least 0.005 Ω.cm, optionally at least 0.01 Ω.cm.

Optionally, the silicon is n-doped, p-doped or a mixture thereof.

Optionally, the at least one surface has a {111} or {100} orientation. Optionally, the at least one surface has a (111) or (100) orientation.

Optionally, the method is conducted at a temperature of 0°C to 30°C, optionally about 20°C.

Optionally, a bias is not applied to the silicon during etching of the material to be etched.

Optionally, the at least one surface of the material to be etched is etched to a depth of at least 0.5 microns.

Optionally, the etched silicon comprises pores extending into at least one etched surface formed by etching the at least one surface.

Optionally, the pores have a diameter of at least 50 nm.

Optionally, the etched silicon comprises pillars extending out from at least one etched surface formed by etching the at least one surface.

Optionally, the pillars have a length of at least 0.5 microns.

Optionally, the material to be etched is in the form of bulk silicon, optionally a silicon wafer. Optionally, the method comprises the step of breaking the etched bulk silicon into a plurality of etched bulk silicon fragments.

Optionally, the silicon is in the form of a silicon powder.

Optionally, at least some of the copper metal is formed on the at least one surface of the silicon to be etched by a process selected from thermal evaporation and sputtering.

Optionally, the copper metal is deposited on the at least one silicon surface through a patterned mask.

In a second aspect, the invention provides etched silicon obtainable by a method according to the first aspect.

In a third aspect, the invention provides an electrode comprising an active material of etched silicon according to the second aspect.

Optionally according to the third aspect, the electrode further comprises a conductive current collector in electrical contact with the active material.

In a fourth aspect, the invention provides a method of forming an electrode according to the third aspect, the method comprising the step of depositing onto the conductive current collector a slurry comprising an etched silicon powder formed according to the first aspect and at least one solvent, and evaporating the at least one solvent.

In a fifth aspect, the invention provides a method of forming an electrode according to the third aspect, the method comprising the step of applying the conductive current collector to etched bulk silicon formed according to the method of the first aspect.

Optionally according to the fifth aspect residual copper in the etched bulk silicon is not removed prior to applying the conductive current collector.

In a sixth aspect, the invention provides a rechargeable metal ion battery comprising an anode, the anode comprising an electrode according to the third aspect capable of inserting and releasing metal ions; a cathode formed from a metal-containing compound capable of releasing and reabsorbing the metal ions; and an electrolyte between the anode and the cathode.

Optionally according to the sixth aspect, the rechargeable metal ion battery is a lithium ion battery.

Description of the Drawings

The invention will now be described in more detail with reference to the Figures, in which:

Figure 1 illustrates schematically a lithium ion battery;

Figure 2A illustrates schematically an etching process according to an embodiment of the invention;

Figure 2B illustrates schematically a first etched silicon product that may be formed by the process of Figure 2A;

Figure 2C illustrates schematically a second etched silicon product that may be formed by the process of Figure 2A;

Figure 3 is a scanning electron microscope (SEM) image of an upper surface of an etched silicon wafer formed by a method according to an embodiment of the invention;

Figure 4A is a SEM image of an upper surface of an etched silicon wafer formed by a method according to an embodiment of the invention;

Figure 4B is a SEM image of the etched silicon wafer of Figure 4A viewed at an angle of 75°;

Figure 5A is a SEM image of an upper surface of an etched silicon wafer formed by a method according to an embodiment of the invention;

Figure 5B is a SEM image of the etched silicon wafer of Figure 5A viewed at an angle of 75°;

Figure 6A is a SEM image of an upper surface of an etched silicon wafer formed by a method according to an embodiment of the invention;

Figure 6B is a SEM image of the etched silicon wafer of Figure 6A viewed at an angle of 75°;

Figure 7A is a SEM image of an upper surface of an etched silicon wafer formed by a method according to an embodiment of the invention;

Figure 7B is a SEM image of the etched silicon wafer of Figure 7A viewed at an angle of 75°;

Figure 8 is a SEM image of an upper surface of a silicon wafer carrying electrolessly deposited copper formed by a method according to an embodiment of the invention;

Figure 9 is a SEM image of an upper surface of a silicon wafer carrying electrolessly deposited copper formed by another method according to an embodiment of the invention;

Figure 10A is a SEM image of an upper surface of an etched silicon wafer formed by a method according to an embodiment of the invention;

Figure 10B is a higher magnification of the SEM image of Figure 10A;

Figure 11A is a SEM image of an upper surface of an etched silicon wafer formed by a method according to an embodiment of the invention;

Figure 11B is a SEM image of the etched silicon wafer of Figure 11A viewed at an angle of 75°;

Figure 12A is a SEM image of an upper surface of an etched silicon wafer formed by a method according to an embodiment of the invention;

Figure 12B is a SEM image of the etched silicon wafer of Figure 12A viewed at an angle of 75°;

Figure 13A is a SEM image of an upper surface of an etched silicon wafer formed by a method according to an embodiment of the invention;

Figure 13B is a SEM image of the etched silicon wafer of Figure 13A viewed at an angle of 75°;

Figure 14A is a SEM image of an upper surface of an etched silicon wafer formed by a method according to an embodiment of the invention;

Figure 14B is a SEM image of the etched silicon wafer of Figure 14A viewed at an angle of 75°;

Figure 15A is a SEM image of an upper surface of an etched silicon wafer formed by a method according to an embodiment of the invention;

Figure 15B is a SEM image of the etched silicon wafer of Figure 15A viewed at an angle of 75°;

Figure 16A is a SEM image of an etched silicon wafer formed by a method according to an embodiment of the invention;

Figure 16B is a higher magnification of the SEM of Figure 16A;

Figure 17 is a SEM image of an etched silicon wafer formed by a method according to an embodiment of the invention;

Figure 18A is a SEM image of a thin silicon wafer carrying pillars formed by a method according to an embodiment of the invention;

Figure 18B is a magnified version of Figure 18A;

Figure 18C is a SEM image of fragments formed by breaking the wafer of Figures 18A and 18B;

Figure 18D is a magnified SEM image of a fragment of Figure 18C showing pillars extending from the fragment surface;

Figure 19A is a SEM image of silicon fibres harvested by scraping the surface of an etched silicon wafer carrying silicon pillars;

Figure 19B is a SEM image of silicon fibres of Figure 19A showing an end-on view of the harvested silicon fibres; and

Figure 20 is a SEM image of a surface of an etched silicon particle of an etched silicon powder formed by a method according to an embodiment of the invention.

Detailed Description of the Invention

The process of etching silicon with copper involves a deposition stage in which elemental copper is deposited on a surface of the silicon to cover some but not all of the surface to be etched, and an etching stage in which silicon underlying the deposited copper is etched.

Copper may be deposited on the surface of the silicon by any process known to the skilled person including thermal evaporation, sputtering, electrodeposition and electroless deposition.

If copper is deposited by thermal evaporation, electrodeposition or sputtering then it may be deposited through or over one or more removable masks or templates to define a regular or irregular copper pattern on the surface of the silicon. Exemplary methods of applying a metal using a template are described in Huang et al, "Metal-Assisted Chemical Etching of Silicon: A Review", Advanced Materials 2010, 1-24. Methods such as these may allow more precise control over the size, spacing and arrangement of the resulting silicon structures formed by etching compared to electroless deposition. A suitable removable template can for example be provided by an arrangement of nanospheres or nanoparticles (e.g. SiO_2 nanospheres) or by a patterned anodised aluminium film.

Electroless deposition may produce a random, scattered distribution of copper ions on the silicon surface and may be a cheaper deposition step compared to the other methods listed above.

If copper is deposited by an electroless process then in a first stage silicon is treated with an aqueous solution of hydrogen fluoride and a source of Cu^{2+} ions. The HF reacts with the silicon according to the following half-reaction:

$$Si^{0} + 6F^{-} \rightarrow SiF_6^{2-} + 4e^{-}$$

Electrons generated in etching of silicon cause reduction of aqueous copper ions to elemental copper according to the following half-reaction:

$$2Cu^{2+}(aq) + 4e^{-} \rightarrow 2Cu\ (s)$$

Elemental copper formed by this process is deposited on the surface of the silicon.

The aqueous solution may contain one or more solvents in addition to water, for example water-miscible organic solvents. In a preferred embodiment, the aqueous etching solution is substantially free of other solvents.

Any water-soluble copper salt may be used as the source of copper ions including, without limitation, copper sulphate and copper nitrate. The copper ions may be provided in a concentration range of about 1mM – 5 M, optionally in the range of 10 mM – 1 M, 10-200 mM or 0.1 – 1 M.

During electroless elemental copper formation, it is the copper ions that are reduced by electrons generated in the etching process. It will be appreciated that electroless deposition of copper as described herein will result in some degree of etching at the silicon surface, unlike copper deposition by thermal evaporation or sputtering, and so the deposition stage may include some degree of silicon etching.

In the case of thermally evaporated or sputtered copper, the thickness of copper deposited may be controlled by control of the deposition rate and the percentage coverage of the silicon surface may be controlled by the dimensions of the mask or template structure.

In the case of electroless deposition of copper, the extent of copper formation may be controlled by the concentration of copper ions in the solution, and / or the length of time that the silicon remains in the solution.

Once copper has been deposited on the silicon surface, etching (or further etching in the case of electrolessly deposited copper) may take place in an etching stage in the presence of HF and an oxidant.

The oxidant (or oxidising agent) is a material that gains electrons or transfers oxygen atoms in a chemical redox reaction. The oxidant is preferably one that is less reactive (a weaker oxidant) than hydrogen peroxide. Preferably the oxidant has an oxidation potential with respect to hydrogen less than that of hydrogen peroxide, i.e. less than 1.2 V. The oxidant may be selected from the group consisting of O_2; O_3; fluorine; chlorine; iodine; bromine; chlorine trifluoride; dinitrogen trioxide; metal oxides; propyl nitrate; and the acid or a salt of BrO_3^- NO_3^-, $S_2O_8^{2-}$, NO_2^-, $B_4O_7^{2-,}$ ClO_2^-, ClO_3^- or ClO_4^- or a mixture

thereof. Exemplary salts include ammonium perchlorate, ammonium permanganate, calcium chlorate; calcium hypochlorite; chromium trioxide (chromic anhydride); potassium bromate; potassium chlorate; sodium chlorate; sodium chlorite; and sodium perchlorate. Exemplary acids include chromic acid and perchloric acid. Alkali metal nitrates and ammonium nitrate are preferred.

The oxidant may be provided in a concentration of at least about 0.001 M, optionally at least about 0.01 M, optionally at least about 0.1 M in an aqueous etching solution. The oxidant may be provided in a concentration of up to about 1 M. Preferably, the aqueous etching solution is substantially free of copper ions.

The aqueous etching solution may contain one or more solvents in addition to water, for example water-miscible organic solvents. In a preferred embodiment, the aqueous etching solution is substantially free of other solvents.

HF may be provided in a concentration of at least 0.1 M, optionally about 1-10 M. The same concentration range may be provided for the deposition stage in the case of electroless deposition.

The concentration of HF in the etching stage (and in the deposition stage in the case of electroless deposition), and / or the concentration of the oxidant in the etching stage, may be monitored during the deposition and / or etching process and adjusted as required.

The silicon may be irradiated during the deposition and etching steps. The intensity and wavelength of the light used will depend on the nature of the silicon being etched. The reaction material may be irradiated with a light source having a wavelength in the region of the bandgap of the silicon material being etched. The use of visible light is preferred. The light source may be ambient light; a lamp; or ambient light augmented by light emitted from a lamp.

The etching process may be carried out in any suitable reaction vessel, for example a vessel formed from a HF-resistant material, such as polyethylene or polypropylene or a reaction vessel lined with a HF resistant material such as a HF resistant rubber. If the

silicon is irradiated then the vessel may be light-transmissive. Electroless deposition may likewise be carried out in such a reaction vessel.

In the case of electroless deposition, the deposition and etching stages may take place in a single reaction vessel in which an aqueous solution containing the oxidant(s), and optionally further fluoride, is added to the reaction vessel following formation of elemental copper. The concentration of copper ions may be diluted by addition of the oxidant solution. This may make further deposition of copper less probable than a competing process of etching of silicon by HF and the oxidant.

In another embodiment, the silicon is removed from the aqueous solution comprising copper ions once a desired level of copper has formed on the surface of the silicon, and the etching stage takes place in a separate aqueous solution containing a fluoride source, such as HF, and the oxidant(s), wherein the separate aqueous solution is substantially free of copper ions.

Etching may take place by a non-electrochemical process, i.e. a bias voltage is not applied to the silicon during etching.

Anisotropic etching may form structured silicon, in particular silicon carrying pillars or porous, preferably macroporous, silicon.

An exemplary etching process is illustrated in Figures 2A and 2B, which are not drawn to any scale. With reference to Figure 2A, in a first stage elemental copper 205 is formed on the surface 203 of silicon wafer 201. In a second stage, the area underneath the deposited copper is etched in the presence of the oxidant and HF to form pillars 207 in the surface of the silicon.

Although the invention is illustrated herein with reference to a silicon wafer, it will be appreciated that any substrate having a silicon surface may be used including, without limitation, non-wafer silicon sheets, silicon ribbons and particles of silicon such as silicon flakes and spherical or spheroid silicon particles.

Pillars 209 may have any shape. For example, pillars may be branched or unbranched; substantially straight or bent; and of a substantially constant thickness or tapering.

With reference to Figure 2B, the pillars 207 extending outwardly from, and may be spaced apart on, etched surface 209. The pillars may be wires, nanowires, rods and columns. The pillars may be detached from the etched surface 209 to form silicon fibres. In one arrangement, substantially all pillars 207 may be spaced apart. In another arrangement, some of the pillars 207 may be clustered together.

The cross-sections of the pillars may form regular shapes (e.g. circular, square or triangular) or be irregular in shape (e.g. may contain one or more concave or convex curved sides or branches or spurs extending outwards or combinations thereof). Since the shape of the pillars is partly determined by the shape of the exposed surface areas of silicon after copper deposition, it can be understood that methods comprising electroless copper deposition may tend to produce pillars with irregular shaped cross sections.

Figure 2C illustrates etched silicon comprising pores 211 extending into the silicon formed by etching surface 203 to produce macroporous silicon (i.e. silicon with pores of diameter > 50nm). The process of etching silicon may be substantially the same as illustrated in Figure 2A, except that the copper is deposited such that etching results in formation of pores 211 on the surface 203 of the silicon to be etched and extending downwards into the silicon material, rather than pillars 207 extending from an etched surface 209 of the etched silicon. In contrast to structured silicon having pillars, macroporous silicon may have a substantially continuous connected network of silicon walls at the outer surface of the silicon that has been etched.

The surface of the etched silicon may comprise both regions of porous silicon and regions with pillars. The etched silicon may also combine regions of porous and pillared silicon in an inward extending direction. That is, an outer shell region of the etched silicon may comprise pillared silicon whilst the inner region comprises porous silicon and vice versa.

The extent of copper deposition on the surface of the silicon in the first stage may be controlled by controlling one or more of the length of time that the silicon is exposed to

the solution containing copper ions; the concentration of copper ions in the solution; and the number of moles of copper per unit surface area of silicon exposed to the copper-containing solution.

Pores may extend at least 0.5 microns into the silicon from silicon surface 203, optionally at least 1 micron, optionally at least 2 microns. The pores may have a diameter of at least 100 nm, optionally at least 300nm, optionally at least 0.5 microns. The pores may extend inwards perpendicular to the silicon surface or may extend inwards at any intermediate angle. Not all pores may extend in the same direction, instead the plurality of pores may extend in a plurality of directions. The direction in which the pores extend inwards may change partway down. Two or more pores may join to form an irregular network of pores below the surface of the silicon.

After a substrate has been etched to form pillars and / or porous silicon, the etched surface or surfaces may be treated to detach the pillars and / or form porous silicon fragments. Exemplary treatments include mechanical treatments, for example scraping the etched surface, and ultrasonic treatment. In this embodiment, an etched silicon sheet or wafer preferably has a thickness of around 5 to 200 μm.

It will be appreciated that detached pillars may have the same shape and dimensions as pillars described above. The detached silicon may include porous silicon fragments, discrete detached silicon pillars and silicon pillar clumps.

Figures 2A-2C illustrate etching of only one surface of a silicon starting material, however it will be appreciated that more than one surface of a starting material may be etched. For example, opposing surfaces of wafers or sheets as illustrated in Figures 2A-2C may be etched by depositing copper on each surface followed by etching of each surface. If more than one surface is to be etched then copper deposition and etching may be carried out on a first surface to be etched, and the one or more further surfaces to be etched may be treated likewise in sequence. Alternatively, one or both of copper deposition and etching may occur simultaneously at more than one surface. For example, simultaneous etching may take place by arranging a substrate carrying copper on more

than one surface such that the two or more of the surfaces carrying copper are exposed to the etching composition.

In an embodiment, a starting substrate having a silicon surface, such as a silicon wafer or sheet, may be broken into a plurality of smaller silicon structures before or after etching. In this embodiment, the starting silicon wafer or sheet is preferably thin, e.g. a silicon wafer having a thickness of around 10 to 50 μm. Preferably, the starting substrate is broken gently in order to minimise disturbance and / or damage to the crystalline structure and crystal orientation of the wafer. The starting silicon structure may be broken into particles having an average length of no more than about 500 microns. Average lengths may be determined by taking an SEM image of one or more samples of the broken wafer particles and measuring lengths of particles shown in the image or images.

Figures 2A - 2C illustrate a process of etching a silicon wafer or sheet, however it will be appreciated that the same process may be applied to etching of silicon particles, as described in more detail below, in order to form pores and / or pillars on the surface of the silicon particles.

Pillars may be formed by etching the silicon surface to a depth of more than 0.5 microns, optionally at least 1 micron, optionally at least 2 microns, optionally no more than 10 microns. Optionally, the pillars are formed by etching the silicon surface to a depth in the range of 2-10 microns.

The pillars may have a diameter or thickness in the range of about 0.02 to 0.70 μm, e.g. 0.1 to 0.5μm, for example 0.1 to 0.25μm, preferably in the range 0.04 to 0.50μm. The pillars may have an aspect ratio (defined as the height of the pillar divided by the average thickness or diameter of the pillar at its base) in the range 5:1 to 100:1, preferably in the range 10:1 to 100:1. The pillars may be substantially circular in cross-section but they need not be. Where the pillars have irregular cross-sections comprising a plurality of extended sections with changing direction and/or with branches or spurs then the average thickness of the plurality of such section is used in the calculation of the aspect ratio. The

pillars may extend outwards from the silicon in any direction and may comprise kinks or changes in direction along their length.

The surfaces of pores or pillars may be relatively smooth or they may be rough. The surfaces may be pitted or comprise pores or voids with diameters less than 50nm. The pillar structures may be mesoporous or microporous.

The porosity of the etched silicon may be defined as the percentage ratio of the total volume of the void space or pores introduced into the etched silicon to the volume of the silicon before etching. A higher porosity may provide a higher surface area which may increase the reactivity of the silicon in a device, for example in electrochemical cells, sensors, detectors, filters etc. or it may provide a larger volume for containing ingredients or active agents in medical or consumer product compositions. However, if the porosity is too large the structural integrity (or mechanical strength) of the silicon may be reduced and for example, in devices such as a lithium ion battery, the volume of electrochemically active silicon material is reduced. The porosity of the etched silicon may be at least 5%, optionally at least 10%. Preferably it is at least 20%. The porosity may be less than 90%, optionally less than 80%. Preferably it is no more than 75%.

Dimensions of pores and pillars may be measured using optical methods, for example scanning electron microscopy. Porosity may be measured using known gas or mercury porosimetry techniques or by measuring the mass of the silicon material before and after etching.

Without wishing to be bound by any theory, it is believed that electroless formation of elemental copper includes a first stage during which copper islands are formed that then may extend laterally and join together to form a copper layer. This copper layer may be a monolayer formed by joining together of multiple copper monolayer islands. Further copper deposition results in uniform thickness growth of the copper layer. This is in contrast to electroless formation of silver, which is believed to form clumps of silver interconnected by dendrites, each clump having a thickness of multiple silver atoms.

It will be appreciated that etching of islands of copper as illustrated in Figures 2A and 2B allows formation of pores or pillars. Furthermore, and again without wishing to be bound by any theory, it is believed that a monolayer of copper formed by joining of copper islands will not cover 100% of an underlying silicon surface because packing of an electrolessly formed monolayer of copper, for example by hexagonal packing, and that etching with such a monolayer may still produce a pattern of pores or pillars in the silicon surface.

However, and again without wishing to be bound by any theory, once the copper layer thickness exceeds a monolayer or once the copper layer otherwise covers substantially all of the silicon surface, it is believed that gases generated during etching may have no path for escape from the silicon, resulting in these gases pressing against the underside of the copper layer which in turn may result in poor etching of the silicon. Furthermore, in this case HF and oxidant contained within the etching solution may be blocked by the copper layer from reaching the silicon surface.

However the coverage of the silicon surface by copper must be sufficient enough to achieve the desired porosity or pillar density and dimensions. Preferably at least 10% of the silicon surface to be etched should be covered by the copper layer, optionally at least 20%, at least 50 % or at least 75 %. Copper surface coverage may be less than 99 % or less than 95 %. Copper surface coverage may be measured using optical methods, for example scanning electron microscopy or other known analytical techniques such as electron back-scattered diffractometry or energy dispersive x-ray spectrometry.

Accordingly, in one embodiment, the copper metal formed on the surface of the silicon during the inventive process is in the form of a monolayer and / or in the form of a plurality of isolated islands of copper.

Following formation of the etched silicon structure, residual copper in the etched silicon structure and / or on the surface of the etched silicon structure may be washed out or chemically removed. Alternatively, the residual copper may be retained, for example to improve conductivity of the silicon. The etched silicon structure containing residual

copper may be annealed to form copper silicide, which may improve copper-silicon adhesion.

Silicon

The one or more silicon surfaces of a substrate to be etched may be undoped, n-doped, p-doped or a mixture thereof. Preferably, the silicon is n- or p-doped. Examples of p-type dopants for silicon include B, Al, In, Mg, Zn, Cd and Hg. Examples of n-type dopants for silicon include P, As, Sb and C. Dopants such as germanium and silver can also be used.

The silicon substrate may be a material having silicon at one or more surfaces thereof and a non-silicon core. Examples include particles having a non-silicon (e.g. graphite) core and silicon shell, and a sheet having a non-silicon core sandwiched by silicon layers.

The silicon to be etched may be supported on a surface of another material.

The silicon may be pure silicon or may be an alloy or other mixture of silicon and one or more other materials. The silicon may have a purity of at least 90.00 wt%, optionally at least 99 wt%. Optionally the silicon purity may be less than 99.9999 wt%. The silicon may be metallurgical grade silicon.

The silicon may have a resistivity of at least 0.005 Ω.cm, optionally at least 0.01 Ω.cm, optionally at least 1Ω.cm. The silicon resistivity may be up to about 100 Ω.cm.

The silicon surface of the substrate is optionally selected from (100) and (111) silicon, or a silicon surface that is symmetrically equivalent to (100) or (111) silicon, denoted hereinafter as {100} and {111} silicon respectively. It will be understood that {100} silicon includes the symmetrically equivalent group of planes (100) (010) and (001).

It will be understood that the substrate may include one or more {100} or {111} silicon surfaces and one or more silicon surfaces other than {100} or {111} silicon. For example, flakes of silicon may have at least one (100) or (111) surface and one or more other silicon surfaces.

Etching may be carried out on, for example, bulk silicon or on a silicon powder. Exemplary bulk silicon structures include silicon sheets such as silicon wafers or of metallurgical grade silicon, and silicon sheets or chips formed by breaking a silicon wafer into smaller pieces, or by breaking other forms of bulk silicon into sheets or flakes. Powder particles of silicon may be formed from a silicon source such as metallurgical grade silicon by any process known to the skilled person, for example by grinding or jetmilling bulk silicon to a desired size. Suitable example silicon powders are available as "Silgrain™" from Elkem of Norway.

Where used, bulk silicon such as a silicon wafer may have first and second opposing surfaces, each surface having an area of at least 0.25 cm^2, optionally at least 0.5 cm^2, optionally at least 1 cm^2. Each surface may be substantially planar. Bulk silicon may have a thickness of more than 0.5 micron, optionally more than 1 micron, optionally more than 10 microns, optionally more than 100 microns, optionally in the range of about 100 – 1000 microns.

Where used, particles may be in the form of flakes or wires, or cuboid, substantially spherical or spheroid particles. They may be multifaceted or may have substantially continuous curved surfaces. Non-spherical core particles may have an aspect ratio of at least 1.5 : 1, optionally at least 2 : 1. Silicon flakes preferably have an aspect ratio of at least 2 : 1.

The particles may have a size with a largest dimension up to about 100µm, preferably less than 50µm, more preferably less than 30µm.

The particles may have at least one smallest dimension less than one micron. Preferably the smallest dimension is at least 0.5 microns.

Particle sizes may be measured using optical methods, for example scanning electron microscopy.

In a composition containing a plurality of particles, for example a powder, preferably at least 20%, more preferably at least 50% of the particles have smallest dimensions in the

ranges described above. Particle size distribution may be measured using laser diffraction methods or optical digital imaging methods.

Battery formation

Etched silicon formed as described herein may be used to form the anode of a rechargeable metal ion battery. The battery may be as described with reference to Figure 1.

In the case where bulk silicon is etched, an anode current collector may be formed on one side of the bulk silicon and another side of the bulk silicon having an etched surface may come into contact with the electrolyte of the battery. The current collector may be a metal foil, for example copper, nickel or aluminium, or a non-metallic current collector such as carbon paper

The present inventors have found that etching may be carried out with a relatively small quantity of copper ions as compared to a corresponding process using silver ions. Accordingly, in one embodiment etched bulk silicon, such as a silicon wafer, may be used to form the anode of a metal ion battery without first washing or otherwise treating the bulk silicon to remove residual metal in the wafer. Residual copper present in the wafer may serve to increase conductivity of the anode. Etched silicon containing copper may be annealed to form copper silicide at the copper-silicon interface to improve adhesion of the copper to the silicon.

In the case where the silicon is in particulate forma slurry comprising the particulate silicon and one or more solvents may be deposited over an anode current collector to form an anode layer. The silicon particles may be one or more of etched silicon particles formed by etching a particulate starting material or by fracturing a larger starting material; porous silicon fragments detached from an etched porous silicon surface; and discrete silicon fibres or clumps of silicon fibres formed by detaching silicon pillars from an etched silicon surface. Silicon particles may be provided as a powder of the particles. The slurry may further comprise a binder material, for example polyimide, polyacrylic acid (PAA) and alkali metal salts thereof, polyvinylalchol (PVA) and polyvinylidene

fluoride (PVDF), sodium carboxymethylcellulose (Na-CMC) and optionally, non-active conductive additives, for example carbon black, carbon fibres, ketjen black or carbon nanotubes. In addition to providing the silicon particles to act as an active material in the battery, one or more further active materials may also be provided in the slurry. Exemplary further active materials include active forms of carbon such as graphite or graphene,. Active graphite may provide for a larger number of charge / discharge cycles without significant loss of capacity than active silicon, whereas silicon may provide for a higher capacity than graphite. Accordingly, an electrode composition comprising a silicon-containing active material and a graphite active material may provide a lithium ion battery with the advantages of both high capacity and a large number of charge / discharge cycles. The slurry may be deposited on a current collector, which may be as described above. Further treatments may be done as required, for example to directly bond the silicon particles to each other and/or to the current collector. Binder material or other coatings may also be applied to the surface of the composite electrode layer after initial formation.

Examples of suitable cathode materials include $LiCoO_2$, $LiCo_{0.99}Al_{0.01}O_2$, $LiNiO_2$, $LiMnO_2$, $LiCo_{0.5}Ni_{0.5}O_2$, $LiCo_{0.7}Ni_{0.3}O_2$, $LiCo_{0.8}Ni_{0.2}O_2$, $LiCo_{0.82}Ni_{0.18}O_2$, $LiCo_{0.8}Ni_{0.15}Al_{0.05}O_2$, $LiNi_{0.4}Co_{0.3}Mn_{0.3}O_2$ and $LiNi_{0.33}Co_{0.33}Mn_{0.34}O_2$. The cathode current collector is generally of a thickness of between 3 to 500µm. Examples of materials that can be used as the cathode current collector include aluminium, stainless steel, nickel, titanium and sintered carbon.

The electrolyte is suitably a non-aqueous electrolyte containing a lithium salt and may include, without limitation, non-aqueous electrolytic solutions, solid electrolytes and inorganic solid electrolytes. Examples of non-aqueous electrolyte solutions that can be used include non-protic organic solvents such as propylene carbonate, ethylene carbonate, butylenes carbonate, dimethyl carbonate, diethyl carbonate, gamma butyro lactone, 1,2-dimethoxy ethane, 2-methyl tetrahydrofuran, dimethylsulphoxide, 1,3-dioxolane, formamide, dimethylformamide, acetonitrile, nitromethane, methylformate, methyl acetate, phosphoric acid trimester, trimethoxy methane, sulpholane, methyl sulpholane and 1,3-dimethyl-2-imidazolidione.

Examples of organic solid electrolytes include polyethylene derivatives polyethyleneoxide derivatives, polypropylene oxide derivatives, phosphoric acid ester polymers, polyester sulphide, polyvinyl alcohols, polyvinylidine fluoride and polymers containing ionic dissociation groups.

Examples of inorganic solid electrolytes include nitrides, halides and sulphides of lithium salts such as Li_5NI_2, Li_3N, LiI, $LiSiO_4$, Li_2SiS_3, Li_4SiO_4, LiOH and Li_3PO_4.

The lithium salt is suitably soluble in the chosen solvent or mixture of solvents. Examples of suitable lithium salts include LiCl, LiBr, LiI, $LiClO_4$, $LiBF_4$, $LiBC_4O_8$, $LiPF_6$, $LiCF_3SO_3$, $LiAsF_6$, $LiSbF_6$, $LiAlCl_4$, CH_3SO_3Li and CF_3SO_3Li.

Where the electrolyte is a non-aqueous organic solution, the battery is provided with a separator interposed between the anode and the cathode. The separator is typically formed of an insulating material having high ion permeability and high mechanical strength. The separator typically has a pore diameter of between 0.01 and 100μm and a thickness of between 5 and 300μm. Examples of suitable electrode separators include a micro-porous polyethylene film.

Etched silicon structures comprising pores or elongated pillar-like structures, porous silicon fragments or detached silicon fibres as described herein may be used in a wide range of applications in addition to rechargeable metal ion batteries including, without limitation, electrochemical cells, lithium air batteries, flow cell batteries, other energy storage devices such as fuel cells, thermal batteries, photovoltaic devices such as solar cells, filters, sensors, electrical and thermal capacitors, microfluidic devices, gas/vapour sensors, thermal or dielectric insulating devices, devices for controlling or modifying the transmission, absorption or reflectance of light or other forms of electromagnetic radiation, chromatography or wound dressings.

Porous silicon particles may also be used for the storage, controlled delivery or timed release of ingredients or active agents in consumer care products including oral hygiene and cosmetic products, food or other nutritional products, or medical products including pharmaceutical products that deliver drugs internally or externally to humans or animals.

Etched silicon may also form architectured conducting or semiconducting components of electronic circuitry.

Examples

General procedure

In a first stage, a n-doped silicon wafer (about 1 cm^2) having (100) orientation and having a resistivity in the range of about 1-10 Ω.cm was placed in 50ml of a first solution of HF and either $CuSO_4$ or $Cu(NO_3)_2$. Copper is allowed to form on the surface of the silicon wafer for a first period of time, after which the silicon wafer carrying copper is gently rinsed with deionised water.

In a second stage, the silicon wafer was then placed in a second solution of HF and NH_4NO_3 for at least 30 minutes to form etched silicon.

In an optional third step, the etched silicon wafer was washed with water.
The surface of only one side of a silicon wafer is etched in this general procedure, however it will be appreciated that surfaces on both sides of a silicon wafer may be etched by carrying out the general procedure on both sides of the wafer. Each of the copper deposition and etching steps may be carried out on one surface at a time, or on both surfaces simultaneously.

Examples 1-5

In the first stage, a silicon wafer was placed in a first solution of 20mM $CuSO_4$ +7M HF, and in the second stage the wafer was placed in a second solution of 0.2M NH_4NO_3 +7M HF for 3 hours. Both stages were carried out at room temperature.

The wafer was kept in the first solution for the periods of time shown in Table 1 below.

Table 1

Example	Time in first solution (seconds)	Figures
1	10	3
2	20	4A and 4B
3	60	5A and 5B
4	90	6A and 6B
5	120	7A and 7B

With reference to Figures 3-7, it can be seen that the density and / or length of pillars is generally greater at shorter times in the first solution.

Without wishing to be bound by any theory, it is believed that this is due to formation of a uniform copper film of more than monolayer thickness at longer times in the first solution, which results in substantially isotropic etching of the underlying silicon, and / or prevents escape of gases (in particular hydrogen) generated during the etching process. This can be seen in Figures 8 and 9, which illustrate the surface of silicon after 20 seconds and after 120 seconds in the first solution respectively. Figure 8 shows a plurality of isolated islands of copper formed on the surface of the silicon wafer, whereas Figure 9 shows a substantially uniform film of copper on the surface of the silicon wafer.

Accordingly, in one embodiment it is preferred that the silicon is exposed to the first solution for a relatively short period of time, and that the second solution is substantially free of copper. In this example, the second solution comprises ammonium nitrate, however it will be appreciated that other water-soluble nitrates may be used, in particular metal nitrates other than copper nitrate.

Example 2 was repeated except that 10 wt% methanol was included in the second solution. The extent of etching was found to be considerably reduced as compared to Example 2, producing silicon with a small number of shallow pores.

Example 6

A silicon wafer was treated as described in Example 2, except that the second stage was conducted at a temperature of 60 – 70°C.

With reference to Figure 10A and the magnified image of Figure 10B, the extent of etching is lower than that of Example 2 (Figures 4A and 4B), illustrating that the extent of etching may be controlled, at least in part, by the etching temperature.

Examples 7 and 8

A silicon wafer was treated as described in Example 2, except that the concentration of NH_4NO_3 was 0.4 M in Example 7, and 0.6 M in Example 8.

No significant difference was observed in the etched silicon produced in Examples 2, 7 and 8.

Examples 9-12

A silicon wafer was treated according to the general method wherein in the first stage a silicon wafer was placed in a solution of 20mM $CuSO_4$ +7M HF for 30 seconds, and in the second stage the wafer was placed in a solution of 0.2M NH_4NO_3 +7M HF for 1.5 hours. Both stages were carried out at room temperature.

The resistivity and doping of the wafer was varied as illustrated in Table 2 below.

Table 2

Example	**Si doping**	**Si resistivity (Ω.cm)**	**Figures**
9	n-doped	0.01~0.03 Ω.cm	11A and 11B

10	n-doped	0.08~0.1 Ω.cm	12A and 12B
11	n-doped	1~10 Ω.cm	13A and 13B
12	p-doped	1~10 Ω.cm	14A and 14B

Pillars were formed in all cases, as shown in Figures 11 – 14. However, at lower resistivities, in particular up to about 0.001 Ω.cm, it was found that etching tended to be more isotropic.

Example 13

A silicon wafer was treated according to the general method, except that silicon having the (110) orientation was etched.

In the first stage the silicon wafer was placed in a solution of 20mM $CuSO_4$ +7M HF for 20 seconds, and in the second stage the wafer was placed in a solution of 0.2M NH_4NO_3 +7M HF for 1.5 hours.

The etching process produced pores rather than pillars in the silicon, as shown in Figures 15A and 15B, in contrast to the pillars formed in the analogous process using silicon wafers having the (100) orientation, as described with reference to Examples 1-5.

Example 14

A silicon wafer was treated according to the general method, except that silicon having the (110) orientation was used, and the silicon was cleaved. The cleaved edge has a (111) plane.

In the first stage the cleaved silicon wafer was placed in a solution of 0.2M $CuSO_4$ +7M HF for 30 seconds, and in the second stage the wafer was placed in a solution of 0.2M NH_4NO_3 +7M HF for 1.5 hours.

Figure 16A shows the (110) surface on top of the cleaved wafer, and the (111) surface is below. A clear difference can be seen in etching of the (111) and (110) surfaces, with deeper etching of the (111) surface.

Figure 16B is a magnification of the etched (111) surface of Figure 16A.

Example 15

A silicon wafer was treated according to the general method, except that silicon having a (111) orientation was used, and the resistivity of the wafer was in the range of about 0.0008 – 0.001 Ω.cm.

In the first stage the cleaved silicon wafer was placed in a solution of 20mM $CuSO_4$ +7M HF for 30 seconds, and in the second stage the wafer was placed in a solution of 0.2M NH_4NO_3 +7M HF for 1.5 hours.

With reference to Figure 17, it can be seen that the degree of anisotropic etching is less at this low resistivity than etching of (111) silicon at a higher resistivity, as shown in Figures 16A and 16B. White spots present in Figure 17 may be an etching by-product.

Example 16

The silicon wafer in this example was a thin (100) n-doped (boron) silicon wafer with a thickness of around 20 μm and having a resistivity of 1-20 Ohm-cm.

The silicon wafer is treated according to the general method wherein in the first stage a silicon wafer was placed in a solution of 20mM $CuSO_4$ + 7M HF for 30 seconds, and in the second stage the wafer was placed in a solution of 0.2mM NH_4NO_3 + 7M HF for 30 minutes.

With reference to Figure 18A and magnified image 18B, pillars were formed to a height of 2μm.

The etched wafer was then broken by gentle application of pressure to produce etched fragments as illustrated in Figure 18C. A magnified image of a fragment formed by

fragmentation of the wafer is shown in Figure 18D, showing pillars extending from the wafer fragment.

The silicon wafer of this example was etched on one surface only, however it will be appreciated that the etching process could have been repeated on the surface opposing the etched surface in order to form a silicon wafer having

Example 17

The silicon wafer in this example p-type, (100), 1~100 Ω.cm silicon wafer with a thickness of around 200 μm.

The silicon wafer is treated according to the general method, wherein in the first stage a silicon wafer was placed in a solution of 20mM $CuSO_4$ + 7M HF for 30 seconds, and in the second stage the wafer was placed in a solution of 0.2M NH_4NO_3 + 7M HF for 30 minutes.

The pillars of the etched silicon wafer were then scraped off with a razor blade to provide discrete silicon fibres and clumps of fibres as illustrated by Figures 19A and 19B.

Example 18

1g of silicon powder available from Elkem having a diameter in the range of 200 – 800 microns and a purity of 99.8% was treated as described with reference to Example 2.

Figure 20 illustrates pores formed on the surface of the silicon powder.

The etched silicon as described herein may be used to form the anode of a rechargeable metal ion battery.

The invention has been described with reference to anodes of rechargeable batteries that operate by absorption and desorption of lithium ions, however it will be appreciated that etched silicon structures as described herein may be applicable to other metal ion batteries, for example sodium or magnesium ion batteries. Moreover, it will be appreciated that etched silicon as described herein may be used in devices other than

metal ion batteries, for example filters, other energy storage devices such as fuel cells, photovoltaic devices such as solar cells, sensors, and capacitors. Etched silicon as described herein may also form conducting or semiconducting components of electronic circuitry.

Although the present invention has been described in terms of specific exemplary embodiments, it will be appreciated that various modifications, alterations and/or combinations of features disclosed herein will be apparent to those skilled in the art without departing from the scope of the invention as set forth in the following claims.

Claims

1. A method of etching silicon, the method comprising the steps of: partially covering at least one silicon surface of a material to be etched with copper metal; and exposing the at least one surface to an aqueous etching composition comprising an oxidant and a source of fluoride ions.

2. A method according to claim 1 wherein at least some of the copper metal is formed on the at least one surface of the material to be etched by an electroless deposition process.

3. A method according to claim 2 wherein the electroless deposition process comprises exposing the at least one surface of the material to be etched to an aqueous deposition composition comprising a copper salt and a source of fluoride ions.

4. A method according to claim 3 wherein the oxidant is selected from the group consisting of O_2; O_3; and the acid or salt of NO_3^-, $S_2O_8^{2-}$, NO_2^-, $B_4O_7^{2-}$ or ClO_4^- or a mixture thereof.

5. A method according to claim 4 wherein the oxidant is selected from the group consisting of alkali metal nitrates, ammonium nitrate and mixtures thereof.

6. A method according to any preceding claim wherein the aqueous etching composition is substantially free of copper ions.

7. A method according to any of claims 3-5 wherein the aqueous etching composition is formed by adding the oxidant and, optionally, further fluoride ions to the aqueous deposition composition.

8. A method according to claim 7 wherein the oxidant and optional further fluoride ions are added in aqueous form, and wherein the concentration of copper ions is diluted by addition of the aqueous oxidant and optional further fluoride.

9. A method according to claim 8 wherein the concentration of copper ions is diluted by addition of the aqueous oxidant and optional further fluoride to substantially stop further electroless deposition of copper once the electrolessly deposited copper has formed of a plurality of isolated islands of copper, the isolated islands optionally having a diameter in the range of 50-200 nm, optionally 50-100 nm.

10. A method according to claim 8 or 9 wherein the concentration of copper ions is diluted by addition of the aqueous oxidant and optional further fluoride to substantially stop further electroless deposition of copper once the electrolessly deposited copper has formed a monolayer of copper.

11. A method according to any of claims 3-6 wherein the material to be etched is removed from the aqueous deposition composition following electroless deposition and before being exposed to the aqueous etching composition.

12. A method according to claim 11 wherein the electrolessly deposited copper forms of a plurality of isolated islands of copper, and wherein the material to be etched is removed from the first aqueous composition to provide the plurality of isolated islands of copper on the at least one silicon surface, the isolated islands optionally having a diameter in the range of 50-200 nm.

13. A method according to claim 11 or 12 wherein the electrolessly deposited copper forms a monolayer of copper, and wherein the material to be etched is removed from the first aqueous composition to provide the monolayer of copper on the at least one silicon surface.

14. A method according to any preceding claim wherein the at least one surface is etched to form silicon pillars extending from an etched silicon surface formed by etching of the at least one surface.

15. A method according to claim 14 comprising the further step of detaching the silicon pillars from the etched silicon surface.

16. A method according to any preceding claim wherein the source of fluoride ions in the aqueous etching composition is hydrogen fluoride.

17. A method according to any of claims 3-16 wherein the source of fluoride ions in the aqueous deposition composition is hydrogen fluoride.

18. A method according to claim 16 or 17 wherein the concentration of hydrogen fluoride in the aqueous deposition composition and in the aqueous etching composition is independently in the range of 1 to 10 M.

19. A method according to any of claims 3-18, wherein the concentration of the copper salt in the aqueous deposition composition is in the range of 0.001 to 5 M.

20. A method according to any preceding claim wherein the aqueous etching composition is substantially free of alcohols.

21. A method according to any of claims 3-20 wherein the at least one surface is exposed to the aqueous deposition composition for less than 2 minutes, optionally no more than 1 minute.

22. A method according to any preceding claim wherein the silicon has a resistivity of at least 0.005 Ω.cm.

23. A method according to claim 22 wherein the silicon has a resistivity of at least 0.01 Ω.cm.

24. A method according to any preceding claim, wherein the silicon is n-doped, p-doped or a mixture thereof.

25. A method according to any preceding claim wherein the at least one surface to be etched has a {111} or {100} orientation.

26. A method according to claim 25, wherein the material to be etched has a (111) or (100) orientation.

27. A method according to any preceding claim, wherein the method is conducted at a temperature of 0°C to 30°C, optionally about 20°C.

28. A method according to any preceding claim wherein a bias is not applied to the silicon during etching of the material to be etched.

29. A method according to any preceding claim wherein the at least one surface of the material to be etched is etched to a depth of at least 0.5 microns.

30. A method according to any preceding claim wherein the etched silicon comprises pores extending into at least one etched surface formed by etching the at least one surface.

31. A method according to claim 30 wherein the pores have a diameter of at least 50 nm.

32. A method according to any of claims 1-29 wherein the etched silicon comprises pillars extending out from at least one etched surface formed by etching the at least one surface.

33. A method according to claim32 wherein the pillars have a length of at least 0.5 microns.

34. A method according to any preceding claim wherein the material to be etched is in the form of bulk silicon, optionally a silicon wafer.

35. A method according to claim 34 comprising the step of breaking the etched bulk silicon into a plurality of etched bulk silicon fragments.

36. A method according to claim 35 wherein the plurality of etched bulk silicon fragments form a powder.

37. A method according to any of claims 1-33 wherein the material to be etched is in the form of a silicon powder.

38. A method according to claim 37 wherein the silicon powder comprises silicon flakes.

39. A method according to claim 38 wherein the silicon flakes have at least one surface having oriented {111} or {100} silicon.

40. A method according to any preceding claim wherein at least some of the copper metal is formed on the at least one surface of the material to be etched by a process selected from thermal evaporation and sputtering.

41. A method according to claim 40 wherein the copper metal is deposited on the at least one silicon surface through a patterned mask.

42. Etched silicon obtainable by a method according to any preceding claim.

43. An electrode comprising an active material of etched silicon according to claim 42.

44. An electrode according to claim 43, wherein the electrode further comprises a conductive current collector in electrical contact with the active material.

45. A method of forming an electrode according to claim 44, the method comprising the step of depositing onto the conductive current collector a slurry comprising one or more of detached silicon pillars formed according to the method of claim 15; silicon fragments formed according to the method of claim 35; or an etched silicon powder formed according to the method of claim 37 and at least one solvent, and evaporating the at least one solvent.

46. A method of forming an electrode according to claim 44, the method comprising the step of applying the conductive current collector to etched bulk silicon formed according to the method of claim 34.

47. A method according to claim 46 wherein residual copper in the etched bulk silicon is not removed prior to applying the conductive current collector.

48. A rechargeable metal ion battery comprising an anode, the anode comprising an electrode according to claim 43 or 44 capable of inserting and releasing metal ions; a cathode formed from a metal-containing compound capable of releasing and reabsorbing the metal ions; and an electrolyte between the anode and the cathode.

49. A rechargeable metal ion battery according to claim 48 wherein the metal ion battery is a lithium ion battery.

FIGURE 1

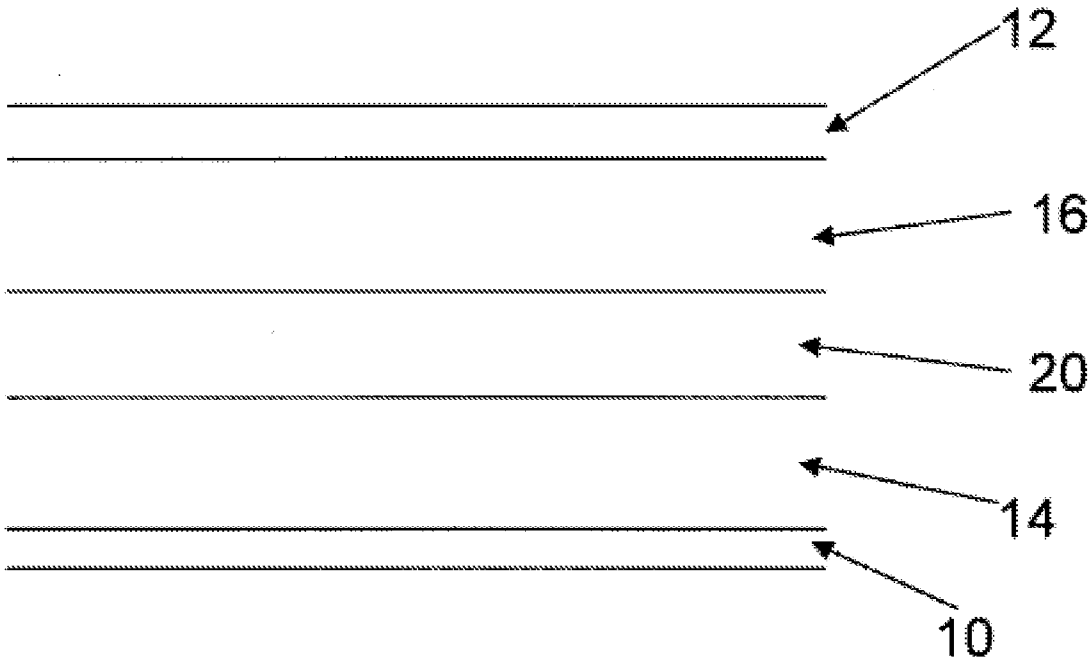


FIGURE 2A

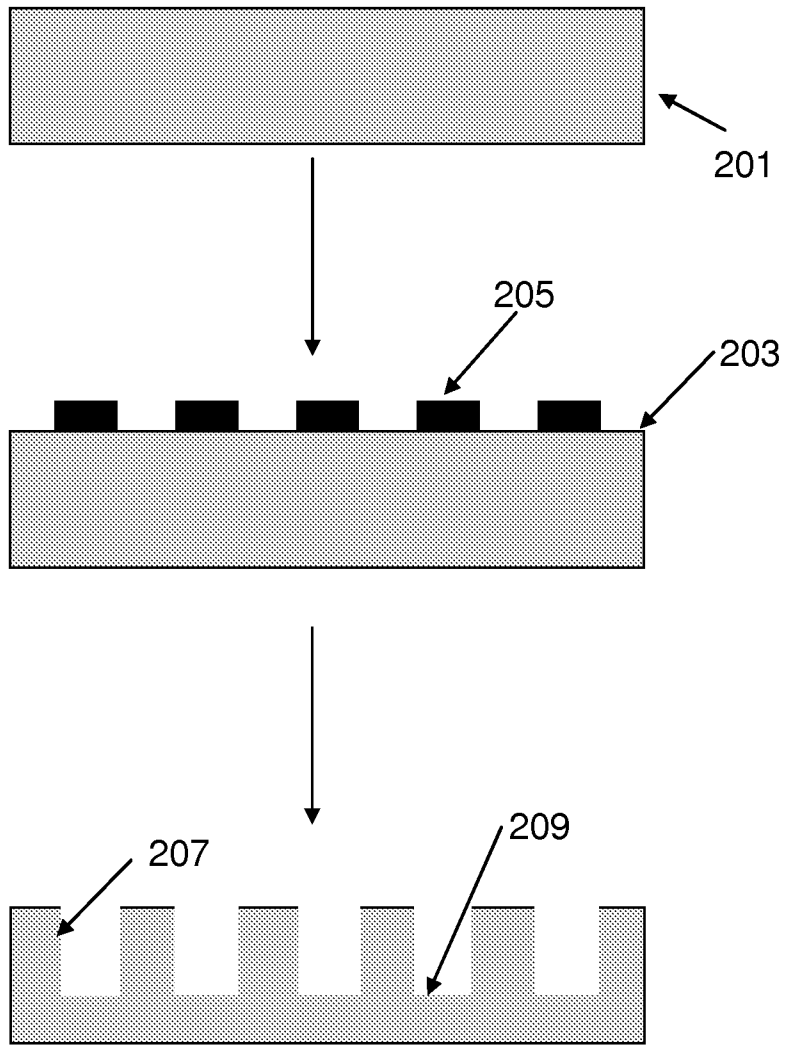


FIGURE 2B

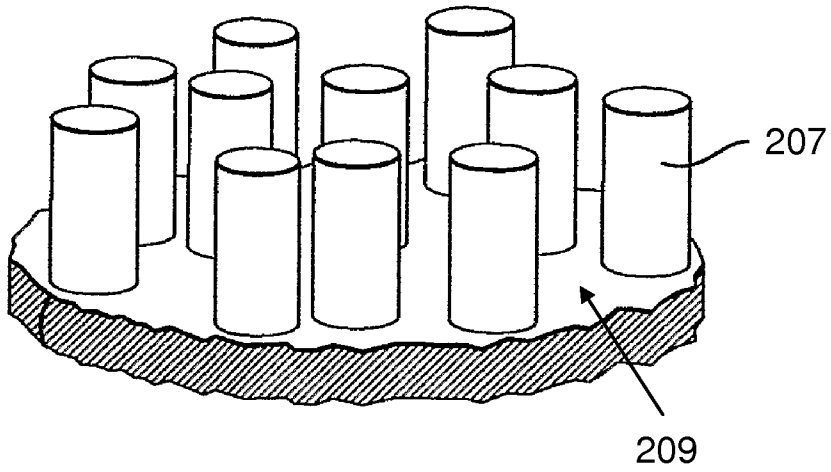


FIGURE 2C

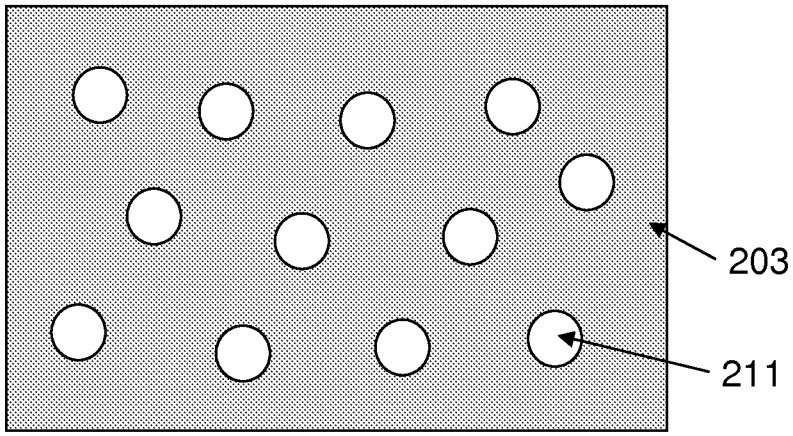


FIGURE 3

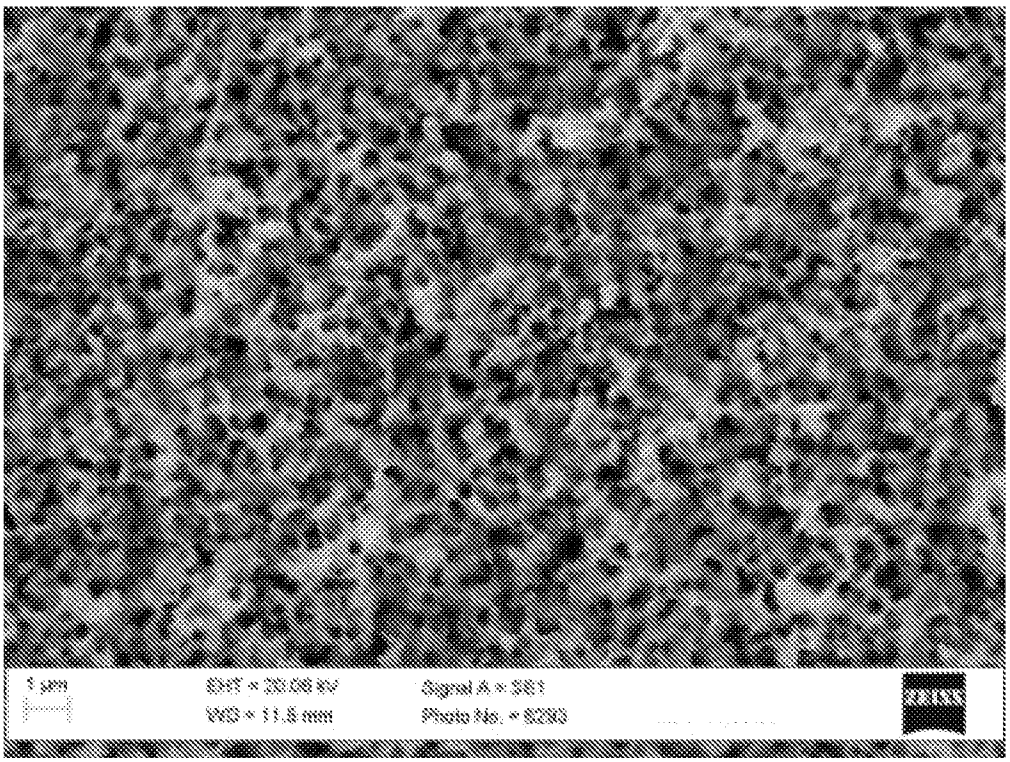


FIGURE 4A

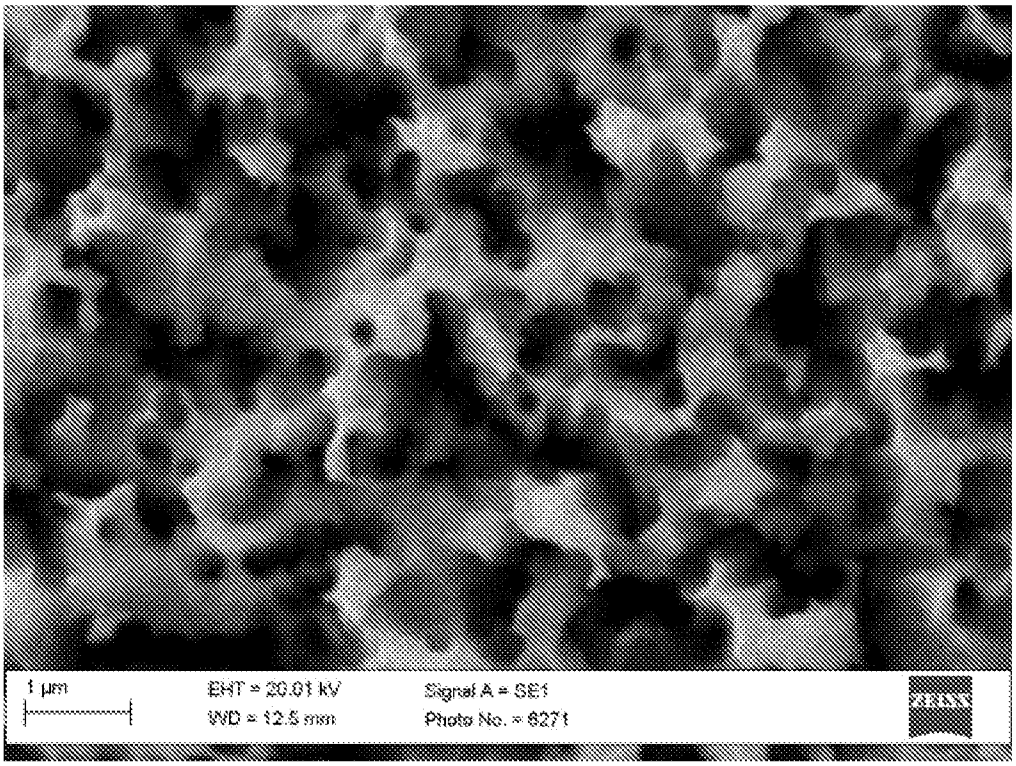


FIGURE 4B

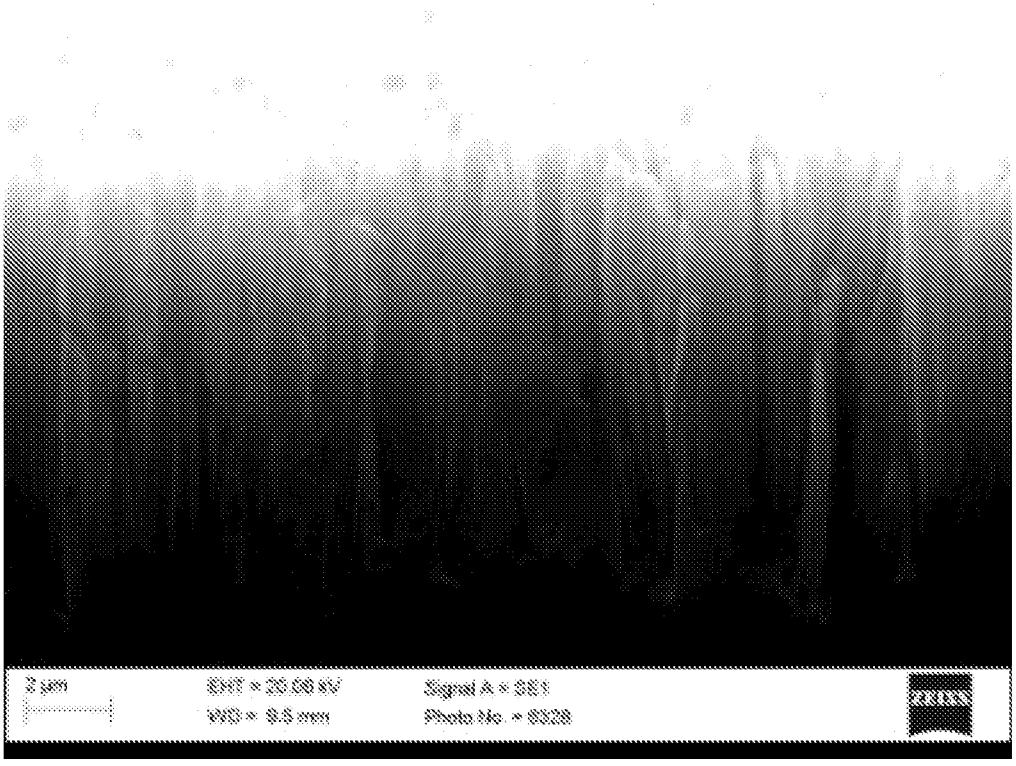


FIGURE 5A

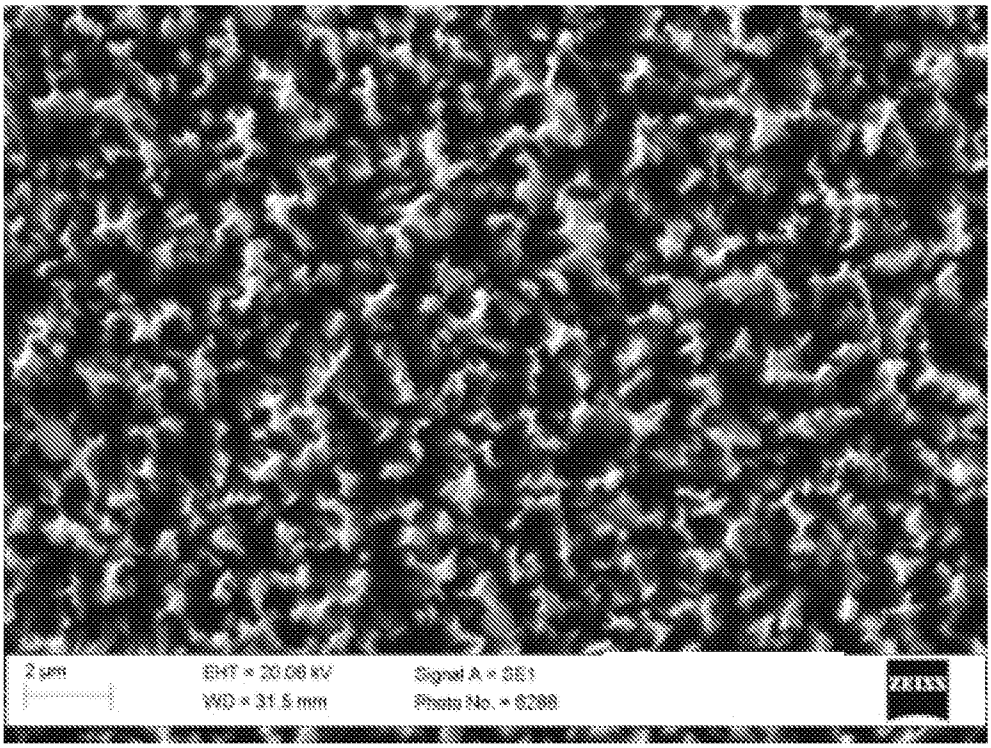
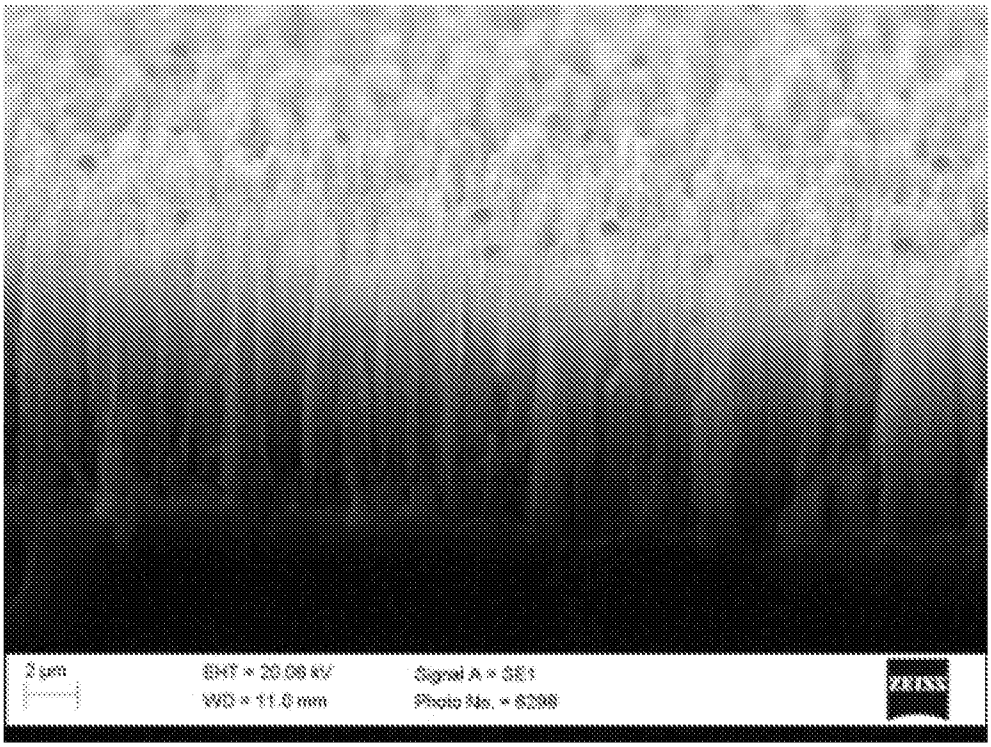


FIGURE 5B



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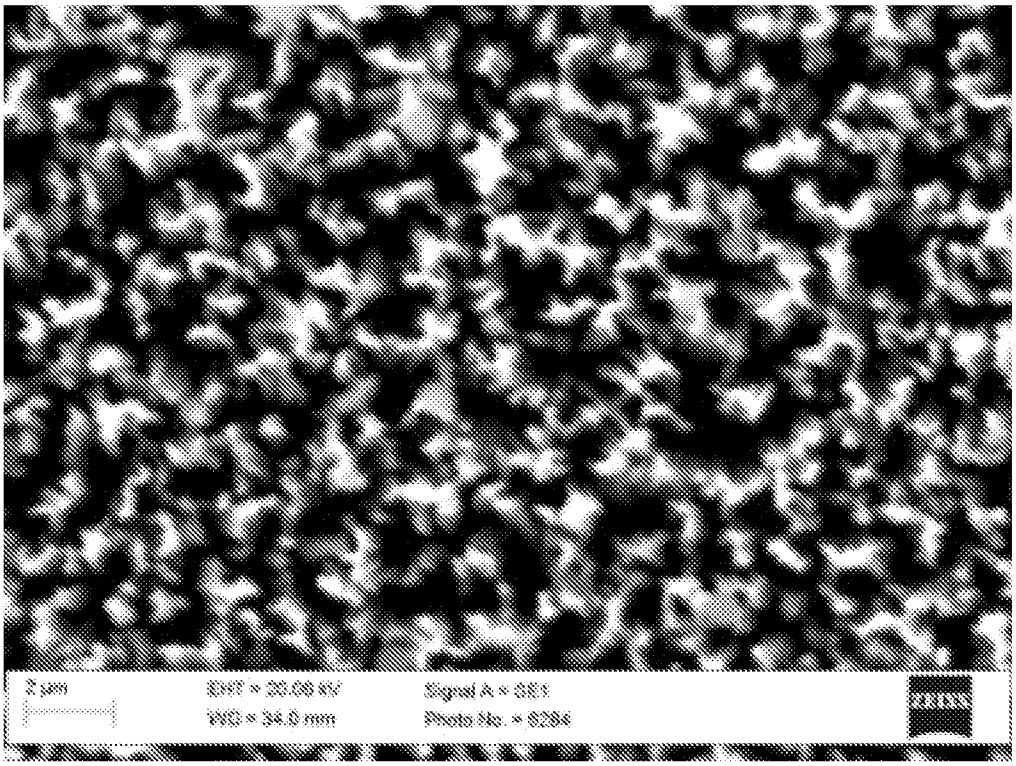
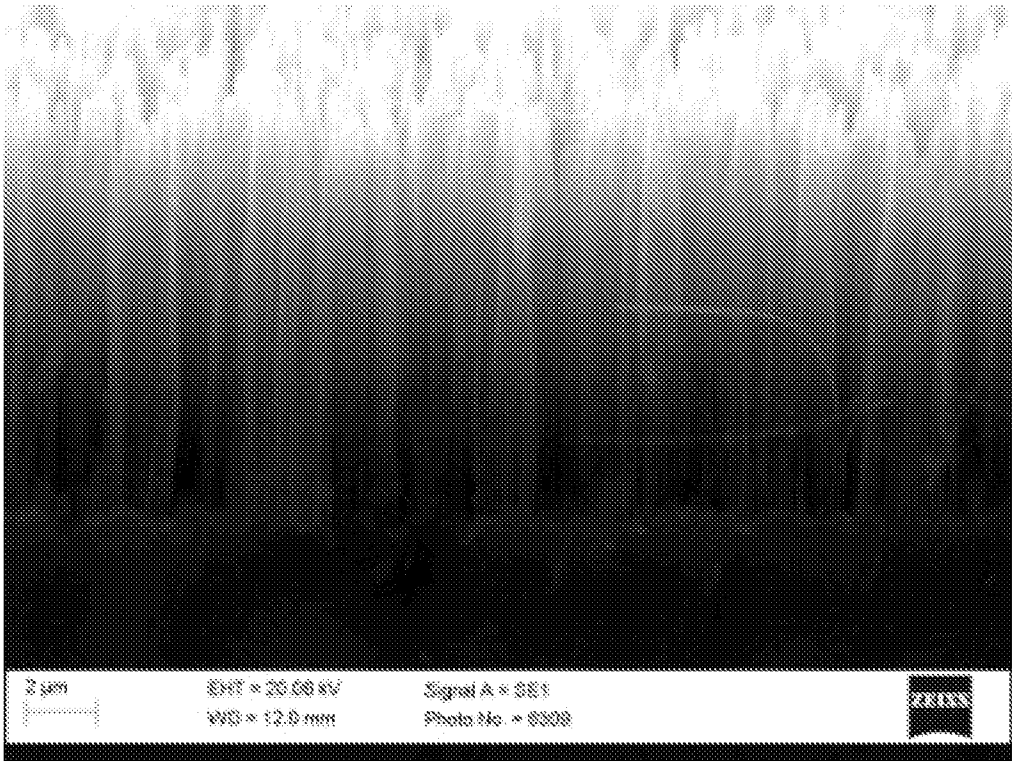


FIGURE 6B



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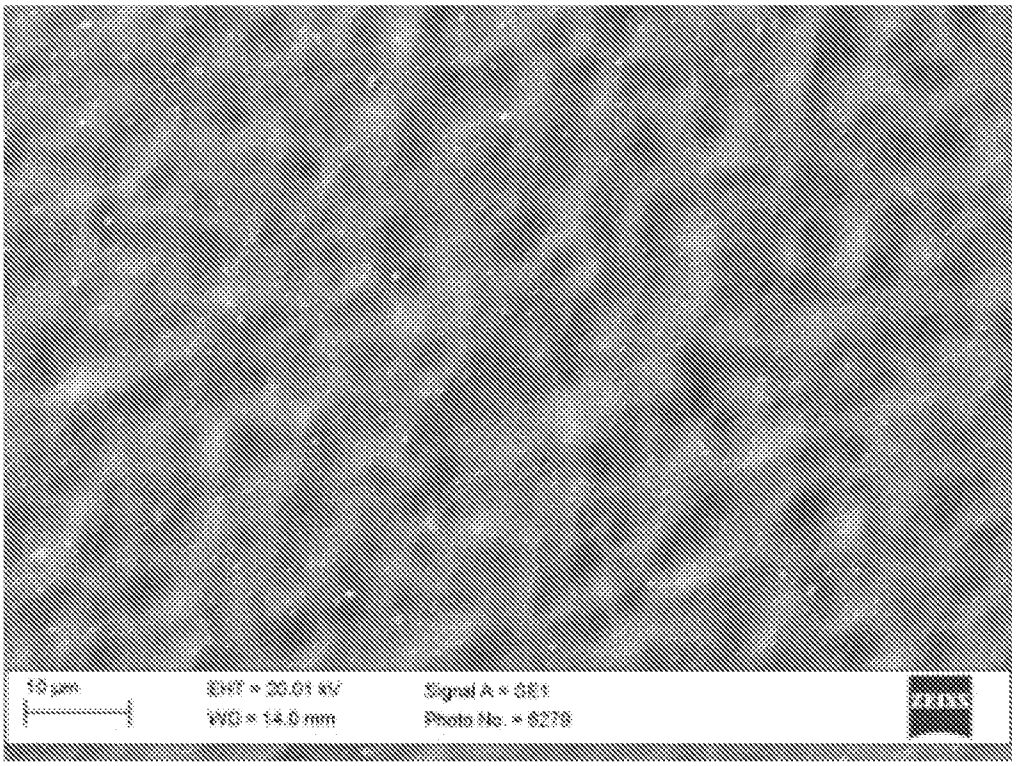


FIGURE 7B

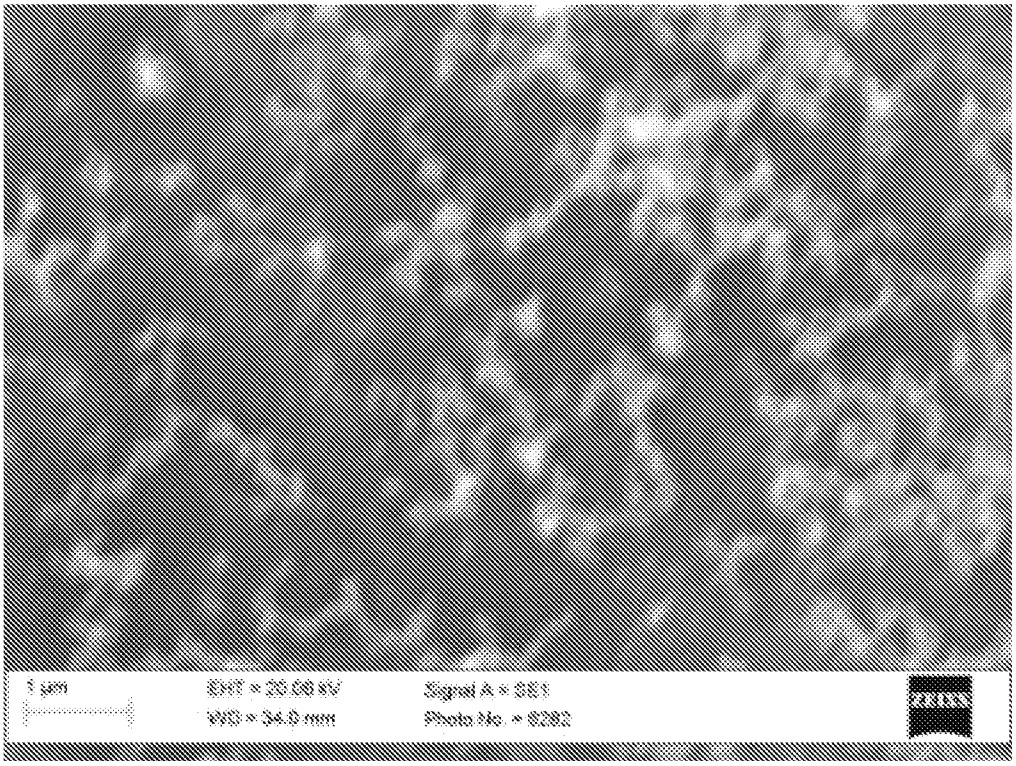


FIGURE 8

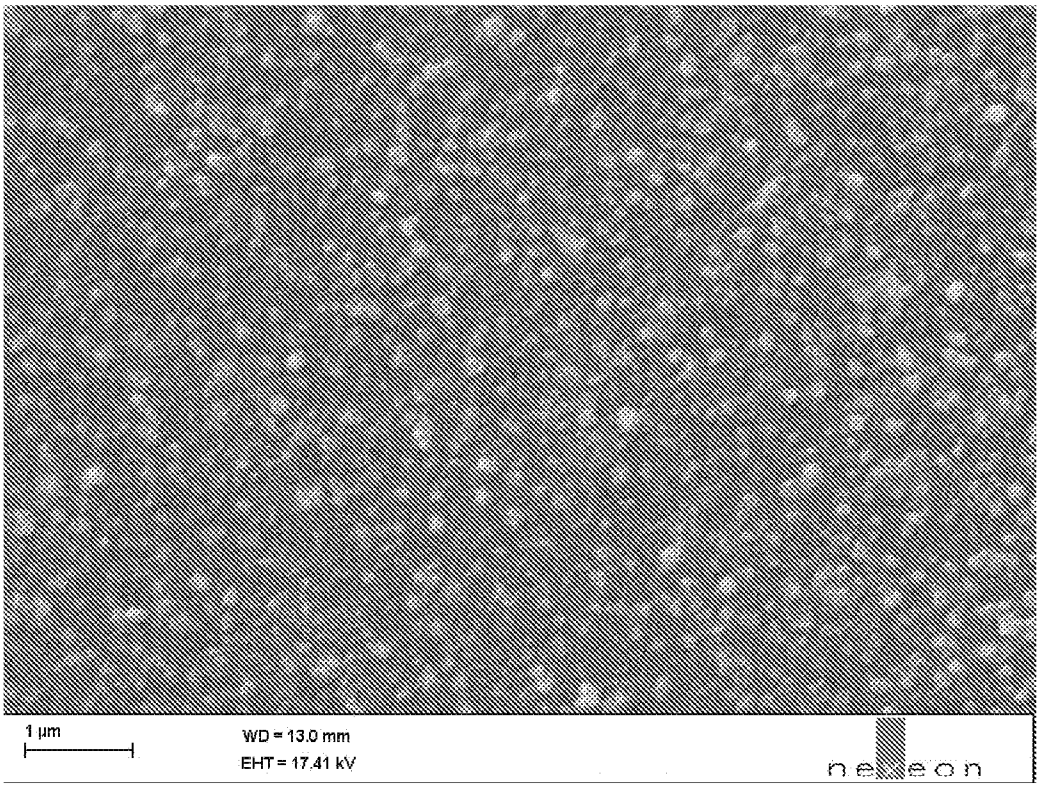


FIGURE 9

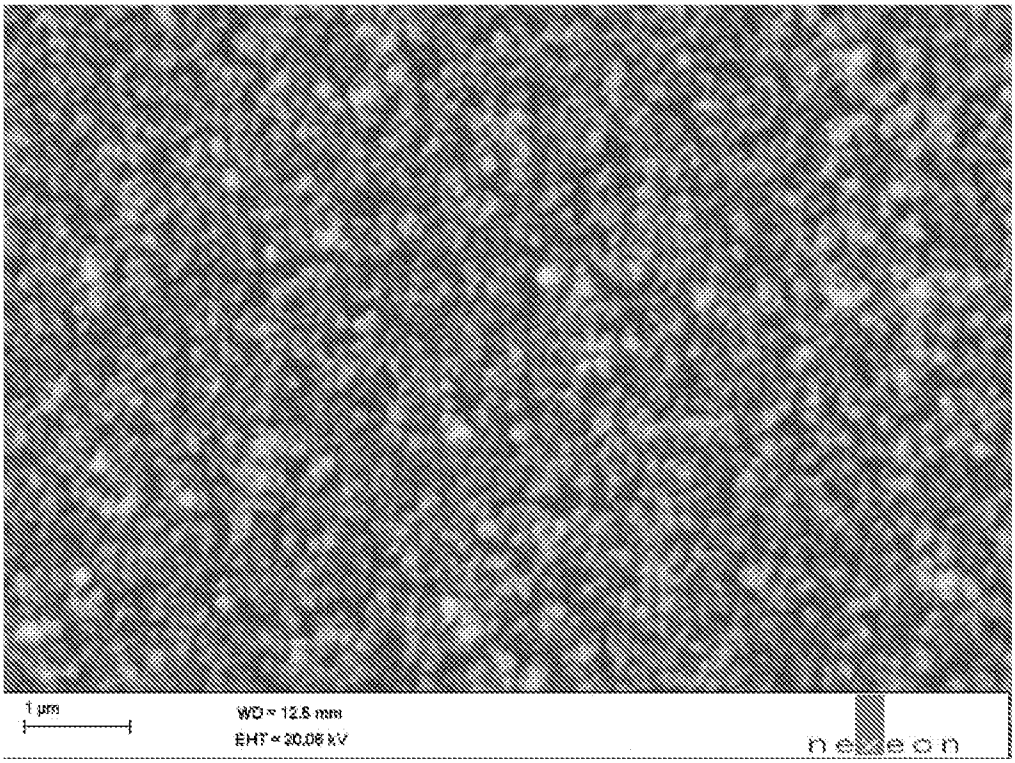


FIGURE 10A

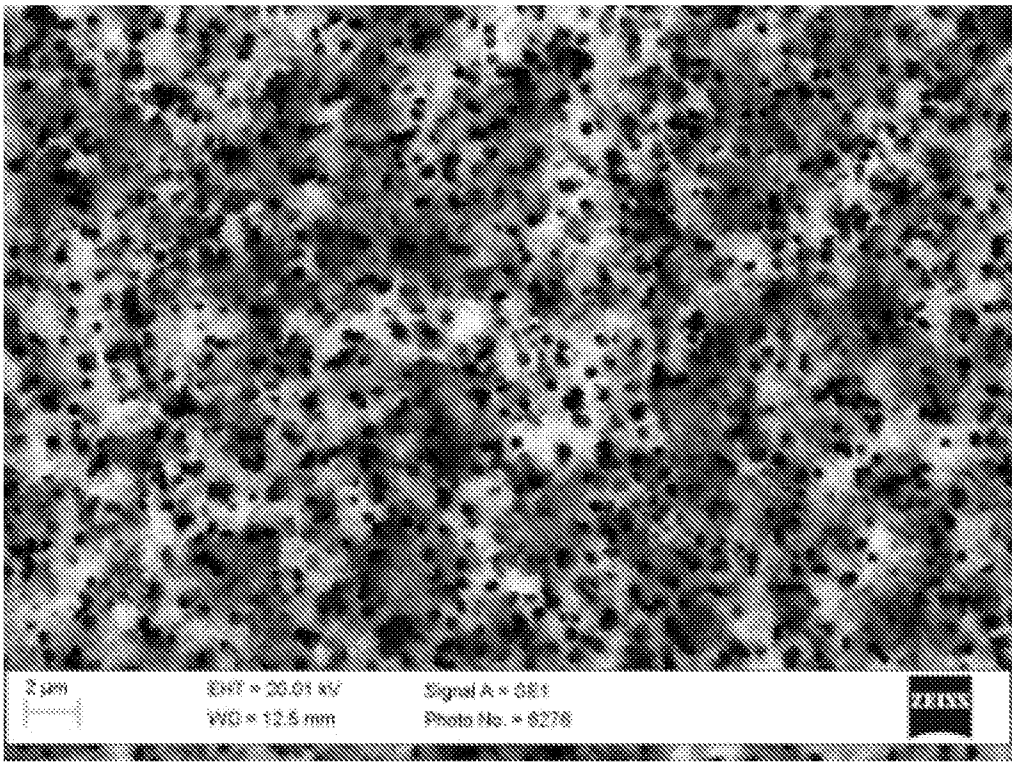


FIGURE 10B

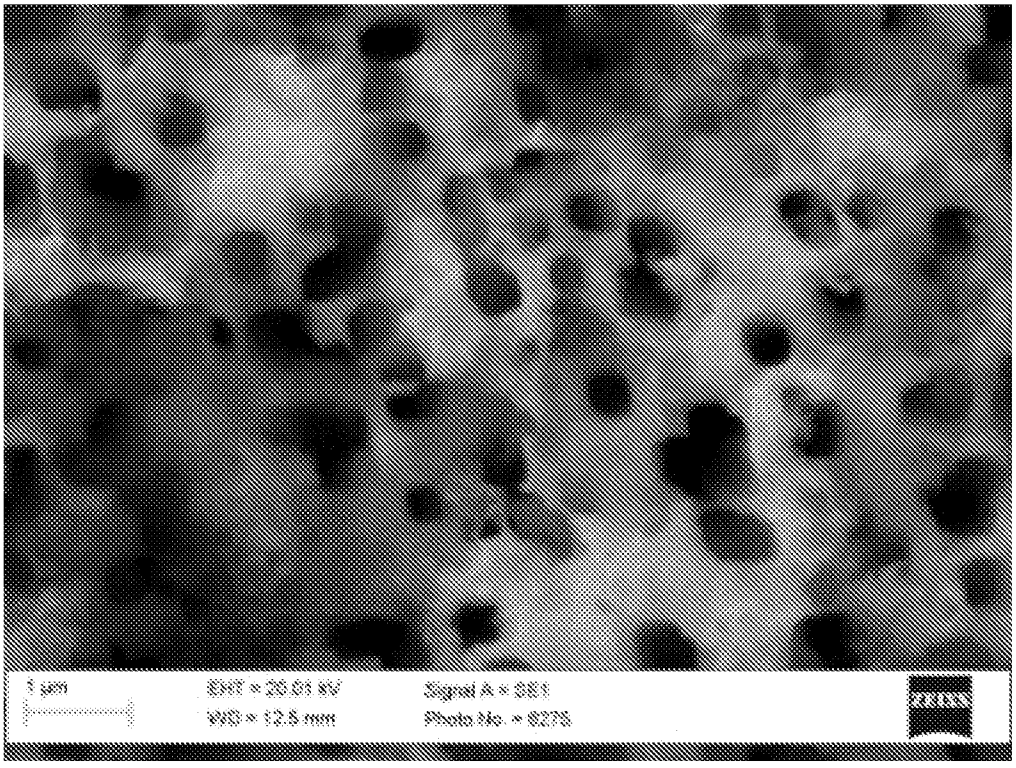


FIGURE 11A

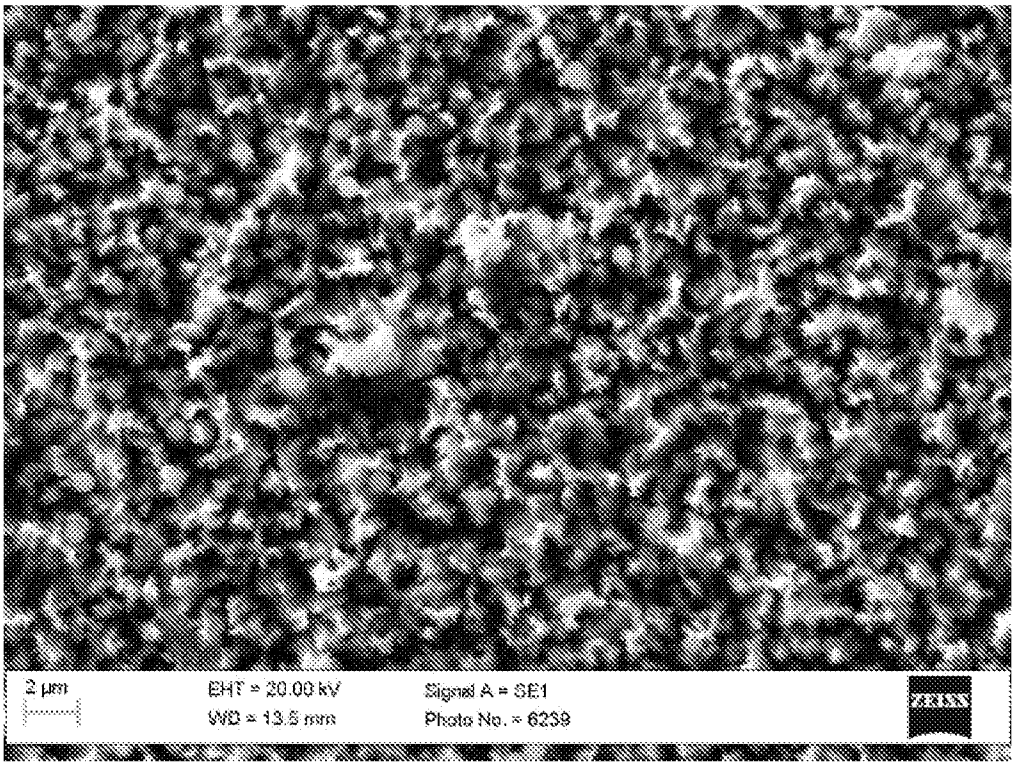
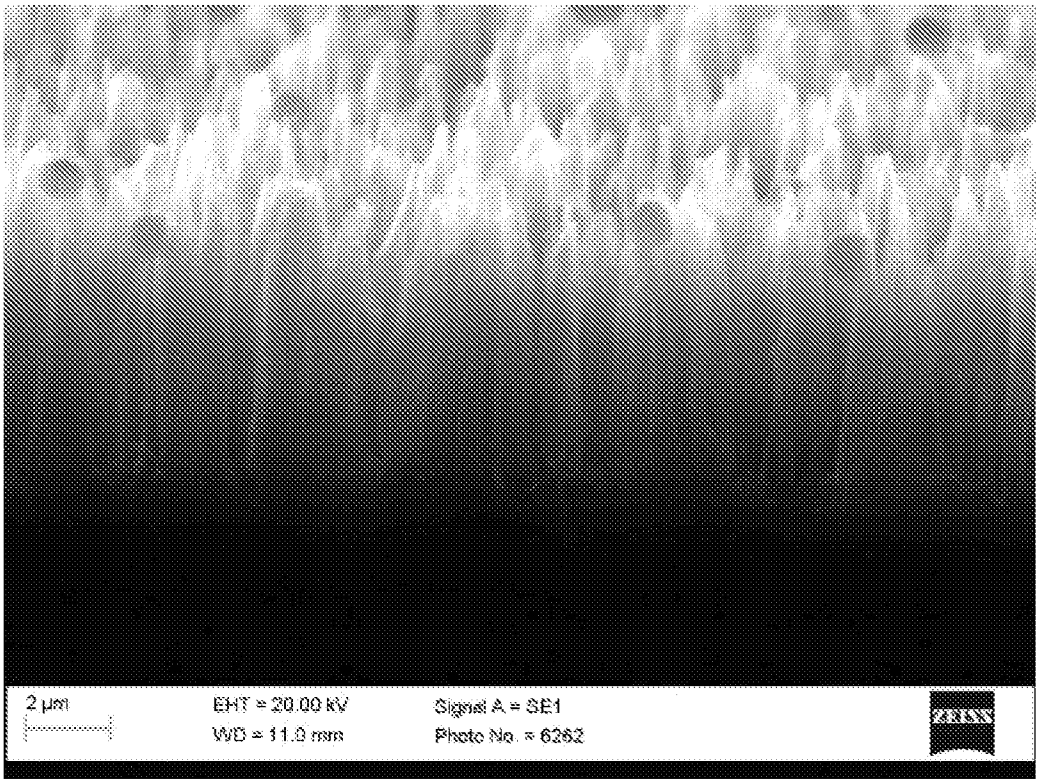


FIGURE 11B



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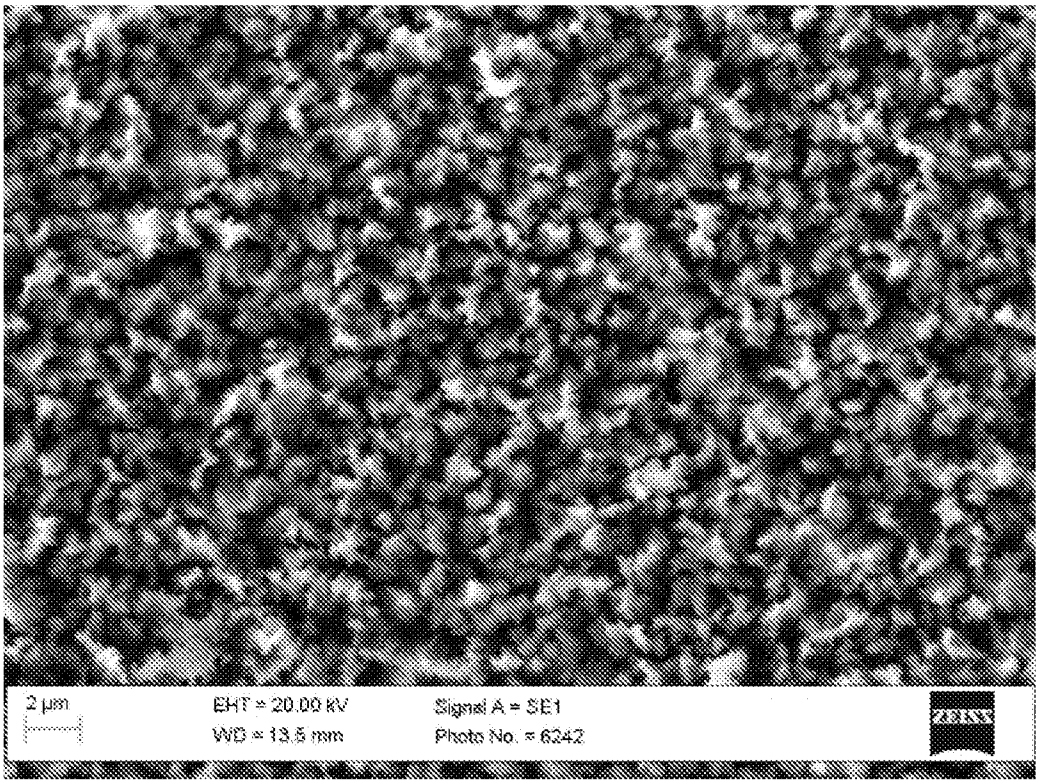
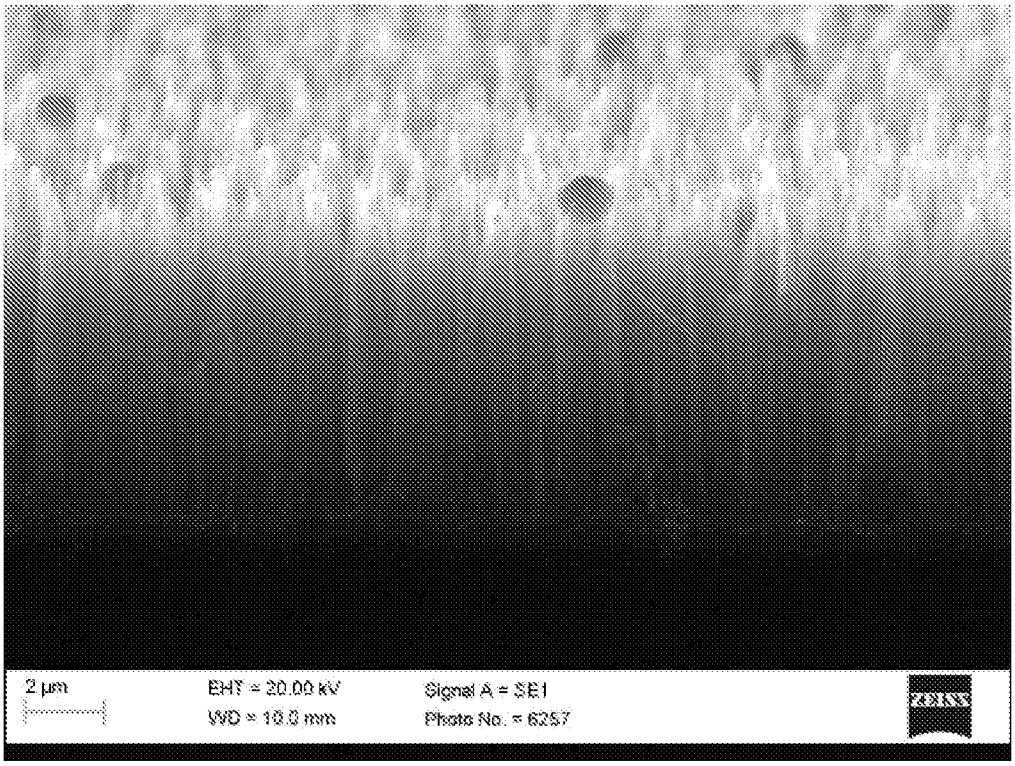


FIGURE 12B



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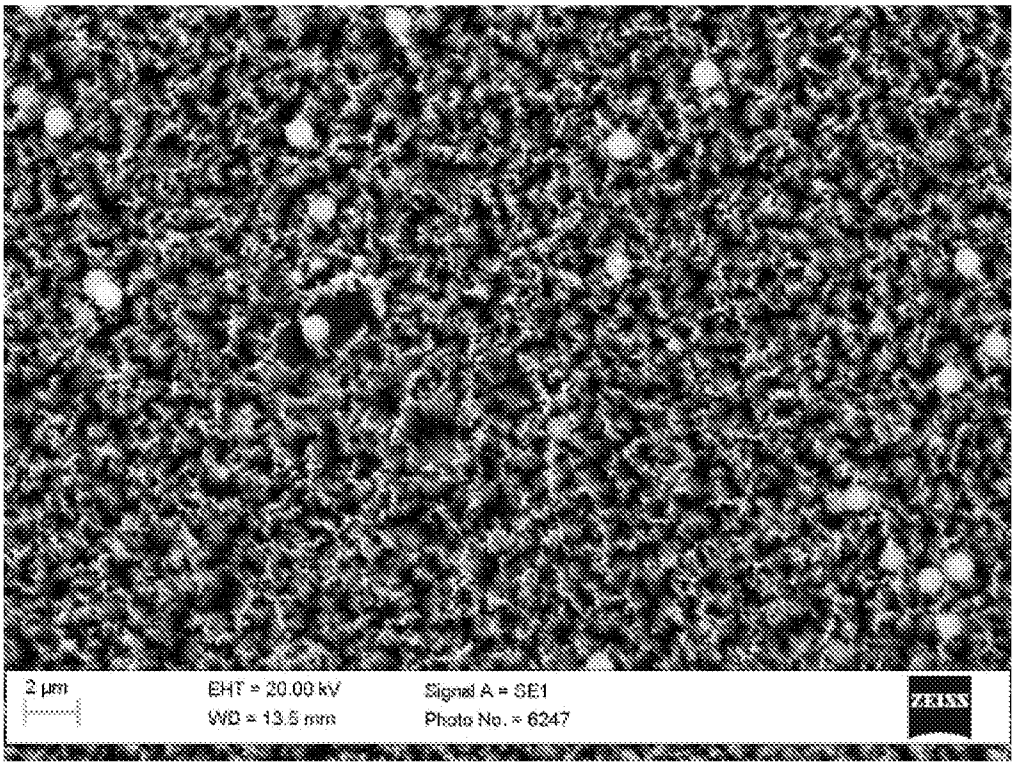


FIGURE 13B

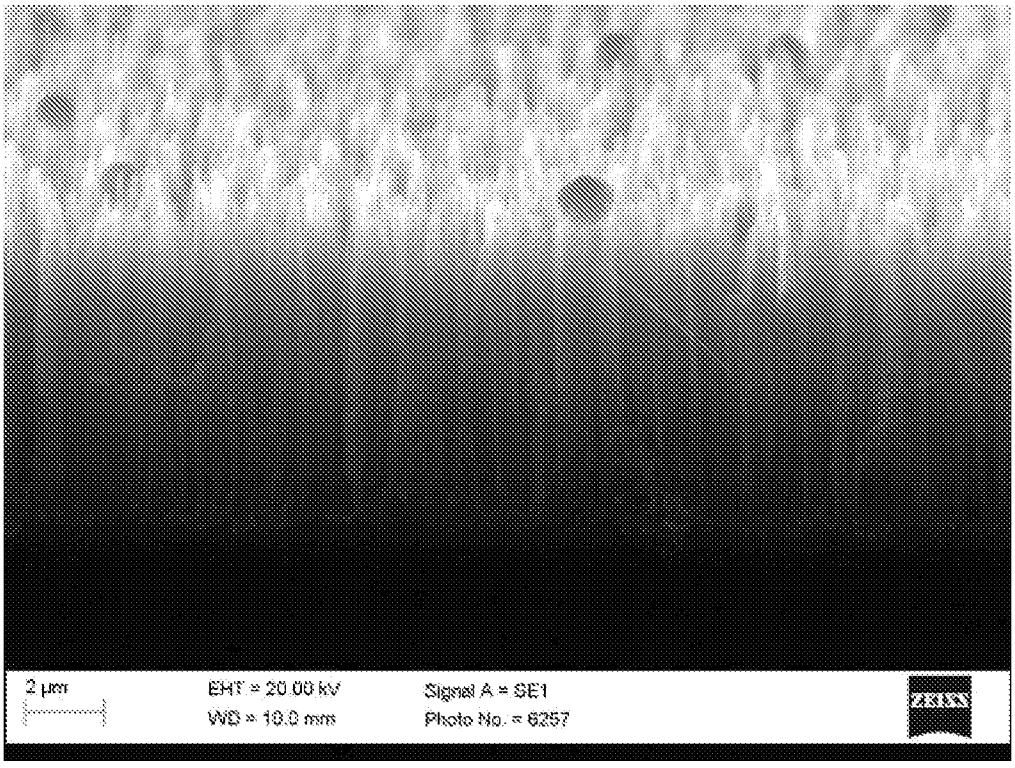


FIGURE 14A

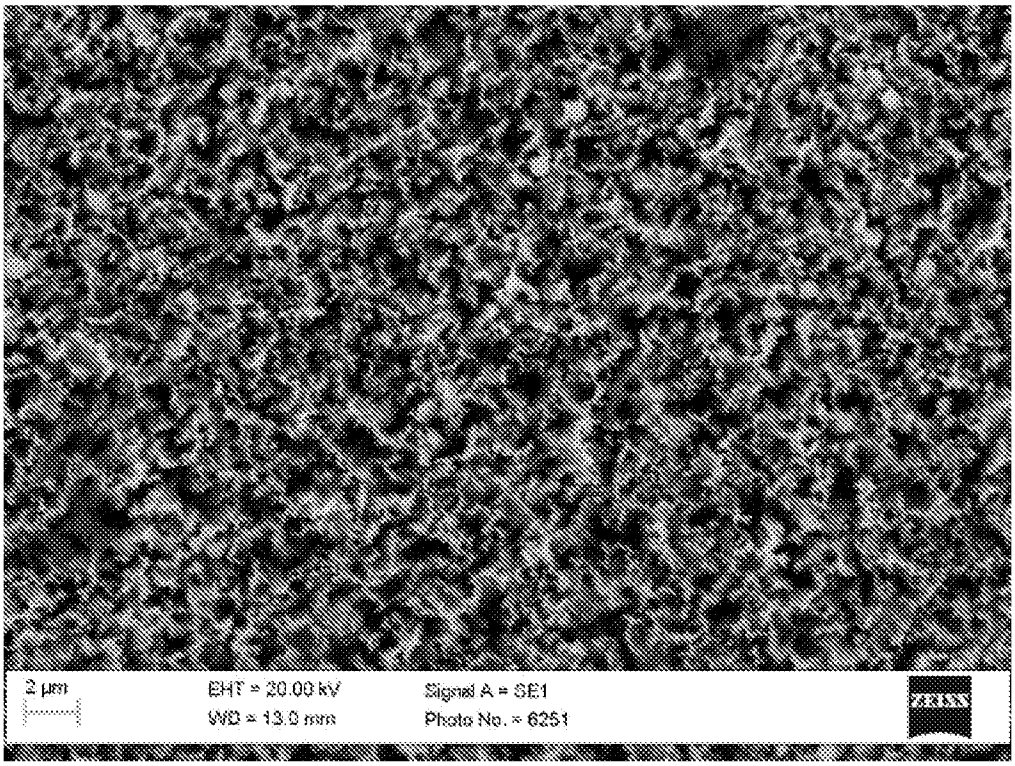


FIGURE 14B

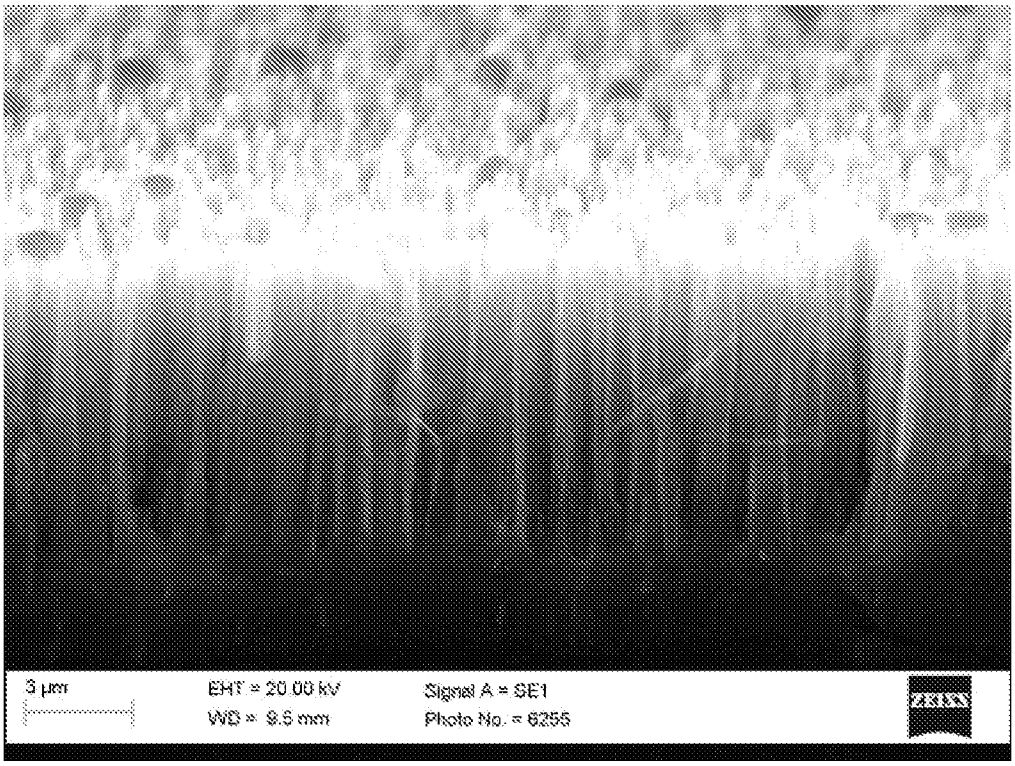


FIGURE 15A

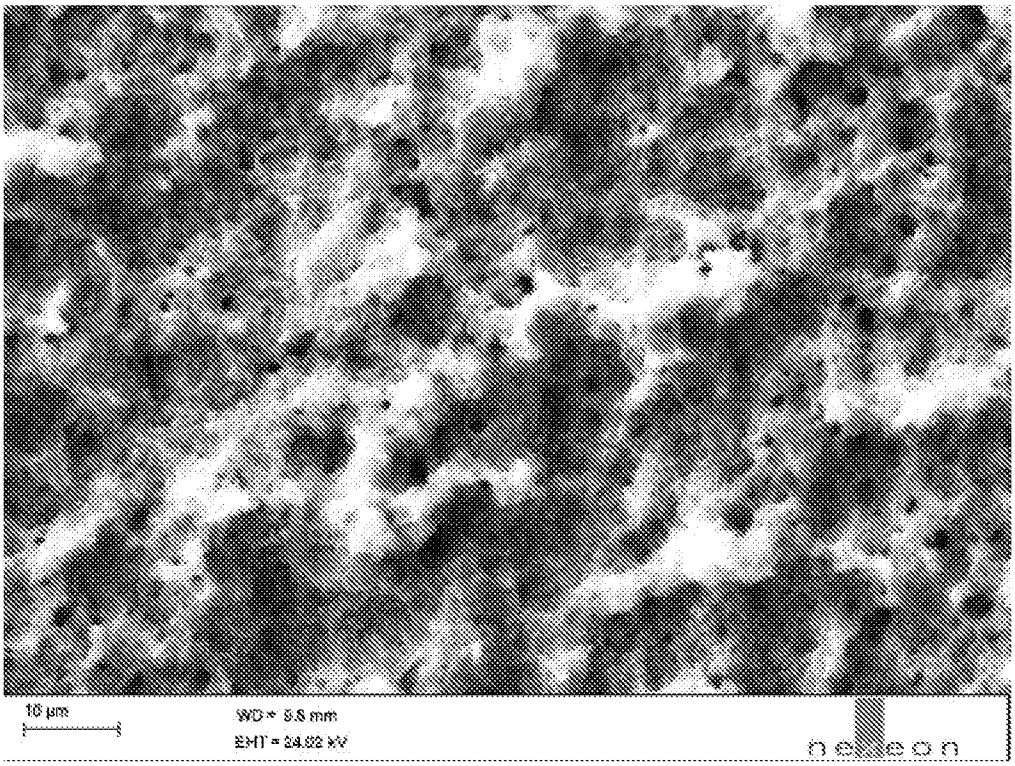


FIGURE 15B

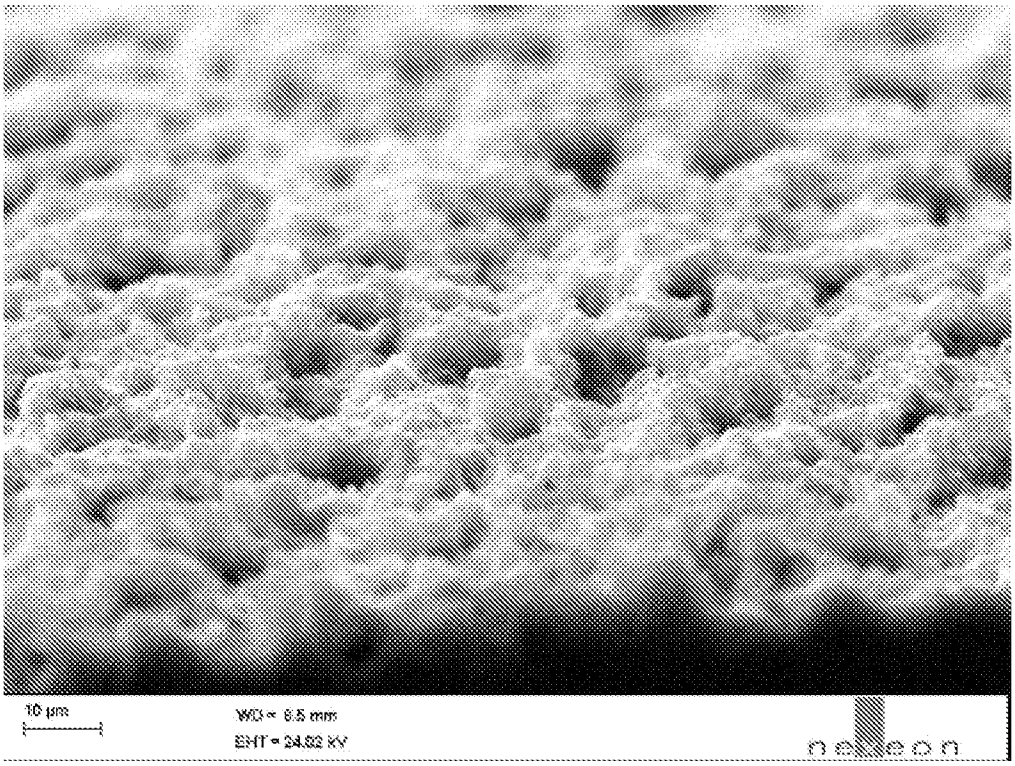


FIGURE 16A

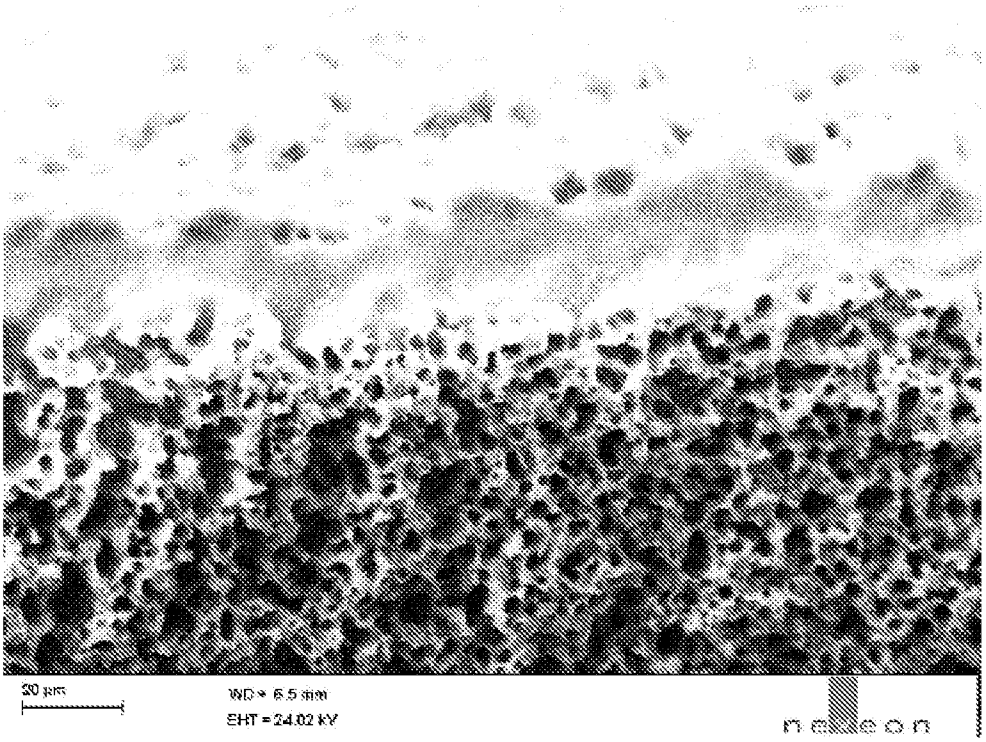


FIGURE 16B

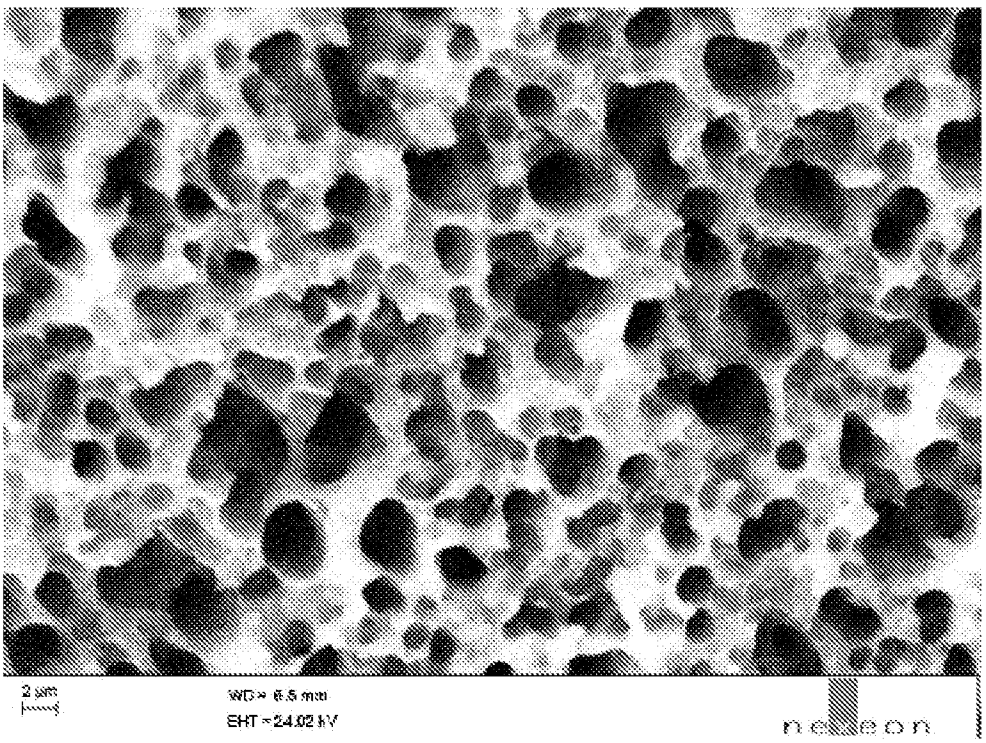


FIGURE 17

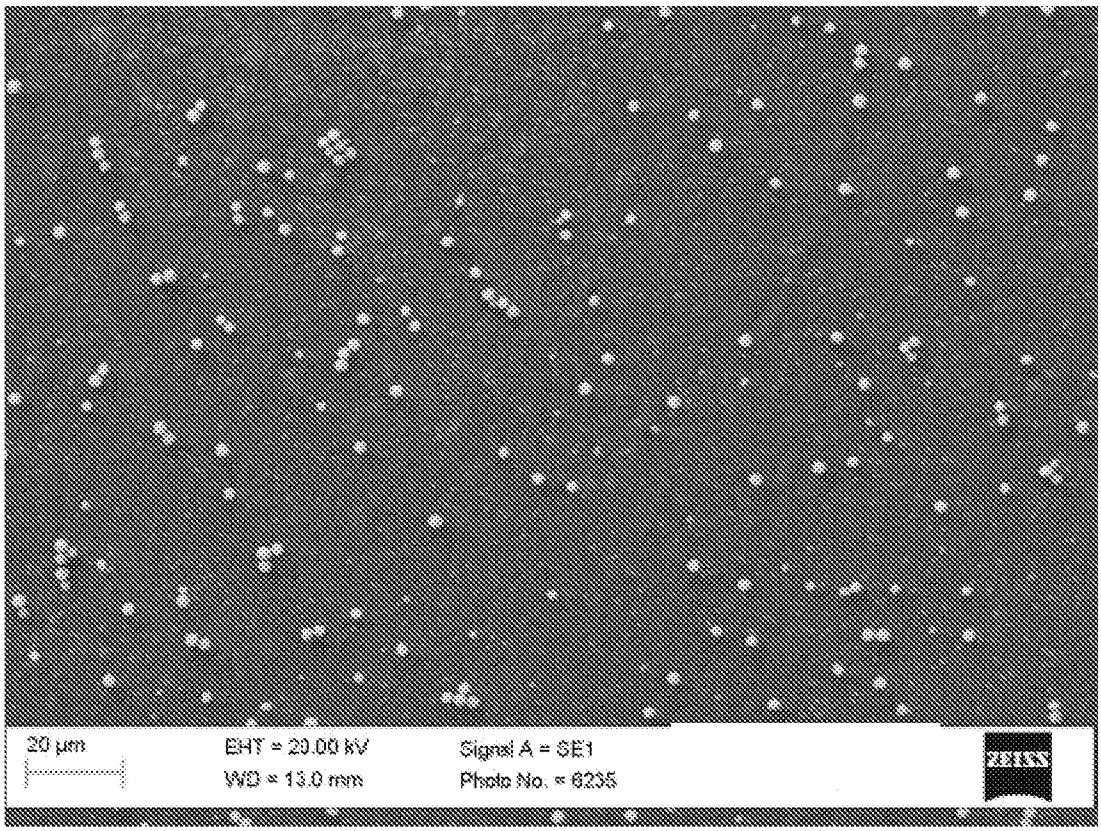


FIGURE 18A

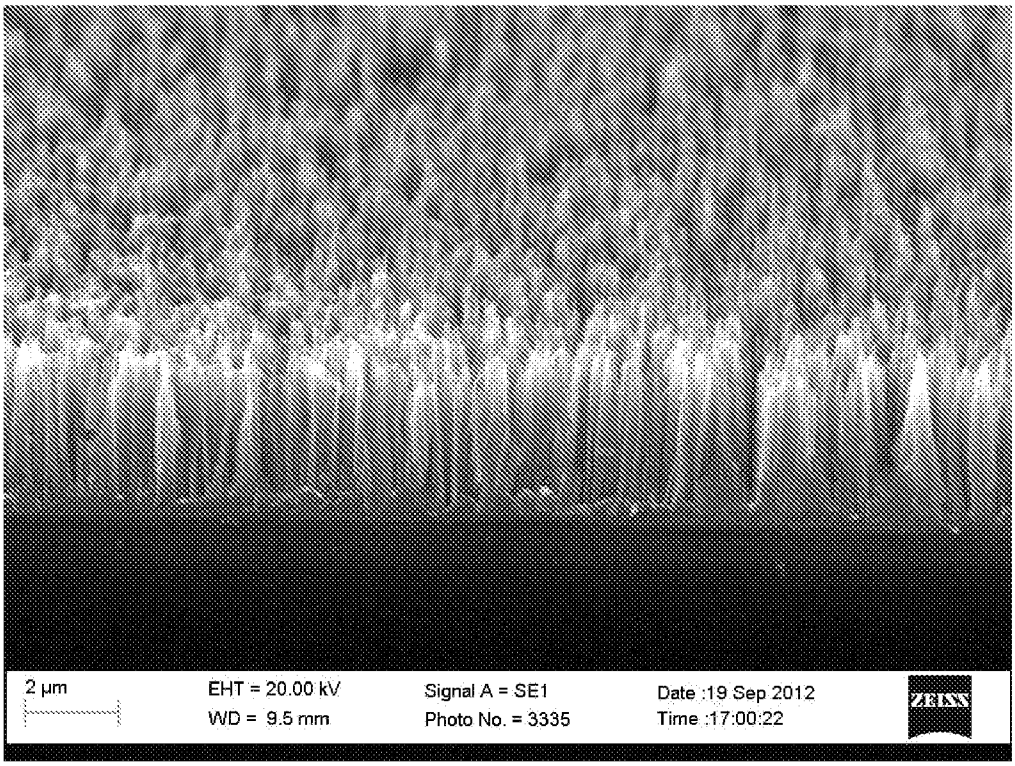


FIGURE 18B

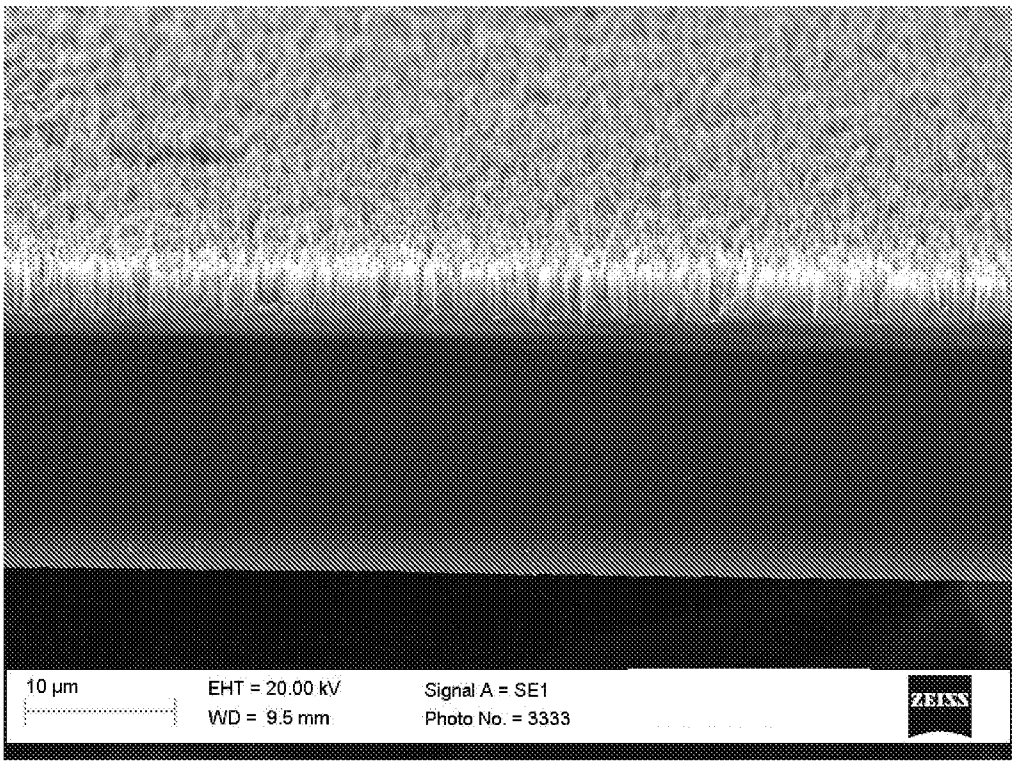


FIGURE 18C

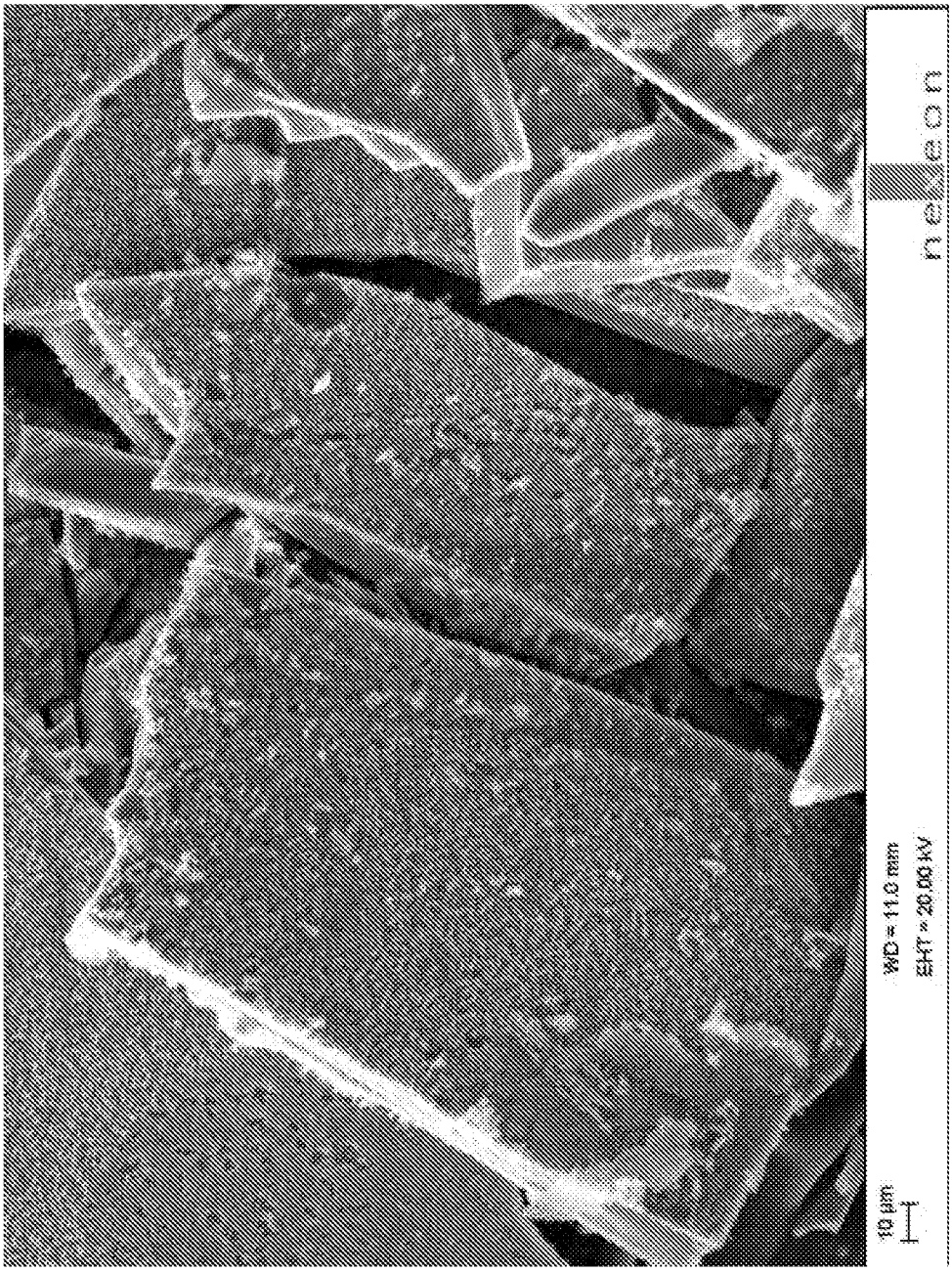


FIGURE 18D

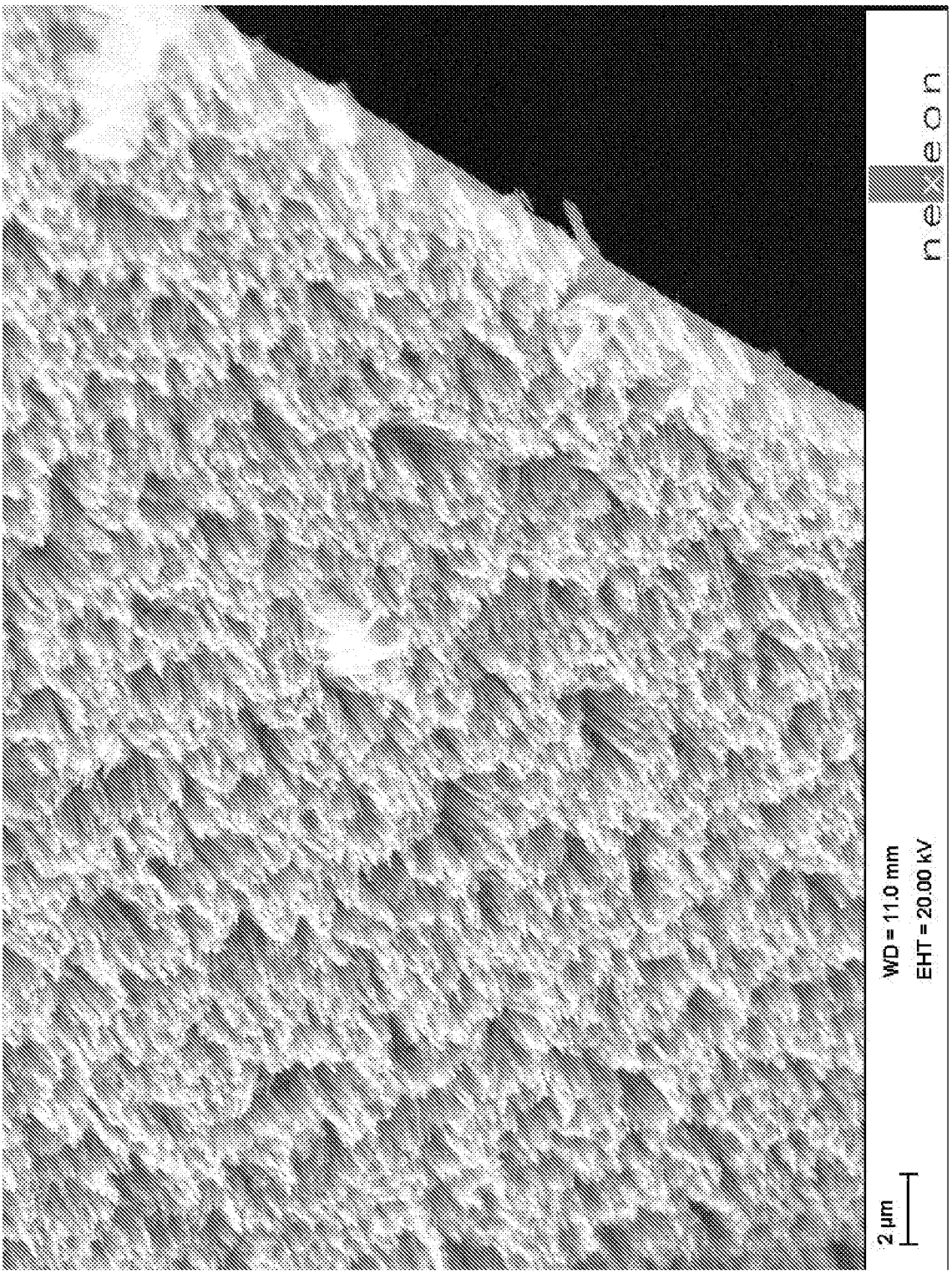


FIGURE 19A

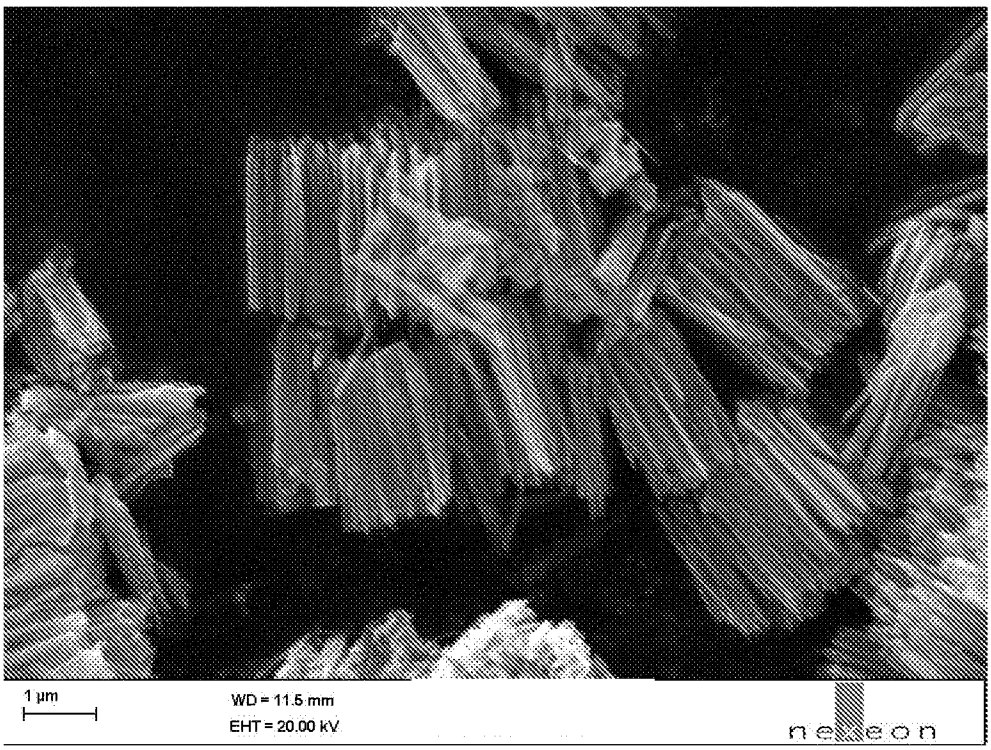


FIGURE 19B

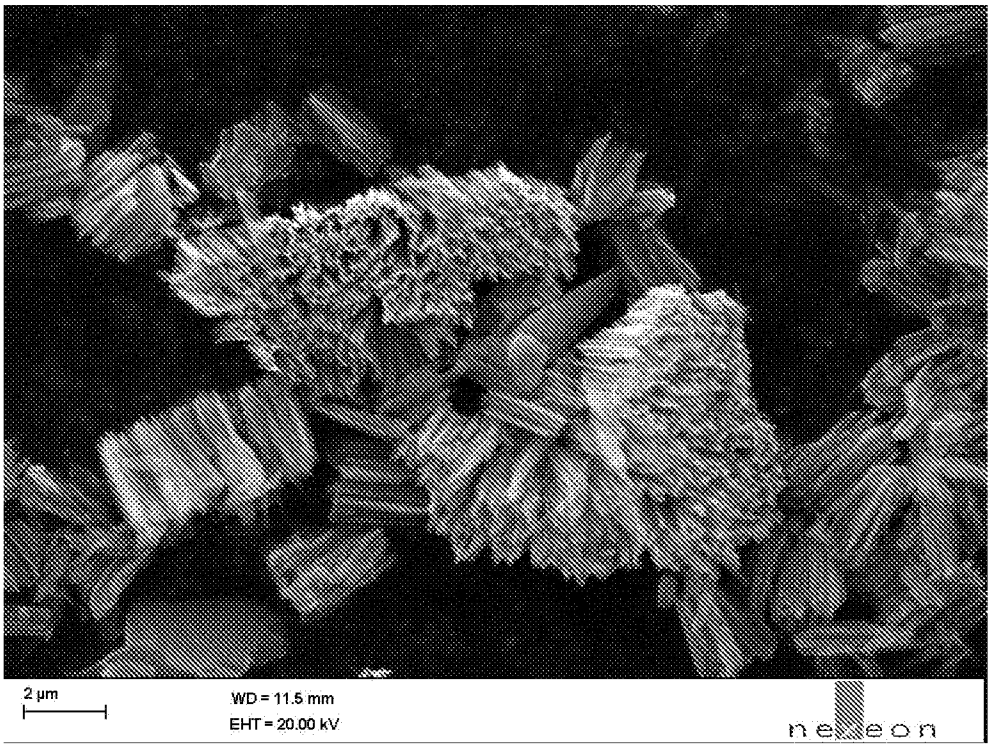
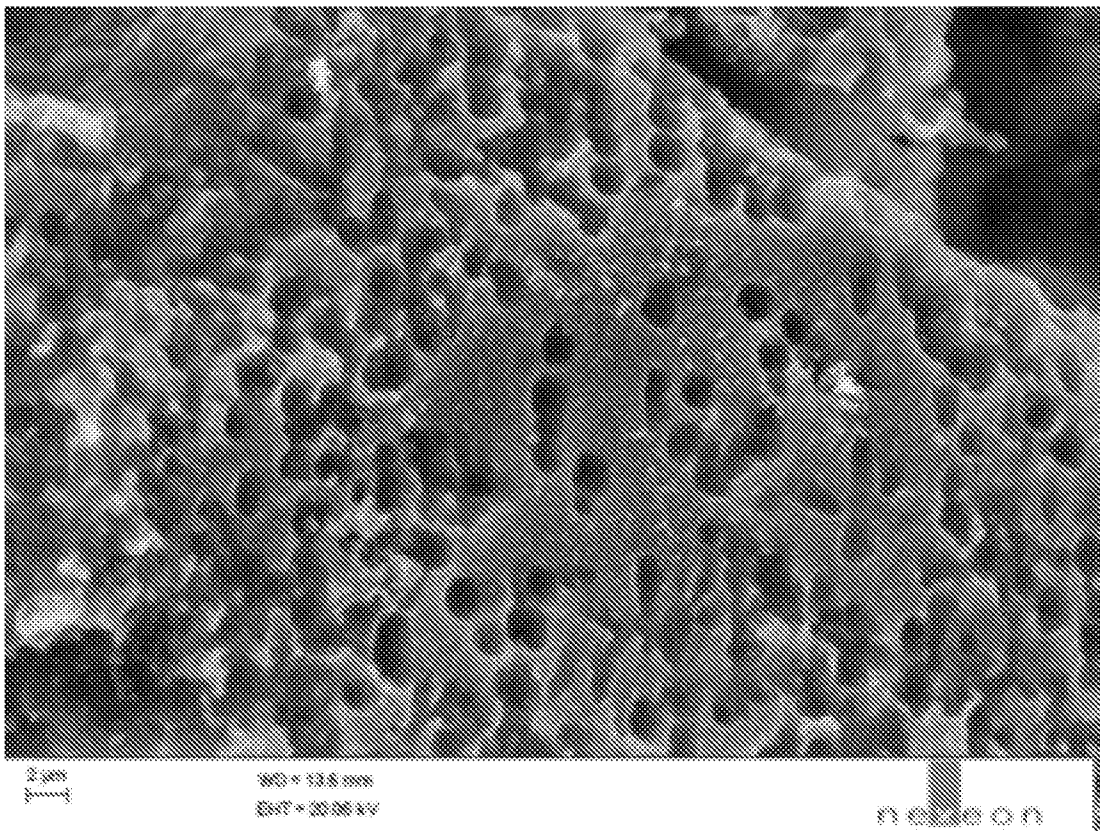


FIGURE 20



INTERNATIONAL SEARCH REPORT

International application No
PCT/GB2012/052483

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01M4/04 H01L31/18 B44C1/22 H01M4/02 H01M4/70
H01M4/38 H01M4/66
ADD.
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X,P	US 2012/178204 A1 (TOOR FATIMA [US] ET AL) 12 July 2012 (2012-07-12) the whole document * see [0011] - [0018]; claims * -----	1-49
X	WO 2007/083152 A1 (IMP INNOVATIONS LTD [GB]; GREEN MINO [GB]) 26 July 2007 (2007-07-26) cited in the application the whole document * see p.4, l. 1 - p.7, l.27; claims * -----	1-49
Y	WO 2010/040985 A1 (NEXEON LTD [GB]; GREEN MINO [GB]; LIU FENG-MING [GB]) 15 April 2010 (2010-04-15) the whole document * see p.7, l. 15 - p.8, l.4; p.14, l.7 - p.16, l. 21; claims * -----	1-49
	-/--	

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
12 December 2012	04/01/2013

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Stellmach, Joachim

1

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C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	EP 2 226 374 A1 (S O I TEC SILICON [FR]) 8 September 2010 (2010-09-08) the whole document * see [001] - [0023]; claims *	1-49
Y	EP 2 051 317 A1 (PANASONIC CORP [JP]) 22 April 2009 (2009-04-22) the whole document * see [0034] - [0068]; claims *	1-49
Y	US 2010/301276 A1 (LEE JOONG KEE [KR] ET AL) 2 December 2010 (2010-12-02) cited in the application the whole document * see [0023] - [0031]; Fig1 ;claims *	1-49
Y	US 2010/112451 A1 (SHIBUTANI SATOSHI [JP] ET AL) 6 May 2010 (2010-05-06) the whole document * see Fig.1; [0076] - [0079]; claims *	1-49
Y	WO 2009/010758 A2 (NEXEON LTD [GB]; GREEN MINO [GB]) 22 January 2009 (2009-01-22) cited in the application the whole document * see p.6, l.1 - p.8, l.7; 5; claims *	1-49
Y	PENG K ET AL: "Uniform, axial-orientation of one dimensional single-crystal silicon nanostructure arrays", ANGEWANDTE CHEMIE. INTERNATIONAL EDITION, WILEY VCH VERLAG, WEINHEIM, vol. 44, 1 January 2005 (2005-01-01), pages 2737-2742, XP002431331, ISSN: 1433-7851, DOI: 10.1002/ANIE.200462995 the whole document * see p.2738, left col.; Fig 4 *	1-49
Y	QIU T ET AL: "Self-assembled growth and optical emission of silver-capped silicon nanowires", APPLIED PHYSICS LETTERS, AIP, AMERICAN INSTITUTE OF PHYSICS, MELVILLE, NY, US, vol. 84, no. 19, 10 May 2004 (2004-05-10), pages 3867-3869, XP012061406, ISSN: 0003-6951, DOI: 10.1063/1.1753063 the whole document * see p.3668, Fig.2 *	1-49

1

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/GB2012/052483

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2012178204 A1	12-07-2012	NONE	
WO 2007083152 A1	26-07-2007	BR PI0707164 A2	02-08-2011
		CA 2637737 A1	26-07-2007
		CN 101390198 A	18-03-2009
		EP 1977443 A1	08-10-2008
		JP 5043041 B2	10-10-2012
		JP 2009524264 A	25-06-2009
		KR 20090004858 A	12-01-2009
		US 2010233539 A1	16-09-2010
		WO 2007083152 A1	26-07-2007
WO 2010040985 A1	15-04-2010	CN 102239583 A	09-11-2011
		EP 2335307 A1	22-06-2011
		GB 2464158 A	14-04-2010
		JP 2012505505 A	01-03-2012
		KR 20110082171 A	18-07-2011
		TW 201027829 A	16-07-2010
		US 2011269019 A1	03-11-2011
		WO 2010040985 A1	15-04-2010
EP 2226374 A1	08-09-2010	EP 2226374 A1	08-09-2010
		US 2012094501 A1	19-04-2012
		WO 2010099982 A1	10-09-2010
EP 2051317 A1	22-04-2009	CN 101356666 A	28-01-2009
		EP 2051317 A1	22-04-2009
		JP 2008171802 A	24-07-2008
		KR 20080069604 A	28-07-2008
		US 2010291441 A1	18-11-2010
		WO 2008072460 A1	19-06-2008
US 2010301276 A1	02-12-2010	KR 20100127990 A	07-12-2010
		US 2010301276 A1	02-12-2010
US 2010112451 A1	06-05-2010	CN 101496199 A	29-07-2009
		JP 4164541 B2	15-10-2008
		US 2010112451 A1	06-05-2010
		WO 2008044683 A1	17-04-2008
WO 2009010758 A2	22-01-2009	AT 535033 T	15-12-2011
		AT 548768 T	15-03-2012
		CA 2693460 A1	22-01-2009
		CN 101790805 A	28-07-2010
		EP 2183804 A2	12-05-2010
		EP 2194596 A2	09-06-2010
		EP 2204868 A2	07-07-2010
		EP 2533331 A2	12-12-2012
		EP 2533332 A2	12-12-2012
		HK 1138943 A1	19-10-2012
		HK 1140855 A1	06-07-2012
		JP 4834814 B2	14-12-2011
		JP 2010533637 A	28-10-2010
		JP 2011046603 A	10-03-2011
		JP 2011222522 A	04-11-2011
		KR 20100058486 A	03-06-2010
		RU 2010100662 A	27-08-2011
		TW 200917550 A	16-04-2009

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/GB2012/052483

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
		US 2010178565 A1	15-07-2010
		US 2011067228 A1	24-03-2011
		WO 2009010758 A2	22-01-2009