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GB 1427443
GB 1379856
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H4L
(71) Applicants
Robert Bosch GmbH,
Postfach 50, 7000
Stuttgart 1, Federal
Republic of Germany
(72) Inventors
Günter Hönig,
Edmund Jeenicke,
Immanuel Krauter,
Manfred Schenk
(74) Agents
Dr. Walther Wolff & Co., 6
Buckingham Gate, London
SW1E 6JP

(54) **A voltage converter**

(57) A voltage-frequency converter comprises a chargeable and dischargeable store (14), a comparison stage (10) as well as a trigger device (11) connected therebehind, wherein the charging and/or discharging signal for the store is obtained from special signal sources (27, 28). A linear voltage-frequency conversion is given with constant charging and discharging signals. Non-linear signal conversions are possible in the case of variable charging and discharging voltages. A further embodiment comprises a digitally operating monostable trigger device, whereby exact, reproduceable and quantisizable period durations in the output signal of the converter and thereby a very exact voltage-frequency conversion are possible.

FIG. 2

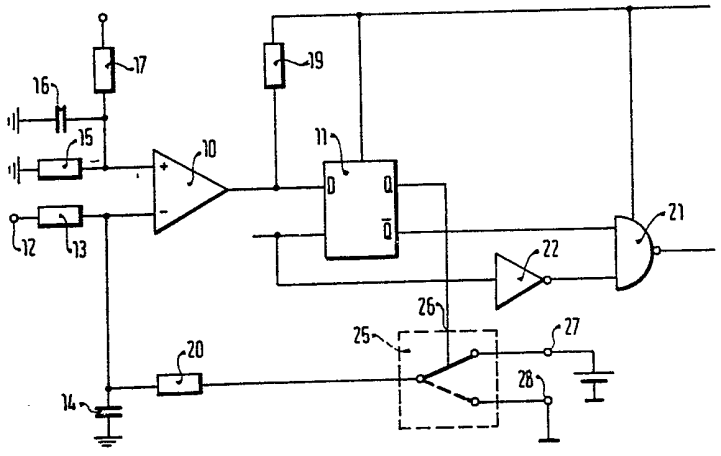

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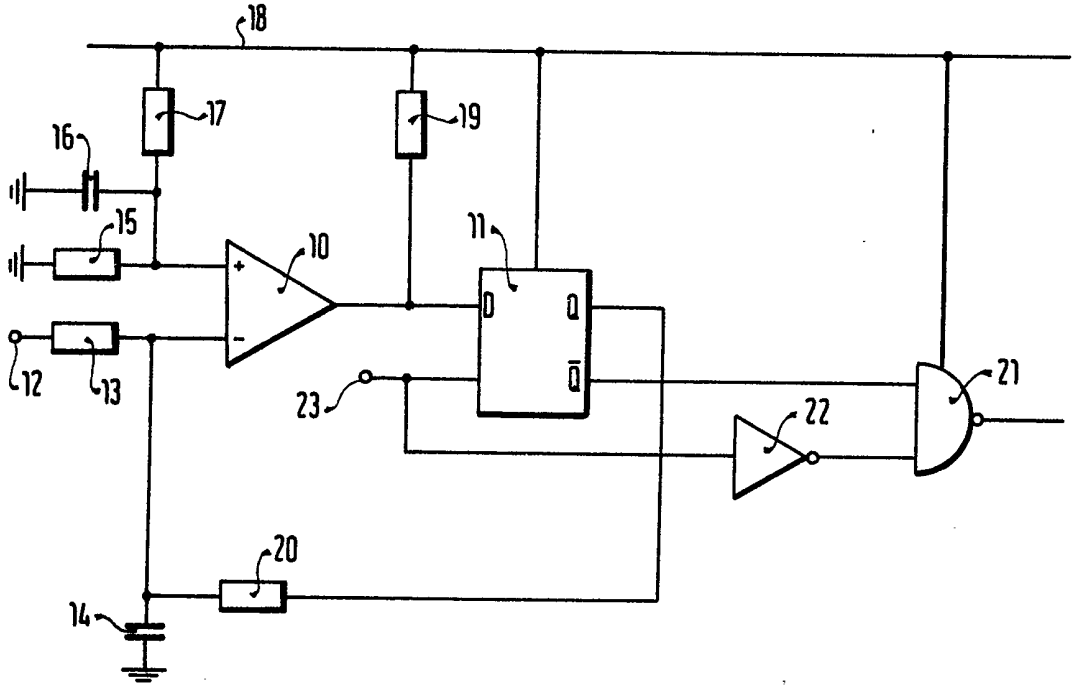
FIG. 1


18
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$\overline{Q}$
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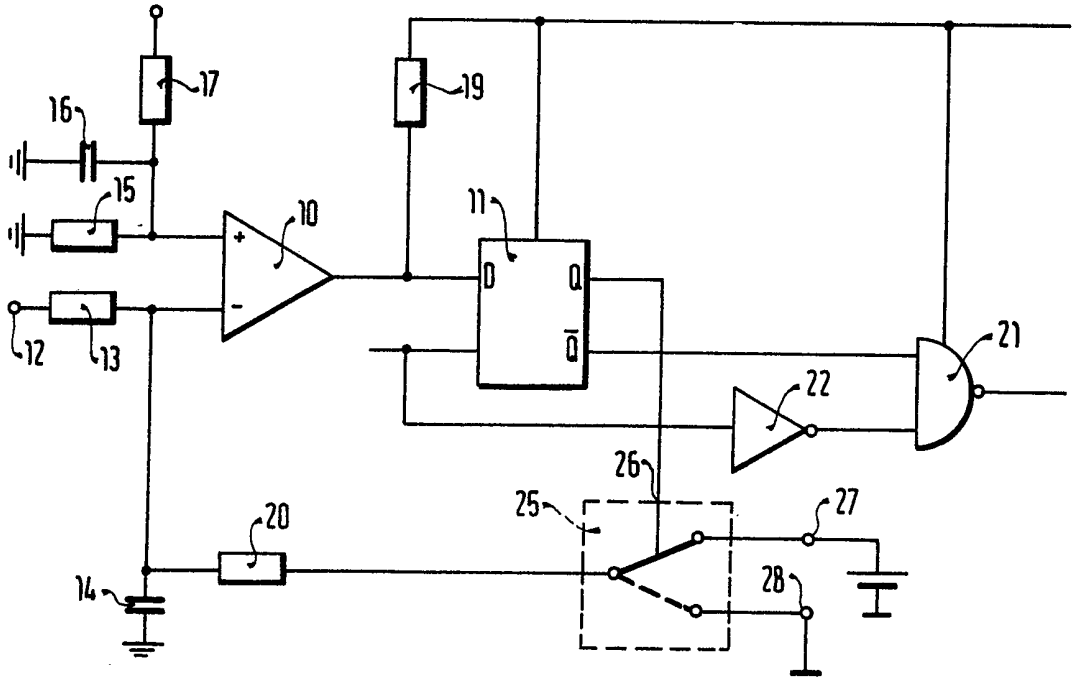
14

FIG. 2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28
14

FIG. 3

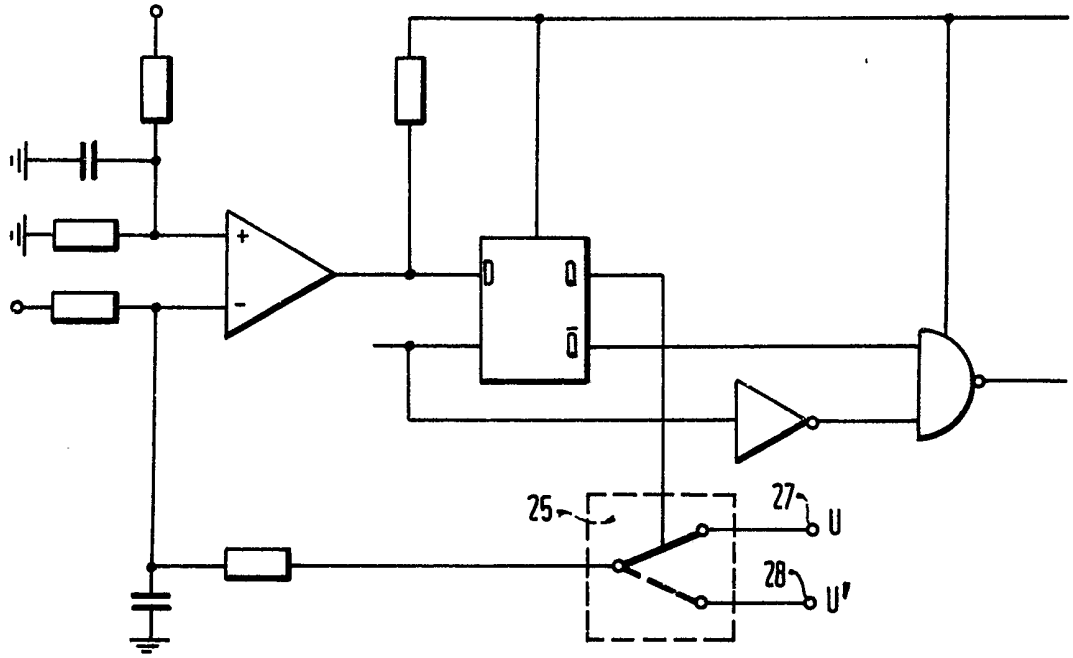


FIG. 4

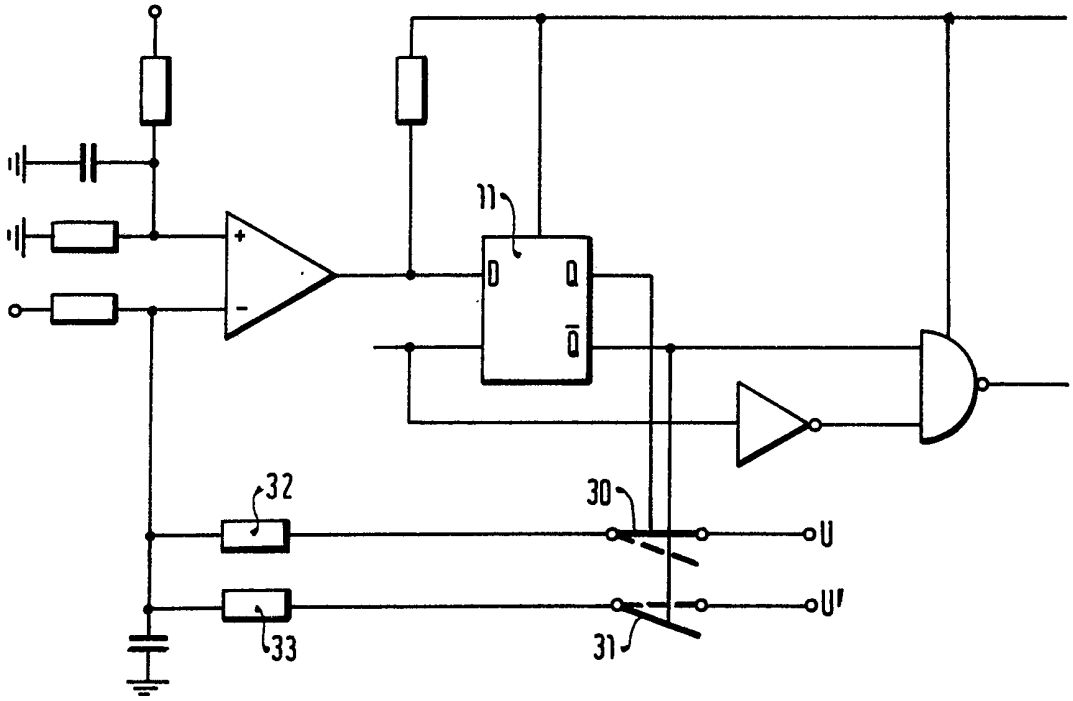


FIG. 5

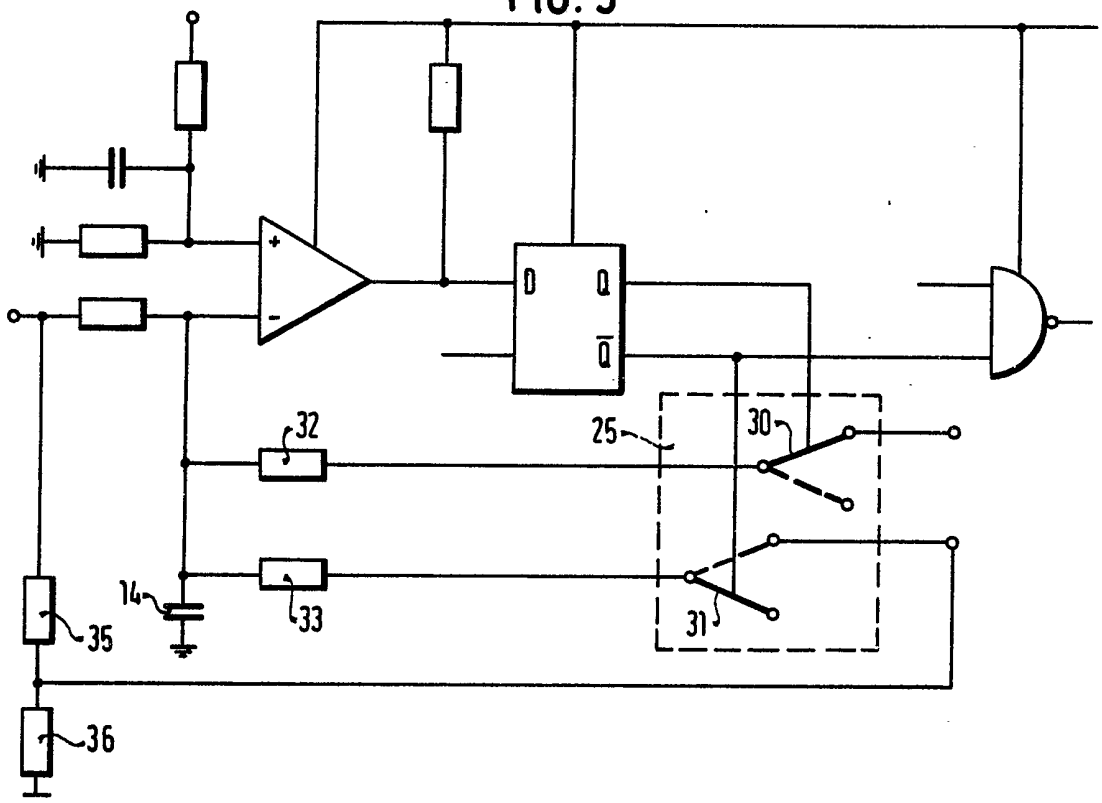


FIG. 6

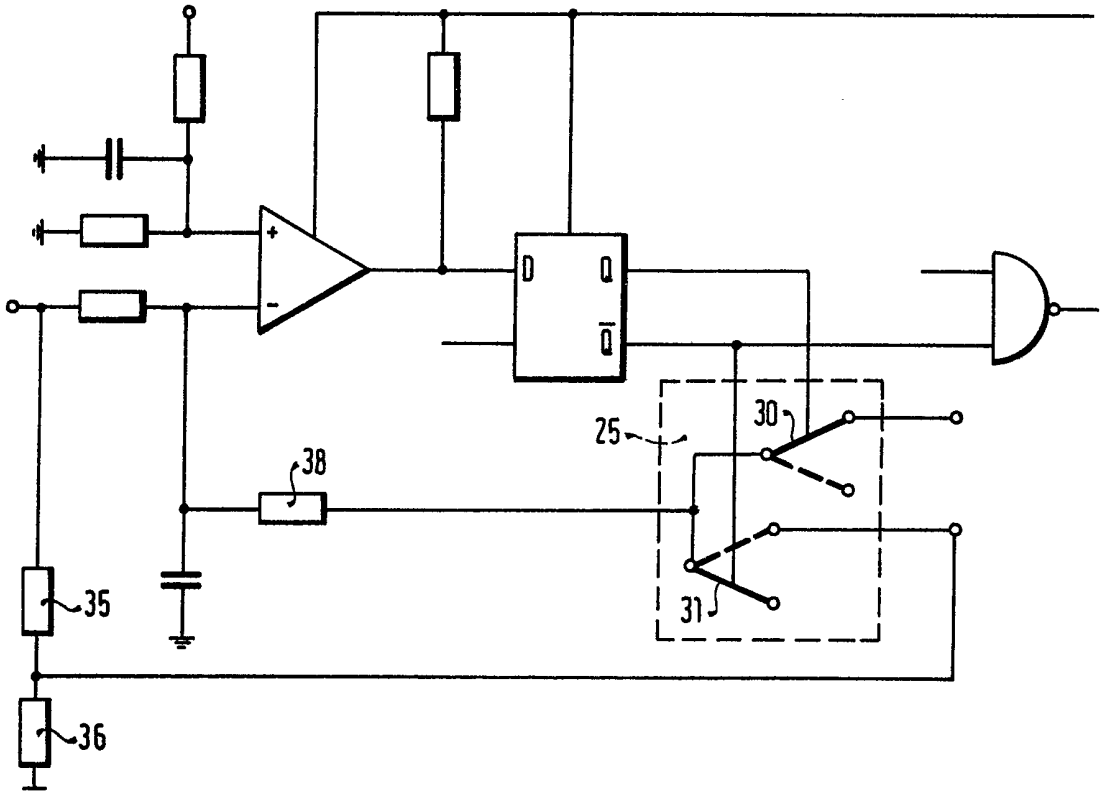


FIG. 7

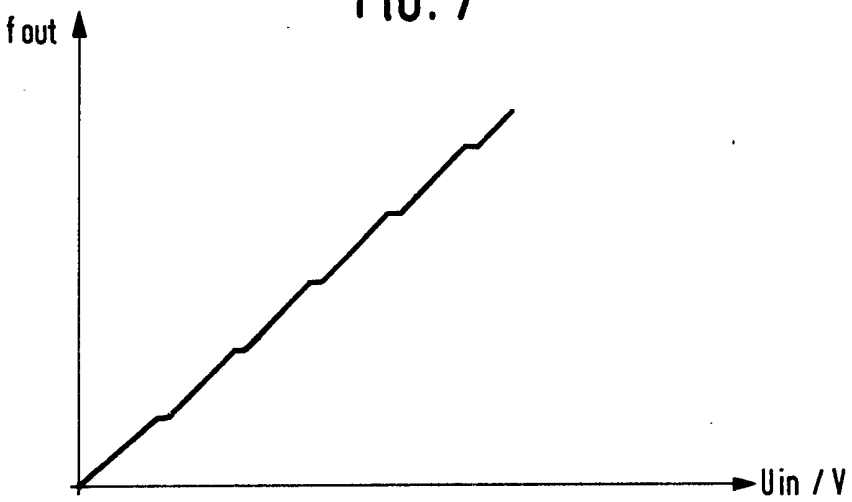
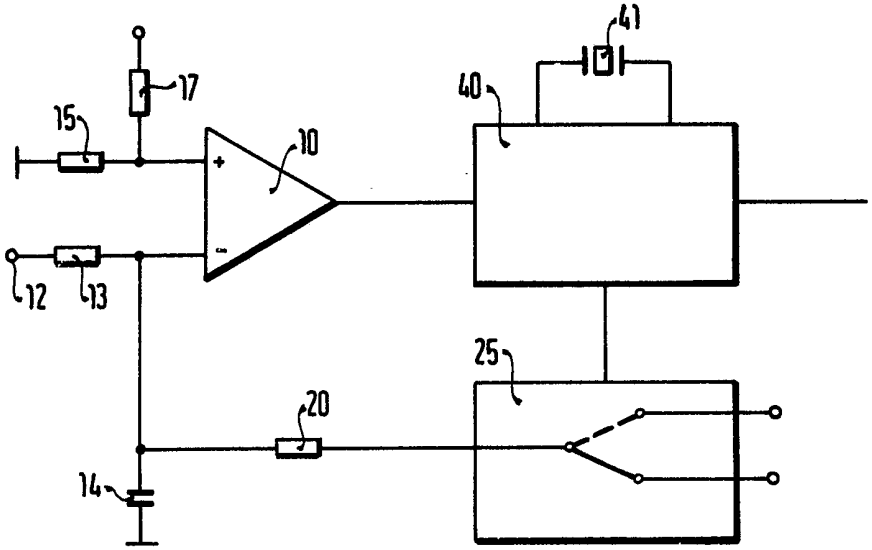


FIG.8

a)



b)

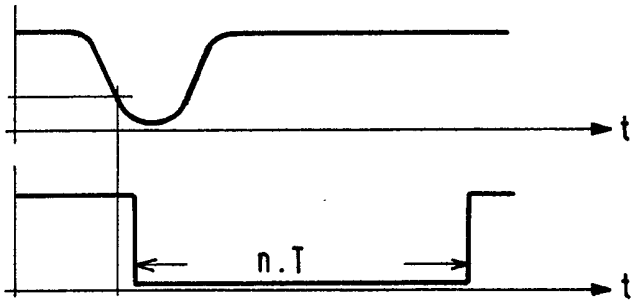


FIG. 9

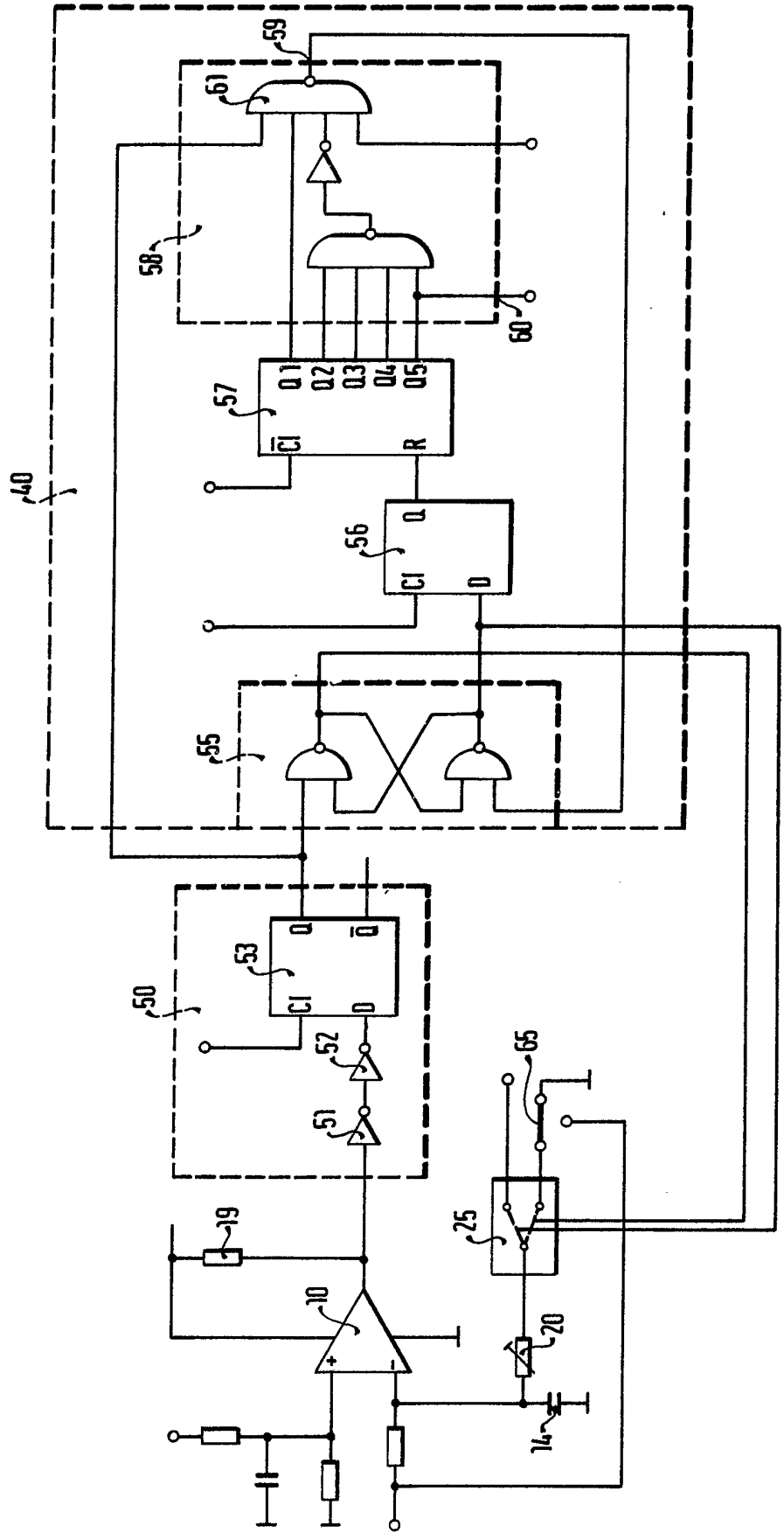
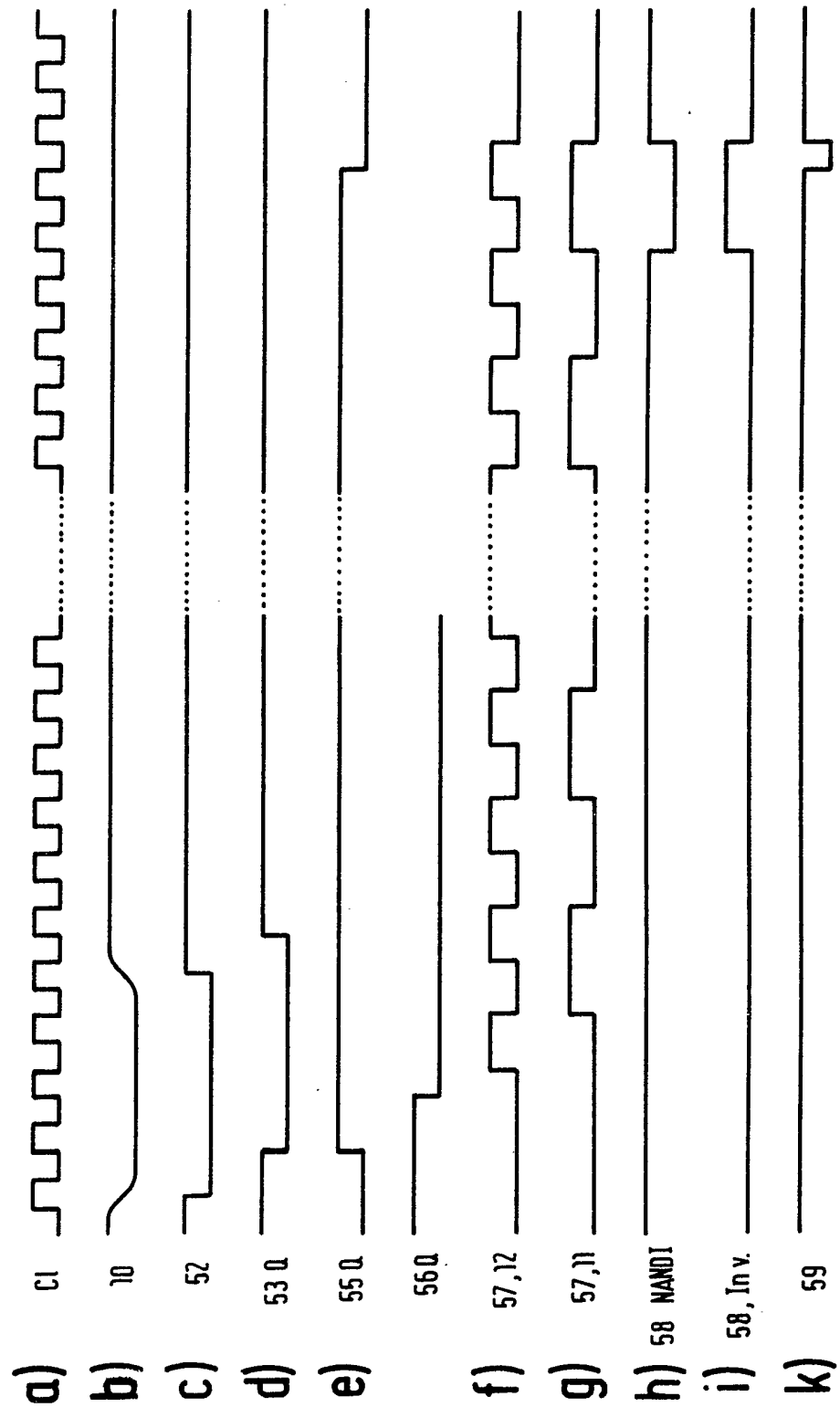

59
61
58
60
57
Q1
Q2
Q3
Q4
Q5
C1
R
40
56
Q
C1
D
55
53
Q
C1
D
50
52
51
65
25
19
10
20
14

FIG. 10



SPECIFICATION

A voltage converter

The present invention relates to a voltage-frequency converter.

Typically, known voltage-frequency converters comprise a differential amplifier as comparator, to one input of which is applied a constant signal, while the other input is connected with the input terminal of the converter. At the output side, the converter is connected to the D-input of a D-flip-flop, the Q-output of which is fed through a resistor to a capacitor connected between ground and the other input of the comparator. A frequency signal corresponding to the analog input signal is present at the output of the D-flipflop.

The principle of the known circuit arrangement is based on the alternating charging and discharging of the capacitor, wherein the frequency of the charge alternation depends on the input voltage and a voltage-frequency conversion is thus given.

As a rule, the output signal of the D-flipflop is fed together with a clock pulse signal to an AND-gate or a NAND-gate, the output of which then provides a signal controlled in its frequency.

The known circuit operates satisfactorily on the whole. It has however its weaknesses where the input signal of the comparator must be tied to an absolute, fixed potential as reference voltage, since the same reference voltage is in practice one very often needed within a more comprehensive system, however then leads to voltage fluctuations and thus level matching problems by reason of the then given varying current withdrawal from this reference voltage source. Although these problems are manageable with high technical effort by special stabilising circuits, these usually complicated stabilising circuits however tend to be too expensive for use in mass production. It is therefore desirable to provide a relatively simple and accurate voltage-frequency converter which is nevertheless favourable in costs, is universally usable and beyond that allows any desired transmission behaviour to be realized.

According to the present invention, there is now provided a voltage-frequency converter comprising charge storage means, a comparator circuit having input means to receive an input voltage to be converted into a corresponding frequency, a trigger device having input means coupled to output means of the comparator circuit, and switch means operable under the control of the trigger device to apply either a charging signal or a discharging signal to the charge storage means.

It is advantageous for the trigger device, as known from the state of the art, to be replaced by a digital and a monostable trigger stage operating at a high cyclic frequency, since an extremely short reaction time at the analog switch is then attainable from the output signal of the comparator, which must be clock-synchronised. Thereby, frequency lockings (constant frequency for a finite increment of input voltage) are largely suppressed.

Embodiments of the present invention will now be more particularly described by way of example with reference to the accompanying drawings, in which:—

Fig. 1 illustrates a basic voltage-frequency converter of known type,

Figs. 2 to 6 each illustrate a respective voltage-frequency converter embodying the present invention,

Fig. 7 is a diagram illustrating the relationship between output frequency and input voltage for the converters illustrated in the Figs. 2 to 6,

Fig. 8 is a block schematic diagram of a further embodiment with a corresponding time diagram,

Fig. 9 is a more detailed circuit diagram of a yet further voltage-frequency converter embodying the present invention and provided with a quantized time base, and

Fig. 10 shows a pulse time diagram in respect of the converter of Fig. 9.

Referring now to the drawings, Fig. 1 illustrates the known voltage-frequency converter already mentioned in the introduction. It includes a comparator 10 and a D-flipflop 11. An input terminal 12 of the converter is connected through a resistor 13 to the negative input of the comparator 10, which in turn is coupled through a capacitor 14 to ground. The positive input of the comparator 10 is connected through a parallel circuit of a resistor 15 and a capacitor 16 to ground and through a resistor 17 to a positive supply line 18. At the output side, the comparator is connected directly with the D-input of the D-flipflop 11 and also through a resistor 19 with the positive supply line 18. A resistor 20 connects the Q-output of the D-flipflop 11 with the negative input of the comparator 10. A NAND-gate 21, which has one input connected with the $\overline{Q}$-output of the D-flipflop 11, through an inverter 22 receives at its second input a clock signal which comes from an input terminal 23 and is also conducted to a second input of the D-flipflop.

As already mentioned in the introduction, the frequency of the potential alternation of the output Q of the D-flipflop 11 corresponds to the analog value of the input voltage present at the input terminal 12. The logic circuit, which includes the NAND-gate 21 and which is connected to the Q output of the D-flipflop, serves to reshape the relatively low frequency output signal of the D-flipflop into a more readily processable consequential signal. It is now significant in the case of the converter illustrated by Fig. 1 that the charging or discharging of the capacitor 14 is determined directly by the output potential of the D-flipflop. When the voltage-frequency converter is part of a comprehensive electronic system with a high and varying power consumption, then the provision of stable reference voltages at the positive input of the comparator becomes involved and thereby costly.

To mitigate this difficulty, the charging and discharging processes at the capacitor 14 are now

decoupled from the individual circuit elements, such as for example the D-flipflop 11. Thereby, a reference voltage source of only relatively low output capacity is then still required and can consequently also be provided at lower costs.

Fig. 2 shows a basic realization of this proposal in the form of a change-over switch 25, which is connected by its control input 26 with the Q-output of the D-flipflop 11, by its output with the resistor 20 and by its two input terminals 27 and 28 respectively with a reference voltage and with ground. While the output signal of the D-flipflop in the case of the converter illustrated by Fig. 1 thus determines the charging and discharging process directly in its value, the D-flipflop 11 in the case of the converter illustrated by Fig. 2 only steers different fixed potentials to the resistor 20.

By reason of this decoupling of the output signal of the D-flipflop 11 from the charging and discharging signals for the capacitor 14, any desired signal level may be provided at each of the input connections 27 and 28 of the switch 25. Particularly in mind in this case are non-linear signal courses in order to produce voltage-frequency converters of non-linear input-output characteristics. Fig. 3 indicates a corresponding embodiment by the inscription of both the input terminals 27 and 28 of the switch 25 by U and U', respectively.

Fig. 4 differes from Fig. 3 in that the switch 25 is realised not as a change-over switch, but as two individual switches 30 and 31. Both switches 30 and 31 are connected at the output sides through a respective resistor 32 and 33 with the capacitor 14. The switches 30 and 31 then expediently receive their drive separately through respective ones of the outputs Q and $\overline{Q}$ of the D-flipflop 11.

Fig. 5 shows a modification of the converter illustrated by Fig. 4 to obtain a non-linear voltage-frequency conversion characteristic by connecting a voltage divider with two resistors 35 and 36 between the input terminal 12 and ground and connecting the junction of both the resistors with the input terminal of the switch 31. The discharging current of the capacitor 14 flowing through the resistor 33 is thus dependent on the input voltage, which acts as a non-linearity on the output signal of the converter.

Fig. 6 illustrates a modification of the converter illustrated by Fig. 5. Both the resistors 32 and 33 of Fig. 5 are now combined in a single resistor 38. The potential at the junction of resistor 38 and both the switches 30 and 31 is also drawn in the circuit diagram and clarifies the influence of this potential in dependence on both the input voltages to the switch 25. Through this measure, the influence of the parasitic output capacitances of the analog switch is substantially eliminated in so far as the analog inputs are of low impedance.

The aforedescribed embodiments of the voltage-frequency converter are simple in their construction, reliable in operation and beyond that also permit non-linear functions between input signal and output signal to be realized. When they are to be employed in signal processing systems operating at a high cyclic frequency, then there appears a small disadvantage of the rigid coupling between clock signal of the D-flipflop 11 and the actuation of the switch 25. The condition illustrated by Fig. 7 can namely then arise that a strictly unique relationship between input signal and output signal is not given for all values of the input signal and that dwell settings designated as "frequency lockings" result. These frequency lockings are shown exaggeratedly in Fig. 7 and are due to the comparator output signal being synchronised to a certain extent with the clock frequency by virtue of the direct coupling between comparator 10 and D-flipflop 11. The problem of the frequency locking or pulling, illustrated in Fig. 7 and appearing with the converters described so far, can be reduced drastically by an arrangement as illustrated in the form of a block schematic diagram in Fig. 8a.

The voltage-frequency converter illustrated by Fig. 8a includes a digitally quantised time base generator in the form of a digitally operating monostable trigger stage 40. A crystal-controlled oscillator 41 is coupled directly with the trigger stage 40 and serves to quantize this time base signal. The remaining parts of this arrangement again correspond with those of the aforedescribed converters.

Fig. 8b illustrates the operating principle of the circuit arrangement of Fig. 8a. When the output signal of the comparator 10 switches over by reason of the steady charging process of the capacitor 14, then the trigger stage 40 also switches for a defined time duration n.T on the occurrence of the next clock pulse. Thereby, the switch 25 is switched into discharging position for the capacitor 14 and the comparator output value again goes back to its initial setting. Independently thereof, the on-time of the trigger stage 40 runs down. A pulsed signal of constant pulse time and a frequency dependent on the input voltage thus results at the output of the converter.

With the chosen input polarity of the comparator 10, a rising output frequency results for a rising input voltage. If thereagainst a reversed proportionality or generally a reversed relationship is desired, then this lets itself be attained through a polarity of other kind at the inputs of the comparator 10 and of the reference voltage.

It is finally still a characteristic feature of the arrangement illustrated by Fig. 8 that very low frequencies can be generated by it in association with a defined input voltage by an appropriate choice of ontime of the trigger stage 40, wherein this on-time is formed by multiples of extremely short cyclic period durations.

Fig. 9 shows an example of the trigger stage 40 of Fig. 8a. A synchronising stage 50, which comprises a Schmitt trigger stage (inverters 51 and 52) connected in front of a D-flipflop 53, couples the comparator 10 with a digitally operating trigger device 40, which comprises a bistable trigger stage 55, a D-flipflop 56, a counter 57 and a decoder 58. While the first input of the

bistable trigger stage 55 is connected with the Q-output of the D-flipflop 53, the second input of this trigger stage 55 is connected to an output 59 of the decoder. Both outputs Q and $\overline{Q}$ of the bistable trigger stage 55 are coupled with the switch 25 and there take care of an appropriate connection of the resistor 20 with either one of two different potentials. The output signal of the voltage-frequency converter is derivable at a second output 60 of the decoding stage 58. Connected in front of the output 59 is a NAND-gate 61, one input of which is coupled with the output Q of the D-flipflop 53 in the synchronising stage 50. This connection has the purpose that the flipflop 55 after run-down of k (k= 1,2 . . . ∞) monoflop periods can switch over only after the comparator 10 has again changed its output signal. Both the D-flipflops 53 and 56, the counter 57 as well as the NAND-gate 61 are pulsed at a very high clock pulse frequency supplied by the oscillator 41 illustrated in Fig. 8, but not in Fig. 9.

The mode of operation of the converter illustrated by Fig. 9 is now to be explained by reference to Fig. 10. As long as the input potential at the negative input of the comparator 10 is smaller than that at the positive input, the output potential of the comparator 10 lies at a high value (Fig. 10b). Thereby, the Q-output of the D-flipflop 53 also displays a logic 1 (Fig. 10d) and the input signal at the following D-flipflop 56 is correspondingly positive. In consequence thereof, the counter remains set to zero. A zero signal is present at the output 60 of the decoding stage 58.

When the effective input polarity of the comparator 10 reverses, then the output signal value thereof goes back, the D-flipflop 53 switches to 0, the output signal of the succeeding D-flipflop 56 likewise drops to zero and the counter 57 thus at a certain output value starts a count at the clock frequency. At the same time, the switch 25 a so switches into a new switch position and thereby discharges the capacitor 14. When the voltage across the capacitor again drops below the potential of the positive input of the comparator, then the output signal thereof again rises independently of the counting process.

When a certain count value has been attained in the counter and detector by means if the decoding stage 58, then the flipflop 55 is again switched over by means of the signal at the output 59 of the decoding stage 58 and the entire arrangement is disposed in its initial position. A switch 65 at one of the inputs of the switch 25 indicates the possibility of switching this discharge signal over from a constant value 0 to the variable input value or a corresponding fraction thereof. In dependence on this switch setting, either a linear or a non-linear relationship results between input voltage and output frequency.

The input circuit of the comparator 10 may be modified by connecting the junction of capacitor 14 and resistor 20 not to the negative input of the comparator 10 as shown in Fig. 9, but instead to the positive input of the comparator 10. This positive input would now preferably be connected not directly to the junction of the reference voltage potential divider (R15 and R17 in Fig. 2), but rather through a series resistor, the capacitor (C16 of Fig. 2) connected between that junction and ground then preferably being omitted. Due to this modification, the signals at the inputs of the switching device must also be interchanged, as a result of which it is now no longer the discharge time of the store that is constant, but the charging time thereof. Only now does the circuit operate in such a manner that an increase in the input voltage also causes an increase in the output frequency.

The constant voltage at the comparator input determines the "freewheeling" frequency. If one dispenses with this constant voltage, then one obtains a transfer function, i.e. output frequency as a function of input voltage, which passes through the origin. The reference voltage potential divider is likewise not necessary for the linear voltage-controlled oscillator when the transfer characteristic thereof is to pass through the origin.

The particular advantages of this modification include a lower component sensitivity and more favourable conditions for initial adjustment.

As already mentioned, suitably designed embodiments of the above-described voltage-frequency converters can represent very reliable and accurately operating signal converters of relatively simple construction. Particularly in mind for their use are signal-preparing circuits in connection with the control of electrical equipments in motor vehicles, for example fuel injection or ignition generation and timing.

CLAIMS

1. A voltage-frequency converter comprising charge storage means, a comparator circuit having input means to receive an input voltage to be converted into a corresponding frequency, a trigger device having input means coupled to output means of the comparator circuit, and switch means operable under the control of the trigger device to apply either a charging signal or a discharging signal to the charge storage means.

2. A voltage-frequency converter as claimed in claim 1, comprising two sources of constant potential of respectively differing value for the charging signal and for the discharging signal thereby to cause a substantially linear voltage-frequency conversion.

3. A voltage-frequency converter as claimed in claim 1, comprising means to cause at least one of the charging signal and the discharging signal to vary as a function of time thereby to cause a non-linear voltage-frequency conversion.

4. A voltage-frequency converter as claimed in claim 3, comprising means to cause at least one of the charging signal and the discharging signal to vary as a function of the input voltage.

5. A voltage-frequency converter as claimed in any one of the preceding claims, wherein the trigger device comprises a bistable trigger stage, a counter and a decoding stage coupled in cascade

in that order, the switch means being operable under the control of the bistable trigger stage.

6. A voltage-frequency converter as claimed in claim 5, comprising a source of source of clock pulses of realtively high frequency coupled to the bistable trigger stage.

7. A voltage-frequency converter as claimed in claim 6, comprising a synchronising stage to couple the output means of the comparator circuit to the input means of the trigger device.

8. A voltage-frequency converter as claimed in any one of the preceding claims, comprising a crystal-controlled oscillator to generate a signal at a frequency which is counted down to determine the duration of the on-time of the trigger device in a monostable state thereof.

9. A voltage-frequency converter substantially as hereinbefore described with reference to and as illustrated by Fig. 2 of the accompanying drawings.

10. A voltage-frequency converter substantially as hereinbefore described with reference to and as illustrated by Fig. 3 of the accompanying drawings.

11. A voltage-frequency converter substantially as hereinbefore described with reference to and as illustrated by Fig. 4 of the accompanying drawings.

12. A voltage-frequency converter substantially as hereinbefore described with reference to and as illustrated by Fig. 5 of the accompanying drawings.

13. A voltage-frequency converter substantially as hereinbefore described with reference to and as illustrated by Fig. 6 of the accompanying drawings.

14. A voltage-frequency converter substantially as hereinbefore described with reference to and as illustrated by Figs. 7 and 8 of the accompanying drawings.

15. A voltage-frequency converter substantially as hereinbefore described with reference to and as illustrated by Figs. 9 and 10 of the accompanying drawings.

16. An electrical control equipment for use in a motor vehicle and comprising a voltage-frequency converter as claimed in any one of the preceding claims.

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