



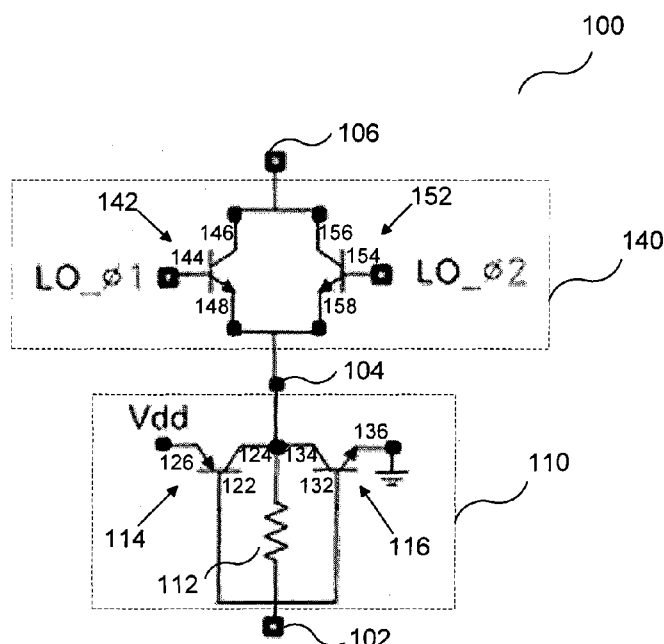
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(54) **Title:** HARMONIC FREQUENCY CONVERSION CIRCUIT

(57) **Abstract:** A harmonic frequency conversion circuit, including an inverter, and a first and second transistor, may include at least one of a resistor or a capacitor connected between a first terminal and a second terminal. The inverter comprises of a P-channel transistor and a N-channel transistor each having a three electrodes. The first and second electrodes of the P-channel and the N-channel transistor are connected to the first and second terminal respectively. The first and second transistor each has three electrodes. The first electrode of the first and second transistors is connected to receive a first local oscillation signal and the second local oscillation signal respectively. The second electrodes of the first and the second transistors are connected to each other at a third terminal. The third electrodes of the first and the second transistors are connected to one of the first terminal or the second terminal of the inverter.

HARMONIC FREQUENCY CONVERSION CIRCUIT

Cross-reference to Related Applications

[0001] The present application claims the benefit of the US provisional patent application No. 61/693,474 filed on 27 August 2012, the entire contents of which are incorporated herein by reference for all purposes.

Technical Field

[0002] Embodiments relate generally to frequency converters, and more particularly to a harmonic frequency conversion circuit.

Background

[0003] Frequency modulators, demodulators and mixers are key functional circuits to perform frequency conversion by multiplying two signals. As it is a multiplication in the time domain, these function circuits can carry both the phase and amplitude information. Frequency converters using modulator, demodulator and mixer may take consideration of or use not only the frequency conversion, but also the phase and amplitude information. The phase and amplitude modulation technique is one of the key techniques used in millimeter-wave communication system, especially for low power high-speed access systems. Normally, it is achieved by a complex and costly down-converter or up-converter chain, which includes baseband modulator, mixers, filters, and amplifiers etc. Now this traditional system can be simplified by replacing up-converting mixers and

associated filters with a vector modulator that directly modulates data onto a carrier signal using orthogonal I (in-phase) and Q (quadrature phase) input signal from baseband for simultaneous amplitude and phase conversion.

[0004] Sub-harmonic, fourth-harmonic, and image-reject type mixers could also be designed with proper arrangement or generation of multiple phases through the phase generation network connected to the local oscillator (LO). The sub-harmonic or fourth-harmonic mixers design would lower down the required LO frequency to half or quarter of the LO frequency required by the traditional fundamental mixer. Therefore it will simplify the LO chain and system integration. The image-reject mixer or modulator/demodulator can suppress the image frequency to certain level by using proper phase combination and thus improve the system linearity. The harmonic and image rejection frequency conversion techniques are especially important for millimeter-wave and broadband communication and radar system.

[0005] There are many techniques of harmonic mixer to simplify the LO requirements, but only a few research works discuss about the millimeter wave modulation and demodulation technique. Modulator and demodulator circuits have been integrated using Semiconductor SiGe (silicon-germanium) HBT (heterojunction bipolar transistor), GaAs (gallium arsenide) HBT and RF (radio frequency) CMOS (complementary metal-oxide-semiconductor) technologies. Harmonic modulators and demodulators are seldom discussed, which bring more challenges for the phase control and integration.

[0006] For modulators or demodulator, the current technologies are mostly based on the fundamental operation, i.e. the fundamental carrier frequency is modulated with

baseband signals, which are either IQ signals or differential IQ signals. The reason may be that the operating frequency of the carrier frequency is low and the fundamental modulator/demodulator are already very complex, which involve lots of amplitude and phase control of high frequency signals with good amplitude and phase balance characteristics.

[0007] The sub-harmonic or harmonic mixers have been reported in GaAs design and some on-board circuit implementation. Only recently, it becomes hot topic to be implemented on the low cost silicon chipset. The sub-harmonic mixer and fourth-harmonic mixer having been reported, which is majorly based on the Gerber cell prototype with tail transistor or resistor to control the bias condition.

Summary

[0008] Various embodiments provide a harmonic frequency conversion circuit. The harmonic frequency conversion circuit may include an inverter having a first terminal and a second terminal. The inverter may include at least one of a resistor or a capacitor connected between the first terminal and the second terminal; a P-channel transistor having a first electrode, a second electrode and a third electrode; and a N-channel transistor having a first electrode, a second electrode and third electrode. The first electrode of the P-channel transistor and the first electrode of the N-channel transistor are connected to the first terminal, and the second electrode of the P-channel transistor and the second electrode of the N-channel transistor are connected to the second terminal. The harmonic frequency conversion circuit may further include a transistor pair connected to the inverter and including a first transistor and a second transistor; wherein

the first transistor has a first electrode, a second electrode and a third electrode; and the second transistor has a first electrode, a second electrode and a third electrode. The first electrode of the first transistor is connected to receive a first local oscillation signal and the first electrode of the second transistor is connected to receive a second local oscillation signal. The second electrode of the first transistor and the second electrode of the second transistor are connected to each other at a third terminal. The third electrode of the first transistor and the third electrode of the second transistor are connected to one of the first terminal or the second terminal of the inverter.

Brief Description of the Drawings

[0009] In the drawings, like reference characters generally refer to the same parts throughout the different views. The drawings are not necessarily to scale, emphasis instead generally being placed upon illustrating the principles of the invention. In the following description, various embodiments are described with reference to the following drawings, in which:

Fig. 1 shows a harmonic frequency conversion circuit 100 according to various embodiments.

Fig. 2A shows a harmonic frequency up-conversion circuit according to various embodiments.

Fig. 2B shows a harmonic frequency down-conversion circuit according to various embodiments.

Fig. 3A shows a harmonic frequency up-conversion circuit according to various embodiments.

Fig. 3B shows a harmonic frequency down-conversion circuit according to various embodiments.

Fig. 4A shows a harmonic frequency up-conversion circuit according to various embodiments.

Fig. 4B shows a harmonic frequency down-conversion circuit according to various embodiments.

Fig. 5A shows a harmonic frequency up-conversion circuit according to various embodiments.

Fig. 5B shows a harmonic frequency down-conversion circuit according to various embodiments.

Fig. 6A shows a harmonic frequency up-conversion circuit according to various embodiments.

Fig. 6B shows a harmonic frequency down-conversion circuit according to various embodiments.

Fig. 7 shows an exemplary layout of an up-conversion sub-harmonic IQ SSB (single sideband) modulator together with an IQ network according to various embodiments.

Fig. 8 shows a transceiver including a sub-harmonic IQ modulator/demodulator according to various embodiments.

Fig. 9 shows a differential IQ sub-harmonic up-conversion DSB (double sideband) mixer/modulator 900 according to various embodiments.

Fig. 10 shows an IQ fourth-harmonic down-conversion SSB mixer/demodulator according to various embodiments.

Description

[0010] Various embodiments provide a harmonic frequency conversion circuit, which may be configured to be used or included in a modulator, a demodulator or a mixer for a transceiver.

[0011] In an embodiment, a "circuit" in the context of this description may be understood as any kind of a logic implementing entity, which may be special purpose circuitry or a processor executing software stored in a memory, firmware, or any combination thereof. Thus, in an embodiment, a "circuit" may be a hard-wired logic circuit or a programmable logic circuit such as a programmable processor, e.g. a microprocessor (e.g. a Complex Instruction Set Computer (CISC) processor or a Reduced Instruction Set Computer (RISC) processor). A "circuit" may also be a processor executing software, e.g. any kind of computer program, e.g. a computer program using a virtual machine code such as e.g. Java. Any other kind of implementation of the respective functions which will be described in more detail below may also be understood as a "circuit" in accordance with an alternative embodiment.

[0012] Fig. 1 shows a harmonic frequency conversion circuit 100 according to various embodiments.

[0013] As shown in Fig. 1, the harmonic frequency conversion circuit 100 may include an inverter 110 having a first terminal 102 and a second terminal 104. The inverter 110 may include at least one of a resistor 112 or a capacitor connected between the first terminal 102 and the second terminal 104; wherein the resistor 112 is shown in Fig. 1. The inverter 110 may also include a P-channel transistor 114 having a first

electrode 122, a second electrode 124 and a third electrode 126; and a N-channel transistor 116 having a first electrode 132, a second electrode 134 and a third electrode 136. The first electrode 122 of the P-channel transistor 114 and the first electrode 132 of the N-channel transistor 116 are connected to the first terminal 102, and the second electrode 124 of the P-channel transistor 114 and the second electrode 134 of the N-channel transistor 116 are connected to the second terminal 104.

[0014] The harmonic frequency conversion circuit 100 may further include a transistor pair 140 connected to the inverter 110, wherein the transistor pair 140 includes a first transistor 142 and a second transistor 152. The first transistor 142 has a first electrode 144, a second electrode 146 and a third electrode 148; and the second transistor 152 has a first electrode 154, a second electrode 156 and a third electrode 158. The first electrode 144 of the first transistor 142 is coupled or connected to receive a first local oscillation signal LO_Ø1 and the first electrode 154 of the second transistor 152 is coupled or connected to receive a second local oscillation signal LO_Ø2. The second electrode 146 of the first transistor 142 and the second electrode 156 of the second transistor 152 are connected to each other at a third terminal 106.

[0015] In various embodiments, the first electrode 144 of the first transistor 142 may be configured to receive the first local oscillation signal LO_Ø1. By way of example, the first electrode 144 of the first transistor 142 may be coupled or connected to a signal generator, e.g. a local oscillator (LO), to receive the first local oscillation signal LO_Ø1. The first electrode 154 of the second transistor 152 may be configured to receive the second local oscillation signal LO_Ø2. By way of example, the first electrode 154 of the

second transistor 152 may be coupled or connected to a signal generator, e.g. a local oscillator (LO), to receive the second local oscillation signal LO_Ø2.

[0016] In various embodiments, the third electrode 148 of the first transistor 142 and the third electrode 158 of the second transistor 152 are connected to one of the first terminal 102 or the second terminal 104 of the inverter 110. In the embodiments shown in Fig. 1, the third electrode 148 of the first transistor 142 and the third electrode 158 of the second transistor 152 are connected to the second terminal 104, i.e. the transistor pair 140 is connected to the second terminal 104 of the inverter 110, so as to form a harmonic frequency up-conversion circuit 100. In various embodiments as show in other figures below, the transistor pair 140 may be connected to the first terminal 102 of the inverter 110, to form a harmonic frequency down-conversion circuit.

[0017] The transistors of the harmonic frequency conversion circuit 100, including the P-channel transistor 114, the N-channel transistor 116, the first transistor 142 and the second transistor 152, may be various types of transistors, such as FET (field effect transistor, e.g. MOSFET (Metal Oxide Semiconductor Field Effect Transistor) or JFET (Junction Gate Field Effect Transistor), BJT (bipolar junction transistor), IGBT (Insulated Gate Bipolar Transistor), and HEMT (High Electron Mobility Transistor), etc. By way of example, the P-channel transistor 114 may be a P-MOS, a P-BJT, or a P-HEMT transistor, and the N-channel transistor 116 may be a N-MOS, a N-BJT, or a N-HEMT transistor.

[0018] In various embodiments, the transistors in the harmonic frequency conversion circuit 100 may be same or different types of transistors. By way of example, the first transistor 142 and the second transistor 152 of the transistor pair 140 may be BJT

transistors, while the transistors 114 and 116 in the inverter 110 may be CMOS (complementary metal-oxide-semiconductor) transistors.

[0019] In various embodiments, the inverter 110 may include a resistor 112, or a capacitor (not shown), or a resistor connected with a capacitor in parallel, between the first terminal 102 and the second terminal 104.

[0020] Depending on the types of transistors used for the P-channel transistor 114 and the N-channel transistor 116, the first electrode 122 of the P-channel transistor 114 and the first electrode 132 of the N-channel transistor 116 may be gate electrodes or base electrodes. For example, the first electrode 122 may be a gate electrode when the P-channel transistor 114 is a FET. Similarly, the second electrode 124 of the P-channel transistor and the second electrode 134 of the N-channel transistor may be one of drain electrode or collector electrode. The third electrode 126 of the P-channel transistor and the third electrode 136 of the N-channel transistor may be one of source electrode or emitter electrode.

[0021] In various embodiments, the third electrode 126 of the P-channel transistor 114 is coupled or connected to a DC supply (Vdd), and the third electrode 136 of the N-channel transistor 116 is connected to the ground.

[0022] Depending on the types of transistors used for the first transistor 142 and the second transistor 152, the first electrode 144 of the first transistor and the first electrode 154 of the second transistor may be one of gate electrode or base electrode. Similarly, the second electrode 146 of the first transistor and the second electrode 156 of the second transistor may be one of drain electrode or collector electrode. The third electrode 148 of

the first transistor and the third electrode 158 of the second transistor may be one of source electrode or emitter electrode.

[0023] In various embodiments, at least one DC source and necessary bias network may be included in the harmonic frequency conversion circuit 100 to provide a bias voltage for the operation of the transistors 114, 116, 142, 152.

[0024] In various embodiments, the harmonic frequency conversion circuit 100 may further include a DC bias (not shown) coupled or connected to the third terminal 106. The DC bias may be supplied to the third terminal 106 through a resistor or an inductor, e.g., to avoid RF leakage to DC.

[0025] In various embodiments, the harmonic frequency conversion circuit 100 may further include at least one of a resistor, an inductor, a LC tank or transmission lines coupled or connected to the third terminal 106.

[0026] The first local oscillation signal LO_Ø1 and the second local oscillation signal LO_Ø2 may be the same signal or may be different signals. The first local oscillation signal LO_Ø1 and the second local oscillation signal LO_Ø2 may have the same amplitude. In various embodiments, the first local oscillation signal LO_Ø1 and the second local oscillation signal LO_Ø2 may have a 180-degree phase difference.

[0027] According to various embodiments, the third electrode 148 of the first transistor 142 and the third electrode 158 of the second transistor 152 are connected to the second terminal 104 of the inverter 110, i.e. the transistor pair 140 is connected to the second terminal 104 of the inverter 110. Accordingly, the harmonic frequency conversion circuit 100 may be configured to receive an intermediate frequency (IF) signal at the first terminal 102 of the inverter, and configured to output a radio frequency (RF) signal from the third terminal 106.

[0028] In various embodiments, when the transistor pair 140 is connected to the second terminal 104 of the inverter 110, the inverter 110 and the transistor pair 140 form a first sub-harmonic frequency up-conversion cell. The harmonic frequency conversion circuit 100 may include a further inverter and a further transistor pair forming a second sub-harmonic frequency up-conversion cell. The first cell may be configured to receive a 0 degree phase shifted intermediate frequency (IF) signal (also referred to as an in-phase IF signal) at the first terminal thereof. The second cell may be configured to receive a 90 degree phase shifted intermediate frequency (IF) signal (also referred to as an quadrature phase IF signal) at the first terminal thereof. The harmonic frequency conversion circuit formed thereof may be referred to as a sub-harmonic IQ frequency up-conversion circuit.

[0029] In various embodiments, the harmonic frequency conversion circuit 100 may further include a second sub-harmonic frequency up-conversion cell, a third sub-harmonic frequency up-conversion cell, and a fourth sub-harmonic frequency up-conversion cell, wherein each of the second cell, the third cell and the fourth cell includes an inverter and a transistor pair similar to the inverter 110 and the transistor pair 140 of the first sub-harmonic frequency up-conversion cell described above. The first cell and the second cell may be connected to each other at their third terminals, and the third cell and the fourth cell may be connected to each at their third terminals. The first cell may be configured to receive a 0 degree phase shifted intermediate frequency signal at the first terminal thereof; the second cell may be configured to receive a 180 degree phase shifted intermediate frequency signal at the first terminal thereof, the third cell may be configured to receive a 270 degree phase shifted intermediate frequency signal at the first terminal thereof; and the fourth cell may be configured to receive a 90 degree phase

shifted intermediate frequency signal at the first terminal thereof. The harmonic frequency conversion circuit formed thereof may be referred to as a differential IQ sub-harmonic frequency up-conversion circuit.

[0030] According to various embodiments, the third electrode 148 of the first transistor 142 and the third electrode 158 of the second transistor 152 may be connected to the first terminal 102 of the inverter 110, i.e. the transistor pair 140 is connected to the first terminal 102 of the inverter 110. Accordingly, the harmonic frequency conversion circuit 100 may be configured to receive a radio frequency (RF) signal at the third terminal 106, and configured to output an intermediate frequency (IF) signal from the second terminal 104 of the inverter 110.

[0031] In various embodiments, when the transistor pair 140 is connected to the first terminal 102 of the inverter 110, the inverter 110 and the transistor pair 140 form a first sub-harmonic frequency down-conversion cell.

[0032] In various embodiments, the harmonic frequency conversion circuit 100 may further include a further inverter and a further transistor pair forming a second sub-harmonic frequency down-conversion cell. The first cell may be configured to receive a 0 degree phase shifted radio frequency signal (also referred to as an in-phase RF signal) at the third terminal thereof, and the second cell may be configured to receive a 90 degree phase shifted radio frequency signal (also referred to as a quadrature phase RF signal) at the third terminal thereof. The harmonic frequency conversion circuit formed thereof may be referred to as a sub-harmonic IQ frequency down-conversion circuit.

[0033] In various embodiments, the harmonic frequency conversion circuit 100 may further include a second sub-harmonic frequency down-conversion cell, a third sub-

harmonic frequency down-conversion cell, and a fourth sub-harmonic frequency down-conversion cell, wherein each of the second cell, the third cell and the fourth cell includes an inverter and a transistor pair similar to the inverter 110 and the transistor pair 140 of the first sub-harmonic frequency down-conversion cell described above. The first cell and the second cell may be connected to each other at their third terminals, and the third cell and the fourth cell may be connected to each at their third terminals. The first cell and the second cell may be configured to receive a 180 degree phase shifted radio frequency signal at their third terminals, and the third cell and the fourth cell may be configured to receive a 270 degree phase shifted radio frequency signal at their third terminals. The harmonic frequency conversion circuit formed thereof may be referred to as a differential IQ sub-harmonic frequency down-conversion circuit.

[0034] According to various embodiments, the harmonic frequency conversion circuit 100 may include a further transistor pair connected to the inverter 110, wherein the transistor pair 140 and the further transistor pair are connected in parallel. The first local oscillation signal received by the transistor pair 140 and the first local oscillation signal received by the further transistor pair may have a 90-degree phase difference, and the second local oscillation signal received by the transistor pair 140 and the second local oscillation signal received by the further transistor pair may have a 90-degree phase difference.

[0035] In further embodiments, the harmonic frequency conversion circuit 100 may include a second transistor pair, a third transistor pair and a fourth transistor pair, wherein the transistor pair 140, the second transistor pair, the third transistor pair and the fourth transistor pair are connected with each other in parallel and are connected to the inverter

110. The first local oscillation signals received by the transistor pair 140, the second transistor pair, the third transistor pair and the fourth transistor pair may have a 45-degree phase difference in sequence. The second local oscillation signals received by the transistor pair 140, the second transistor pair, the third transistor pair and the fourth transistor pair have a 45-degree phase difference in sequence.

[0036] The harmonic frequency conversion circuit 100 described in various embodiments above may be configured to be used in at least one of a modulator, a demodulator or a mixer. Especially for the harmonic conversion cells, we only use

[0037] Various embodiments of the harmonic frequency conversion circuit 100 described above will be described in more detail with reference to the figures below. In various embodiments, the symmetrical transistor pair 140 may include more than two transistors, for example, the transistor pair 140 may be a transistor array having any even number of the transistors, such as 4, 6, 8, ...transistors. In various embodiments, the harmonic frequency conversion circuit 100 may include multiple inverter combination with the similar configuration as the inverter 110, or may include a single inverter 110 having multiple transistors inside of the inverter. The transistor pair 140 and frequency inverter 110 show in Fig. 1 may be used as the fundamental blocks and may be combined in various manner to form various types of harmonic frequency conversion circuits, as will be described with regard to Figs. 2A-2B, 3A-3B, 4A-4B, 5A-5B, 6A-6B, 9 -10 below.

[0038] Various embodiments are based on the fundamental frequency conversion circuit including the transistor pair and the inverter in combination. By using the fundamental frequency conversion circuit, different types of modulator, demodulator and

mixer, including sub-harmonic, fourth-harmonic, 8th-harmonic conversions etc., are may be provided in various embodiments.

[0039] Various embodiments may simplify the harmonic circuits, in which the fundamental sub-harmonic frequency conversion circuit is formed by the confronted transistor pair together with the inverter. The inverter may be used for both up and down frequency conversion or modulation, and the required signal with different phases may be input to or generated from the inverter. This may simplify the requirement for both the bias and I/O (input/output) matching circuit, and may also benefit the layout simplification.

[0040] The harmonic frequency conversion circuit of various embodiments may also provide better conversion gain and broad band input data or information, since the inverter inside of the frequency conversion circuit not only performs the function of impedance matching but also provides the necessary gain for the input or output IF signal or data. The basic isolation among the carrier, the IF/data and RF may also be provided by the inverter.

[0041] The harmonic frequency conversion circuit of various embodiments may provide low power consumption, since the combination of the inverter and the harmonic transistor pair may provide good DC bias condition without using the folded structures. This combination may simplify the circuit and layout for tradeoff the power consumption reduction.

[0042] The harmonic frequency conversion circuit of various embodiments may lower down the requirements for the carrier, since the harmonic frequency conversion scheme or modulation scheme can reduce the requirement of the LO (local oscillator)

operation frequency by the targeted number of the harmonic. For example, the sub-harmonic may require half of the LO frequency required by the fundamental scheme and the 4th harmonic may require one quarter of the LO frequency required by the fundamental frequency conversion scheme. The performance of LO including power consumption, phase noise etc. may be decreased with the increase of the LO frequency, but the design complexity may be increased with the increase of the LO frequency. Thus, various embodiments using the harmonic scheme may simplify the LO design.

[0043] The harmonic frequency conversion circuit of various embodiments may simplify the overall transceiver architecture, since the harmonic frequency conversion provides simplified LO for the mixer and modulator/demodulator operation. For example, for the modulator, baseband data may be directly modulated to RF/microwave/millimeter data without carrying out the frequency conversion using up-conversion mixer. For the demodulator, RF/ microwave/ Millimeter-wave data may be directly demodulated to baseband data without carrying out the frequency conversion using down-conversion mixer.

[0044] Figs. 2A-2B show harmonic frequency conversion circuits according to various embodiments.

[0045] Fig. 2A shows a harmonic frequency up-conversion circuit 200 according to various embodiments, which may be configured to be used in a up-conversion mixer or modulator.

[0046] As shown in Fig. 2A, the harmonic frequency up-conversion circuit 200 is similar to the harmonic frequency conversion circuit 100 of Fig. 1, and includes the inverter 110 and the transistor pair 140. In this embodiment, the transistor pair 140 is

connected to the second terminal of the inverter 110. Various embodiments described with reference to Fig. 1 above are also valid for the harmonic frequency up-conversion circuit 200.

[0047] The P-transistor (Q1) 114, the N-transistor (Q2) 116 and the resistor (R1) 112 form the inverter 110, which is connected with the transistor pair 140 including the first transistor (Q3) 142 and the second transistor (Q4) 152 at the second terminal 104, and is configured to receive IF signal or IF data at the first terminal 102. The resistor (R1) 112 inside the inverter 110 may be used to tradeoff between the gain and input/output matching. Though the resistor R1 is shown in the embodiments of Fig. 2A, it is understood that a capacitor, or a resistor connected in parallel with a capacitor, may be provided between the first terminal 102 and the second terminal 104 of the inverter 110. The “source” (or “emitter”) electrode 126 of the P-transistor Q1 inside the inverter 110 may be coupled or connected to a DC supply (Vdd) directly or through lumped elements or transmission line. The “source” (or “emitter”) electrode 136 of the N-transistor Q2 may be connected to the ground.

[0048] In various embodiments, IF signal (e.g., for an up-conversion mixer) or IF data (e.g., for an up-conversion modulator) from the baseband or other digital source may be feed into the “gate” (or “base”) electrodes 122, 132 of the transistors Q1 and Q2 through the first terminal 102, as shown in Fig. 2A. The first transistor Q3 and the second transistor Q4 are connected in confront, with their “source” (or “emitter”) electrodes 148, 158 connected with each other and their “drain” (or “collector”) electrodes 146, 156 connected with each other as shown in Fig. 2A. The “gate” (or “base”) electrodes 144, 154 of the transistors Q3 and Q4 are connected with the first LO signal LO-Ø1 and the

second LO signal LO-Ø2 with or without DC 260, respectively. For sub-harmonic frequency conversion operation, the LO signals LO-Ø1 and LO-Ø2 may be anti-phase, i.e., may have a 180-degree phase difference. The amplitude of the LO signals LO-Ø1 and LO-Ø2 may be equal. The DC bias 206 may be applied together with the LO signals LO-Ø1 and LO-Ø2 for the transistor “gate” (or “base”) bias purpose.

[0049] The harmonic frequency up-conversion circuit 200 may convert the IF signal or data received at the first terminal 102 to a RF signal or data, and may output the RF signal or data from the third terminal 106. In various embodiments, the third terminal 106 may be coupled or connected to the DC bias 260, e.g. by connecting to a bias network or a DC supply network or both. In various embodiments, the third terminal 106 (i.e. the common node connected with the “drain” or “collector” electrodes 146, 156 of the transistor Q3 and Q4 may be further connected to inductors, resistors, LC tank, transmission lines or their combination for matching and/or bias purpose.

[0050] Fig. 2B shows a harmonic frequency down-conversion circuit 290 according to various embodiments, which may be configured to be used in a down-conversion mixer or demodulator.

[0051] As shown in Fig. 2B, the harmonic frequency down-conversion circuit 290 is similar to the harmonic frequency up-conversion circuit 200 of Fig. 2A, with the difference that the transistor pair 140 is connected to the first terminal 102 of the inverter 110. Various embodiments described with reference to Fig. 2A above are also valid for the harmonic frequency down-conversion circuit 290.

[0052] For the down-conversion circuit 290, RF signal or data may be received at the third terminal 106 and may be converted to IF signal or data. The IF signal (e.g., for

down-conversion mixer) or data (e.g., for down-conversion demodulator) to baseband or other digital source may be output from the “drain” (or “collector”) electrodes 124, 134 of the transistors Q1 and Q2 at the second terminal 104, as shown in Fig. 2B. The common node of “gate” (or “base”) electrodes 122, 132 of transistors Q1 and Q2 are connected to the common node of “source” (or “emitter”) electrodes 148, 158 of the transistor Q3 and Q4 at the first terminal 102. The other connections and signals, such as LO-Ø1, LO-Ø2, RF, DC, etc. are similar to the connections and signals for the up-conversion circuit 200.

[0053] The harmonic frequency conversion circuits 200, 290 of Figs. 2A-2B may be referred to as a sub-harmonic frequency up-conversion circuit and a sub-harmonic frequency down-conversion circuit, respectively.

[0054] Figs. 3A-3B show harmonic frequency conversion circuits according to various embodiments.

[0055] Fig. 3A shows a harmonic frequency up-conversion circuit 300 according to various embodiments, which may be configured to be used in an up-conversion mixer or modulator. In the embodiments of Fig. 3A, the harmonic frequency up-conversion circuit 300 may be referred to as a fourth-harmonic up-conversion circuit. The fourth-harmonic up-conversion circuit 300 is similar to the sub-harmonic up-conversion circuit 200 of Fig. 2A, with the difference that the fourth-harmonic up-conversion circuit 300 includes a further transistor pair 340 connected in parallel with the transistor pair 140. Various embodiments described with reference to Fig. 2A are also valid for the fourth-harmonic up-conversion circuit 300.

[0056] As shown in Fig. 3A, the inverter 110 is similar to the inverter 110 of the circuit 200. The P-transistor transistor Q1, the N-transistor Q2 and the resistor R1 form the inverter 110, which is connected with IF signal or data at the first terminal 102. The inverter 110 is further connected to the transistor pair 140 (Q3 & Q4) and the further transistor pair 340 (Q5 & Q6) at the second terminal 104. The resistor R1 inside the inverter 110 may be used to tradeoff between the gain and input/output matching. The “source” (or “emitter”) electrodes 126 of the P-transistor Q1 is connected to the DC supply (Vdd) directly or through lumped elements or transmission line, and the “source” (or “emitter”) electrodes 136 of the N-transistor Q2 is connected to the ground.

[0057] In the fourth-harmonic up-conversion circuit 300, the IF signal (for up-conversion mixer) or data (for up-conversion modulator) from baseband or other digital source is feed into the “gate” (or “base”) electrodes 122, 132 of the transistors Q1 and Q2 as shown in Fig. 3A. The transistor pair Q3 and Q4 are connected in confront with their “source” (or “emitter”) electrodes connected each other and their “drain” (or “collector”) electrodes connected each other. The “gate” (or “base”) electrodes of the transistors Q3 and Q4 are connected with two LO signals LO-Ø1 and LO-Ø2 with or without DC respectively. The further transistor pair 340 also includes a first transistor Q5 342 and a second transistor Q6 352. The connection between the transistors Q5 and Q6 may be similar to the connection between the transistors Q3 and Q4 of the transistor pair 340 described above. The first transistor Q5 and the second transistor Q6 of the further transistor pair 340 may be connected, with their “source” (or “emitter”) electrodes connected with each other and their “drain” (or “collector”) electrodes connected with each other as shown in Fig. 3A. The “gate” (or “base”) electrodes of the transistors Q5

and Q6 are connected with a third LO signal LO-Ø3 and a fourth LO signal LO-Ø4 with or without DC 260, respectively.

[0058] For fourth-harmonic conversion operation, the LO signals LO-Ø1 and LO-Ø2 of the transistor pair 140 may be anti-phase, i.e., may have a 180-degree phase difference, and the amplitude of the LO signals LO-Ø1 and LO-Ø2 may be equal. Similarly, the LO signals LO-Ø3 and LO-Ø4 of the transistor pair 340 may have a 180-degree phase difference, and the amplitude of the LO signals LO-Ø3 and LO-Ø4 may be equal. The LO signals of different transistor pairs, e.g., LO-Ø1 and LO-Ø3, may have a 90-degree phase difference, and the LO signals LO-Ø2 and LO-Ø4 may have a 90-degree phase difference. In various embodiments, the LO signals of LO-Ø1, LO-Ø3, LO-Ø2 and LO-Ø4 may have the same amplitude and may have phase difference of 90 degrees in sequence. By way of example, LO-Ø1 may be 0 degree phase shifted, LO-Ø2 may be 180 degree phase shifted, LO-Ø3 may be 90 degree phase shifted, and LO-Ø4 may be 270 degree phase shifted. The DC 260 may be applied together with LO-Ø1, LO-Ø2, LO-Ø3 and LO-Ø4 for the transistor "gate" (or "base") bias purpose. The common node 106 connected with "drain" (or "collector") electrodes of the transistors Q3, Q4, Q5 and Q6 may be coupled or connected to a RF connection node and/or a DC bias 260, and may be further connected to inductors, resistors, LC tank, transmission lines or their combination for matching and/or bias purpose.

[0059] Fig. 3B shows a harmonic frequency down-conversion circuit 390 according to various embodiments, which may be configured to be used in a down-conversion mixer or demodulator.

[0060] As shown in Fig. 3B, the harmonic frequency down-conversion circuit 390 (also referred to as a fourth-harmonic down-conversion circuit) is similar to the harmonic frequency up-conversion circuit 300 of Fig. 3A, with the difference that the transistor pair 140 and the further transistor pair 340 are connected to the first terminal 102 of the inverter 110. Various embodiments described with reference to Fig. 3A above are also valid for the harmonic frequency down-conversion circuit 390.

[0061] In the down-conversion circuit 390, the IF signal (e.g., for down-conversion mixer) or data (e.g. for down-conversion demodulator) to baseband or other digital source may be output from the “drain” (or “collector”) electrodes 124, 134 of the transistors Q1 and Q2 at the second terminal 104 as shown in Fig. 3B. The common node of “gate” (or “base”) electrodes 122, 132 of transistors Q1 and Q2 are connected to the common node of “source” (or “emitter”) electrodes of the transistors Q3, Q4, Q5 and Q6 at the first terminal 102. The other connections and signals, such as LO-Ø1, LO-Ø2, LO-Ø3, LO-Ø4, RF, DC etc. are similar to the connections and signals for the up-conversion circuit 300.

[0062] Figs. 4A-4B show harmonic frequency conversion circuits according to various embodiments.

[0063] Fig. 4A shows a harmonic frequency up-conversion circuit 400 according to various embodiments, which may be configured to be used in an up-conversion mixer or modulator. In the embodiments of Fig. 4A, the harmonic frequency up-conversion circuit 400 may be referred to as a 8th-harmonic up-conversion circuit. The 8th-harmonic up-conversion circuit 400 is similar to the sub-harmonic up-conversion circuit 200 of Fig. 2A and the fourth-harmonic up-conversion circuit 300 of Fig. 3A, with the difference that

the 8th-harmonic up-conversion circuit 400 includes four transistor pairs 140, 340, 440, 450 connected in parallel with each other. Various embodiments described with reference to Fig. 2A and Fig. 3A are also valid for the 8th-harmonic up-conversion circuit 400. Although the circuit 400 shown in Fig. 4A includes four transistor pairs connected to the inverter to form the 8th-harmonic up-conversion circuit, it is understood that more than four transistor pairs may be connected to the inverter in the analogous manner to form various harmonic up-conversion circuit, such as 16th-harmonic and 32-th harmonic up-conversion circuit. In various embodiments, the harmonic conversion circuit of up to N-th harmonics may be formed, wherein $N/2$ transistor pairs may be provided to connect to one inverter, and N LO signals having the same amplitude but having phase difference by $360\text{degree}/N$ in sequence may be provided to the N-th harmonic conversion circuit.

[0064] As shown in Fig. 4A, the inverter 110 is similar to the inverter 110 of the circuits 200, 300. The P-transistor transistor Q1, the N-transistor Q2 and the resistor R1 form the inverter 110, which is connected with IF signal or data at the first terminal 102. The inverter 110 is further connected to a first transistor pair 140 (Q3 & Q4), a second transistor pair 340 (Q5 & Q6), a third transistor pair 440 (Q3 & Q4) and a fourth transistor pair 450 (Q5 & Q6) at the second terminal 104. The resistor R1 inside the inverter 110 may be used to tradeoff between the gain and input/output matching. The “source” (or “emitter”) electrodes 126 of the P-transistor Q1 is connected to the DC supply (Vdd) directly or through lumped elements or transmission line, and the “source” (or “emitter”) electrodes 136 of the N-transistor Q2 is connected to the ground.

[0065] In various embodiments, the LO signals within the same transistor pair may have a 180-degree phase difference, and may have the same or substantially the same

amplitude. By way of example, the first transistor pair 140 may receive LO signals LO_0 and LO_180 having a 180-degree phase difference between each other.

[0066] For 8th-harmonic conversion operation, the LO signals LO_0, LO_45, LO_90, LO_135, LO_180, LO_225, LO_270, LO_315 may have the same amplitude, and may have phase difference of 45 degrees in sequence (i.e. 0, 45, 90, 135, 180, 225, 270, 315 degree phase shifted). By way of example, the first transistor pair 140 may receive LO signals LO_0 and LO_180, the second transistor pair 340 may receive LO signals LO_90 and LO_270, the third transistor pair 440 may receive LO signals LO_45 and LO_225, and the fourth transistor pair 450 may receive LO signals LO_135 and LO_315, as shown in Fig. 4A. The DC 260 may be applied together with the LO signals LO_0, LO_45, LO_90, LO_135, LO_180, LO_225, LO_270 and LO_315 for the transistor “gate” (or “base”) bias purpose. The common node 106 connected with “drain” (or “collector”) electrodes of the transistor pairs 140, 340, 440, 450 may be coupled or connected to a RF connection node and/or the DC bias 260, and may be further connected to inductors, resistors, LC tank, transmission lines or their combination for matching and/or bias purpose.

[0067] Fig. 4B shows a harmonic frequency down-conversion circuit 490 according to various embodiments, which may be configured to be used in a down-conversion mixer or demodulator.

[0068] As shown in Fig. 4B, the harmonic frequency down-conversion circuit 490 (also referred to as a 8th-harmonic down-conversion circuit) is similar to the harmonic frequency up-conversion circuit 400 of Fig. 4A, with the difference that the transistor pairs 140, 340, 440, 450 are connected to the first terminal 102 of the inverter 110.

Various embodiments described with reference to Fig. 4A above are also valid for the harmonic frequency down-conversion circuit 490.

[0069] In the down-conversion circuit 490, the IF signal (for down-conversion mixer) or data (for down-conversion demodulator) to baseband or other digital source may be output from the “drain” (or “collector”) electrodes 124, 134 of the transistors Q1 and Q2 at the second terminal 104 as shown in Fig. 4B. The common node of “gate” (or “base”) electrodes 122, 132 of transistors Q1 and Q2 are connected to the common node of “source” (or “emitter”) electrodes of the transistor Q3, Q4, Q5 and Q6 at the first terminal 102. The other connections and signals, such as LO_0, LO_45, LO_90, LO_135, LO_180, LO_225, LO_270 and LO_315, RF, DC etc. may be similar to the connections and signals for the up-conversion circuit 400. In various embodiments, the transistors with the same name may be different, for example, the transistors Q3, Q4 of the first transistor pair 140 may be different from the transistors Q3, Q4 of the third transistor pair 440.

[0070] Figs. 5A-5B show harmonic frequency conversion circuits according to various embodiments.

[0071] Fig. 5A shows a harmonic frequency up-conversion circuit 500 according to various embodiments, which may be configured to be used in an up-conversion mixer or modulator. The harmonic frequency up-conversion circuit 500 may include the sub-harmonic up-conversion circuit 200 of Fig. 2A having an inverter 110 and a transistor pair 140. Various embodiments described with reference to Fig. 2A are also valid for the harmonic frequency up-conversion circuit 500.

[0072] The harmonic frequency up-conversion circuit 500 may include a further sub-harmonic up-conversion circuit similar to the sub-harmonic up-conversion circuit 200, wherein the further sub-harmonic up-conversion circuit includes an inverter 510 and a transistor pair 540 having similar components and connections as those of the inverter 110 and the transistor pair 140. In various embodiments, the inverter 510 may include a P-transistor (Q1) 514, a N-transistor (Q2) 516 and a resistor (R) 512, and may be connected with the transistor pair 540 including a first transistor (Q3) 542 and a second transistor (Q4) 552 at the second terminal 504. The inverter 510 may be configured to receive IF signal or IF data at the first terminal 502. The resistor R 512 inside the inverter 510 may be used to tradeoff between the gain and input/output matching. Though the resistor R1 is shown in the embodiments of Fig. 5A, it is understood that a capacitor, or a resistor connected in parallel with a capacitor, may be provided between the first terminal 502 and the second terminal 504 of the inverter 510. The “source” (or “emitter”) electrode of the P-transistor 514 inside the inverter 510 may be coupled or connected to a DC supply (Vdd) directly or through lumped elements or transmission line. The “source” (or “emitter”) electrode of the N-transistor 516 may be connected to the ground.

[0073] In various embodiments, the inverter 110 may be configured to receive in-phase signal/data (i.e. “I” signal/data) and the inverter 512 may be configured to receive quadrature phase signal/data (i.e. “Q” signal/data). By way of example, the inverter 110 may receive 0 degree phase shifted IF signal (denoted by IF_0) or 0 degree phase shifted IF data (denoted by Data_0) at its first terminal 102; and may be connected to the transistor pair 140 at its second terminal 104. The transistor pair 140 may output 0 degree phase shifted RF signal (denoted by RF_0) at the third terminal 106. By way of example,

the inverter 510 may receive 90 degree phase shifted IF signal (denoted by IF_90) or 90 degree phase shifted IF data (denoted by Data_90) at its first terminal 502, and may be connected to the transistor pair 540 at its second terminal 504. The transistor pair 540 may output 90 degree phase shifted RF signal (denoted by RF_90) at the third terminal 506.

[0074] The third terminal 106 of the transistor pair 140 and the third terminal 506 of the transistor pair 540 may be connected to inductors, resistors, LC tank, transmission lines or their combination for matching and/or bias purpose. The third terminals 106, 506 may be connected to inductors for DC bias and RF blocking. In the embodiments shown in Fig. 5A, the common node 106 connected with “drain” (or “collector”) electrodes 146, 156 of the transistor pair 140 may be coupled or connected to a DC bias 560 (VDD) through an inductor L1 562, and the common node 506 connected with “drain” (or “collector”) electrodes of the transistor pair 540 may be coupled or connected to the DC bias 560 (VDD) through an inductor L2 564. The inductors L1 and L2 may have the same or different values or parameters.

[0075] In various embodiments as shown in Fig. 5A, the harmonic frequency up-conversion circuit 500 may further include a 90 degree hybrid coupler 566, wherein the nodes 106, 506 for output RF_0 and RF_90 may be connected to two ports of the four-port 90 degree hybrid coupler 566 through two capacitors C1 and C2, respectively. The other two ports i.e. output port and isolation port, of the 90 degree hybrid coupler 566 may be used for upper sideband (USB) frequency conversion signal or low sideband (LSB) frequency conversion signal. In this manner, the harmonic frequency up-conversion circuit 500 may be configured to generate upper side band (USB)

mixed/modulated signal or low side band (LSB) mixed/modulated signal for conversion from in-phase and quadrature-phase IF signal/data.

[0076] The harmonic frequency up-conversion circuit 500 according to the embodiments of Fig. 5A may be referred to or used as a sub-harmonic IQ frequency up-conversion SSB (single sideband) mixer/modulator.

[0077] Fig. 5B shows a harmonic frequency down-conversion circuit 590 according to various embodiments, which may be configured to be used in a down-conversion mixer or demodulator.

[0078] As shown in Fig. 5B, the harmonic frequency down-conversion circuit 590 is similar to the harmonic frequency up-conversion circuit 500 of Fig. 5A, with the difference that the transistor pairs 140, 540 are respectively connected to the first terminal 102, 502 of the inverters 110, 510. Various embodiments described with reference to Fig. 5A above are also valid for the harmonic frequency down-conversion circuit 590.

[0079] In Fig. 5B, the inverter 110 may be configured to output in-phase signal/data (i.e. "I" signal/data) and the inverter 512 may be configured to output quadrature phase signal/data (i.e. "Q" signal/data). By way of example, the transistor pair 140 may receive 0 degree phase shifted RF signal (denoted by RF_0) at the third terminal 106, and the inverter 110 may output 0 degree phase shifted IF signal (denoted by IF_0) or 0 degree phase shifted IF data (denoted by Data_0) at its second terminal 104. By way of example, the transistor pair 540 may receive 90 degree phase shifted RF signal (denoted by RF_90) at the third terminal 506, and the inverter 510 may output 90 degree phase shifted IF signal (denoted by IF_90) or 90 degree phase shifted IF data (denoted by Data_90) at its second terminal 504.

[0080] The third terminal 106 of the transistor pair 140 and the third terminal 506 of the transistor pair 540 may be connected to inductors, resistors, LC tank, transmission lines or their combination for matching and/or bias purpose. In the embodiments shown in Fig. 5B, the common node 106 connected with “drain” (or “collector”) electrodes 146, 156 of the transistor pair 140 may be coupled or connected to the DC bias 560 (VDD) through the inductor L1 562, and the common node 506 connected with “drain” (or “collector”) electrodes of the transistor pair 540 may be coupled or connected to the DC bias 560 (VDD) through the inductor L2 564. The inductors L1 and L2 may have the same or different values or parameters.

[0081] In various embodiments, the nodes 106, 506 for output RF_0 and RF_90 may be connected to the 90 degree hybrid coupler 566 through two capacitors C1 and C2, respectively. In this manner, the harmonic frequency down-conversion circuit 590 may be configured to add upper side band (USB) mixed/modulated signal or low side band (LSB) mixed/modulated signal for conversion to in-phase and quadrature-phase IF signal/data.

[0082] The harmonic frequency down-conversion circuit 590 according to the embodiments of Fig. 5B may be referred to or used as a sub-harmonic IQ frequency down-conversion SSB (single sideband) mixer/demodulator.

[0083] Figs. 6A-6B show harmonic frequency conversion circuits according to various embodiments.

[0084] Fig. 6A shows a harmonic frequency up-conversion circuit 600 according to various embodiments, which may be configured to be used in an up-conversion mixer or modulator with image rejection. The harmonic frequency up-conversion circuit 600 may

include the sub-harmonic up-conversion circuit 200 of Fig. 2A having an inverter 110 and a transistor pair 140, is similar to the harmonic frequency up-conversion circuit 500 of Fig. 5A. Various embodiments described with reference to Fig. 2A and Fig. 5A are also valid for the harmonic frequency up-conversion circuit 600.

[0085] The harmonic frequency up-conversion circuit 600 may further include a second sub-harmonic up-conversion circuit 200B, a third sub-harmonic up-conversion circuit 200C and a fourth sub-harmonic up-conversion circuit 200D. The circuits 200B, 200C, 200D are similar to the sub-harmonic up-conversion circuit 200, may each include an inverter and a transistor pair having similar components and connections as those of the inverter 110 and the transistor pair 140 of the sub-harmonic frequency up-conversion circuit 200.

[0086] In each of the sub-harmonic up-conversion circuits 200, 200B, 200C, 200D, a P-transistor Q1, a N-transistor Q2 and a resistor R1/R forms an inverter, which may be configured to receive IF signal or data from baseband or other digital sources. In various embodiments, the common node of “gate” (or “base”) electrodes of transistors Q1 and Q2 of the inverters may be connected to differential “I” signal/data or differential “Q” signal/data input from baseband or other sources. The resistor R1/R inside the inverters may be used to tradeoff between the gain and input/output matching. By way of example, the sub-harmonic up-conversion circuit 200, 200B may be configured to receive differential “I” signal/data, wherein the circuit 200 may receive 180 degree phase shifted IF signal/data (denoted by IF_180 or data_180) at its first terminal 102, and the circuit 200B may receive 0 degree phase shifted IF signal/data (denoted by IF_0 or data_0) at its first terminal 102B. By way of example, the sub-harmonic up-conversion circuit 200C,

200D may be configured to receive differential “Q” signal/data, wherein the circuit 200C may receive 270 degree phase shifted IF signal/data (denoted by IF_270 or data_270) at its first terminal 102C, and the circuit 200D may receive 90 degree phase shifted IF signal/data (denoted by IF_90 or data_90) at its first terminal 102D.

[0087] For harmonic conversion operation, LO signals of LO_0, LO_90, LO_180 and LO_270 provided to the sub-harmonic up-conversion circuits 200, 200B may have the same amplitude, and may have a phase difference of 90 degrees in sequence (i.e. 0, 90, 180, 270 degrees). The DC bias may be applied together with LO_0, LO_90, LO_180 and LO_270 for the transistor “gate” (or “base”) bias purpose. The sub-harmonic up-conversion circuit 200 and the second sub-harmonic up-conversion circuit 200B are connected to each other at their third terminal 106. The common node 106 connected with “drain” (or “collector”) electrodes of the transistor pairs in the circuits 200, 200B may output a 180 degree phase shifted RF signal (denoted by RF_180). The common node 106 may be coupled or connected to the DC bias 560 through the inductor L1 562. In various embodiments, the common node 106 may also be connected to inductors, resistors, LC tank, transmission lines or their combination for matching and/or bias purpose.

[0088] Similarly, LO signals of LO_0, LO_90, LO_180 and LO_270 provided to the sub-harmonic up-conversion circuits 200C, 200D may have the same amplitude, and may have a phase difference of 90 degrees in sequence (i.e. 0, 90, 180, 270 degrees). The DC bias may be applied together with LO_0, LO_90, LO_180 and LO_270 for the transistor “gate” (or “base”) bias purpose. The third sub-harmonic up-conversion circuit 200C and the fourth sub-harmonic up-conversion circuit 200D are connected to each other at their

third terminal 606. The common node 606 connected with “drain” (or “collector”) electrodes of the transistor pairs in the circuits 200C, 200D may output a 270 degree phase shifted RF signal (denoted by RF_270). The common node 606 may be coupled or connected to the DC bias 560 through the inductor L2 564. In various embodiments, the common node 606 may also be connected to inductors, resistors, LC tank, transmission lines or their combination for matching and/or bias purpose. The inductors L1 and L2 may have the same or different values or parameters.

[0089] In various embodiments, the harmonic frequency up-conversion circuit 600 may further include a 90 degree hybrid coupler 566, wherein the nodes 106, 606 for output RF_180 and RF_270 may be connected to the 90 degree hybrid coupler 566 through two capacitors C1 and C2, respectively. In this manner, the harmonic frequency up-conversion circuit 600 may be configured to generate upper side band (USB) mixed/modulated signal or low side band (LSB) mixed/modulated signal for conversion from in-phase and quadrature-phase IF signal/data. The IF signal or data input with different phases may be combined with the different LO phases for the frequency up-conversion operation with either LSB or USB. The operation performs the function with image rejection frequency conversion. In various embodiments, necessary biases and the matching network may be included as described above. In various embodiments, the DC block capacitor-or matching capacitor may be included into the circuit 600.

[0090] The harmonic frequency up-conversion circuit 600 according to the embodiments of Fig. 6A may be referred to or used as a differential IQ sub-harmonic frequency up-conversion SSB mixer/modulator with image rejection.

[0091] In various embodiments, more than four sub-harmonic frequency conversion circuits 200 may be connected in parallel. A power divider or a balun may be used to carry out frequency conversion with different phase combination of the IF/data and the LO signals for up-conversion, or with different phase combination of LO signal and RF signals for down-conversion.

[0092] In various embodiments, for different phase signal generation, both the passive network and transistor network may be used for the required signal generation. The passive network, such as transmission line, lumped coupler or poly phase filter, may be used. In various embodiments, active transistor network, such as active balun or phase shifter may be used. The differential or quadrature VCO (voltage-controlled oscillator) may be used to generate either differential or differential quadrature signals.

[0093] Fig. 6B shows a harmonic frequency down-conversion circuit 690 according to various embodiments, which may be configured to be used in a down-conversion mixer or demodulator with image rejection.

[0094] As shown in Fig. 6B, the harmonic frequency down-conversion circuit 690 is similar to the harmonic frequency up-conversion circuit 600 of Fig. 6A, with the difference that the circuit 690 includes the harmonic down-conversion circuit 290 of Fig. 2B and additional three harmonic down-conversion circuits 290B, 290C, 290D having the similar configuration as the harmonic down-conversion circuit 290. Various embodiments described with reference to Fig. 2B and Fig. 6A above are also valid for the harmonic frequency down-conversion circuit 690.

[0095] In each of the harmonic down-conversion circuits 290, 290B, 290C, 290D, the common node of “gate” (or “base”) of transistors Q1 and Q2 may be connected to the

common node of “source” (or “emitter”) of the transistor Q3 and Q4, as shown in Fig. 6B.

[0096] In various embodiments, the inverters of the harmonic down-conversion circuits 290, 290B, 290C, 290D may be configured to output differential “I” signal/data (e.g. differential “I” IF signal or data of 0 degree denoted by IF_0 or Data_0, and differential “I” IF signal or data of 180 degree denoted by IF_180 or Data_180), or output differential “Q” signal/data (e.g. differential “Q” IF signal or data of 90 degree denoted by IF_90 or Data_90, and differential “Q” IF signal or data of 270 degree denoted by IF_270 and Data_270). The resistors R1/R inside the inverters may be used to tradeoff between the gain and input/output matching. The “source” (or “emitter”) electrodes of the P-transistors inside of the inverters may be connected to Vdd (DC supply) directly or through lumped elements or transmission lines etc.

[0097] For harmonic conversion operation, LO signals of LO_0, LO_90, LO_180 and LO_270 may have the same amplitude and may have phase difference of 90 degrees in sequence (i.e. 0, 90, 180, 270 degrees), similar to the embodiments of Fig. 6A above. The DC can be applied together with LO_0, LO_90, LO_180 and LO_270 for the transistor “gate” (or “base”) bias purpose. The common node 106, 606 connected with “drain” (or “collector”) of the transistor pairs may be connected to inductors, resistors, LC tank, transmission lines or their combination for matching and/or bias purpose.

[0098] The harmonic frequency down-conversion circuit 690 according to the embodiments of Fig. 6B may be referred to or used as a differential IQ sub-harmonic frequency down-conversion SSB mixer/demodulator with image rejection.

[0099] Fig. 7 shows an exemplary layout 700 of an up-conversion sub-harmonic Differential IQ SSB modulator together with a Differential IQ network according to various embodiments, which may be used in a transceiver.

[00100] As shown in Fig. 7, a passive Differential IQ network 710 (also referred to as a DQ network) is provided to convert the input differential LO signal (LO_0, LO_180) into differential quadrature output LO signals (LO_0, LO_180, LO_90 and LO_270) with phases of 0, 180, 90 and 270 degrees. The output LO signals may be supplied to the sub-harmonic differential IQ modulator 600 (also referred to as sub-harmonic DQ modulator). The sub-harmonic differential IQ modulator may be the harmonic frequency up-conversion circuit 600 described in Fig. 6A above, including four sub-harmonic frequency conversion cells 200 of Fig. 2A, and including two spiral inductors below the 90 degree hybrid coupler for DC bias purpose as well as for RF signal blocking to avoid the RF leakage to DC. The DC supply circuits may be used, but are not described in detail. The 90 degree hybrid coupler is integrated with the core modulator 600 as in Fig. 6A. The GSSGSSG pads 720 are used for probe touching for differential quadrature IF/data inputs. The GSSG pads 730 at the bottom is to feed in differential LO signals LO_0 and LO_180. The GSGSG Pads 740 on the top are used to obtain either LSB signal or USB signal. The harmonic frequency conversion circuits of various embodiments may be capable of suppressing the sub-harmonic leakage and image signal to provide good linearity and spectrum purity for the modulator as well as for the transmitter.

[00101] Fig. 8 shows a transceiver 800 including a sub-harmonic Differential IQ modulator/ demodulator according to various embodiments.

[00102] As an exemplary embodiment for the harmonic modulator/demodulator application in the transceiver front end, Fig. 8 shows the application of the sub-harmonic Differential IQ modulator/demodulator (also referred to as sub-harmonic DQ modulator/demodulator) in the transceiver 800. The use of the sub-harmonic Differential IQ modulator 810 (e.g. IQ modulator 500, 600 of Figs. 5A and 6A) and the sub-harmonic Differential IQ demodulator 820 (e.g. IQ demodulator 590, 690 of Figs. 5B and 6B) of various embodiments above may dramatically simplify the transceiver architecture by reducing the components and LO chain, and thus reducing the chip area and the total power consumption. The required LO frequency may be reduced to half of that of the normal fundamental modulator.

[00103] As shown in Fig. 8, a synthesizer 830 for LO drive may be shared by both the transmitter side and the receiver side. The Differential IQ networks 832, 834 (also referred to as DQ networks) may be used to convert the differential LO signals (LO_0 and LO_180) from the synthesizer 830 to differential quadrature LO signals (LO_0, LO_90, LO_180, LO_270), as shown in Fig. 8. In various embodiments, the Differential IQ networks 832, 834 may be integrated with the IQ modulator/demodulator, similar to the embodiment of Fig. 7. When USB is needed for the transceiver system, the LSB may be connected to 50ohm load. At the transmitter side, the USB may be connected to a power amplifier 840. At the receiver side, the USB may be connected to a low-noise amplifier 850.

[00104] Fig. 9 shows a differential IQ sub-harmonic up-conversion DSB (double sideband) mixer/modulator 900 according to various embodiments.

[00105] In Fig. 9, the differential IQ sub-harmonic frequency conversion circuit of various embodiments may be used in a modulator or mixer with double side band. The differential IQ sub-harmonic up-conversion DSB mixer/modulator 900 is similar to the circuit 600 of Fig. 6A, with the difference that the 90 degree hybrid 566 is replaced by a power combiner/divider 966 to collect both USB and LSB as the DSB. The power combiner/divider 966 may also be replaced by a transformer for power combination.

[00106] In various embodiments, the 90 degree hybrid coupler 566 in the circuits 500, 590, 690 of Figs. 5A, 5B, 6B may also be replaced by a power combiner/divider, to form the corresponding circuits for DSB modulator/demodulator.

[00107] Fig. 10 shows an IQ fourth-harmonic down-conversion SSB mixer/demodulator 1000 according to various embodiments.

[00108] In Fig. 10, the mixer/demodulator 1000 may include a fourth-harmonic frequency down-conversion circuit 390 described in Fig. 3B above for converting RF signal into in-phase IF signal (IF_I) or IF data (Data_I). The mixer/demodulator 1000 may include a further fourth-harmonic frequency down-conversion circuit 390B similar to the circuit 390, for converting RF signal into quadrature-phase IF signal (IF_Q) or IF data (Data_Q). In this manner, I and Q signals may be generated from the RF signals received at the node 106 and 1006. The mixer/demodulator 1000 may include a 90 degree hybrid 566 to input either USB or LSB for the SSB operation.

[00109] Similar to the configuration of Fig. 10, the up-conversion fourth-harmonic frequency up-conversion circuit 300 of Fig. 3A may be used to form the IQ fourth-harmonic frequency up-conversion modulator/mixer.

[00110] Compared to the double sideband (DSB) modulator/demodulator, the single sideband (SSB) modulator/demodulator may be useful in the modulation applications wherein the desired and undesired RF sidebands are too close in frequency to be separated using a simple band pass filter or where minimum group delay is required.

[00111] While the invention has been particularly shown and described with reference to specific embodiments, it should be understood by those skilled in the art that various changes in form and detail may be made therein without departing from the spirit and scope of the invention as defined by the appended claims. The scope of the invention is thus indicated by the appended claims and all changes which come within the meaning and range of equivalency of the claims are therefore intended to be embraced.

Claims

What is claimed is:

1. A harmonic frequency conversion circuit, comprising:
 - an inverter having a first terminal and a second terminal, said inverter comprising:
 - at least one of a resistor or a capacitor connected between the first terminal and the second terminal;
 - a P-channel transistor having a first electrode, a second electrode and a third electrode;
 - a N-channel transistor having a first electrode, a second electrode and a third electrode;wherein the first electrode of the P-channel transistor and the first electrode of the N-channel transistor are connected to the first terminal, and the second electrode of the P-channel transistor and the second electrode of the N-channel transistor are connected to the second terminal; and
 - a transistor pair connected to the inverter and comprising a first transistor and a second transistor; the first transistor having a first electrode, a second electrode and a third electrode; and the second transistor having a first electrode, a second electrode and a third electrode,
 - wherein the first electrode of the first transistor is connected to receive a first local oscillation signal and the first electrode of the second transistor is connected to receive a second local oscillation signal;

wherein the second electrode of the first transistor and the second electrode of the second transistor are connected to each other at a third terminal;

wherein the third electrode of the first transistor and the third electrode of the second transistor are connected to one of the first terminal or the second terminal of the inverter.

2. The harmonic frequency conversion circuit of claim 1, wherein
the first electrode of the P-channel transistor and the first electrode of the N-channel transistor are one of gate electrode or base electrode,
the second electrode of the P-channel transistor and the second electrode of the N-channel transistor are one of drain electrode or collector electrode,
the third electrode of the P-channel transistor and the third electrode of the N-channel transistor are one of source electrode or emitter electrode.
3. The harmonic frequency conversion circuit of claim 1 or 2, wherein
the third electrode of the P-channel transistor is connected to a DC supply, and the third electrode of the N-channel transistor is connected to the ground.
4. The harmonic frequency conversion circuit of any one of claims 1 to 3, wherein
the first electrode of the first transistor and the first electrode of the second transistor are one of gate electrode or base electrode,
the second electrode of the first transistor and the second electrode of the second transistor are one of drain electrode or collector electrode, and

the third electrode of the first transistor and the third electrode of the second transistor are one of source electrode or emitter electrode.

5. The harmonic frequency conversion circuit of any one of claims 1 to 4, further comprising a DC bias connected to the third terminal.
6. The harmonic frequency conversion circuit of any one of claims 1 to 5, further comprising at least one of a resistor, an inductor, a LC tank or transmission lines connected to the third terminal.
7. The harmonic frequency conversion circuit of any one of claims 1 to 6, wherein the first local oscillation signal and the second local oscillation signal have a 180-degree phase difference.
8. The harmonic frequency conversion circuit of any one of claims 1 to 7, wherein the third electrode of the first transistor and the third electrode of the second transistor are connected to the second terminal of the inverter.
9. The harmonic frequency conversion circuit of claim 8, configured to receive an intermediate frequency signal at the first terminal of the inverter, and configured to output a radio frequency signal from the third terminal.

10. The harmonic frequency conversion circuit of claim 9,
wherein the inverter and the transistor pair form a first sub-harmonic frequency up-conversion cell,
wherein the harmonic frequency conversion circuit further comprises a further inverter and a further transistor pair forming a second sub-harmonic frequency up-conversion cell,
wherein the first cell is configured to receive a 0 degree phase shifted intermediate frequency signal at the first terminal thereof, and the second cell is configured to receive a 90 degree phase shifted intermediate frequency signal at the first terminal thereof.
11. The harmonic frequency conversion circuit of claim 9,
wherein the inverter and the transistor pair form a first sub-harmonic frequency up-conversion cell,
wherein the harmonic frequency conversion circuit further comprises a second sub-harmonic frequency up-conversion cell, a third sub-harmonic frequency up-conversion cell, and a fourth sub-harmonic frequency up-conversion cell, each of the second cell, the third cell and the fourth cell comprising an inverter and a transistor pair,
wherein the first cell and the second cell are connected to each other at their third terminals, and the third cell and the fourth cell are connected to each at their third terminals,

wherein the first cell is configured to receive a 0 degree phase shifted intermediate frequency signal at the first terminal thereof, the second cell is configured to receive a 180 degree phase shifted intermediate frequency signal at the first terminal thereof, the third cell is configured to receive a 270 degree phase shifted intermediate frequency signal at the first terminal thereof, and the fourth cell is configured to receive a 90 degree phase shifted intermediate frequency signal at the first terminal thereof.

12. The harmonic frequency conversion circuit of any one of claims 1 to 7, wherein the third electrode of the first transistor and the third electrode of the second transistor are connected to the first terminal of the inverter.
13. The harmonic frequency conversion circuit of claim 12, configured to receive a radio frequency signal at the third terminal, and configured to output an intermediate frequency signal from the second terminal of the inverter.
14. The harmonic frequency conversion circuit of claim 13, wherein the inverter and the transistor pair form a first sub-harmonic frequency down-conversion cell, wherein the harmonic frequency conversion circuit further comprises a further inverter and a further transistor pair forming a second sub-harmonic frequency down-conversion cell,

wherein the first cell is configured to receive a 0 degree phase shifted radio frequency signal at the third terminal thereof, and the second cell is configured to receive a 90 degree phase shifted radio frequency signal at the third terminal thereof.

15. The harmonic frequency conversion circuit of claim 13,
- wherein the inverter and the transistor pair form a first sub-harmonic frequency down-conversion cell,
- wherein the harmonic frequency conversion circuit further comprises a second sub-harmonic frequency down-conversion cell, a third sub-harmonic frequency down-conversion cell, and a fourth sub-harmonic frequency down-conversion cell, each of the second cell, the third cell and the fourth cell comprising an inverter and a transistor pair,
- wherein the first cell and the second cell are connected to each other at their third terminals, and the third cell and the fourth cell are connected to each at their third terminals,
- wherein the first cell and the second cell are configured to receive a 180 degree phase shifted radio frequency signal at their third terminals, and the third cell and the fourth cell are configured to receive a 270 degree phase shifted radio frequency signal at their third terminals.

16. The harmonic frequency conversion circuit of any one of claims 1 to 15, comprising a further transistor pair connected to the inverter, wherein the transistor pair and the further transistor pair are connected in parallel.
17. The harmonic frequency conversion circuit of claim 16, wherein the first local oscillation signal received by the transistor pair and the first local oscillation signal received by the further transistor pair have a 90-degree phase difference, and the second local oscillation signal received by the transistor pair and the second local oscillation signal received by the further transistor pair have a 90-degree phase difference.
18. The harmonic frequency conversion circuit of any one of claims 1 to 15, further comprising a second transistor pair, a third transistor pair and a fourth transistor pair, wherein the transistor pair, the second transistor pair, the third transistor pair and the fourth transistor pair are connected with each other in parallel and are connected to the inverter.
19. The harmonic frequency conversion circuit of claim 18, wherein the first local oscillation signals received by the transistor pair, the second transistor pair, the third transistor pair and the fourth transistor pair have a 45-degree phase difference in sequence, and

the second local oscillation signals received by the transistor pair, the second transistor pair, the third transistor pair and the fourth transistor pair have a 45-degree phase difference in sequence.

20. The harmonic frequency conversion circuit of any one of claims 1 to 19, configured to be used in at least one of a modulator, a demodulator or a mixer.

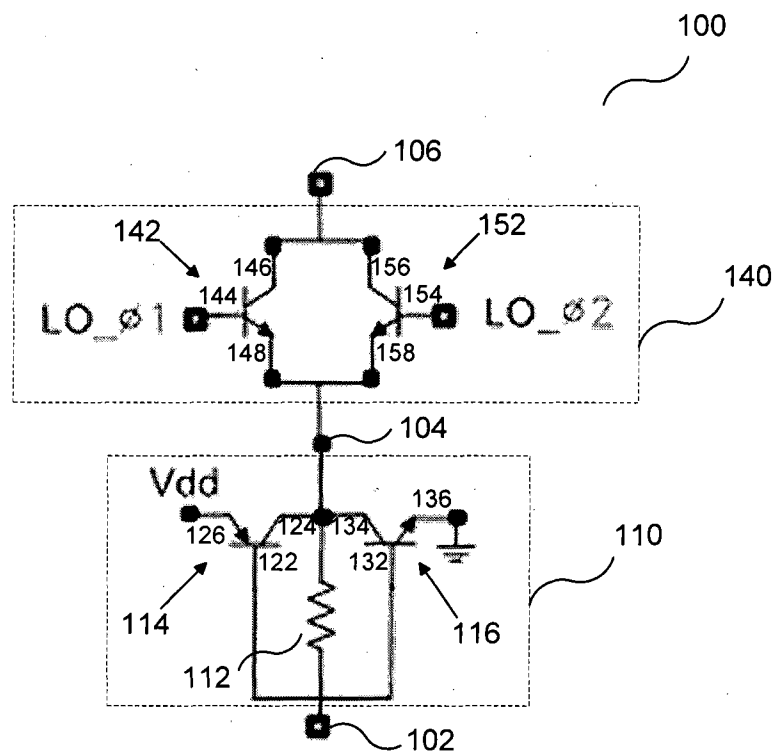


Fig. 1

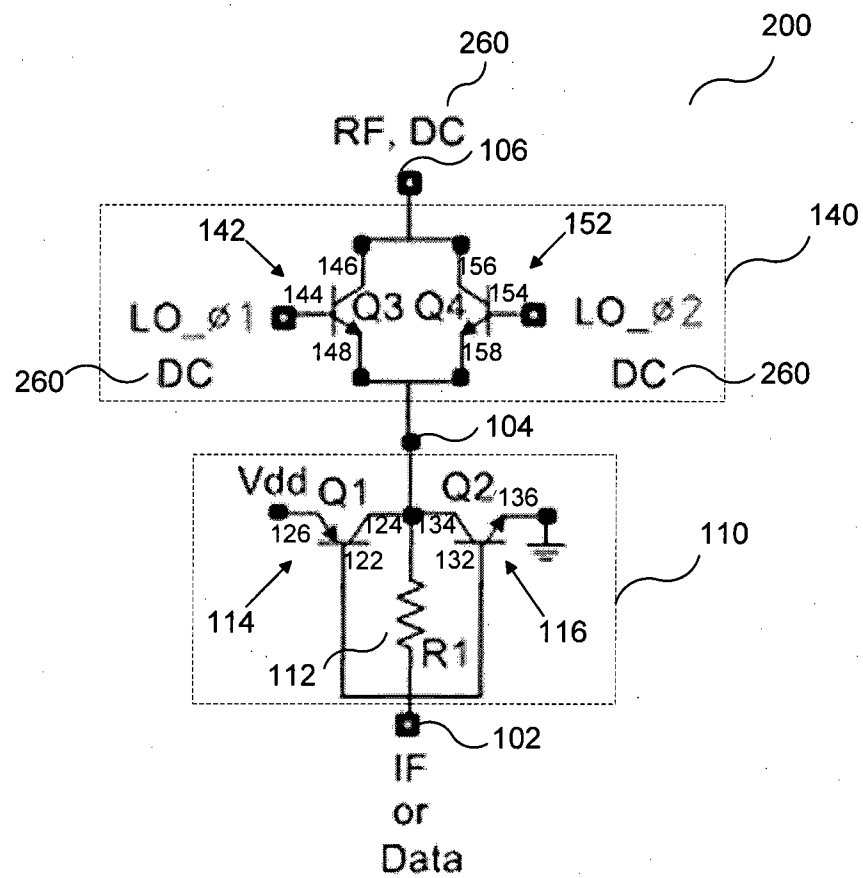


Fig. 2A

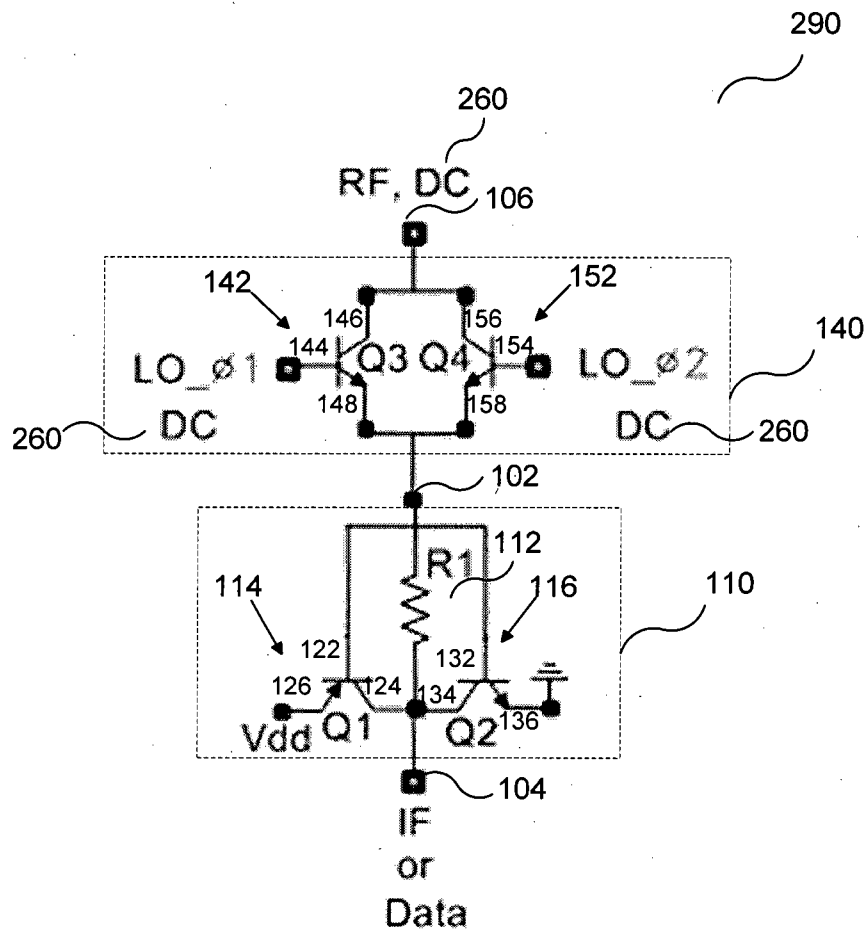


Fig. 2B

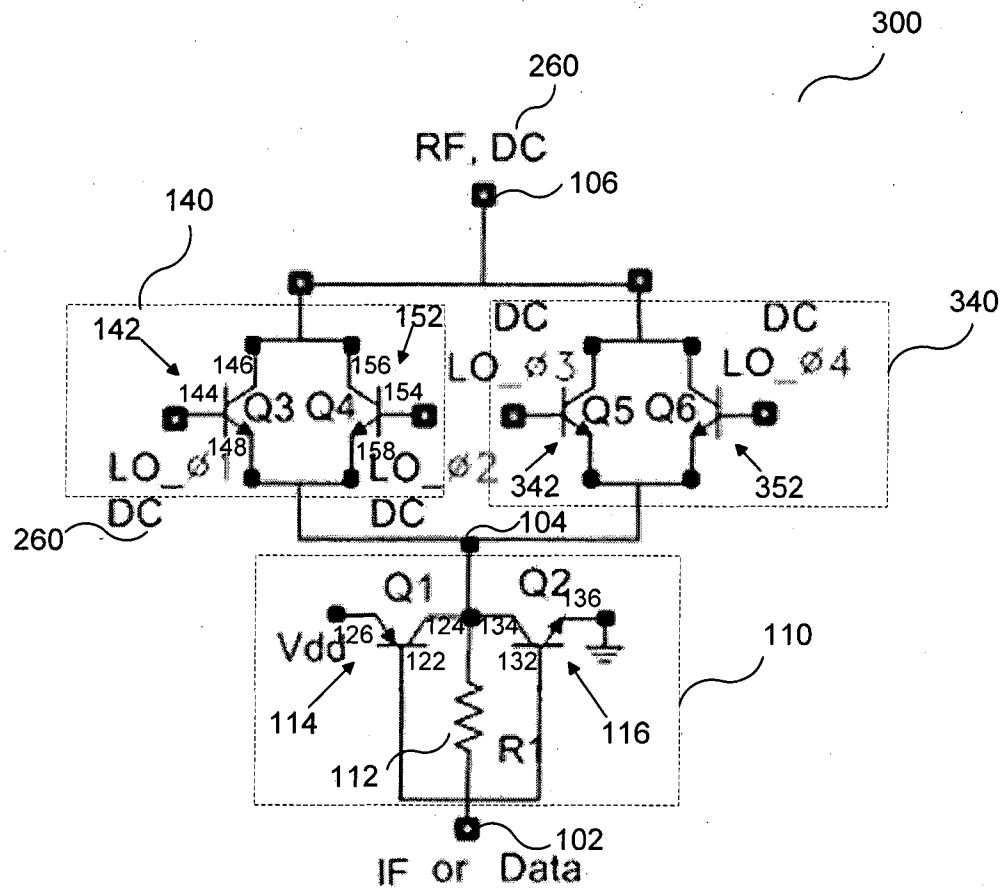


Fig. 3A

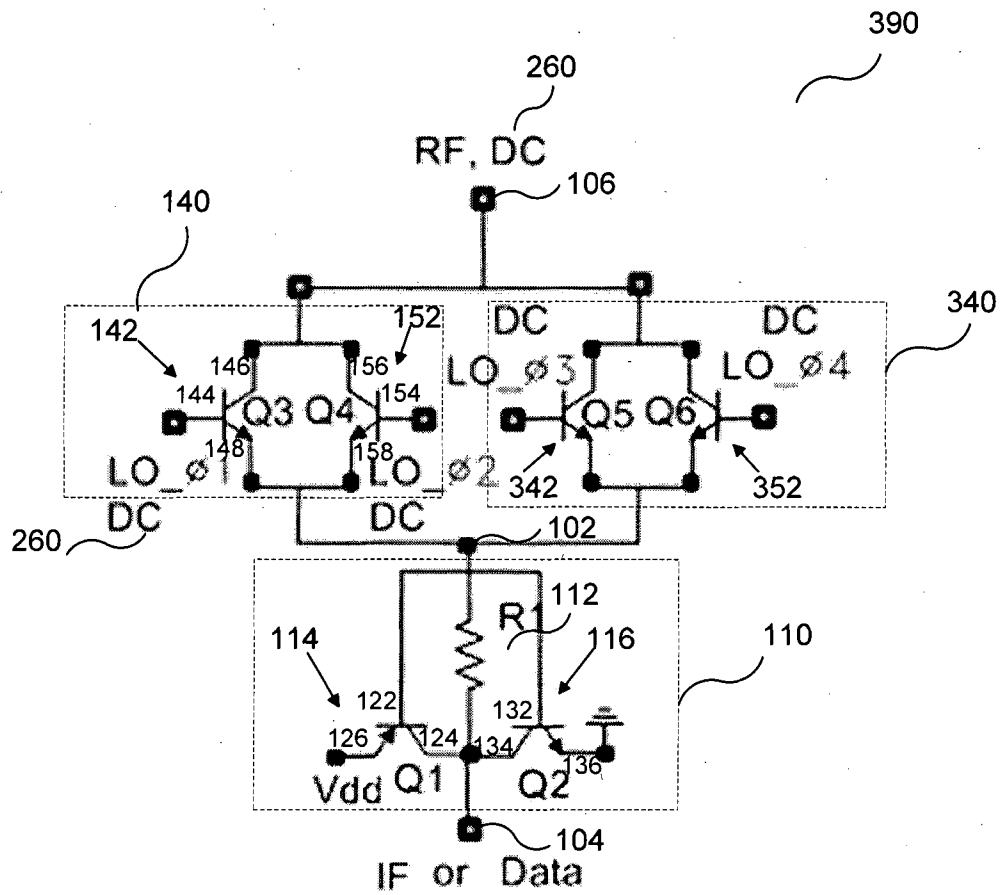


Fig. 3B

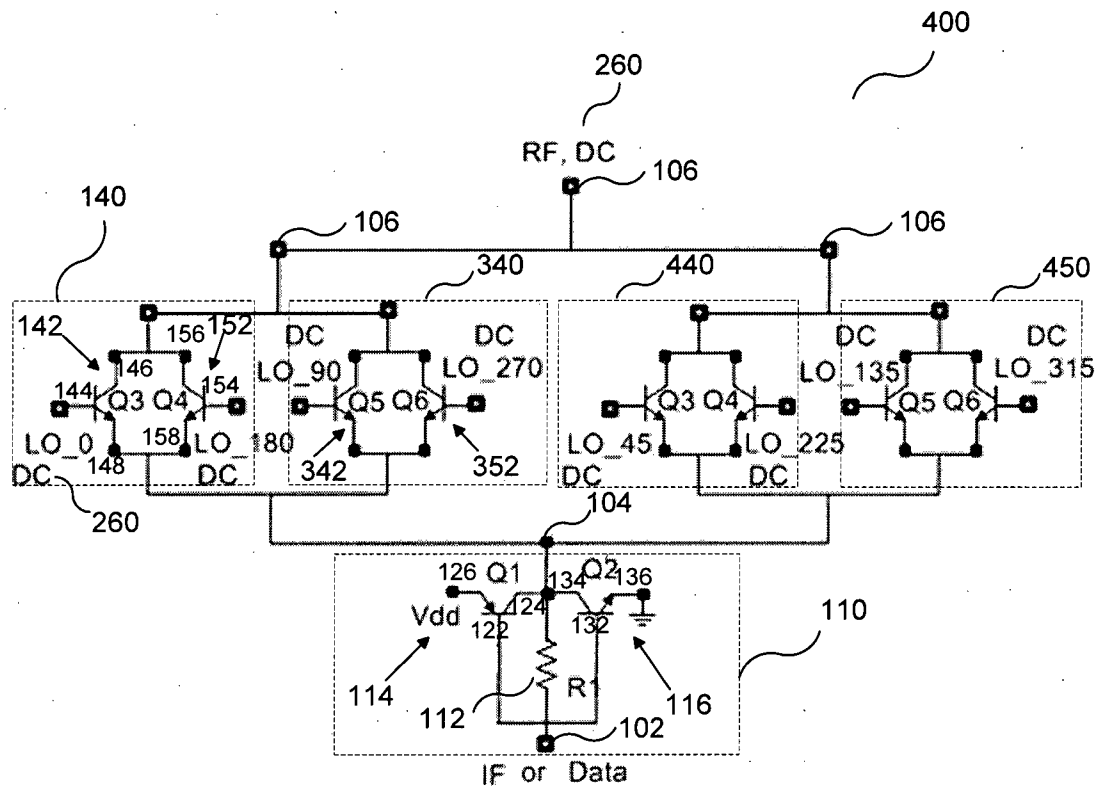


Fig. 4A

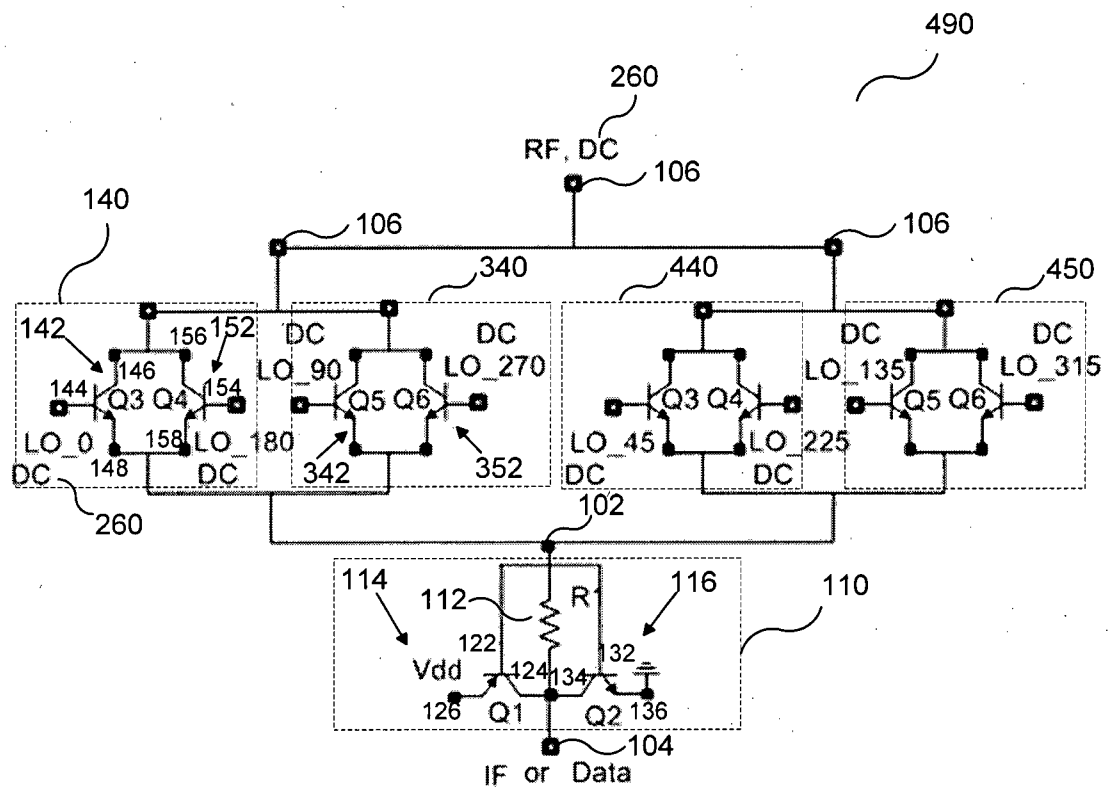


Fig. 4B

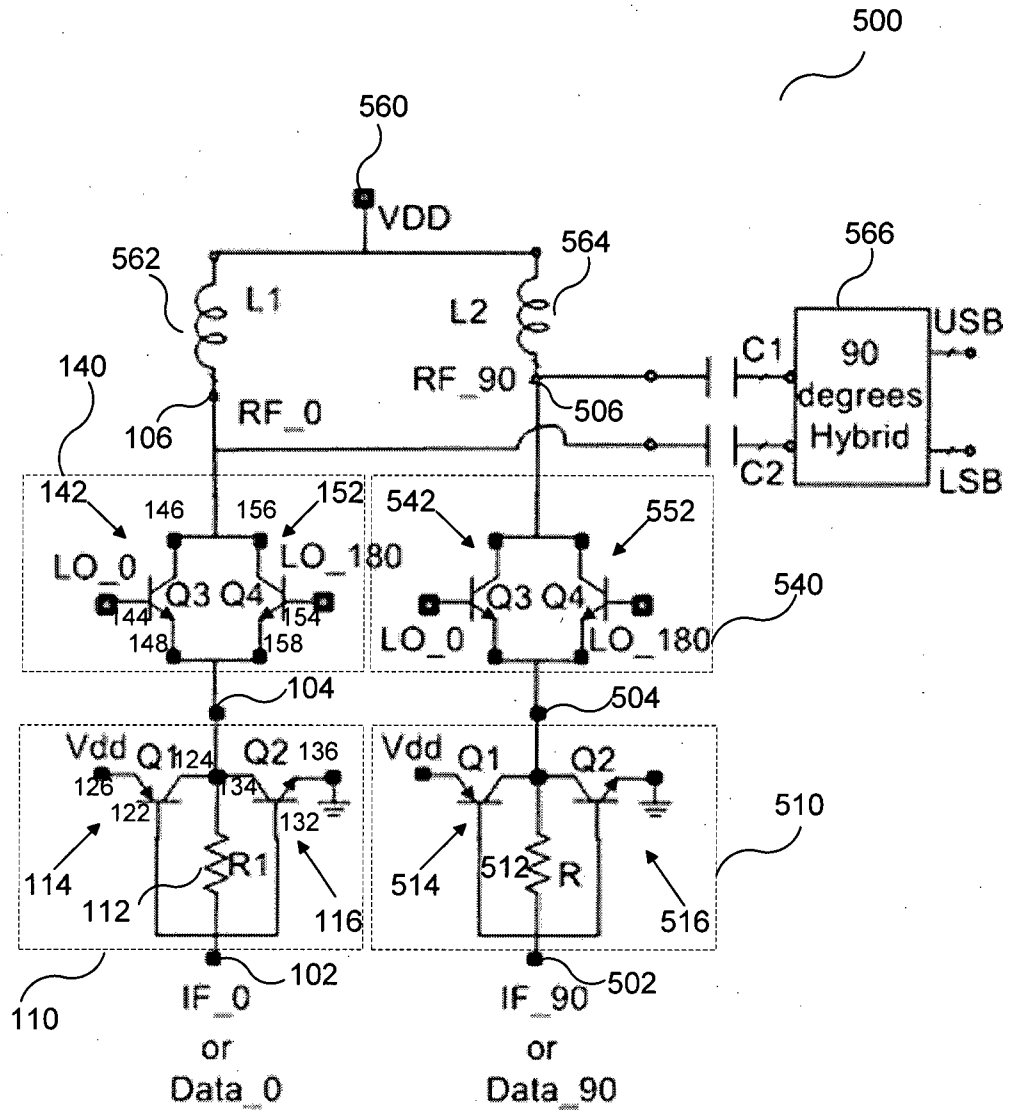


Fig. 5A

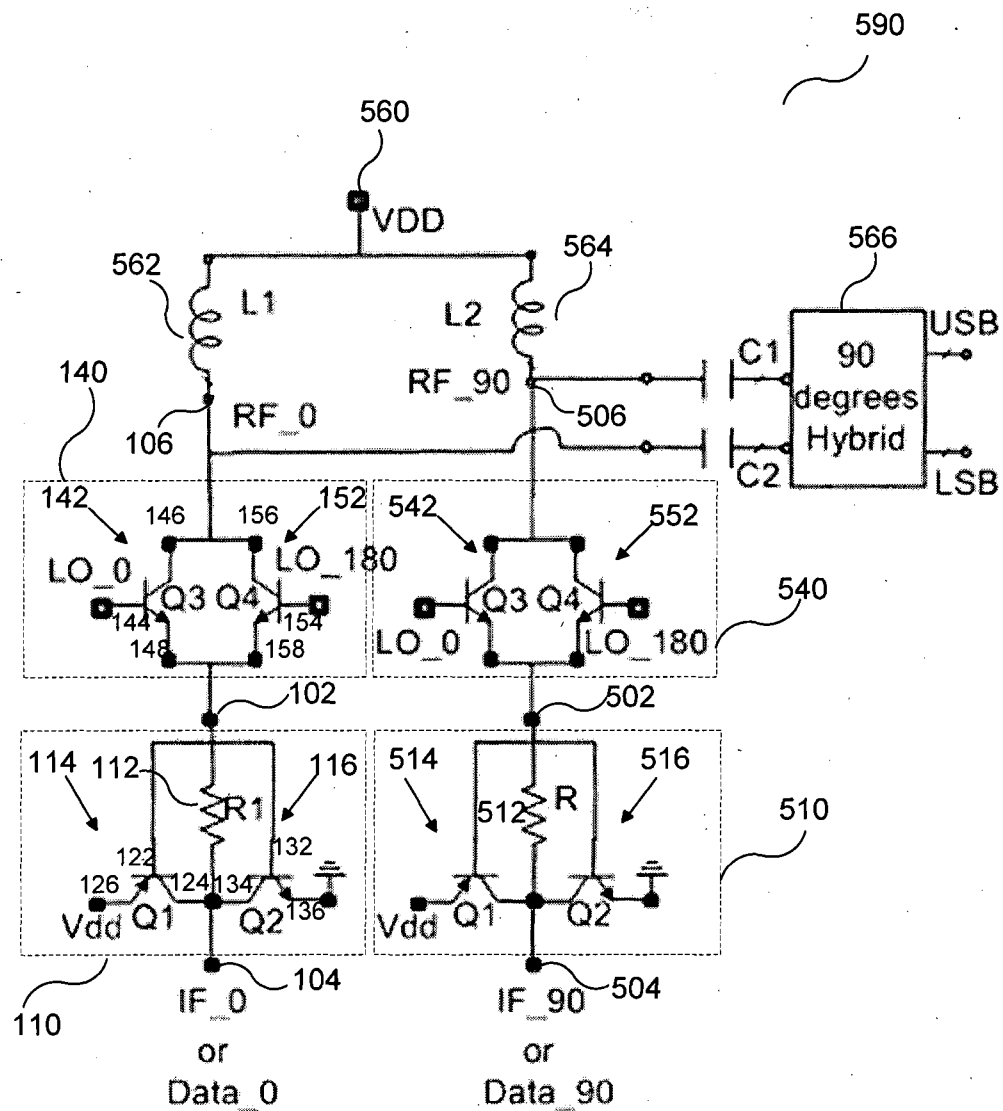


Fig. 5B

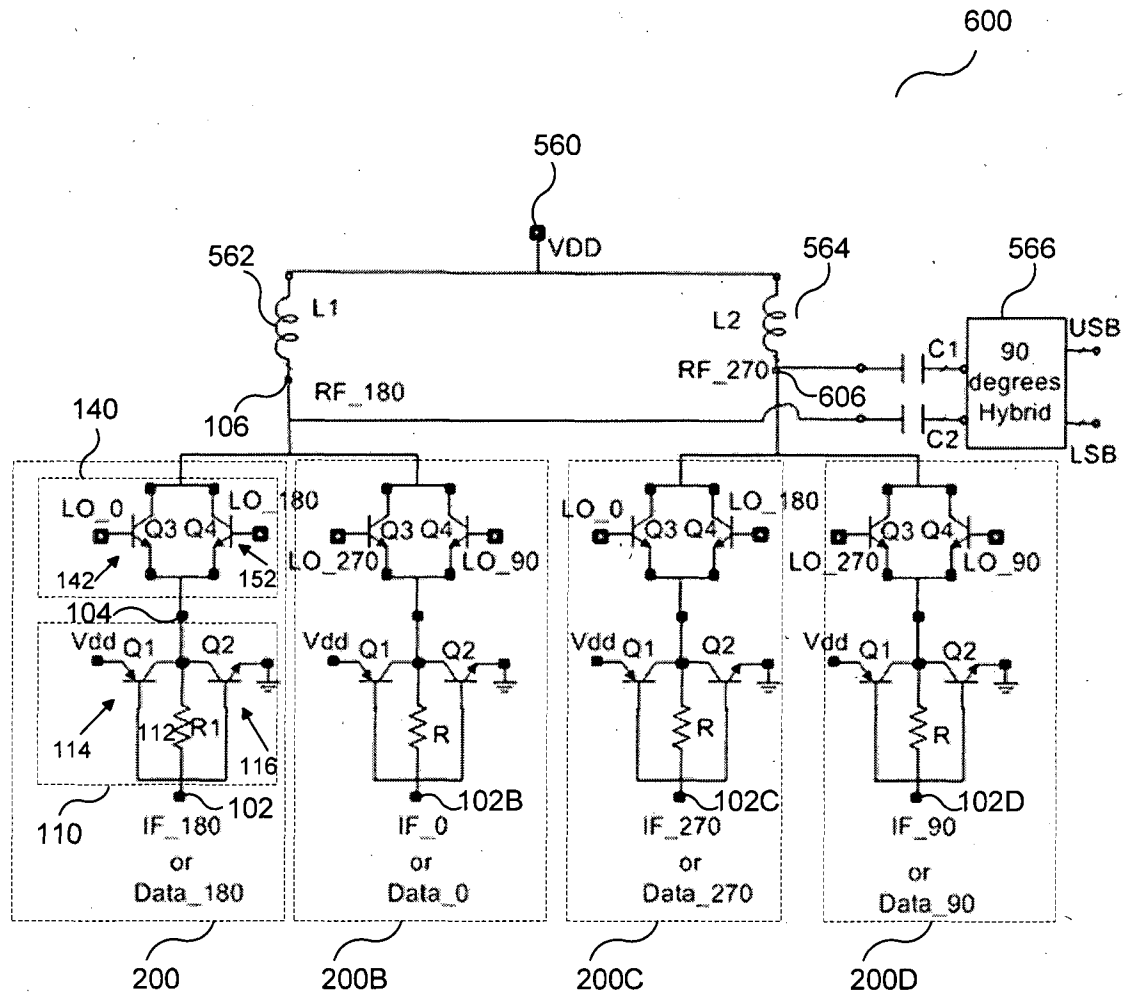


Fig. 6A

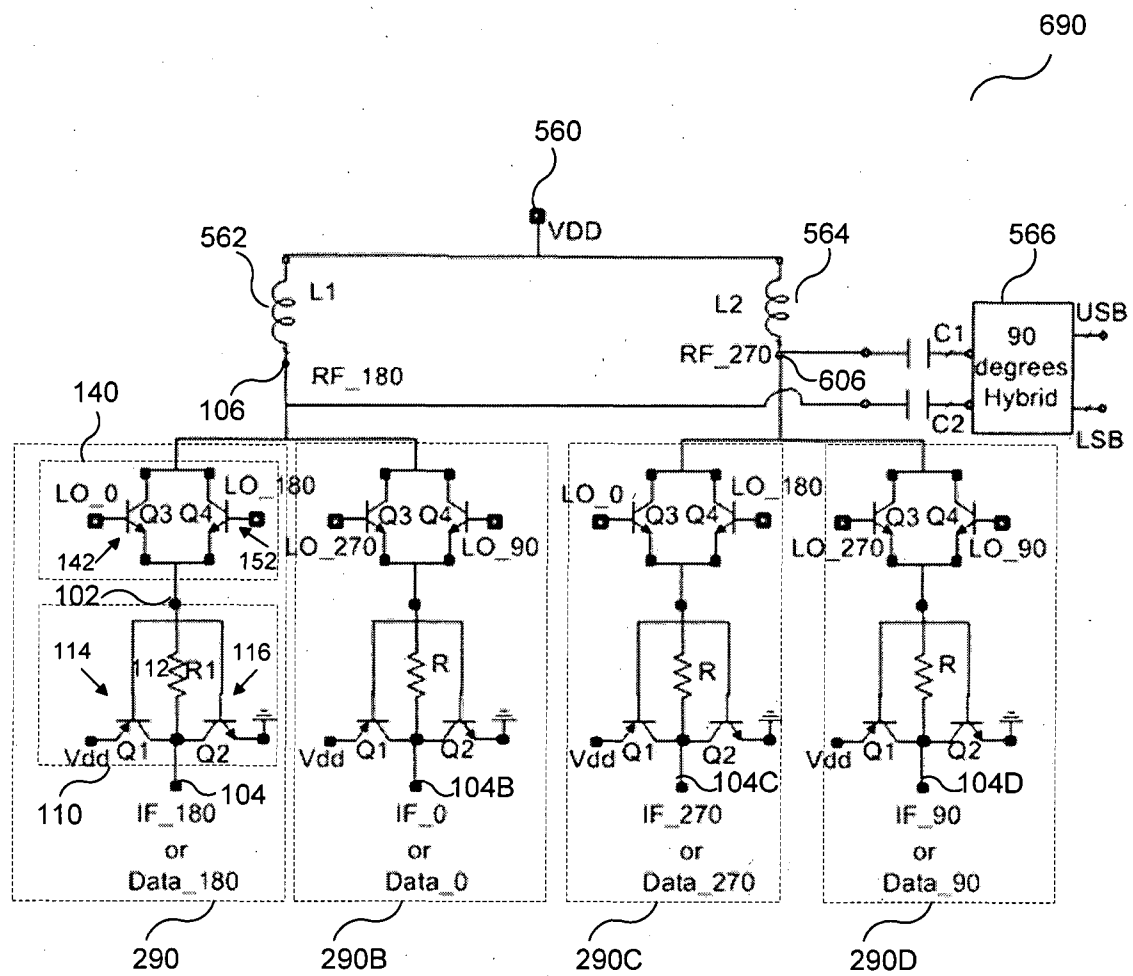


Fig. 6B

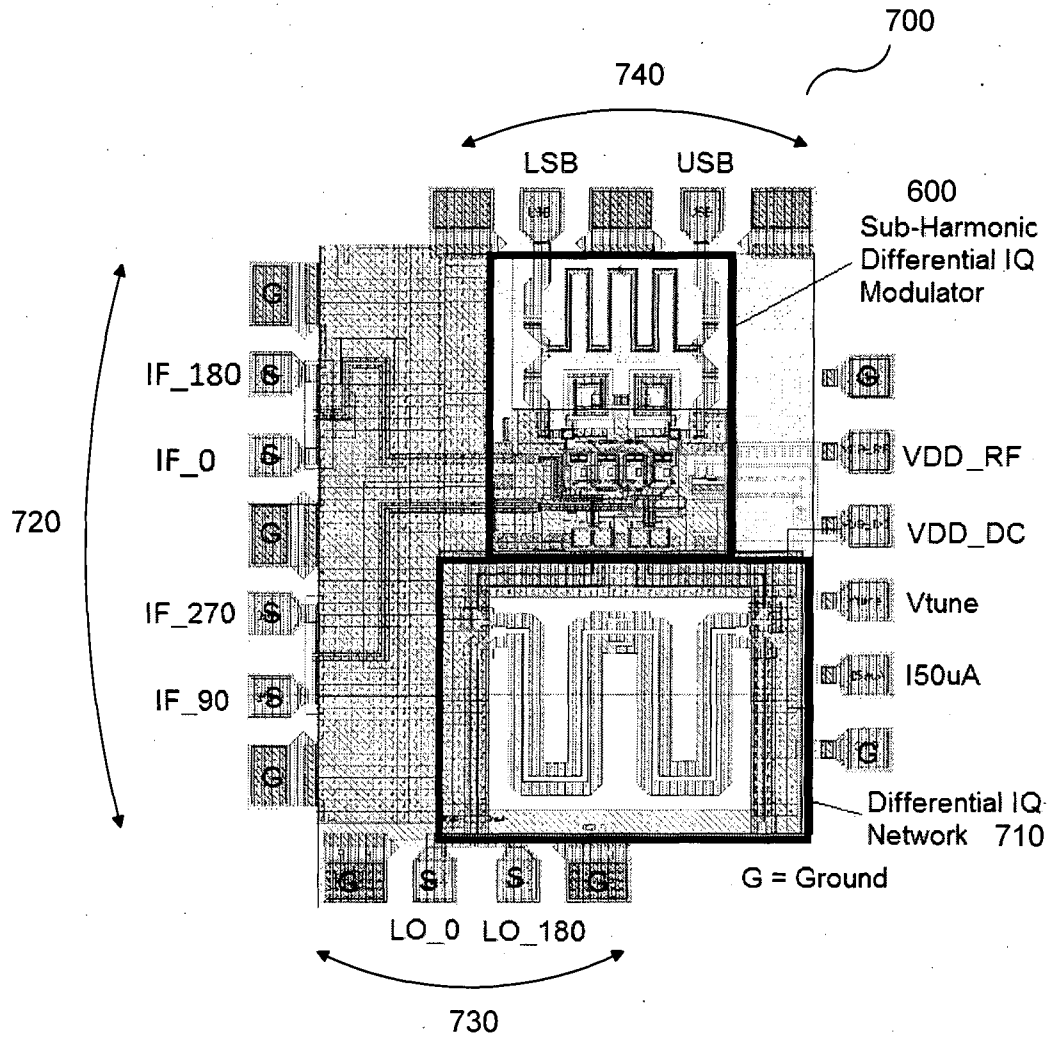


Fig. 7

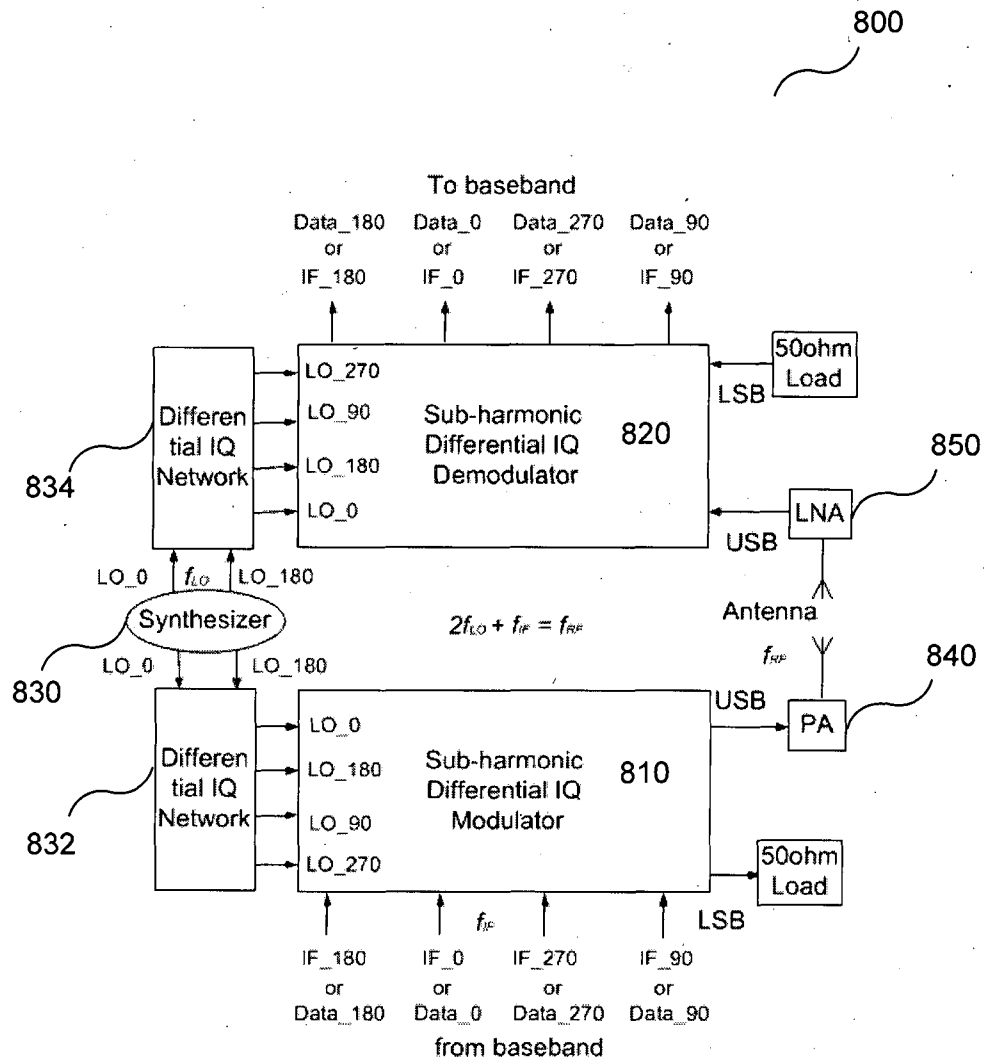


Fig. 8

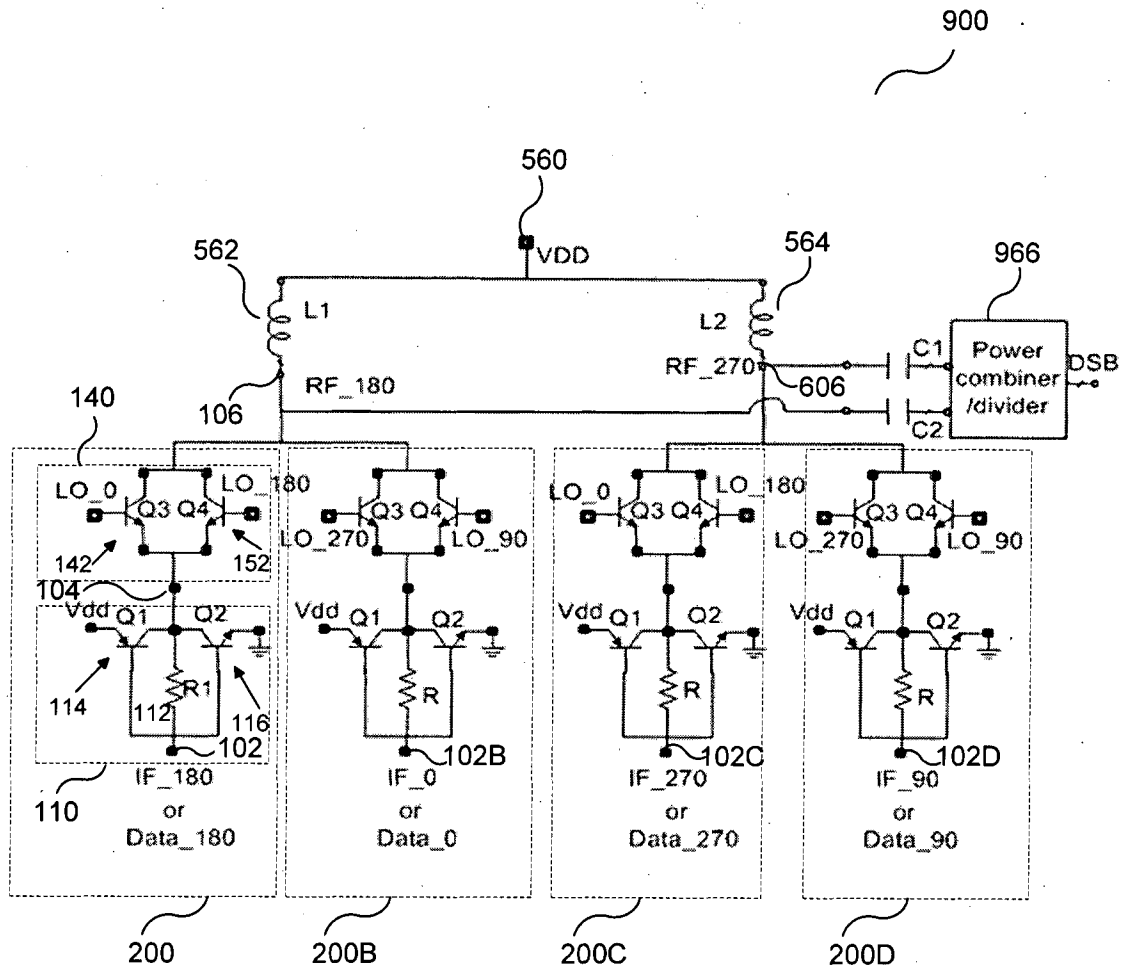


Fig. 9

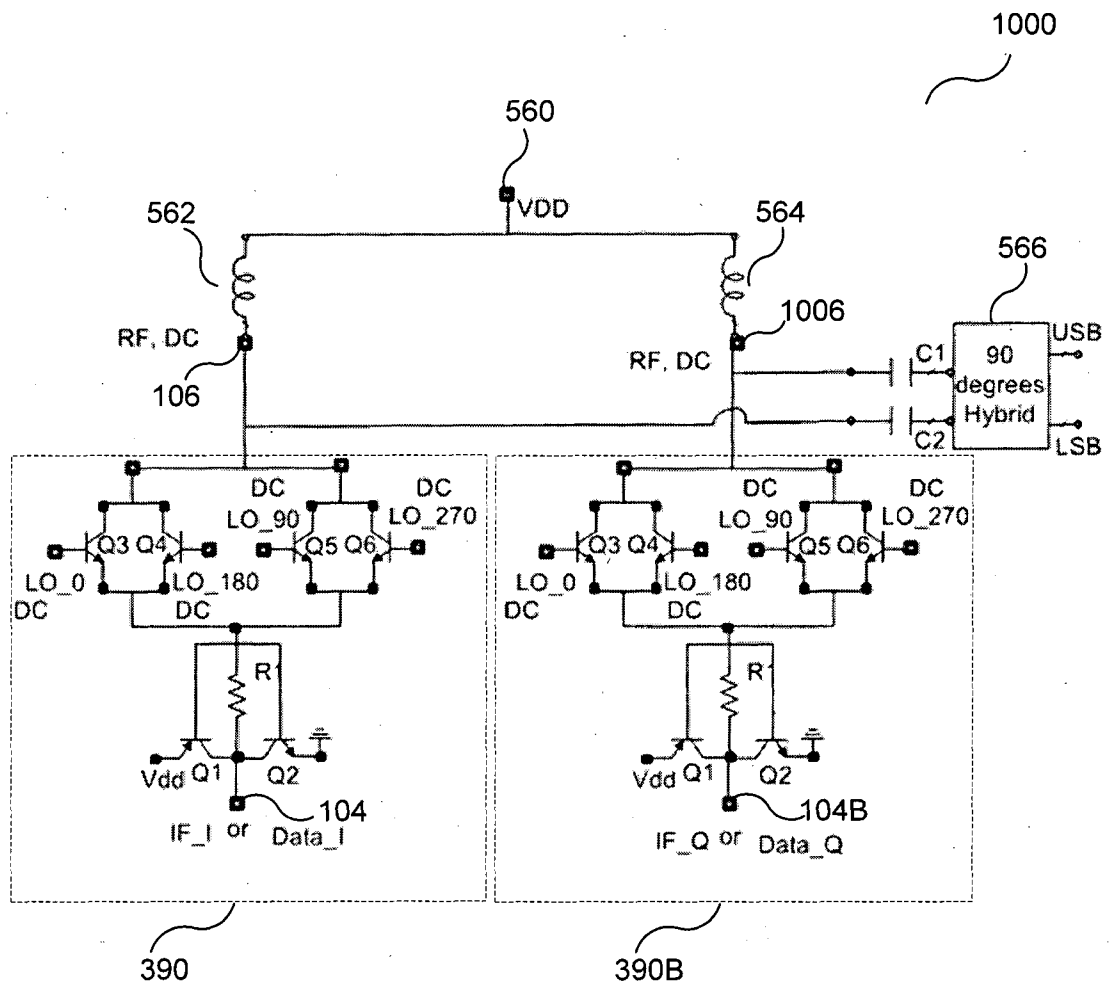


Fig. 10

INTERNATIONAL SEARCH REPORT

 International application No.
PCT/SG2013/000373

A. CLASSIFICATION OF SUBJECT MATTER

H03D 7/12 (2006.01) H04B 1/40 (2006.01)

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPODOC and WPI with IPC/CC H03D7/00, H04B1/00 and keywords frequency converter, heterodyne, transistor, inverter circuit, local oscillator, intermediate frequency, radio frequency

GOOGLE PATENTS and ESPACENET with the following keywords – frequency converter, heterodyne, inverter, mixer, local oscillation, radio frequency, intermediate frequency, circuit

PATENT LENS with the following keywords - MA, Kai Xue ; HOU, Shou Xian; YEO, Kiat Seng; NANYANG TECHNOLOGICAL UNIVERSITY

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
	Documents are listed in the continuation of Box C	



Further documents are listed in the continuation of Box C



See patent family annex

* "A"	Special categories of cited documents: document defining the general state of the art which is not considered to be of particular relevance	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"E"	earlier application or patent but published on or after the international filing date	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"O"	document referring to an oral disclosure, use, exhibition or other means	"&"	document member of the same patent family
"P"	document published prior to the international filing date but later than the priority date claimed		
Date of the actual completion of the international search 16 October 2013		Date of mailing of the international search report 16 October 2013	
Name and mailing address of the ISA/AU AUSTRALIAN PATENT OFFICE PO BOX 200, WODEN ACT 2606, AUSTRALIA Email address: pct@ipaustalia.gov.au Facsimile No.: +61 2 6283 7999		Authorised officer Vinod Menon AUSTRALIAN PATENT OFFICE (ISO 9001 Quality Certified Service) Telephone No. 0262832763	

INTERNATIONAL SEARCH REPORT C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		International application No. PCT/SG2013/000373
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2010/0029239 A1 (ASURI) 04 February 2010 Abstract; paragraphs [0004], [0020], [0025], [0028], [0035]-[0040], [0071]; fig 1, fig 2, fig 4, fig 5, fig 7, fig 8	1-20
Form PCT/ISA/210 (fifth sheet) (July 2009)		

INTERNATIONAL SEARCH REPORT Information on patent family members		International application No. PCT/SG2013/000373	
This Annex lists known patent family members relating to the patent documents cited in the above-mentioned international search report. The Australian Patent Office is in no way liable for these particulars which are merely given for the purpose of information.			
Patent Document/s Cited in Search Report		Patent Family Member/s	
Publication Number	Publication Date	Publication Number	Publication Date
US 2010/0029239 A1	04 Feb 2010	EP 2316162 A2	04 May 2011
		EP 2316162 B1	10 Apr 2013
		EP 2541758 A1	02 Jan 2013
		JP 2011530244 A	15 Dec 2011
		KR 20110051215 A	17 May 2011
		TW 201012049 A	16 Mar 2010
		US 2010029239 A1	04 Feb 2010
		US 8095103 B2	10 Jan 2012
		WO 2010014989 A2	04 Feb 2010
End of Annex			

Due to data integration issues this family listing may not include 10 digit Australian applications filed since May 2001.

Form PCT/ISA/210 (Family Annex)(July 2009)