(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
21 February 2019 (21.02.2019)

WIPO | PCT

(10) International Publication Number
WO 2019/036252 A1

(51) International Patent Classification:
H01L 21/02 (2006.01) *H01L 21/28* (2006.01)
H01L 21/324 (2006.01)

(21) International Application Number:
PCT/US2018/045771

(22) International Filing Date:
08 August 2018 (08.08.2018)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:

62/547,360	18 August 2017 (18.08.2017)	US
62/593,530	01 December 2017 (01.12.2017)	US
16/052,963	02 August 2018 (02.08.2018)	US

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

(54) Title: METHODS FOR IMPROVING PERFORMANCE IN HAFNIUM OXIDE-BASED FERROELECTRIC MATERIAL USING PLASMA AND/OR THERMAL TREATMENT

(57) Abstract: A method of forming ferroelectric hafnium oxide (HfO_2) in a substrate processing system includes arranging a substrate within a processing chamber of the substrate processing system, depositing an HfO_2 layer on the substrate, performing a plasma treatment of the HfO_2 layer, and annealing the HfO_2 layer to form ferroelectric hafnium HfO_2.

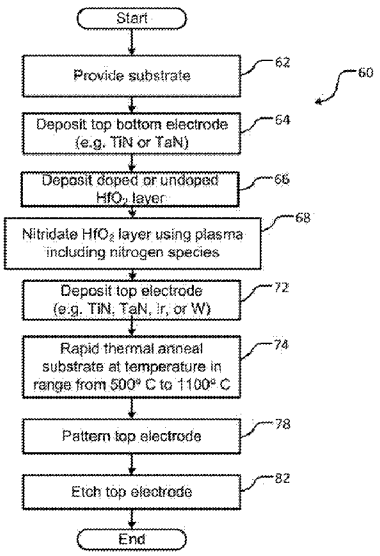

FIG. 2

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[Continued on next page]

Declarations under Rule 4.17:

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

Published:

— *with international search report (Art. 21(3))*

METHODS FOR IMPROVING PERFORMANCE IN HAFNIUM OXIDE-BASED FERROELECTRIC MATERIAL USING PLASMA AND/OR THERMAL TREATMENT

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims priority to U.S. Utility Application No. 16/052,963, filed August 2, 2018 and also claims the benefit of U.S. Provisional Application No. 62/593,530, filed on December 1, 2017, and U.S. Provisional Application No. 62/547,360, filed on August 18, 2017. The entire disclosures of the applications referenced above are incorporated herein by reference.

FIELD

[0002] The present disclosure relates to methods for processing substrates, and more particularly to methods for improving performance in devices including hafnium oxide-based ferroelectric material using plasma and/or thermal treatment.

BACKGROUND

[0003] The background description provided here is for the purpose of generally presenting the context of the disclosure. Work of the presently named inventors, to the extent it is described in this background section, as well as aspects of the description that may not otherwise qualify as prior art at the time of filing, are neither expressly nor impliedly admitted as prior art against the present disclosure.

[0004] The discovery of ferroelectric behavior in hafnium oxide (HfO_2)-based materials rejuvenated research into ferroelectric memory (FeRAM). Conventional ferroelectric materials such as lead zirconate titanate (PZT) do not have an adequate switching window for thicknesses below 50 nanometers (nm). Therefore PZT cannot be used for devices having features sizes that are less than 50 nm (e.g., a film thinner than 50 nm).

[0005] HfO_2 has excellent ferroelectric switching hysteresis down to thicknesses of 5 nm due to a high coercive field. HfO_2 is also a good candidate for 3D memory structures. HfO_2 has been widely used in CMOS technology as a gate dielectric. In these applications, HfO_2 is deposited using conformal atomic layer deposition (ALD). Therefore, HfO_2 may be suitable for integration into 3D FeRAM using the current 3D NAND integration schemes.

SUMMARY

[0006] A method of forming ferroelectric hafnium oxide (HfO_2) in a substrate processing system includes arranging a substrate within a processing chamber of the substrate

processing system, depositing an HfO_2 layer on the substrate, performing a plasma treatment of the HfO_2 layer, and annealing the HfO_2 layer to form ferroelectric hafnium HfO_2.

[0007] In other features, the HfO_2 layer is deposited using atomic layer deposition (ALD). The method further includes doping the HfO_2 layer. Doping the HfO_2 layer includes doping the HfO_2 layer with at least one of silicon, aluminum, yttria, lanthanum, and zirconium. Doping the HfO_2 layer includes doping the HfO_2 layer with between 0 to 60 mol % of a dopant species. Depositing the HfO_2 layer includes alternating cycles of depositing HfO_2 onto the substrate and doping the deposited HfO_2. A thickness of the HfO_2 layer is between 6 and 12 nm. Alternating cycles of depositing the HfO_2 layer and performing the plasma treatment of the HfO_2 layer.

[0008] In other features, performing the plasma treatment includes using at least one plasma gas species to perform the plasma treatment. The at least one plasma gas species includes at least one of molecular nitrogen (N_2), ammonia (NH_3), molecular oxygen (O_2), ozone (O_3), argon (Ar), and argon and molecular hydrogen (Ar/H_2). Performing the plasma treatment includes performing the plasma treatment with molecular nitrogen (N_2), and performing the plasma treatment with N_2 causes HfO_xN_y to form on a surface of the HfO_2 layer.

[0009] In other features, performing the plasma treatment includes performing the plasma treatment for between 15 and 60 seconds. Performing the plasma treatment includes performing the plasma treatment at a radio frequency (RF) power between 500 and 1200 watts. The RF power is provided at between 1 and 15 MHz. Annealing the HfO_2 layer includes annealing the HfO_2 layer at a temperature between 500 and 1100 °C. Annealing the HfO_2 layer includes annealing the HfO_2 layer at a temperature between 800 and 1000 °C. Depositing a top electrode on the HfO_2 layer prior to the annealing. The top electrode comprises at least one of tantalum nitride, titanium nitride, and tungsten. Depositing the HfO_2 layer on the substrate includes depositing the HfO_2 layer on one of an underlying layer and a bottom electrode formed on the substrate.

[0010] A method of treating a substrate including ferroelectric hafnium oxide (HfO_2) in a substrate processing system includes arranging a substrate including an insulator layer within a processing chamber of the substrate processing system, performing at least one of a thermal treatment and a plasma treatment of the insulator layer, depositing an HfO_2 layer on the insulator layer, and annealing the HfO_2 layer to form ferroelectric hafnium HfO_2.

[0011] In other features, the insulator layer includes one of silicon dioxide (SiO_2) and silicon oxynitride (SiON). Performing the at least one of the thermal treatment and the plasma treatment includes sequentially performing the thermal treatment and the plasma

treatment. Performing the at least one of the thermal treatment and the plasma treatment includes increasing a temperature of the substrate to between 200 and 600 °C for 1 to 30 minutes. Performing the at least one of the thermal treatment and the plasma treatment includes providing at least one of N_2, N_2/H_2, NH_3, O_2, and O_3 to the processing chamber.

[0012] In other features, the method further includes performing a plasma treatment of the HfO_2 layer. The HfO_2 layer is deposited using atomic layer deposition (ALD). The method further includes doping the HfO_2 layer.

[0013] A method of treating a substrate including ferroelectric hafnium oxide (HfO_2) in a substrate processing system includes arranging a substrate including an insulator layer within a processing chamber of the substrate processing system, depositing at least one first HfO_2 layer on the insulator layer, performing at least one of a thermal treatment and a plasma treatment of the at least one first HfO_2 layer, depositing at least one second HfO_2 layer on the at least one first HfO_2 layer, and annealing the at least one second HfO_2 layer and the at least one first HfO_2 layer to form a ferroelectric hafnium HfO_2 layer.

[0014] In other features, the insulator layer includes one of silicon dioxide (SiO_2) and silicon oxynitride (SiON). Performing the at least one of the thermal treatment and the plasma treatment includes sequentially performing the thermal treatment and the plasma treatment. Performing the at least one of the thermal treatment and the plasma treatment includes increasing a temperature of the substrate to between 200 and 600 °C for 1 to 30 minutes. Performing the at least one of the thermal treatment and the plasma treatment includes providing at least one of N_2, N_2/H_2, NH_3, O_2, and O_3 to the processing chamber.

[0015] In other features, the at least one first HfO_2 layer is deposited in accordance with a dose time that is greater than a dose time used to deposit the at least one second HfO_2 layer. The method further includes performing at least one of a thermal treatment and a plasma treatment of the insulator layer prior to depositing the at least one first HfO_2 layer. The at least one first HfO_2 layer and the at least one second HfO_2 layer are deposited using atomic layer deposition (ALD).

[0016] Further areas of applicability of the present disclosure will become apparent from the detailed description, the claims and the drawings. The detailed description and specific examples are intended for purposes of illustration only and are not intended to limit the scope of the disclosure.

BRIEF DESCRIPTION OF THE DRAWINGS

[0017] The present disclosure will become more fully understood from the detailed description and the accompanying drawings, wherein:

[0018] FIGs. 1A and 1B are side cross-sectional views of substrates including nitridated HfO_2 according to the present disclosure;

[0019] FIG. 2 is a flowchart of an example of a method for reducing leakage current in HfO_2 based ferromagnetic material according to the present disclosure;

[0020] FIG. 3 is a flowchart of an example of a method for depositing and doping the HfO_2 according to the present disclosure;

[0021] FIG. 4 is a functional block diagram of an example of a substrate processing chamber for depositing, optional doping and nitridating the HfO_2 according to the present disclosure;

[0022] FIG. 5 is a side cross-sectional view of a substrate including a stack including a metal layer, a ferromagnetic layer, an insulator layer and a semiconductor layer according to the present disclosure;

[0023] FIG. 6 is a flowchart of an example of a method for depositing, optional doping and nitridating the HfO_2 in the substrate of FIG. 5;

[0024] FIG. 7 is a flowchart of an example of another method for depositing, optional doping and plasma treatment of a substrate according to the present disclosure;

[0025] FIG. 8 is a flowchart of an example of another method for depositing, optional doping and plasma treatment of a substrate according to the present disclosure;

[0026] FIG. 9 is a flowchart of an example of a method for depositing, doping and plasma treatment of a substrate according to the present disclosure;

[0027] FIG. 10 is a functional block diagram of a substrate processing system using transformer coupled plasma for performing plasma treatment;

[0028] FIGS. 11A, 11B, 11C, 11D, 11E, and 11F are side cross-sectional views of an example process including pretreatment of an insulator layer according to the present disclosure;

[0029] FIGS. 12A, 12B, 12C, 12D, 12E, and 12F are side cross-sectional views of an example process including treatment of one or more HfO_2 layers according to the present disclosure; and

[0030] FIG. 13 is a flowchart of an example of a method for pretreating an insulator layer and/or treating one or more HfO_2 layers according to the present disclosure.

[0031] In the drawings, reference numbers may be reused to identify similar and/or identical elements.

DETAILED DESCRIPTION

[0032] However, thermal stability of HfO_2 is an obstacle for commercialization in FeRAM applications. Although temperatures of 600–650 °C are high enough to crystallize as-deposited amorphous HfO_2 into the ferroelectric phase, many integration schemes require a thermal budget of at least 1000 °C. The higher process temperature degrades HfO_2-based FeRAM by increasing leakage current and/or shorting the devices.

[0033] Sources of leakage after high temperature annealing include defect generation at a top electrode/HfO_2 interface. Another source of leakage current includes film cracking of HfO_2. With the cracking of HfO_2, atoms from the top and bottom electrodes (typically TiN) can freely diffuse into HfO_2, which eventually causes failure of the device.

[0034] A method according to the present disclosure reduces leakage current in HfO_2-based ferroelectric material. In addition to other steps described further below, the method according to the present disclosure includes depositing doped or undoped HfO_2 on an underlying layer and performing plasma treatment of the HfO_2 film using molecular nitrogen (N_2), ammonia (NH_3), molecular oxygen (O_2), ozone (O_3), argon (Ar), and/or argon and molecular hydrogen (Ar/H_2) plasma. A top electrode such as titanium nitride (TiN), tantalum nitride (TaN), iridium (Ir), or tungsten (W) is then deposited on the treated HfO_2 film. The substrate is annealed using rapid thermal annealing at a predetermined temperature in a range from 500ºC to 1100ºC. A similar approach can be used for stacks including metal, ferromagnetic, insulator and semiconductor (MFIS) layers.

[0035] Plasma treatment is used to improve the thermal stability of HfO_2-based ferroelectric material. The plasma treatment densifies the HfO_2 film, which shrinks (less volume) and cracks less during subsequent high-temperature annealing. In FIGs. 2, 3 and 6, the plasma treatment includes nitridation. In FIGs. 7-9, other plasma treatments using Ar, Ar/H_2, O_2, O_3, and/or NH_3 are disclosed.

[0036] For example, use of N_2 plasma forms HfO_xN_y at the surface of the HfO_2. The nitridation of the surface of the HfO_2 reduces the generation of defects at the top electrode/HfO_2 interface in the subsequent processing steps, which mitigates the leakage current.

[0037] In other examples, pretreating the substrate with a plasma and/or thermal treatment process prior to and/or between cycles of ALD of HfO_2 further reduces leakage and widens a memory window of the device.

[0038] Referring now to FIGs. 1A and 1B, examples of devices including hafnium oxide (HfO_2)-based ferroelectric material according to the present disclosure are shown. In FIG.

1A, a substrate 10 includes one or more underlying layers 12 and a bottom electrode 14 arranged on the underlying layer 12. In some examples, the bottom electrode 14 includes titanium nitride (TiN), tantalum nitride (TaN), iridium (Ir), or tungsten (W), although other electrode materials can be used. In some examples, the bottom electrode 14 is deposited using atomic layer deposition (ALD), chemical vapor deposition (CVD) or physical vapor deposition (PVD).

[0039] A HfO_2 layer 16 is deposited. In some examples, the deposited HfO_2 layer 16 has a thickness in a range from 5 nm to 12nm. In some examples, the HfO_2 layer 16 is doped using a dopant species selected from a group consisting of silicon (Si), aluminum (Al), yttrium (Yt), zirconium (Zr), and/or lanthanum (La). In some examples, the HfO_2 layer 16 is deposited using atomic layer deposition (ALD), although other processes can be used. For example, thermal ALD or plasma-enhanced ALD can be used. In some examples, the HfO_2 layer 16 is undoped. In other examples, the HfO_2 layer 16 is doped to a predetermined doping level from greater than 0 mol% to less than or equal to 60 mol% of the selected dopant species. In some examples, the HfO_2 layer 16 is doped to a predetermined doping level from 3 mol% to 5 mol% of the selected dopant species.

[0040] In some examples, T ALD supercycles are performed to deposit the doped HfO_2 layer, where T is an integer greater than one. Each ALD supercycle includes N ALD HfO_2 cycles and M ALD cycles of the dopant species, where T, N and M are integers greater than zero. The N ALD HfO_2 cycles and M ALD cycles of the dopant species within each of the supercycles can be performed in any order. In some examples, the plasma treatment is performed between two or more of the T supercycles and/or after the T supercycles.

[0041] Plasma treatment of the HfO_2 layer 16 is performed. For example, the HfO_2 layer 16 is nitridated by plasma including a nitrogen gas species. For example, molecular nitrogen (N_2) gas may be used. In some examples, the nitridation is performed during a predetermined period in a range from 15s to 60s. In some examples, the RF power may be in a range from 100W to 15kW. In some examples, the plasma power is in a range from 500W to 1200W. In some examples, the RF frequency may be in a range from 1 MHz to 15 MHz. In some examples, the RF frequency is 2.0 MHz and/or 13.56 MHz.

[0042] After nitridation, a top electrode 18 is deposited on the HfO_2 layer 16. In some examples, the top electrode 18 includes TiN, TaN, Ir or W, although other electrode materials can be used. In some examples, the top electrode 18 is deposited using atomic layer deposition (ALD), chemical vapor deposition (CVD) or physical vapor deposition (PVD).

[0043] After depositing the top electrode 18, the substrate 10 is annealed at a predetermined temperature in a range from 500ºC to 1100ºC. In other examples, the

annealing temperature is in a range from 800ºC to 1000ºC. After annealing, the top electrode 18 is patterned. For example, a mask 20 may be used. The top electrode is etched using wet etching or dry etching. In some examples, the mask 20 is optionally removed after etching. In other examples, the mask is not removed.

[0044] In FIG. 1B, a specific example of the device is shown. A substrate 30 includes a silicon (Si) layer 32. A bottom electrode 34 made of TiN is arranged on the Si layer 32. A Si-doped HfO_2 layer 36 is deposited on the bottom electrode 34. The Si-doped HfO_2 layer 36 is treated using one of the plasma treatments described herein and then a top electrode 38 made of TiN is deposited on the Si-doped HfO_2 layer 36. The substrate 30 is annealed at a predetermined temperature. The top electrode 38 is patterned using an inert metal layer 40 such as platinum (Pt) and etched using wet or dry etching.

[0045] Referring now to FIG. 2, a method 60 includes providing a substrate. At 64, a bottom electrode layer (including TiN, TaN, Ir or W) is deposited on the substrate. At 66, a doped or undoped HfO_2 layer is deposited on the bottom electrode layer. At 68, the HfO_2 layer is nitridated using plasma and a nitrogen species. At 72, a top electrode layer (including TiN, TaN, Ir or W) is deposited on the nitridated HfO_2 layer. At 74, the substrate is processed using rapid thermal annealing to a temperature in a range from 500ºC to 1100ºC. In some examples, the top electrode is patterned at 78 and etched at 82.

[0046] Referring now to FIG. 3, a method 90 for depositing the doped HfO_2 layer using T ALD supercycles is shown. At 92, N ALD HfO_2 cycles are performed and M ALD cycles of the dopant species are performed (where T, N and M are integers greater than zero). As can be appreciated, the N ALD HfO_2 cycles and the M ALD cycles of the dopant species can be performed in any order during a given supercycle. At 96, the method returns to 92 if additional supercycles need to be performed or ends if the T supercycles are completed.

[0047] Referring now to FIG. 4, an example substrate processing system 100 for depositing and optionally doping the HfO_2 layer using atomic layer deposition (ALD) and nitridating the HfO_2 layer is shown. While the deposition and doping of the HfO_2 layer and subsequent nitridation are being performed in the same processing chamber in this example, separate processing chambers can be used. For example, nitridation can also be performed in a transformer coupled plasma (TCP) chamber (e.g. as shown in FIG. 10), a plasma-enhanced chemical vapor deposition (PECVD) chamber, a high pressure CVD (HPCVD) chamber, and/or a chamber using a remote plasma source.

[0048] The substrate processing system 100 includes a processing chamber 102 that encloses other components of the substrate processing chamber 100 and contains the RF plasma. The substrate processing chamber 100 includes an upper electrode 104 and a

substrate support, such as an electrostatic chuck (ESC) 106. During operation, a substrate 108 is arranged on the ESC 106.

[0049] For example only, the upper electrode 104 may include a showerhead 109 that introduces and distributes process gases. The showerhead 109 may include a stem portion including one end connected to a top surface of the processing chamber. A base portion is generally cylindrical and extends radially outwardly from an opposite end of the stem portion at a location that is spaced from the top surface of the processing chamber. A substrate-facing surface or faceplate of the base portion of the showerhead includes a plurality of holes through which process gas or purge gas flows. Alternately, the upper electrode 104 may include a conducting plate and the process gases may be introduced in another manner.

[0050] The ESC 106 includes a conductive baseplate 110 that acts as a lower electrode. The baseplate 110 supports a heating plate 112, which may correspond to a ceramic multi-zone heating plate. A thermal resistance layer 114 may be arranged between the heating plate 112 and the baseplate 110. The baseplate 110 may include one or more coolant channels 116 for flowing coolant through the baseplate 110.

[0051] An RF generating system 120 generates and outputs an RF voltage to one of the upper electrode 104 and the lower electrode (e.g., the baseplate 110 of the ESC 106). The other one of the upper electrode 104 and the baseplate 110 may be DC grounded, AC grounded or floating. For example only, the RF generating system 120 may include an RF voltage generator 122 that generates the RF voltage that is fed by a matching and distribution network 124 to the upper electrode 104 or the baseplate 110. In other examples, the plasma may be generated inductively or remotely.

[0052] A gas delivery system 130 includes one or more gas sources 132-1, 132-2,..., and 132-N (collectively gas sources 132), where N is an integer greater than zero. The gas sources supply one or more deposition precursors and mixtures thereof. The gas precursors may include precursor gases for the HfO_2 layer and/or other layers. The gas sources may also supply purge gas and gases including a nitrogen species for plasma nitridation and/or other gas species (such as Ar, Ar/H_2, NH_3, O_2, O_3, etc.) for other plasma treatments. Vaporized precursor may also be used. The gas sources 132 are connected by valves 134-1, 134-2, ..., and 134-N (collectively valves 134) and mass flow controllers 136-1, 136-2, ..., and 136-N (collectively mass flow controllers 136) to a manifold 138. An output of the manifold 138 is fed to the processing chamber 102. For example only, the output of the manifold 138 is fed to the showerhead 109. In some examples, an optional ozone generator 140 may be provided between the mass flow controllers 136 and the manifold 138. In some

examples, the substrate processing system 100 may include a liquid precursor delivery system 141. The liquid precursor delivery system 141 may be incorporated within the gas delivery system 130 as shown or may be external to the gas delivery system 130. The liquid precursor delivery system 141 is configured to provide precursors that are liquid and/or solid at room temperature via a bubbler, direct liquid injection, vapor draw, etc.

[0053] A temperature controller 142 may be connected to a plurality of thermal control elements (TCEs) 144 arranged in the heating plate 112. For example, the TCEs 144 may include, but are not limited to, respective macro TCEs corresponding to each zone in a multi-zone heating plate and/or an array of micro TCEs disposed across multiple zones of a multi-zone heating plate as described in more detail in FIGS. 2A and 2B. The temperature controller 142 may be used to control the plurality of TCEs 144 to control a temperature of the ESC 106 and the substrate 108.

[0054] The temperature controller 142 may communicate with a coolant assembly 146 to control coolant flow through the channels 116. For example, the coolant assembly 146 may include a coolant pump and reservoir. The temperature controller 142 operates the coolant assembly 146 to selectively flow the coolant through the channels 116 to cool the ESC 106.

[0055] A valve 150 and pump 152 may be used to evacuate reactants from the processing chamber 102. A system controller 160 may be used to control components of the substrate processing system 100. A robot 170 may be used to deliver substrates onto, and remove substrates from, the ESC 106. For example, the robot 170 may transfer substrates between the ESC 106 and a load lock 172. Although shown as separate controllers, the temperature controller 142 may be implemented within the system controller 160. The temperature controller 142 may be further configured to implement one or more models to estimate temperatures of the ESC 106 according to the principles of the present disclosure.

[0056] Generally, more nitrogen is incorporated into the HfO_2 surface at high plasma power, accompanied by less film cracking. However, the leakage current may not strictly follow the amount of incorporated nitrogen. For example, one sample treated by 1000 W plasma may be leakier than another sample treated by only 500 W. Higher plasma power may also damage the HfO_2 film structure, which in turn increases leakage current. In addition, since HfN is not ferroelectric, the plasma nitridation process may decrease remnant polarization (Pr).

[0057] Conversely, extending the plasma time at 500W reduces the leakage current after 1000 °C / 1s anneal, while a period of 15s may not be sufficient to mitigate the leakage current. For example, HfO_2 is typically over-nitridated after 60s plasma while the leakage

current is as low as 10^{-8} A. However, the ferroelectric property of the HfO_2 may be severely degraded (e.g., Pr = 7 μC/cm^2) when the plasma time is greater than 60s.

[0058] Referring now to FIG. 5, nitridation and optional doping of HfO_2 can also be used for stacks including metal, ferromagnetic, insulator, and semiconductor (MFIS) layers. A substrate 200 includes one or more underlying layers such as a semiconductor layer 210 that may include one or more diffusion regions 214. An insulator layer 220 is deposited on the semiconductor layer 210. In some examples, the insulator layer 220 includes silicon dioxide (SiO_2) or silicon nitride (SiN). A ferromagnetic layer including doped or undoped HfO_2 layer 224 (as described above) is deposited on the insulator layer 220. The doped or undoped HfO_2 layer 224 is processed using the selected plasma treatment. A metal layer 228 is deposited on the doped or undoped HfO_2 layer 224. In some examples, the metal layer 228 includes TiN, TaN, Ir or W. After depositing the metal layer 228, the substrate is annealed using rapid thermal annealing at a temperature in a range from 500ºC to 1100ºC.

[0059] Referring now to FIG. 6, a method 250 for depositing, optional doping and nitridating the HfO_2 in the stack of FIG. 5 is shown. At 252, a semiconductor substrate is provided. At 254, an insulator layer is deposited on the semiconductor substrate. In some examples, the insulator layer includes silicon dioxide (SiO_2) or silicon nitride (SiN). At 256, a doped or undoped HfO_2 layer is deposited on the insulator layer. At 268, the HfO_2 layer is nitridated using plasma including nitrogen species. At 272, a metal layer is deposited on the HfO_2 layer. In some examples, the metal layer includes TiN, TaN, Ir or W. At 274, rapid thermal annealing is performed on the substrate at a temperature in a range from 500ºC to 1100ºC. In some examples, the metal layer is patterned at 278 and etched at 282.

[0060] In some examples, the insulator layer, the doped or undoped HfO_2 layer, and the nitridation are performed in the same processing chamber or using different processing chambers. The insulator layer, the doped or undoped HfO_2 layer, and/or the metal layer can be deposited using any of the processes described above.

[0061] Referring now to FIG. 7, other gas species can be used during plasma treatment of the substrate to reduce leakage current. More particularly, gas species including ammonia (NH_3), molecular oxygen (O_2), argon (Ar) or a mixture of argon and molecular hydrogen (Ar/H_2) can be used. In FIG. 7, a method 330 includes providing a substrate. At 332, a bottom electrode layer (including TiN, TaN, Ir or W) is deposited on the substrate. At 336, a doped or undoped HfO_2 layer is deposited on the bottom electrode layer. At 338, the HfO_2 layer is treated using plasma with a plasma gas species selected from a group consisting of N_2, NH_3, O_2, O_3, Ar and/or Ar/H_2. At 340, a top electrode layer (including TiN, TaN, Ir or W) is deposited on the nitridated HfO_2 layer. At 342, the substrate is processed using rapid

thermal annealing to a temperature in a range from 500ºC to 1100ºC. The top electrode is patterned at 344 and etched at 346.

[0062] Referring now to FIG. 8, a method 350 for depositing, optional doping and plasma treating the HfO_2 in the stack of FIG. 5 is shown. At 352, a semiconductor substrate is provided. At 354, an insulator layer is deposited on the semiconductor substrate. In some examples, the insulator layer includes silicon dioxide (SiO_2) or silicon nitride (SiN). At 356, a doped or undoped HfO_2 layer is deposited on the insulator layer. At 358, the HfO_2 layer is treated using plasma with a plasma gas species selected from a group consisting of N_2, NH_3, Ar, O_2, and/or Ar/H_2. At 360, a metal layer is deposited on the HfO_2 layer. In some examples, the metal layer includes TiN, TaN, Ir or W. At 362, rapid thermal annealing is performed on the substrate at a temperature in a range from 500ºC to 1100ºC. In some examples, the metal layer is patterned at 364 and etched at 366.

[0063] In some examples, the insulator layer, the doped or undoped HfO2 layer, and the plasma treatment are performed in the same processing chamber or using different processing chambers. The insulator layer, the doped or undoped HfO_2 layer, and/or the metal layer can be deposited using any of the processes described above.

[0064] Referring now to FIG. 9, a method 400 for depositing the doped HfO_2 layer using T ALD supercycles with intervening plasma treatment is shown. At 402, N ALD HfO_2 cycles are performed and M ALD cycles of the dopant species are performed, where T, N and M are integers greater than zero. As can be appreciated, the N ALD HfO_2 cycles and the M ALD cycles of the dopant species can be performed in any order during a given supercycle. At 404, the HfO_2 layer is treated using plasma with a plasma gas species selected from a group consisting of N_2, NH_3, Ar, O_2 O_3, and/or Ar/H_2. At 406, the method returns to 402 if additional supercycles need to be performed or ends if the T supercycles are completed.

[0065] Referring now to FIG. 10, an example of a substrate processing system 510 for performing TCP plasma treatment according to the present disclosure is shown. The substrate processing system 510 includes a coil driving circuit 511. In some examples, the coil driving circuit 511 includes an RF source 512 and a tuning circuit 513. The tuning circuit 513 may be directly connected to one or more inductive coils 16. Alternatively, the tuning circuits 513 may be connected by an optional reversing circuit 515 to one or more of the coils 516. The tuning circuit 513 tunes an output of the RF source 512 to a desired frequency and/or a desired phase, matches an impedance of the coils 516 and splits power between the TCP coils 516. The reversing circuit 515 is used to selectively switch the polarity of current through one or more of the TCP coils 516. Examples of the reversing circuit 515 are shown and described in commonly assigned U.S. Patent Application No. 14/673,174 by Sato

et al., titled "Systems And Methods For Reversing RF Current Polarity At One Output Of A Multiple Output RF Matching Network," filed March 30, 2015.

[0066] In some examples, a plenum 520 may be arranged between the TCP coils 516 and a dielectric window 524 to control the temperature of the dielectric window with hot and/or cold air flow. The dielectric window 524 is arranged along one side of a processing chamber 528. The processing chamber 528 further comprises a substrate support (or pedestal) 532. The substrate support 532 may include an electrostatic chuck (ESC), or a mechanical chuck or other type of chuck. Process gas is supplied to the processing chamber 528 and plasma 540 is generated inside of the processing chamber 528. The plasma 540 etches an exposed surface of the substrate 534. An RF source 550 and a bias matching circuit 552 may be used to bias the substrate support 532 during operation to control ion energy.

[0067] A gas delivery system 556 may be used to supply a process gas mixture to the processing chamber 528. The gas delivery system 556 may include process and inert gas sources 557, a gas metering system 558 such as valves and mass flow controllers, and a manifold 559. A gas delivery system 560 may be used to deliver gas 562 via a valve 561 to the plenum 520. The gas may include cooling gas (air) that is used to cool the TCP coils 516 and the dielectric window 524. A heater/cooler 564 may be used to heat/cool the substrate support 532 to a predetermined temperature. An exhaust system 565 includes a valve 566 and pump 567 to remove reactants from the processing chamber 528 by purging or evacuation.

[0068] A controller 554 may be used to control the etching process. The controller 554 monitors system parameters and controls delivery of the gas mixture, striking, maintaining and extinguishing the plasma, removal of reactants, supply of cooling gas, and so on. Additionally, as described below in detail, the controller 554 may control various aspects of the coil driving circuit 511, the RF source 550, and the bias matching circuit 552, etc.

Examples

[0069] Plasma treatment of the HfO_2 in a TCP chamber was tested at 4.2 mol% Si doping. The as-deposited HfO_2 exhibited leakage current at the level of 10^{-7} A after 1000 °C / 1 sec anneal. Treatment with N_2 plasma decreased the leakage current by one order of magnitude, down to 10^{-8} A using the same 1000 °C / 1 sec anneal. Other plasma treatments using NH_3, Ar, and Ar/H_2 gas species were also tested. NH_3 and Ar/H_2 plasma treatment decreased the leakage current by a factor of 2 after 1000 °C / 1 sec anneal. At lower anneal temperatures (e.g. 800 °C), all of the plasma treatments (N_2, NH_3, Ar, and Ar/H_2) improved the leakage current as compared to the sample without plasma treatment. Plasma

nitridation slightly degraded the remnant polarization (Pr) of the ferroelectric HfO_2. However, the Pr value (15–17 $\mu C/cm^2$) still meets the target spec of 15 $\mu C/cm^2$. The same results are achieved with NH_3 and Ar/H_2 plasma.

[0070] A sample with higher doping (e.g. 5.7 mol% Si in HfO_2) was also studied with the same plasma treatments. The higher doping concentration is not optimal due to the wakeup effect in the initial cycles. The N_2 plasma improved leakage current in the HfO_2 with 5.7 mol% Si. whereas NH_3, Ar, and Ar/H_2 plasma increased the leakage current. The samples treated with Ar and Ar/H_2 plasma fail with only 1000 switching cycles.

[0071] While plasma treatment of HfO_2 before top electrode deposition mitigates the defects at the HfO_2 surface, the defects in the bulk HfO_2 film may be another leakage current source. As a result, some of the methods described herein employ plasma treatment between the supercycles of HfO_2 deposition to further mitigate the defects within the film. For example, rather than one single plasma treatment after 8 nm HfO_2, the substrate is exposed to the plasma treatment after every 1, 2, or 4 nm of HfO_2 deposition.

[0072] In addition to N_2 plasma, Ar/H_2 and NH_3 plasma also decrease the leakage current in HfO_2 after 1000 °C anneal. N_2 plasma is the most effective environment in leakage current improvement. Supercycles of HfO_2 deposition and plasma treatment have the potential to further decrease leakage current in the ferroelectric material. In other examples, the type of plasma can be varied to capacitively coupled plasma (CCP), downstream or remote plasma, or microwave plasma.

Pretreating Substrate and/or Treating HfO_2 Layers

[0073] In other examples, pretreating the substrate with a plasma and/or thermal treatment process prior to and/or between cycles of ALD of HfO_2 further reduces leakage and widens a memory window of the device. For example, in a ferroelectric field-effect transistor (FeFET), ferroelectric HfO_2 is arranged between a metal layer (e.g., a top electrode) and a dielectric layer (e.g., an insulator/interfacial layer) formed on an Si substrate to form an MFIS film stack structure. The insulator layer is critical to performance properties of the MFIS film stack. Flipping of charges in the ferroelectric material shifts a flat band voltage, causes hysteresis in C–V curves, and shifts a threshold voltage (Vth) of the transistor. Defects in the insulator layer and/or at an interface between the insulator layer and the ferroelectric material can cause charge injection, which shifts the flat band voltage and causes C–V hysteresis in an opposite direction to that of the ferroelectric material (causing cancellation of the C—V hysteresis). Accordingly, it is desirable to minimize defects in the insulator layer and/or at the interface between the insulator layer and the ferroelectric material to improve performance of the ferroelectric material.

[0074] Pretreating the substrate with a plasma and/or thermal treatment as described below reduces defects in the insulator layer and/or at the interface between the insulator layer and the ferroelectric material to reduce leakage and widen a memory window of the device as described below in more detail. Pretreatment methods include thermal treatment, plasma treatment, and/or a sequence of thermal and plasma treatment. Gas environments for the treatment may include N_2, N_2/H_2, NH_3, O_2, and/or O_3. Substrates may be pretreated in an ALD processing chamber or in a separate chamber prior to transfer to the ALD processing chamber. In some examples, the pretreatment process may be performed subsequent to performing one or more ALD cycles of HfO_2 (e.g., 0.1–2.0 nm HfO_2) on the surface of the insulator layer. In other examples, the pretreatment process may be performed on the substrate prior to performing ALD and subsequent to one or more cycles of ALD. Deposition conditions of the one or more ALD cycles prior to performing the treatment process may differ from deposition conditions for subsequent ALD cycles. For example, an ozone dose time of the one or more ALD cycles prior to performing the treatment process may be greater than an ozone dose time of subsequent cycles.

[0075] Referring now to FIGS. 11A, 11B, 11C, 11D, 11E, and 11F, an example process for forming a (HfO_2)-based ferroelectric material in a device 600 is shown. In FIG. 11A, the device 600 includes a substrate (e.g., one or more underlying layers) 604 and an interfacial/insulator layer 608 (referred to hereinafter as an insulator layer) arranged on the underlying layers 604. For example, the underlying layers 604 comprise silicon (Si). In some examples, the insulator layer 608 includes silicon dioxide (SiO_2) or silicon oxynitride (SiON) dielectrics. In some examples, the insulator layer 608 is deposited using atomic layer deposition (ALD), chemical vapor deposition (CVD) or physical vapor deposition (PVD). In other examples, the insulator layer 608 may be formed via thermal oxidation of Si. For example, the insulator layer 608 may be formed by thermal oxidation of Si in an oxygen environment with a nitrogen species (e.g., N_2O or N_2) to form SiON, plasma nitridation of SiO_2, etc. The insulator layer 608 may be deposited in a different processing chamber than a chamber used to perform subsequent steps.

[0076] As shown in FIG. 11B, pretreatment of the insulator layer 608 is performed. The pretreatment may be performed in a same or different processing chamber as the deposition of the insulator layer 608. The pretreatment may include thermal treatment, plasma treatment, and/or a sequence of thermal and plasma treatment (e.g., a thermal treatment step followed by a plasma treatment step). The pretreatment removes defects (e.g., unbonded hydrocarbon contaminants) from the surface of the insulator layer 608. For example, exposure to air may cause hydrocarbons to absorb onto the surface of the insulator layer 608. The pretreatment facilitates bonding between the hydrocarbon

contaminants and gases within the processing chamber. The bonded hydrocarbons may then be removed (e.g., purged) from the processing chamber.

[0077] Thermal treatment may include increasing a temperature of the substrate (e.g., using the temperature controller 142) while flowing process gases into the processing chamber. For example, the substrate may be increased to a temperature from 200 to 600 °C from 1 to up to 30 minutes. In some examples, the substrate is increased to a temperature from 300 to 400 °C. The process gases may include N_2, N_2/H_2, NH_3, O_2, and/or O_3. The increased temperature facilitates bonding between the hydrocarbon contaminants and the process gases.

[0078] Plasma treatment may include flowing process gases (N_2, N_2/H_2, NH_3, O_2, O_3, etc.) and striking plasma within the processing chamber. While the plasma treatment may be performed while the temperature of the substrate is increased, the plasma treatment may be performed at significantly lower temperatures than the thermal treatment (e.g., at 50 °C). Accordingly, the plasma treatment facilitates bonding between the hydrocarbon contaminants and the process gases without the greater temperatures of the thermal treatment. The plasma treatment may be performed from 1 to up to 30 minutes.

[0079] As shown in FIG. 11C, an HfO_2 layer 612 is deposited on the insulator layer 608 and a top electrode 616 is deposited on the HfO_2 layer 612. In some examples, the deposited HfO_2 layer 612 has a thickness in a range from 2 nm to 12nm. In some examples, the HfO_2 layer 612 is doped using a dopant species selected from a group consisting of silicon (Si), aluminum (Al), yttrium (Yt), zirconium (Zr), and/or lanthanum (La). In some examples, the HfO_2 layer 612 is deposited using atomic layer deposition (ALD), although other processes can be used. For example, thermal ALD or plasma-enhanced ALD can be used. In some examples, the HfO_2 layer 612 is undoped. In other examples, the HfO_2 layer 612 is doped to a predetermined doping level from greater than 0 mol% to less than or equal to 60 mol% of the selected dopant species. In some examples, the HfO_2 layer 612 is doped to a predetermined doping level from 3 mol% to 5 mol% of the selected dopant species. The HfO_2 layer 612 may be amorphous.

[0080] Plasma treatment of the HfO_2 layer 612 may optionally be performed. For example, the HfO_2 layer 612 is nitridated by plasma including a nitrogen gas species. For example, molecular nitrogen (N_2) gas may be used. In some examples, the nitridation is performed during a predetermined period in a range from 15s to 60s. In some examples, the RF power may be in a range from 100W to 15kW. In some examples, the plasma power is in a range from 500W to 1200W. In some examples, the RF frequency may be in a range from 1 MHz to 15 MHz. In some examples, the RF frequency is 2.0 MHz and/or 13.56 MHz.

[0081] The top electrode 616 is deposited on the HfO_2 layer 612. In some examples, the top electrode 616 includes TiN, TaN, Ir or W, although other electrode materials can be used (e.g., Pt, Au, Pd, Al, Mo, Ni, Ti, etc.). In some examples, the top electrode 616 is deposited using atomic layer deposition (ALD), chemical vapor deposition (CVD), or physical vapor deposition (PVD). After depositing the top electrode 616, the device 600 is annealed at a predetermined temperature in a range from 500 ºC to 1100 ºC. In other examples, the annealing temperature is in a range from 800 ºC to 1000 ºC.

[0082] After annealing, the top electrode 616 is patterned as shown in FIGS. 11D, 11E, and 11F. For example, a mask 620 may be deposited as shown in FIG. 11D. The mask 620 may comprise platinum (Pt). The top electrode 616 is etched using wet etching or dry etching as shown in FIG. 11E. In some examples, the mask 620 is optionally removed after etching as shown in FIG. 11F. In other examples, the mask is not removed.

[0083] Referring now to FIGS. 12A, 12B, 12C, 12D, 12E, and 12F, another example process for forming a (HfO_2)-based ferroelectric material in a device 700 is shown. In FIG. 12A, the device 700 includes a substrate (e.g., one or more underlying layers) 704 and an interfacial/insulator layer 708 (referred to hereinafter as an insulator layer) arranged on the underlying layers 704. For example, the underlying layers 704 comprise silicon (Si). In some examples, the insulator layer 708 includes silicon dioxide (SiO_2) or silicon oxynitride (SiON) dielectrics. In some examples, the insulator layer 708 is deposited using atomic layer deposition (ALD), chemical vapor deposition (CVD) or physical vapor deposition (PVD). In other examples, the insulator layer 708 may be formed via thermal oxidation of Si. For example, the insulator layer 708 may be formed by thermal oxidation of Si in an oxygen environment with a nitrogen species (e.g., N_2O or N_2) to form SiON, plasma nitridation of SiO_2, etc. The insulator layer 708 may be deposited in a different processing chamber than a chamber used to perform subsequent steps.

[0084] As shown in FIG. 12B, optional pretreatment of the insulator layer 708 is performed. The pretreatment may be performed in a same or different processing chamber as the deposition of the insulator layer 708. The pretreatment may include thermal treatment, plasma treatment, and/or a sequence of thermal and plasma treatment (e.g., a thermal treatment step followed by a plasma treatment step). The pretreatment removes defects (e.g., unbonded hydrocarbon contaminants) from the surface of the insulator layer 708 as described above in FIG. 11B.

[0085] As shown in FIG. 12C, one or more ALD cycles are performed to deposit one or more thin layers 710 of HfO_2 (e.g., 0.1–2.0 nm HfO_2) on the insulator layer 708. For example, these initial ALD cycles may be performed at a temperature of 180-300 °C and a

pressure of 0.1 to 2.0 Torr with an ozone dose time of 10-60 seconds, a precursor dose time of 1-5 seconds, and a purge time (i.e., to purge the precursor and ozone) of 30-75 seconds. In some examples, the ozone dose time is greater than the ozone dose time of FIG. 12E. For example, the ozone dose time of FIG. 12C is 45-60 seconds while the ozone does time of FIG. 12E is 10-45 seconds. The increased ozone dose time for the initial ALD cycles may minimize oxygen vacancies at the interface of the insulator layer 708 and the thin layers 710 of HfO_2.

[0086] As shown in FIG. 12D, treatment of the deposited layers 710 of HfO_2 layer is performed. Treatment may include thermal treatment, plasma treatment, and/or a sequence of thermal and plasma treatment (e.g., a thermal treatment step followed by a plasma treatment step) as described above in FIG. 11B.

[0087] As shown in FIG. 12E, remaining layers of HfO_2 are deposited on the layers 710 to form an HfO_2 layer 712 and a top electrode 716 is deposited on the HfO_2 layer 712. In some examples, the deposited HfO_2 layer 712 has a thickness in a range from 2 nm to 12nm. In some examples, the HfO_2 layer 712 is doped using a dopant species selected from a group consisting of silicon (Si), aluminum (Al), yttrium (Yt), zirconium (Zr), and/or lanthanum (La). In some examples, the HfO_2 layer 712 is deposited using atomic layer deposition (ALD), although other processes can be used. For example, thermal ALD or plasma-enhanced ALD can be used. In some examples, the HfO_2 layer 612 is undoped. In other examples, the HfO_2 layer 712 is doped to a predetermined doping level from greater than 0 mol% to less than or equal to 60 mol% of the selected dopant species. In some examples, the HfO_2 layer 712 is doped to a predetermined doping level from 3 mol% to 5 mol% of the selected dopant species. The HfO_2 layer 712 may be amorphous.

[0088] Additional plasma treatment of the completed HfO_2 layer 712 may optionally be performed. For example, the HfO_2 layer 712 is nitridated by plasma including a nitrogen gas species. For example, molecular nitrogen (N_2) gas may be used. In some examples, the nitridation is performed during a predetermined period in a range from 15s to 60s. In some examples, the RF power may be in a range from 100W to 15kW. In some examples, the plasma power is in a range from 500W to 1200W. In some examples, the RF frequency may be in a range from 1 MHz to 15 MHz. In some examples, the RF frequency is 2.0 MHz and/or 13.56 MHz.

[0089] The top electrode 716 is deposited on the HfO_2 layer 712. In some examples, the top electrode 716 includes TiN, TaN, Ir or W, although other electrode materials can be used (e.g., Pt, Au, Pd, Al, Mo, Ni, Ti, etc.). In some examples, the top electrode 716 is deposited using atomic layer deposition (ALD), chemical vapor deposition (CVD), or physical vapor

deposition (PVD). After depositing the top electrode 716, the device 700 is annealed at a predetermined temperature in a range from 500 ºC to 1100 ºC. In other examples, the annealing temperature is in a range from 800 ºC to 1000 ºC.

[0090] After annealing, the top electrode 716 is patterned as shown in FIG. 12F. For example, a mask is deposited, the top electrode 716 is etched, and the mask is removed after etching in a manner similar to that described in FIGS. 11D, 11E, and 11F.

[0091] Referring now to FIG. 13, an example of a method 800 for pretreating an insulator layer and/or treating one or more HfO_2 layers according to the present disclosure begins at 804. At 808, a substrate is provided. For example, a substrate including one or more underlying layers and an insulator layer is arranged on a substrate support in a processing chamber. The insulator layer may include silicon dioxide (SiO_2) or silicon oxynitride (SiON). For example, the interfacial layer may be deposited using atomic layer deposition (ALD), chemical vapor deposition (CVD), or physical vapor deposition (PVD) in the same processing chamber or in a different processing chamber.

[0092] At 812, optional pretreatment of the insulator layer is performed. For example, the pretreatment may include thermal treatment and/or plasma treatment as described above in FIG. 11B. In examples where optional treatment of deposited layers of HfO_2 is performed, the method 800 continues to 816 and 820. Otherwise, the method 800 continues to 824. At 816, one or more cycles of ALD are performed to deposit thin layers of HfO_2 as described above in FIG. 12C. At 820, treatment of the deposited layers of HfO_2 is performed. For example, the treatment of the deposited layers of HfO_2 may include thermal treatment and/or plasma treatment as described above in FIG. 12D. Accordingly, at 812, 816, and 820, the method 800 performs pretreatment of the insulator layer and/or treatment of deposited thin layers of HfO_2. In other words, the method 800 may perform only pretreatment of the insulator layer, only treatment of deposited thin layers of HfO_2, or both pretreatment of the insulator layer and treatment of deposited thin layers of HfO_2.

[0093] At 824, a doped or undoped HfO_2 layer is deposited on the insulator layer (e.g., using ALD) or on thin layers of HfO_2 previously deposited on the insulator layer at 816 and 820. At 828, plasma treatment of the HfO_2 layer may optionally be performed. For example, the HfO_2 layer may be nitridated by plasma including a nitrogen gas species. At 832, a top electrode (e.g., TiN, TaN, Ir or W) is deposited on the HfO_2 layer. For example, the top electrode is deposited using atomic layer deposition (ALD), chemical vapor deposition (CVD), or physical vapor deposition (PVD). At 836, the substrate, insulator layer, HfO_2 layer, and top electrode are annealed at a predetermined temperature in a range from 500 ºC to 1100 ºC (e.g., from 800 ºC to 1000 ºC) to form ferroelectric HfO_2. The top electrode may be

patterned at 840 (e.g., a mask may be patterned onto the top electrode) and etched at 844. The method 800 ends at 848.

Examples

[0094] In one example, an SiO_2 insulator layer was pretreated with ozone (i.e., prior to performing any HfO_2 ALD cycles) in an ALD processing chamber at an ALD temperature (e.g., 200 °C). In this example, leakage current was reduced slightly. Conversely, in an example where the treatment with ozone was performed subsequent to 5-9 cycles HfO_2 ALD (e.g., 0.5 - 0.9 nm), leakage current was reduced a greater amount relative to the sample where the insulator layer was pretreated. Leakage current reduction is indicative of fewer defects in the film stack, which suggests improved C–V hysteresis in MFIS switching.

[0095] In another example, conditions for depositing the initial thin layers (e.g., 2 nm) of HfO_2 may be varied to decrease defects. For example, an O_3 dose time during the intial ALD cycles (e.g., for the first 2 nm) may be greater than the O_3 dose time of ALD cycles performed subsequent to treatment. Accordingly, a leakage feature in ferroelectric switching is suppressed. In an example with the same O_3 dose time for ALD cycles prior to and subsequent to treatment, no FE hysteresis was observed in the C–V curve despite FE switching in the P–E curve. The absence of C–V hysteresis may be attributed to high defect density at the insulator/ferroelectric interface. Charge injection cancels the effect of FE switching. In contrast, in an example with a longer O_3 dose in the first 2 nm of HfO_2 prior to treatment, a memory window of 0.2 V was observed in the C–V curve. The extended O_3 dose time in the first 2 nm decreases the defect density at the interface, and therefore suppresses the charge injection. A memory window, although small, occurred in the C–V curve to indicate ferroelectric switching.

[0096] In another example, a forming gas anneal (FGA) step was performed on the substrate prior to performing the HfO_2 ALD. FGA performed at 300 °C prior to ALD did not further improve the leakage. However, the memory window increased from ~0.3 V in the sample without FGA to ~0.55 V in the sample with FGA performed prior to ALD. Accordingly, combining the pretreatment and treatment methods described herein with FGA may further increase the memory window (e.g., to 1.0 V).

[0097] In these described examples, the sample included an 8 nm HfO_2 layer with 4.2 mol% Si. The HfO_2 thickness may vary from 2 to 12 nm. The HfO_2 layer may be undoped or contain dopants such as Al, Y, Gd, Sr, La, and Zr. The dopant concentration varies between 0 and 6 mol% for Si, while other dopants may have a wider range of 0–60 mol%. Ferroelectric HfO_2 is formed by annealing with a metal cap (e.g. TiN) under N_2 at 600–1000 °C.

[0098] The foregoing description is merely illustrative in nature and is in no way intended to limit the disclosure, its application, or uses. The broad teachings of the disclosure can be implemented in a variety of forms. Therefore, while this disclosure includes particular examples, the true scope of the disclosure should not be so limited since other modifications will become apparent upon a study of the drawings, the specification, and the following claims. It should be understood that one or more steps within a method may be executed in different order (or concurrently) without altering the principles of the present disclosure. Further, although each of the embodiments is described above as having certain features, any one or more of those features described with respect to any embodiment of the disclosure can be implemented in and/or combined with features of any of the other embodiments, even if that combination is not explicitly described. In other words, the described embodiments are not mutually exclusive, and permutations of one or more embodiments with one another remain within the scope of this disclosure.

[0099] Spatial and functional relationships between elements (for example, between modules, circuit elements, semiconductor layers, etc.) are described using various terms, including "connected," "engaged," "coupled," "adjacent," "next to," "on top of," "above," "below," and "disposed." Unless explicitly described as being "direct," when a relationship between first and second elements is described in the above disclosure, that relationship can be a direct relationship where no other intervening elements are present between the first and second elements, but can also be an indirect relationship where one or more intervening elements are present (either spatially or functionally) between the first and second elements. As used herein, the phrase at least one of A, B, and C should be construed to mean a logical (A OR B OR C), using a non-exclusive logical OR, and should not be construed to mean "at least one of A, at least one of B, and at least one of C."

[0100] In some implementations, a controller is part of a system, which may be part of the above-described examples. Such systems can comprise semiconductor processing equipment, including a processing tool or tools, chamber or chambers, a platform or platforms for processing, and/or specific processing components (a wafer pedestal, a gas flow system, etc.). These systems may be integrated with electronics for controlling their operation before, during, and after processing of a semiconductor wafer or substrate. The electronics may be referred to as the "controller," which may control various components or subparts of the system or systems. The controller, depending on the processing requirements and/or the type of system, may be programmed to control any of the processes disclosed herein, including the delivery of processing gases, temperature settings (e.g., heating and/or cooling), pressure settings, vacuum settings, power settings, radio frequency (RF) generator settings, RF matching circuit settings, frequency settings, flow rate settings,

fluid delivery settings, positional and operation settings, wafer transfers into and out of a tool and other transfer tools and/or load locks connected to or interfaced with a specific system.

[0101] Broadly speaking, the controller may be defined as electronics having various integrated circuits, logic, memory, and/or software that receive instructions, issue instructions, control operation, enable cleaning operations, enable endpoint measurements, and the like. The integrated circuits may include chips in the form of firmware that store program instructions, digital signal processors (DSPs), chips defined as application specific integrated circuits (ASICs), and/or one or more microprocessors, or microcontrollers that execute program instructions (e.g., software). Program instructions may be instructions communicated to the controller in the form of various individual settings (or program files), defining operational parameters for carrying out a particular process on or for a semiconductor wafer or to a system. The operational parameters may, in some embodiments, be part of a recipe defined by process engineers to accomplish one or more processing steps during the fabrication of one or more layers, materials, metals, oxides, silicon, silicon dioxide, surfaces, circuits, and/or dies of a wafer.

[0102] The controller, in some implementations, may be a part of or coupled to a computer that is integrated with the system, coupled to the system, otherwise networked to the system, or a combination thereof. For example, the controller may be in the "cloud" or all or a part of a fab host computer system, which can allow for remote access of the wafer processing. The computer may enable remote access to the system to monitor current progress of fabrication operations, examine a history of past fabrication operations, examine trends or performance metrics from a plurality of fabrication operations, to change parameters of current processing, to set processing steps to follow a current processing, or to start a new process. In some examples, a remote computer (e.g. a server) can provide process recipes to a system over a network, which may include a local network or the Internet. The remote computer may include a user interface that enables entry or programming of parameters and/or settings, which are then communicated to the system from the remote computer. In some examples, the controller receives instructions in the form of data, which specify parameters for each of the processing steps to be performed during one or more operations. It should be understood that the parameters may be specific to the type of process to be performed and the type of tool that the controller is configured to interface with or control. Thus as described above, the controller may be distributed, such as by comprising one or more discrete controllers that are networked together and working towards a common purpose, such as the processes and controls described herein. An example of a distributed controller for such purposes would be one or more integrated circuits on a chamber in communication with one or more integrated circuits located remotely

(such as at the platform level or as part of a remote computer) that combine to control a process on the chamber.

[0103] Without limitation, example systems may include a plasma etch chamber or module, a deposition chamber or module, a spin-rinse chamber or module, a metal plating chamber or module, a clean chamber or module, a bevel edge etch chamber or module, a physical vapor deposition (PVD) chamber or module, a chemical vapor deposition (CVD) chamber or module, an atomic layer deposition (ALD) chamber or module, an atomic layer etch (ALE) chamber or module, an ion implantation chamber or module, a track chamber or module, and any other semiconductor processing systems that may be associated or used in the fabrication and/or manufacturing of semiconductor wafers.

[0104] As noted above, depending on the process step or steps to be performed by the tool, the controller might communicate with one or more of other tool circuits or modules, other tool components, cluster tools, other tool interfaces, adjacent tools, neighboring tools, tools located throughout a factory, a main computer, another controller, or tools used in material transport that bring containers of wafers to and from tool locations and/or load ports in a semiconductor manufacturing factory.

CLAIMS

What is claimed is:

1. A method of forming ferroelectric hafnium oxide (HfO_2) in a substrate processing system, the method comprising:

arranging a substrate within a processing chamber of the substrate processing system;

depositing an HfO_2 layer on the substrate;

performing a plasma treatment of the HfO_2 layer; and

annealing the HfO_2 layer to form ferroelectric hafnium HfO_2.

2. The method of claim 1, wherein the HfO_2 layer is deposited using atomic layer deposition (ALD).

3. The method of claim 1, further comprising doping the HfO_2 layer.

4. The method of claim 3, wherein doping the HfO_2 layer includes doping the HfO_2 layer with at least one of silicon, aluminum, yttria, lanthanum, and zirconium.

5. The method of claim 3, wherein doping the HfO_2 layer includes doping the HfO_2 layer with between 0 and 5 mol % of a dopant species.

6. The method of claim 1, wherein depositing the HfO_2 layer includes alternating cycles of depositing HfO_2 onto the substrate and doping the deposited HfO_2.

7. The method of claim 1, wherein a thickness of the HfO_2 layer is between 6 and 12 nm.

8. The method of claim 1, further comprising alternating cycles of depositing the HfO_2 layer and performing the plasma treatment of the HfO_2 layer.

9. The method of claim 1, wherein performing the plasma treatment includes using at least one plasma gas species to perform the plasma treatment, wherein the at least one plasma gas species includes at least one of molecular nitrogen (N_2), ammonia (NH_3), molecular oxygen (O_2), ozone (O_3), argon (Ar), and argon and molecular hydrogen (Ar/H_2).

10. The method of claim 1, wherein performing the plasma treatment includes performing the plasma treatment with molecular nitrogen (N_2), and wherein performing the plasma treatment with N_2 causes HfO_xN_y to form on a surface of the HfO_2 layer.

11. The method of claim 1, wherein performing the plasma treatment includes performing the plasma treatment for between 15 and 60 seconds.

12. The method of claim 1, wherein performing the plasma treatment includes performing the plasma treatment at a radio frequency (RF) power between 500 and 1200 watts.

13. The method of claim 12, wherein the RF power is provided at between 1 and 15 MHz.

14. The method of claim 1, wherein annealing the HfO_2 layer includes annealing the HfO_2 layer at a temperature between 500 and 1100 °C.

15. The method of claim 1, wherein annealing the HfO_2 layer includes annealing the HfO_2 layer at a temperature between 800 and 1000 °C.

16. The method of claim 1, further comprising depositing a top electrode on the HfO_2 layer prior to the annealing.

17. The method of claim 16, wherein the top electrode comprises at least one of tantalum nitride, titanium nitride, and tungsten.

18. The method of claim 1, wherein depositing the HfO_2 layer on the substrate includes depositing the HfO_2 layer on one of an underlying layer and a bottom electrode formed on the substrate.

19. A method of treating a substrate including ferroelectric hafnium oxide (HfO_2) in a substrate processing system, the method comprising:

arranging a substrate within a processing chamber of the substrate processing system, wherein the substrate includes an insulator layer;

performing at least one of a thermal treatment and a plasma treatment of the insulator layer;

depositing an HfO_2 layer on the insulator layer; and

annealing the HfO_2 layer to form ferroelectric hafnium HfO_2.

20. The method of claim 19, wherein the insulator layer includes one of silicon dioxide (SiO_2) and silicon oxynitride (SiON).

21. The method of claim 19, wherein performing the at least one of the thermal treatment and the plasma treatment includes sequentially performing the thermal treatment and the plasma treatment.

22. The method of claim 19, wherein performing the at least one of the thermal treatment and the plasma treatment includes increasing a temperature of the substrate to between 200 and 600 °C for 1 to 30 minutes.

23. The method of claim 19, wherein performing the at least one of the thermal treatment and the plasma treatment includes providing at least one of N_2, N_2/H_2, NH_3, O_2, and O_3 to the processing chamber.

24. The method of claim 19, further comprising performing a plasma treatment of the HfO_2 layer.

25. The method of claim 19, wherein the HfO_2 layer is deposited using atomic layer deposition (ALD).

26. The method of claim 19, further comprising doping the HfO_2 layer.

27. A method of treating a substrate including ferroelectric hafnium oxide (HfO_2) in a substrate processing system, the method comprising:

arranging a substrate within a processing chamber of the substrate processing system, wherein the substrate includes an insulator layer;

depositing at least one first HfO_2 layer on the insulator layer;

performing at least one of a thermal treatment and a plasma treatment of the at least one first HfO_2 layer;

depositing at least one second HfO_2 layer on the at least one first HfO_2 layer; and

annealing the at least one second HfO_2 layer and the at least one first HfO_2 layer to form a ferroelectric hafnium HfO_2 layer.

28. The method of claim 27, wherein the insulator layer includes one of silicon dioxide (SiO_2) and silicon oxynitride (SiON).

29. The method of claim 27, wherein performing the at least one of the thermal treatment and the plasma treatment includes sequentially performing the thermal treatment and the plasma treatment.

30. The method of claim 27, wherein performing the at least one of the thermal treatment and the plasma treatment includes increasing a temperature of the substrate to between 200 and 600 °C for 1 to 30 minutes.

31. The method of claim 27, wherein performing the at least one of the thermal treatment and the plasma treatment includes providing at least one of N_2, N_2/H_2, NH_3, O_2, and O_3 to the processing chamber.

32. The method of claim 27, wherein the at least one first HfO_2 layer is deposited in accordance with a dose time that is greater than a dose time used to deposit the at least one second HfO_2 layer.

33. The method of claim 27, further comprising performing at least one of a thermal treatment and a plasma treatment of the insulator layer prior to depositing the at least one first HfO_2 layer.

34. The method of claim 27, wherein the at least one first HfO_2 layer and the at least one second HfO_2 layer are deposited using atomic layer deposition (ALD).

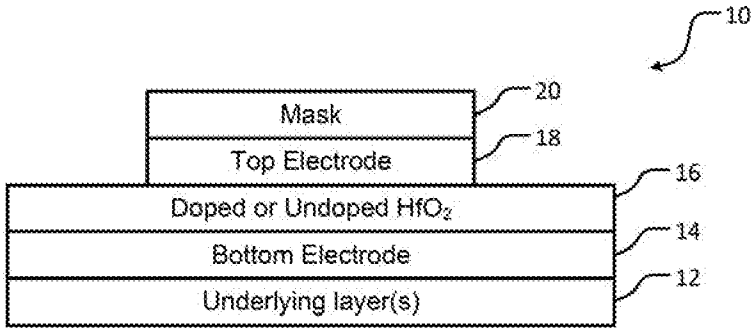
10
20
Mask
18
Top Electrode
16
Doped or Undoped HfO_2
14
Bottom Electrode
12
Underlying layer(s)

FIG. 1A

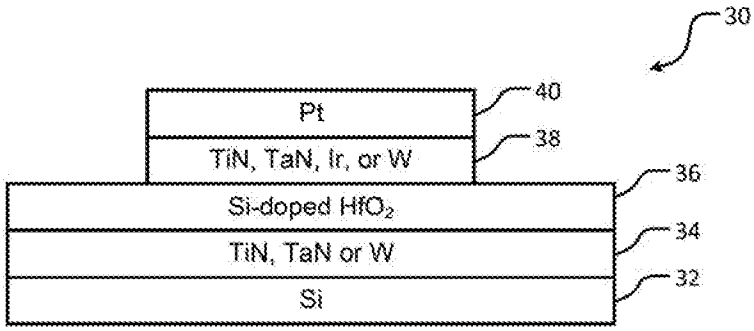
30
40
Pt
38
TiN, TaN, Ir, or W
36
Si-doped HfO_2
34
TiN, TaN or W
32
Si

FIG. 1B

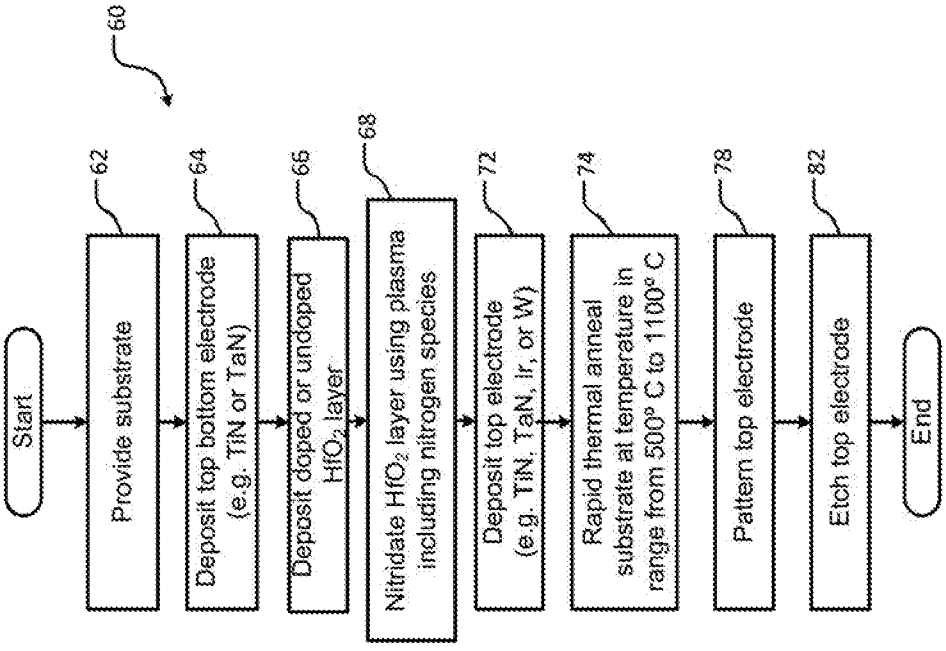
60
Start
62
Provide substrate
64
Deposit top bottom electrode (e.g. TiN or TaN)
66
Deposit doped or undoped HfO_2 layer
68
Nitridate HfO_2 layer using plasma including nitrogen species
72
Deposit top electrode (e.g. TiN, TaN, Ir, or W)
74
Rapid thermal anneal substrate at temperature in range from 500° C to 1100° C
78
Pattern top electrode
82
Etch top electrode
End

FIG. 2

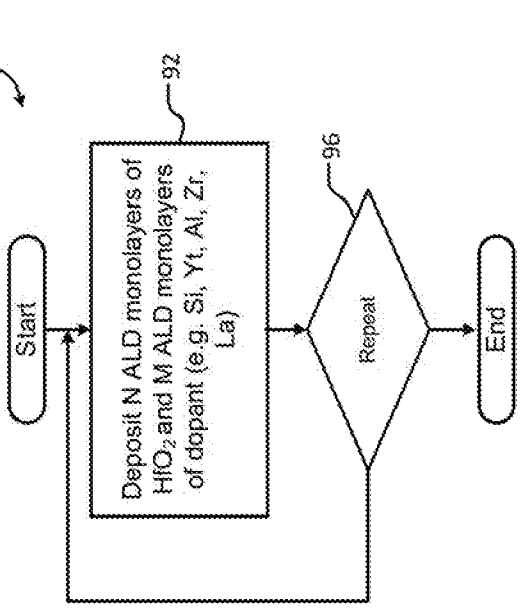
90
Start
92
Deposit N ALD monolayers of HfO_2 and M ALD monolayers of dopant (e.g. Si, Yt, Al, Zr, La)
96
Repeat
End

FIG. 3

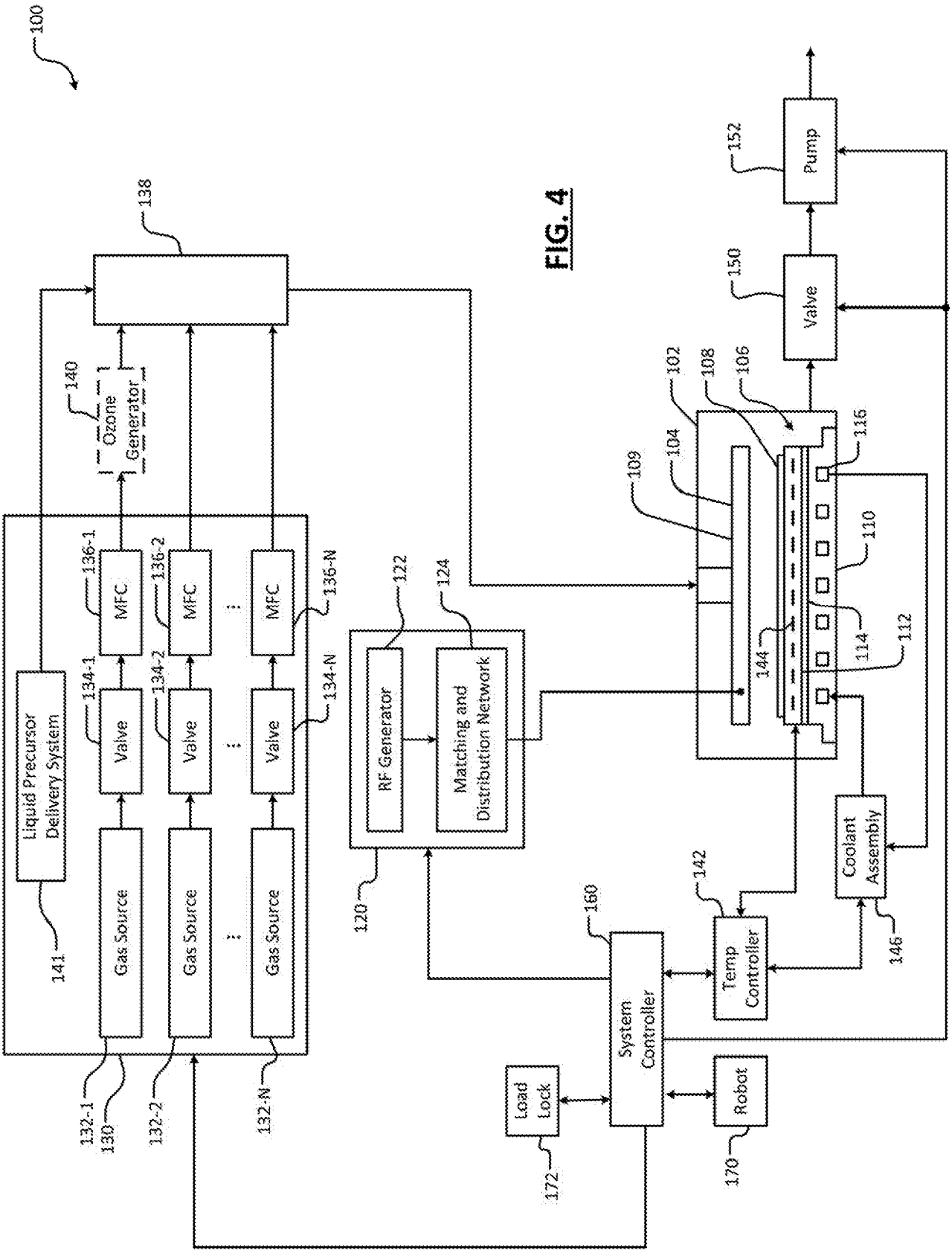
100
138
140
Ozone Generator
136-1
MFC
136-2
MFC
136-N
MFC
134-1
Valve
134-2
Valve
134-N
Valve
Liquid Precursor Delivery System
141
Gas Source
Gas Source
Gas Source
132-1
130
132-2
132-N
122
RF Generator
124
Matching and Distribution Network
120
102
108
106
104
109
116
110
114
112
144
150
Valve
152
Pump
Coolant Assembly
146
142
Temp Controller
160
System Controller
Load Lock
172
Robot
170

FIG. 4

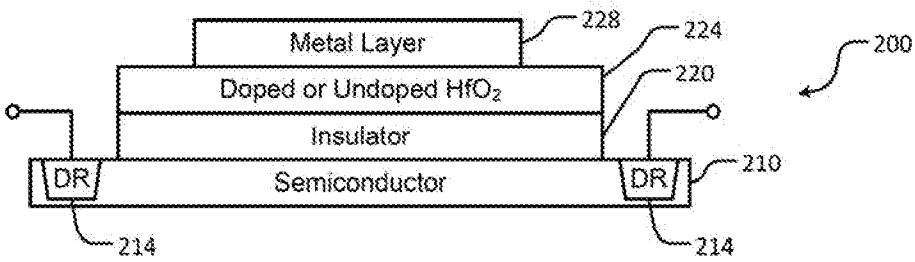
Metal Layer
228
224
200
Doped or Undoped HfO_2
220
Insulator
DR
Semiconductor
DR
210
214
214

FIG. 5

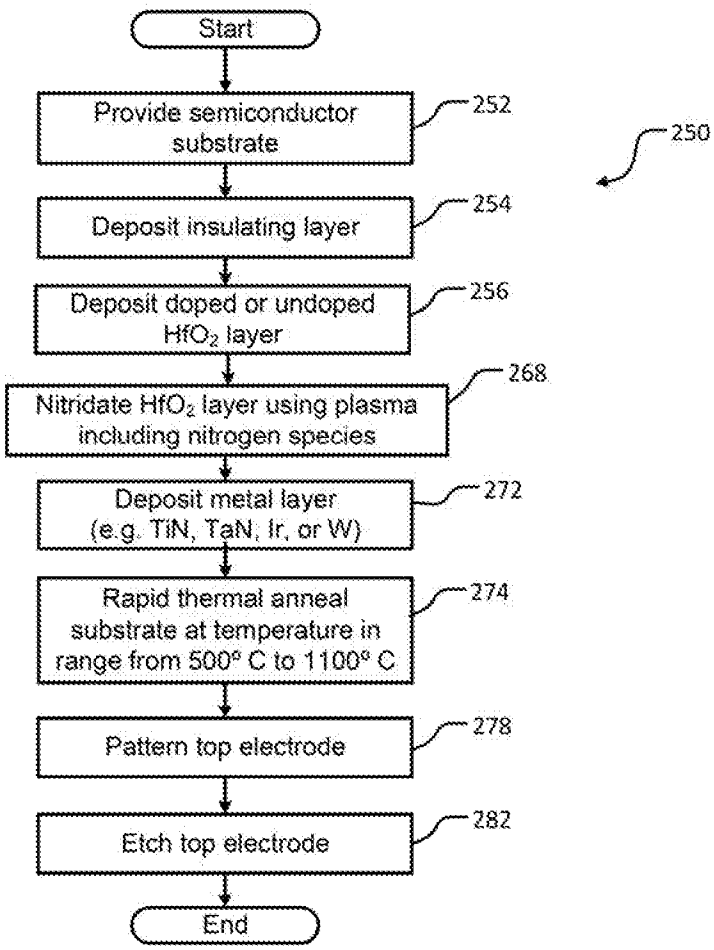
Start
Provide semiconductor substrate
252
250
Deposit insulating layer
254
Deposit doped or undoped HfO_2 layer
256
Nitridate HfO_2 layer using plasma including nitrogen species
268
Deposit metal layer (e.g. TiN, TaN, Ir, or W)
272
Rapid thermal anneal substrate at temperature in range from 500° C to 1100° C
274
Pattern top electrode
278
Etch top electrode
282
End

FIG. 6

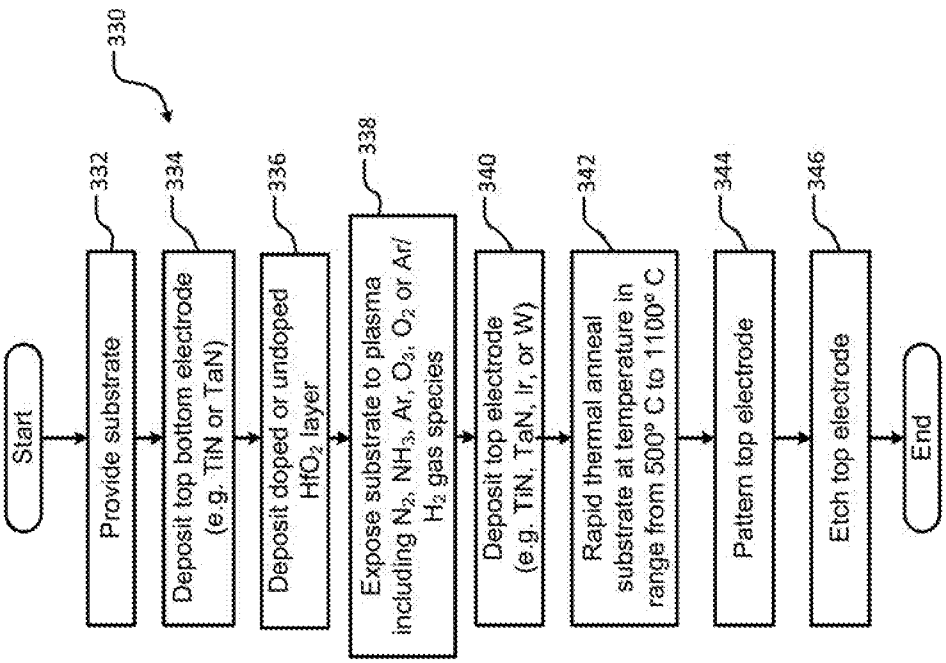
330
Start
Provide substrate
332
Deposit top bottom electrode (e.g. TiN or TaN)
334
Deposit doped or undoped HfO_2 layer
336
Expose substrate to plasma including N_2, NH_3, Ar, O_3, O_2 or Ar/H_2 gas species
338
Deposit top electrode (e.g. TiN, TaN, Ir, or W)
340
Rapid thermal anneal substrate at temperature in range from 500° C to 1100° C
342
Pattern top electrode
344
Etch top electrode
346
End

FIG. 7

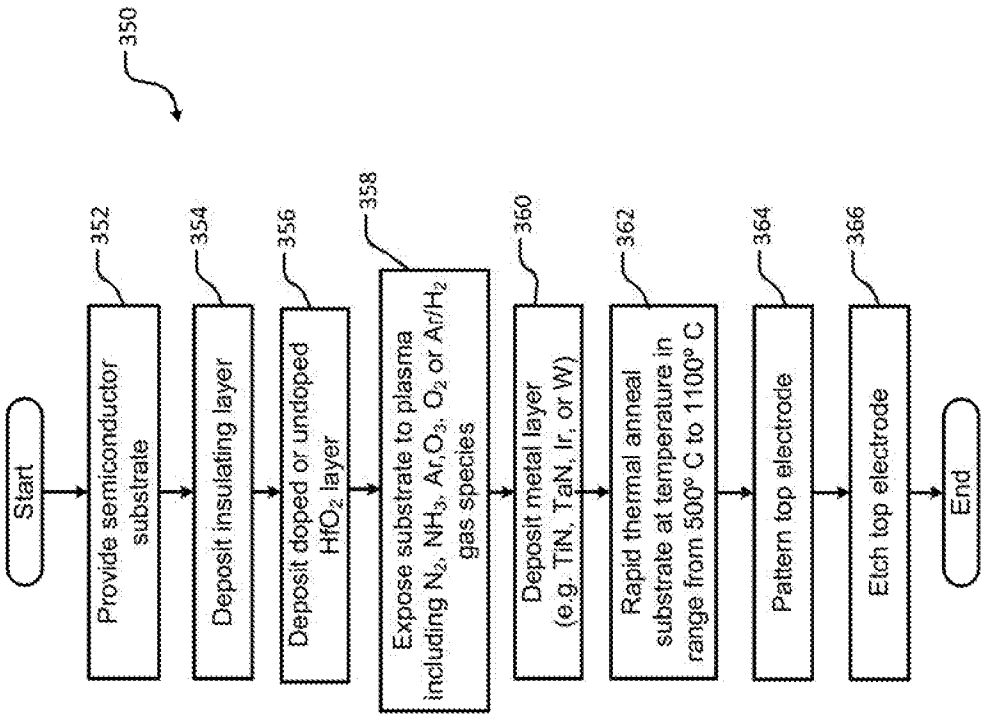
350
Start
Provide semiconductor substrate
352
Deposit insulating layer
354
Deposit doped or undoped HfO_2 layer
356
Expose substrate to plasma including N_2, NH_3, Ar,O_3, O_2 or Ar/H_2 gas species
358
Deposit metal layer (e.g. TiN, TaN, Ir, or W)
360
Rapid thermal anneal substrate at temperature in range from 500° C to 1100° C
362
Pattern top electrode
364
Etch top electrode
366
End

FIG. 8

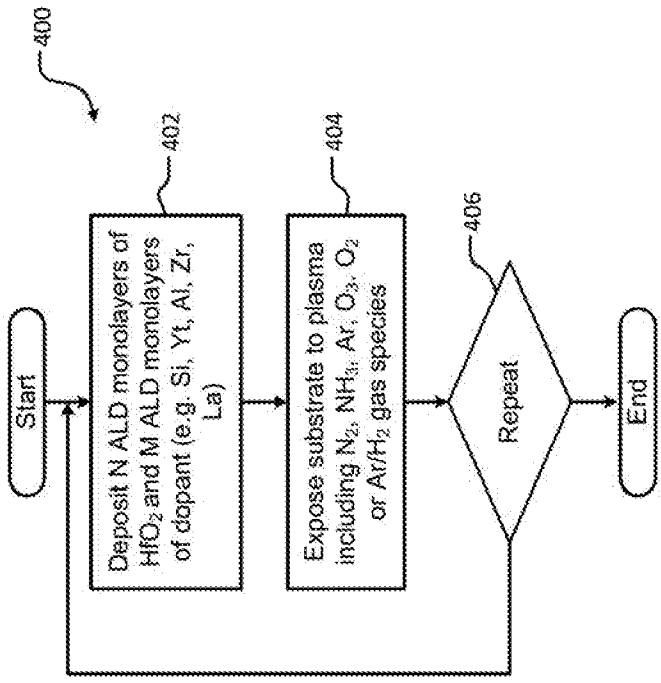
400
Start
Deposit N ALD monolayers of HfO_2 and M ALD monolayers of dopant (e.g. Si, Yt, Al, Zr, La)
402
Expose substrate to plasma including N_2, NH_3, Ar, O_3, O_2 or Ar/H_2 gas species
404
Repeat
406
End

FIG. 9

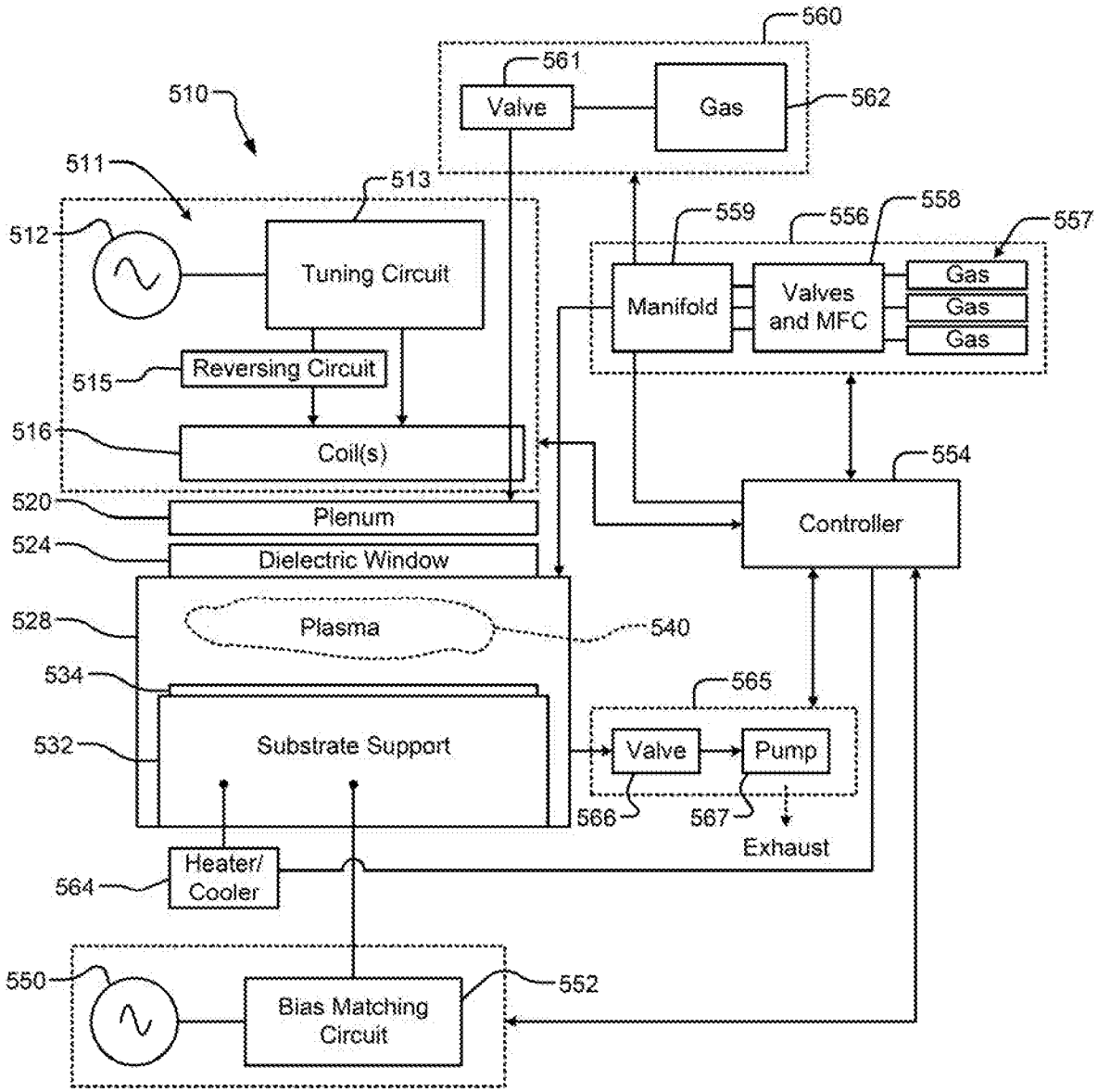
560
561
Valve
Gas
562
510
511
513
512
Tuning Circuit
559
556
558
557
Manifold
Valves and MFC
Gas
Gas
Gas
515
Reversing Circuit
516
Coil(s)
554
520
Plenum
Controller
524
Dielectric Window
528
Plasma
540
534
565
532
Substrate Support
Valve
Pump
566
567
Exhaust
Heater/ Cooler
564
550
Bias Matching Circuit
552

FIG. 10

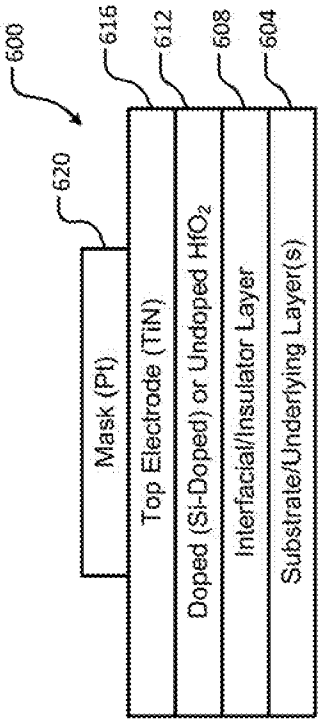

FIG. 11D

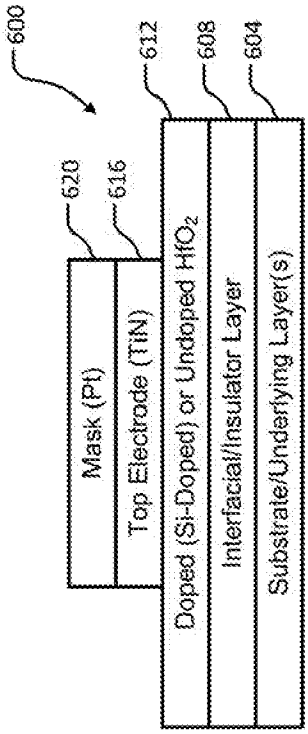

FIG. 11E

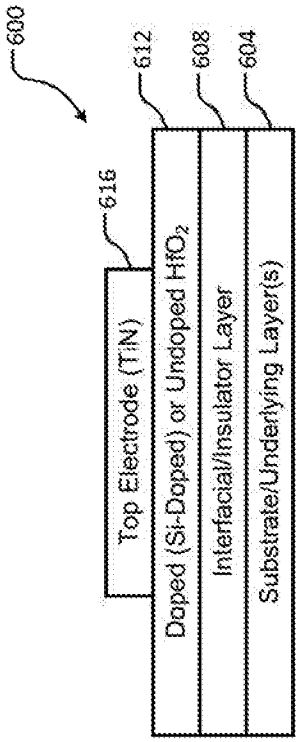

FIG. 11F

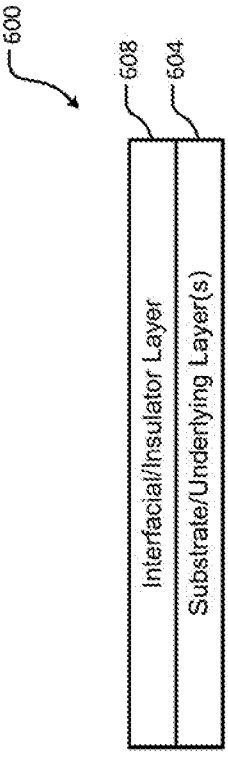

FIG. 11A

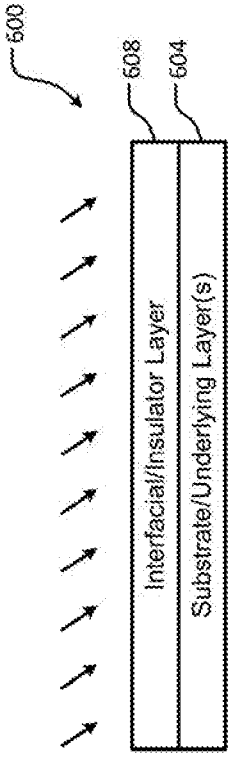

FIG. 11B

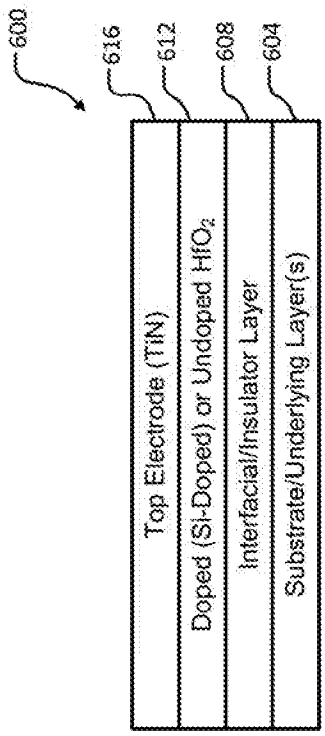

FIG. 11C

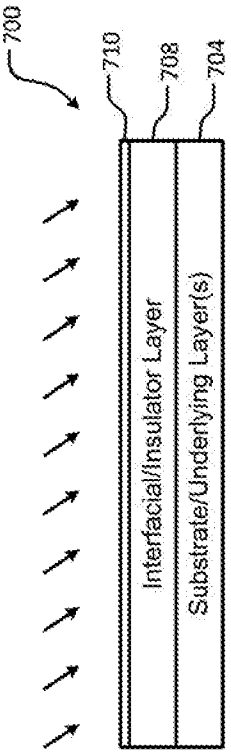

FIG. 12A

FIG. 12D

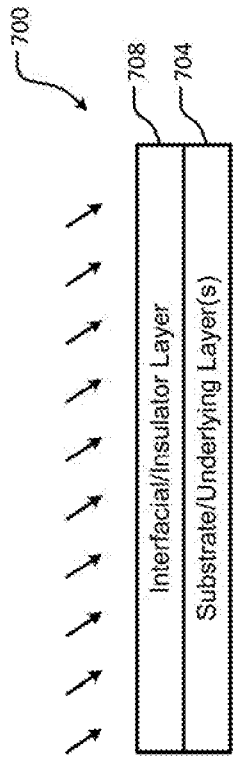

FIG. 12B

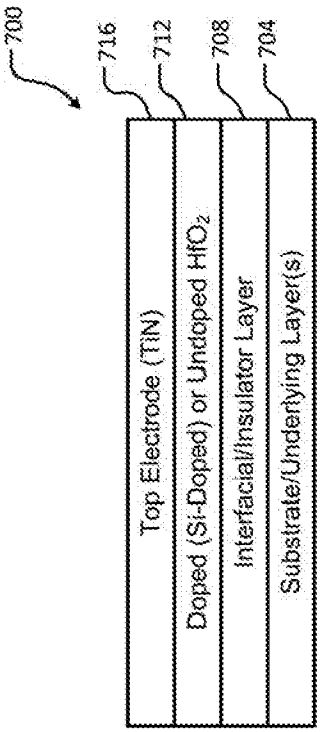

FIG. 12E

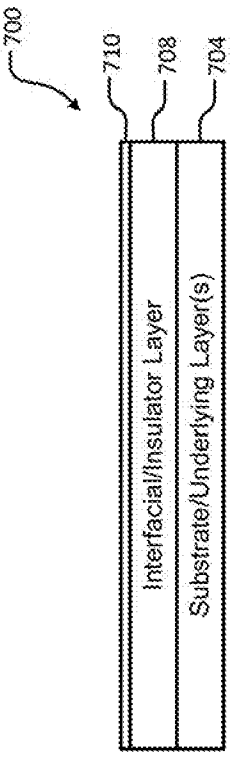

FIG. 12C

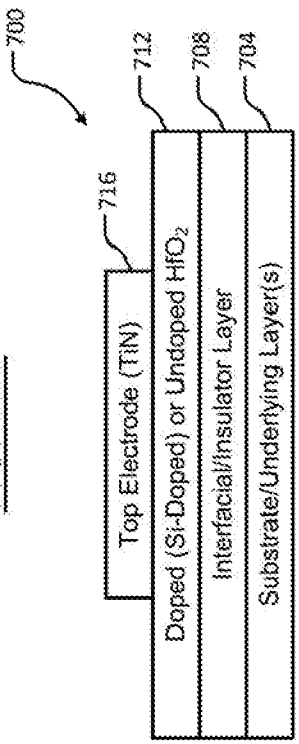

FIG. 12F

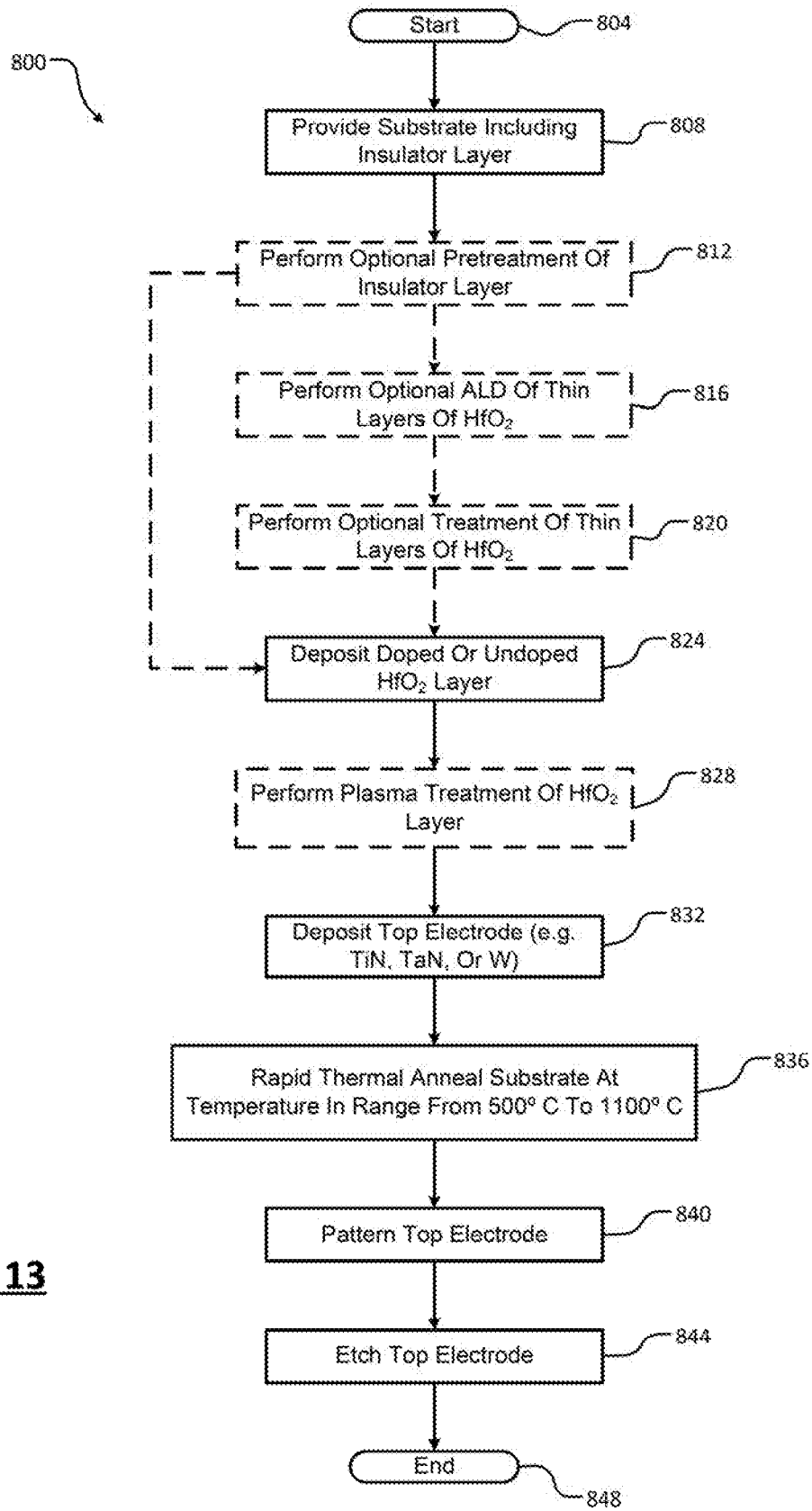
800
Start
804
Provide Substrate Including Insulator Layer
808
Perform Optional Pretreatment Of Insulator Layer
812
Perform Optional ALD Of Thin Layers Of HfO_2
816
Perform Optional Treatment Of Thin Layers Of HfO_2
820
Deposit Doped Or Undoped HfO_2 Layer
824
Perform Plasma Treatment Of HfO_2 Layer
828
Deposit Top Electrode (e.g. TiN, TaN, Or W)
832
Rapid Thermal Anneal Substrate At Temperature In Range From 500° C To 1100° C
836
Pattern Top Electrode
840
Etch Top Electrode
844
End
848

FIG. 13

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2018/045771

A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/02(2006.01)i, H01L 21/324(2006.01)i, H01L 21/28(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 21/02; C23C 16/00; H01L 21/314; H01L 21/316; H01L 21/324; H01L 21/28

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: ferroelectric, hafnium oxide, plasma, nitrogen, anneal, ALD

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 2007-024493 A1 (APPLIED MATERIALS, INC.) 01 March 2007 See paragraphs [0020], [0026], [0032]-[0036], claims 1, 8, 15 and figure 3.	1-7,9-18
Y		8,24,25
A		19-23,26-34
X	SEOKHOON KIM et al. "Atomic Layer Deposition of HfO2 Thin Films on Ultrathin SiO2 Formed by Remote Plasma Oxidation" Journal of the Korean Physical Society, Vol. 52, No. 4, April 2008, pp 1103-1108 See pages 1103-1105 and figure 4.	19-23,26
Y		8,24,25
A	M. LIU et al. "Characterization of HfOxNy gate dielectrics using a hafnium oxide as target" Applied Surface Science 252, 18 January 2006 (online), pp 8673-8676 See pages 8673-8674.	1-34
A	US 2015-0279665 A1 (ULTRATECH, INC.) 01 October 2015 See claims 1-5 and figures 1-2.	1-34
A	US 2005-0271813 A1 (SHREYAS KHER et al.) 08 December 2005 See claims 1-10 and figures 1, 3-4.	1-34

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
28 November 2018 (28.11.2018)	**28 November 2018 (28.11.2018)**

Name and mailing address of the ISA/KR
International Application Division
Korean Intellectual Property Office
189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea
Facsimile No. +82-42-481-8578

Authorized officer
CHOI, Sang Won
Telephone No. +82-42-481-8291

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2018/045771

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
WO 2007-024493 A1	01/03/2007	JP 2009-506537 A	12/02/2009
		KR 10-2008-0046647 A	27/05/2008
		TW 200739726 A	16/10/2007
		US 2007-0049043 A1	01/03/2007
US 2015-0279665 A1	01/10/2015	CN 105177527 A	23/12/2015
		FI 20155099 A	27/09/2015
		JP 2015-188065 A	29/10/2015
		KR 10-2015-0111831 A	06/10/2015
		US 9583337 B2	28/02/2017
US 2005-0271813 A1	08/12/2005	CN 101052745 A	10/10/2007
		CN 101052745 B	23/02/2011
		CN 1934287 A	21/03/2007
		CN 1934287 B	20/06/2012
		EP 1745159 A2	24/01/2007
		EP 1745160 A1	24/01/2007
		JP 2007-537360 A	20/12/2007
		JP 2007-537605 A	20/12/2007
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