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Description

The present invention relates to a digital-to-analog converter (to be referred to as a DA converter hereinafter) which converts a digital signal into an analog signal (dc signal) of a corresponding magnitude and, more particularly, to a PWM-type DA converter which is improved in conversion speed and which is capable of effectively attenuating the ripple components of the pulse width modulated (PWM) waves.

According to a general PWM-type DA converter, an input digital signal to be converted is compared with a reference digital signal which changes in magnitude within one period. Based on the comparison result obtained, a pulse signal (PWM wave) of the pulse width corresponding to the magnitude of the input digital signal is generated. This PWM wave is smoothed to obtain an output analog signal. A DA converter of this type has an advantage in that the conversion precision can be easily improved if the number of bits of the reference digital signal is increased. The PWM-type DA converter is, therefore, widely adopted especially in servo control of motors since it is easily integrated. However, the PWM-type DA converter is also subject to disadvantages. For example, the output dc signal is determined only one period after the reference digital signal. Since the input signal is passed through a low-pass filter for the purpose of smoothing, the conversion speed is slower than that obtainable with DA converters of other types. Furthermore, the smoothing is insufficient and the ripple components tend to be included in the output signal.

US—A—4 096 475 discloses a DA converter which compares N-bit digital data to be converted with a reference digital value changing within a conversion period to generate pulses of a pulse width corresponding to the value of the N-bit data according to the comparison results; the pulses are smoothed to obtain a DC output. The DA converter comprises digital value string generating means in the form of an N-bit binary counter which counts clock pulses. The n lower significant bits of the counter output are fed to the inputs for the n upper significant bits of an N-bit comparator. The (N–n) upper significant bits of the counter output are fed in inverted order to the inputs of the (N–n) lower significant bits of the comparator.

It is an object of the present invention to provide a DA converter which is capable of improving the conversion speed and which is capable of producing dc outputs of good quality by effectively attenuating the ripple components of the PWM waves.

According to the present invention, there is provided a DA converter for comparing N-bit digital data to be converted with a reference digital value changing within a conversion period to generate pulses of a pulse width corresponding to a value of the N-bit data according to the comparison results, and smoothing the pulses to obtain a dc output, said converter comprising:—

digital value string generating means for counting pulses of a predetermined frequency to generate a plurality of digital value strings to be compared with the digital data within one conversion period, each said string generated within the conversion period having a different weighting; and

N-bit comparing means, connected to said digital value string generating means, for sequentially comparing each of the plurality of digital value strings with the digital data so as to output a number of pulses in a conversion period corresponding in number to the number of the digital value strings; characterised in that said digital value string generating means comprises an N-bit ($n+1<N$) binary counter for counting the pulses of the predetermined frequency to sequentially generate binary numbers; a detection circuit which is connected to said n-bit binary counter, which detects if a count of said n-bit binary counter has reached first and second preset numbers, and which outputs a count pulse when the count of said n-bit binary counter reaches the first preset number and outputs a latch signal when the count of said n-bit binary counter reaches the second preset number; and an (N–n) bit binary counter which is connected to said detection circuit and which increments a count by one when the count pulse is received, said n-bit binary counter supplying an output thereof to upper significant ($N-n+1$)th to Nth bits of said N-bit comparing means, and the contents of said ($N-n$) bit binary counter being supplied in reversed order of significance to the least significant bit to ($N-n$)th bits of said N-bit comparing means.

Exemplary embodiments will now be described with reference to the accompanying drawings in which:—

Figures 1(A) and 1(B) show waveforms for explaining the conversion principle of a conventional DA converter;

Figures 2(A) and 2(B) show waveforms for explaining the conversion principle of a known DA converter;

Figure 3 is a circuit diagram of a known DA converter using the principle of Figures 2(A) and 2(B);

Figures 4(A) and 4(B) are views for explaining the mode of operation of the DA converter shown in Figure 3;

Figure 5 is a circuit diagram of a DA converter according to the present invention;

Figures 6(A), 6(B) and 6(C) show waveforms for explaining the mode of operation of the DA converter shown in Figure 5;

Figure 7 is a circuit diagram of another DA converter according to the present invention;

Figure 8 is a circuit diagram of still another DA converter according to the present invention;

Figures 9(A), 9(B) and 9(C) show waveforms for explaining the mode of operation of the DA converter shown in Figure 8; and

Figure 10 is a circuit diagram of yet another DA converter according to the present invention.

The present invention will now be described in detail with reference to the accompanying drawings.

A known principle of DA conversion will first be described with reference to Figures 1(A), 1(B), 2(A) and 2(B). Figures 1(A) and 1(B) show the waveforms for explaining the conversion principle of a prior art DA converter. According to this DA converter, digital value strings (indicated by staircase wave I) sequentially generated within a conversion period W0 are compared with input digital data (indicated by line II). Based on the comparison result obtained, PWM waves of pulse width W are generated within regions wherein the staircase wave I is smaller (or greater) in magnitude than line II. By smoothing the PWM waves, dc signals proportional to W/W0 are obtained. In contrast with this, in the principle of DA conversion shown in Figures 2(A) and 2(B), n strings of digital values (indicated by staircase waves I1, I2, . . ., In) are sequentially generated within the conversion period W0. These digital value strings are compared with the input digital data (indicated by line II). Pulse signals of a predetermined pulse width are generated within regions wherein the staircase waves I1, I2, . . ., In are smaller (or greater) in magnitude than line II. It is to be noted that these staircase waves I1, I2, . . ., In are generated in correspondence with the digital values of the staircase wave I shown in Figure 1(A) and respectively have different weights. These staircase waves are generated as dispersed. With the DA converter of the configuration as described above, the cut-off frequency of the low-pass filter for smoothing the PWM waves can be made sufficiently high since n pulses are generated within one conversion period.

The DA converter of Figure 3 is similar to US—A—4 096 475 and has a 10-bit binary counter 10 of up-counter type which receives clock pulses CK of a predetermined frequency, a comparator 12 which compares two binary numbers and produces an output representing which one of the two binary numbers is greater or smaller, a 10-bit register 14 for temporarily storing 10-bit digital data DD to be converted, and a smoothing circuit 15 comprising, for example, a low-pass filter for smoothing the pulse signals generated by the comparator 12. The 10-bit binary counter 10 counts the received clock pulses CK and generates a 10-bit binary number which is sequentially incremented. When each bit of the 10-bit binary number is represented by Q0, Q1, . . ., Q9 from the least significant bit (to be referred to as LSB hereinafter), the lower six significant bits Q0, Q1, . . ., Q5 are applied to the upper six significant bits of the comparator 12 in this order whereas the upper four significant bits Q6 to Q9 are inverted in order and are applied to the lower four significant bits of the comparator 12. Then, the binary number input to the comparator 12 may be given as:

$$Q9\times2^0+Q8\times2^1+Q7\times2^2+Q6\times2^3+Q0\times2^4+$$

$$Q1\times2^5+Q2\times2^6+Q3\times2^7+Q4\times2^8+Q^5\times2^9$$

$$=(Q9\times2^0+Q8\times2^1+Q7\times2^2+Q6\times2^3)+$$

$$2^4(Q0\times2^0+Q1\times2^1+Q2\times2^2+Q3\times2^3+Q4\times$$

$$2^4+Q5\times2^5)$$

This binary number defines 2^4 binary number strings of 2^6 steps with one step corresponding to 2^4 (the binary number strings are indicated by staircase waves I1 to I16). These binary number strings respectively have different weights

$$(Q9\times2^0+Q8\times2^1+Q7\times2^7+Q6\times2^3).$$

These weights are shown in Table 1 below based upon the relations with bits Q6 to Q9.

TABLE 1

Q9	Q8	Q7	Q6	Decimal number	Q6	Q7	Q8	Q9	Decimal number	
0	0	0	0	0	0	0	0	0	0	
0	0	0	1	1	1	0	0	0	8	
0	0	1	0	2	0	1	0	0	4	
0	0	1	1	3	1	1	0	0	12	o
0	1	0	0	4	0	0	1	0	2	
0	1	0	1	5	1	0	1	0	10	
0	1	1	0	6	0	1	1	0	6	
0	1	1	1	7	1	1	1	0	14	o
1	0	0	0	8	0	0	0	1	1	
1	0	0	1	9	1	0	0	1	9	
1	0	1	0	10	0	1	0	1	5	
1	0	1	1	11	1	1	0	1	13	o
1	1	0	0	12	0	0	1	1	3	
1	1	0	1	13	1	0	1	1	11	o
1	1	1	0	14	0	1	1	1	7	
1	1	1	1	15	1	1	1	1	15	o

Thus, the values from the LSB to the fourth bit input to the comparator 12 are such that the orders of decimal numbers 0 to 15 are dispersed at maximum as shown in the right column of Table 1 above. On the other hand, the digital data DD to be converted is temporarily stored in the 10-bit register 14 and supplied to the comparator 12 in response to a load signal LA. The comparator 12 sequentially compares the digital data DD with the binary number strings supplied from the binary counter 10 and produces the comparison outputs. Some comparison outputs produced by the comparator 12 differ by one step from other comparison outputs according to the weights of the binary number strings to be compared with the digital data DD. For example, when the digital data DD to be converted is

$$555=2^9+2^5+2^3+2^1+2^0=11+2^4\times34,$$

the binary number string reaches the value of the digital data DD, 555, at the 34th step when the weight is 11. Therefore, the comparison outputs are produced by the comparator 12 within the range of 34 steps for the binary number string whose weight exceeds 11. On the other hand, the comparison outputs are produced by the comparator 12 within the range of (34+1) steps for the binary number string whose weight is 11 or less. Thus, the comparison outputs from the comparator 12 are produced in correspondence with (34+1), (34+1), (34+1), 34, (34+1), (34+1), (34+1), 34, (34+1), (34+1), (34+1), 34, (34+1) and 34 steps in the example shown in Table 1. In Table 1, weights with which outputs are obtained in correspondence with 34 steps are indicated with symbol o. Thus, most of the comparison outputs (pulse train) are produced by the comparator 12 over the range of 35 steps; the comparison output are produced over the range of 34 steps at the positions of maximum dispersion in this pulse train within the conversion period. As may be apparent from the above description, the pulse widths only differ in correspondence with one step. Since one step is a very small difference equivalent to the LSB of the digital data to be converted, the pulse widths are nearly equal to each other. The pulse train obtained in this manner is supplied to the smoothing circuit 15. The smoothing circuit 15 converts the PWM wave into a dc output from which the ripple components are effectively attenuated.

In this case, pulses of a pulse width having data of $35/2^6=0.546875$ (100.9%) for a DA conversion true

value of $555/2^{10}=0.541992$ are obtained within a duration of 1/16 the conversion period. Apart from this, a correction of the pulse width by $-1/2^6$ per 1/4 duration of the conversion period

$$(-1/2^6\times 1/4=-0.00391\ (-0.7\%))$$

is considered to be performed with a further correction by $-1/2^6$ of the pulse width per conversion period, i.e.,

$$-1/2^6\times 1/16=-0.00098\ (-0.2\%).$$

When this correction is performed, a DA conversion of $555/2^{10}$ per conversion period is obtained with high accuracy.

In this arrangement, a dc output signal close to an objective value is obtained per duration which is 1/16 the conversion period. At the same time, a correction equivalent to the LSB of the data to be converted is of small fraction and effectively dispersed within one conversion period. Therefore, the conversion speed becomes faster than that of the conventional DA converters. Furthermore, the cut-off frequency of the smoothing circuit (low-pass filter) 15 for smoothing the PWM waves can be made nearly 16 times that with the conventional DA converter. In addition, the ripple components of the PWM waves can be effectively attenuated so that a dc output of good quality may be obtained.

In this converter, the weights of the binary number strings are generated within one period of the staircase wave. However, the present invention is not limited to this. Thus, similar effects may be obtained by generating the weights over a duration of two periods.

The embodiment of the present invention as shown in Figure 5 achieves this. The same reference numerals in Figure 5 as those in Figure 3 denote the same parts. The DA converter of this embodiment comprises a 6-bit binary counter 16 for receiving the clock pulse CK, a 4-bit binary counter 18, a latch circuit 20 for latching the output from the 4-bit binary counter 18, and a detection circuit 22 which supervises the count of the 6-bit binary counter 16 and which generates a count pulse CP for the 4-bit binary counter 18 and a latch pulse LP for the latch circuit 20. When the staircase waves from the 6-bit binary counter 16 have the period as shown in Figure 6(A), a count pulse CP is generated by the detection circuit 22 after a fixed duration from the beginning of each staircase wave, as shown in Figure 6(B), to increment the count of the 4-bit binary counter 18 by one. A latch pulse LP is generated after another fixed duration from the count pulse CP, as shown in Figure 6(C), to latch the count of the 4-bit binary counter 18 in the latch circuit 20. The bits Q0 to Q5 of the output from the 6-bit binary counter 16 are directly supplied to the upper six significant bits of the 10-bit comparator 12, whereas the latched content in the latch circuit 20 is reversed in the order of bits and supplied to the lower four significant bits of the 10-bit comparator 12. Other details of the arrangement remain the same as those of the converter shown in Figure 3. With this configuration, the weights of the respective staircase waves change when the latch pulses LP are generated by the detection circuit 22; all the weights are generated within one conversion period. As may be easily understood, according to this embodiment, it suffices that the output data from the 4-bit binary counter 18 be established substantially within the period of each staircase wave. Therefore, the operation speed of the 4-bit binary counter 18 may be significantly lowered in comparison with that of the 6-bit binary counter 16. This embodiment has an advantage in manufacture of the DA converter in addition to the advantages obtained with the converter of Figure 3.

Figure 7 shows another embodiment of the present invention. According to this embodiment, a 4-bit comparator 24 for comparing the lower four significant bits and a 6-bit comparator 26 for comparing the upper six significant bits are incorporated in place of the 10-bit comparator 12 shown in Figure 5. The 4-bit comparator 24 first compares the inverted signal of the output signal from the 4-bit binary counter 18 with the lower four significant bits of the binary number to be converted. The comparison output from the 4-bit comparator 24 is latched in a latch circuit 28 in response to the latch pulse LP from the detection circuit 22. The latched content in the latch circuit 28 is supplied to the 6-bit comparator 26. The 6-bit comparator 26 has the priority for producing the comparison output over the 4-bit comparator 24, and the 6-bit comparator 26 receives the comparison output from the 4-bit comparator only when the data to be compared coincide with each other. Since the digital data DD to be converted within the conversion period remains constant, the weights of the respective staircase waves change when the latch pulses are generated by the detection circuit 22 as in the case of the embodiment shown in Figure 5. Therefore, the output PWM waves same as those obtainable with the converter shown in Figure 5 are obtained. The operation speeds of the 4-bit binary counter 18 and the 4-bit comparator 24 can be significantly lowered for the same reason as that described with reference to the converter shown in Figure 5. Thus, the converter of Figure 7 achieves the similar effects to those of the converter of Figure 5.

Figure 8 shows a circuit diagram of an embodiment of the present invention. In Figure 8, the same reference numerals as in Figure 5 denote the same parts.

The embodiment shown in Figure 8 differs from the converter of Figure 3 in the following respects. The 6-bit binary counter 16, the 4-bit binary counter 18 and the latch circuit 20 are incorporated in place of the 10-bit binary counter 10. The 4-bit binary counter 18 is rendered operative in response to the output (count pulse CP) from a detection circuit 50 which detects if the count of the 6-bit binary counter 16 has reached a

predetermined value. The count of the 4-bit binary counter 18 is latched by the latch circuit 20 in response to the output (latch pulse LP) from the detection circuit 50 and is then supplied to the comparator 30. The other configuration remains the same. With the embodiment of this configuration, the operation speed of the 4-bit binary counter 18 can be made significantly lower than that of the 6-bit binary counter 16. As may be seen from the above description, the signal supplied to the comparator remains constant for a duration corresponding to one period of the staircase wave. Therefore, the operation speed of the 4-bit binary counter 18 can be significantly lowered if the count pulse CP for rendering the 4-bit binary counter 18 operative is supplied thereto during the initial period of the staircase wave, and if the count of the 4-bit binary counter 18 is latched in the latch circuit 20 and is supplied to the comparator 30 after the counting operation of the 4-bit binary counter 18 is completed, as shown in Figures 9(A), 9(B) and 9(C). In Figures 9(A), 9(B) and 9(C), the latch pulse LP is generated in synchronism with the leading edge of the staircase wave. However, the latch pulse LP need not be generated in synchronism with the leading edge or the trailing edge of the staircase. The latch pulse LP may be generated at the timing as shown in Figures 6(A), 6(B) and 6(C). Thus, the timing for generating the latch pulse LP may be arbitrarily set. Accordingly, the embodiment of Figure 9 provides the same effects as that of Figure 5.

Figure 10 shows an embodiment of the present invention. According to this embodiment, the latch circuit 28 is connected to the output end of the comparator 30 in place of the latch circuit 20 of the embodiment shown in Figure 8. The output from the comparator 30 is latched in the latch circuit 28 in synchronism with the latch pulse LP output from the detection circuit 50 and is supplied to the delay control circuit 34. Although the mode of operation of the embodiment of Figure 10 is basically the same as that of the embodiment shown in Figure 8, the operation speeds of the 4-bit binary counter 18 and the comparator 30 may be significantly lowered by suitably selecting the timings at which the count pulse CP to be supplied to the 4-bit binary counter 18 and the latch pulse LP to be supplied to the latch circuit 28 are generated. In this manner, the embodiment of Figure 10 also provides the same effects as the embodiment of Figure 5.

The present invention is not limited to the embodiments described above. For example, in the embodiments, the present invention is applied to a 10-bit PWM-type DA converter. However, the present invention can be applied to PWM-type DA converters having any number of bits. In the embodiments described above, the number of bits of each staircase wave and the number of bits of the weight were divided into four and six bits. These bits may be divided in many ways depending upon the purpose. In the embodiments described above, the binary counters comprise up-counters. Therefore, the sawtooth waves were generated as the staircase waves. However, if the binary counters comprise up-down counters, the staircase waves of triangular shape may be obtained. A DA converter of similar effects may be obtained in this case. The binary counters may comprise down-counters or synchronous counters.

Claims

1. A DA converter for comparing N-bit digital data (DD) to be converted with a reference digital value changing within a conversion period to generate pulses of a pulse width corresponding to a value of the N-bit data according to the comparison results, and smoothing the pulses to obtain a dc output, said converter comprising:—

digital value string generating means (10) for counting pulses of a predetermined frequency (CK) to generate a plurality of digital value strings to be compared with the digital data within one conversion period, each said string generated within the conversion period having a different weighting; and

N-bit comparing means (12), connected to said digital value string generating means (10), for sequentially comparing each of the plurality of digital value strings with the digital data so as to output a number of pulses in a conversion period corresponding in number to the number of the digital value strings; characterised in that said digital value string generating means (10) comprises an n-bit ($n+1<N$) binary counter (16) for counting the pulses of the predetermined frequency to sequentially generate binary numbers; a detection circuit (22) which is connected to said n-bit binary counter (16), which detects if a count of said n-bit binary counter (16) has reached first and second preset numbers, and which outputs a count pulse (CP) when the count of said n-bit binary counter (16) reaches the first preset number and outputs a latch signal (LP) when the count of said n-bit binary counter (16) reaches the second preset number; and an (N−n) bit binary counter (18) which is connected to said detection circuit (22) and which increments a count by one when the count pulse (CP) is received, said n-bit binary counter (16) supplying an output thereof to upper significant (N−n+1)th to Nth bits of said N-bit comparing means (12), and the contents of said (N−n) bit binary counter (18) being supplied in reversed order of significance to the least significant bit to (N−n)th bits of said N-bit comparing means.

2. A DA converter according to claim 1, characterised in that said digital value string generating means (10) comprises an (N−n) bit latch circuit (20) which is connected to said detection circuit (22) and to said (N−n) bit binary counter (18) and which latches a count of said (N−n) bit binary counter (18) in response to the latch signal.

3. A DA converter according to claim 1, characterised in that said N-bit comparing means (12) comprises a first comparator (24) for comparing contents of the least significant bit to (N−n)th bit; a latch circuit (28) which is connected to said comparator (24) and said detection circuit (22) and which latches an output from said first comparator (24) in response to the latch signal; and a second comparator (26) which

is connected to said latch circuit (28) and which compares the contents of upper significant (N−n+1)th to Nth bits and produces a comparison output with a priority over an output from said latch circuit (28).

4. A DA converter according to claim 1 or claim 2, characterised in that said detection circuit (50) also detects if a count of said n-bit binary counter (16) has reached a third preset number, and outputs a set signal when the count of said n-bit binary counter (16) reaches the third preset value.

5. A DA converter according to claim 4 as dependent on claim 2, characterised in that said comparing means (12) comprises a comparator (30) for comparing the reversed contents of said latch circuit (20) with the lower (N−n) bits of the N-bit digital data; a coincidence circuit (32) for detecting a coincidence between the contents of said n bit counter (16) with the upper n bits of the N-bit digital data; a delay circuit (34) which is connected to said comparator (30) and said coincidence circuit (32) and which delays an output from said coincidence circuit (32) by one period of the pulses of the predetermined frequency (CK) in response to an output from said comparator (30); and a bistable circuit (46) which is connected to said detection circuit (50) and said delay circuit (34), which is set by the set signal, and which is reset by an output signal from said delay circuit (34).

6. A DA converter according to claim 4 as dependent on claim 1 only, characterised in that said comparing means comprises a comparator (30) for comparing the reversed contents of said (N−n) bit binary counter (18) with the lower (N−n) bits of the N-bit digital data; a latch circuit (28) which is connected to said comparator (30) and said detection circuit (50) and which latches an output from said comparator (30) in response to the latch signal; a coincidence circuit (32) for detecting a coincidence between the contents of said n bit binary counter (16) with the upper n bits of the N-bit digital data; a delay circuit (34) which is connected to said latch circuit (28) and said coincidence circuit (32) and which delays an output from said coincidence circuit (32) by one period of the pulses of the predetermined frequency (CK) in response to an output from said latch circuit (28); and a bistable circuit (46) which is connected to said detection circuit (50) and said delay circuit (34), which is set by the set signal, and which is reset by an output signal from said delay circuit (34).

Patentansprüche

1. Digital-Analog-Wandler zum Vergleichen von zu wandelnden N-Bit Digitaldaten (DD) mit einem Referenzdigitalwert, der sich innerhalb einer Wandlerperiode ändert, um Impulse mit einer Impulsbreite zu erzeugen entsprechend einem Wert der N-Bitdaten gemäß den Vergleichsergebnissen, wobei die Impulse geglättet werden, um ein Gleichstromsignal zu erhalten, wobei der Wandler aufweist:

eine Digitalwertdatengruppen-Erzeugungseinrichtung (10) zum Zählen von Impulsen einer vorbestimmten Frequenz (CK), um eine Vielzahl von Digitalwertdatengruppen zu erzeugen, die mit den digitalen Daten innerhalb einer Wandlerperiode zu vergleichen sind, wobei jede Datenkette, die innerhalb der Wandlerperiode erzeugt wurde, eine unterschiedliche Gewichtung aufweist und eine N-Bitvergleichseinrichtung (12), die mit der Digitalwertdatengruppen-Erzeugungseinrichtung (10) verbunden ist, um jede der zahlreichen Digitalwertdatengruppen aufeinanderfolgend mit den Digitaldaten zu vergleichen, um eine Anzahl von Impulsen in einer Wandlerperiode abzugeben, die in der Zahl der Zahl der Digitalwertdatengruppen entspricht, dadurch gekennzeichnet, daß die Digitalwertdatengruppen-Erzeugungseinrichtung (10) einen n-Bit (n+1<N) Binärzähler (16) zum Zählen der Impulse der vorbestimmten Frequenz aufweist, um sequentiell binäre Zahlen zu erzeugen, eine Detektorschaltung (22) enthält, die mit dem n-Bit-Binärzähler (16) verbunden ist, der feststellt, ob eine Zählung des n-Bit-Binärzählers (16) erste und zweite Voreinstellzahlen erreicht hat und der einen Zählimpuls (CP) abgibt, wenn die Zählung des n-Bit-Binärzählers (16) die erste Voreinstellzahl erricht und ein Verriegelungssignal abgibt, wenn die Zählung des n-Bit-Binärzählers (16) den zweiten Voreinstellwert erreicht, und einen (N−n)-Bit-Binärzähler (18) enthält, der mit der Detektorschaltung (22) verbunden ist und eine Zählung um Eins inkremental erhöht, wenn der Zählimpuls (CP) erhalten wird, wobei der n-Bit-Binärzähler (16) ein Ausgangssignal für die oberwertigen Bits (N−n+1 bis N) der N-Bit Vergleichseinrichtung (12) liefert, und wobei der Inhalt des (N−n)-Bit-Binärzählers (18) in umgekehrter Ordnung der Wertigkeit für das geringswertige Bit bis zum (N−n)'tem Bit der N-Bit Vergleichseinrichtung geliefert wird.

2. Digital-Analog-Wandler nach Anspruch 1, dadurch gekennzeichnet, daß die Digitalwertdatengruppen-Erzeugungseinrichtung (10) eine (N−n)-Bit Verriegelungsschaltung (20) aufweist, die mit der Detektorschaltung (22) und dem (N−n)-Bit-Binärzähler (18) verbunden ist und die eine Zählung des (N−n)-Bit-Binärzählers (18) auf ein Verriegelungssignal hin verriegelt bzw. sperrt.

3. Digital-Analog-Wandler nach Anspruch 1, dadurch gekennzeichnet, daß die N-Bit Vergleichseinrichtung (12) einen ersten Komparator (24) zum Vergleichen des Inhalts des geringswertigen Bits bis zum (N−n)'tem Bit, eine Verriegelungsschaltung (28), die mit dem Komparator (24) und der Detektorschaltung (22) verbunden ist und die ein Ausgangssignal vom ersten Komparator (24) auf ein Verriegelungssignal hin verriegelt, und einen zweiten Komparator (26) aufweist, der mit der Verriegelungsschaltung (28) verbunden ist und der den Inhalt der oberwertigen Bits (N−n+1 bis N) vergleicht und ein Vergleichsausgangssignal erzeugt mit einer Priorität über einem Ausgangssignal der Verriegelungsschaltung (28).

4. Digital-Analog-Wandler nach Anspruch 1 oder 2, dadurch gekennzeichnet, daß die Detektorschaltung (50) außerdem feststellt, ob eine Zählung des n-Bit-Binärzählers (16) eine dritte Voreinstellzahl erreicht hat und ein Setzsignal abgibt, wenn die Zählung des n-Bit-Binärzählers (16) den dritten Voreinstellwert erreicht.

5. Digital-Analog-Wandler nach Anspruch 4 in Verbindung mit Anspruch 2, dadurch gekennzeichnet, daß die Vergleichseinrichtung (12) einen Komparator (30) aufweist, um den umgekehrten Inhalt der Verriegelungsschaltung (20) mit den geringeren Bits (N−n) der N-Bit-Digitaldaten zu vergleichen, eine Koinzidenzschaltung (32) enthält, um eine Koinzidenz zwischen dem Inhalt des n-Bit Zählers (16) mit den oberen n-Bits der N-Bit Digitaldaten festzustellen, eine Verzögerungsschaltung (34) aufweist, die mit dem Komparator (30) und der Koinzidenzschaltung (32) verbunden ist und die ein Ausgangssignal der Koinzidenzschaltung (32) um eine Periode der Impulse der vorbestimmten Frequenz (CK) auf ein Ausgangssignal des Komparators (30) hin verzögert und eine bistabile Schaltung (46) aufweist, die mit der Detektorschaltung (50) und der Verzögerungsschaltung (34) verbunden ist, die durch das Setzsignal gesetzt wird und die durch ein Ausgangssignal der Verzögerungsschaltung (34) rückgesetzt wird.

6. Digital-Analog-Wandler nach Anspruch 4 in Verbindung mit Anspruch 1, dadurch gekennzeichnet, daß die Vergleichseinrichtung einen Komparator (30) zum Vergleichen des umgekehrten Inhalts des (N−n)-Bit-Binärzählers (18) mit den geringeren Bits (N−n) der N-Bit Digitaldaten aufweist, eine Verriegelungsschaltung (28) enthält, die mit dem Komparator (30) und der Detektorschaltung (50) verbunden ist und die ein Ausgangssignal des Komparators (30) auf ein Verriegelungssignal hin verriegelt, eine Koinzidenzschaltung (32) aufweist, um eine Koinzidenz zwischen dem Inhalt des n-Bit Binärzählers (16) mit dem oberen n-Bits der N-Bit Digitaldaten festzustellen, eine Verzögerungsschaltung (34) aufweist, die mit der Verriegelungsschaltung (28) und der Koinzidenzschaltung (32) verbunden ist und die ein Ausgangssignal der Koinzidenzschaltung (32) um eine Periode der Impulse der vorgegebenen Frequenz (CK) auf ein Ausgangssignal der Verriegelungsschaltung (28) hin verzögert und eine bistabile Schaltung (46) enthält, die mit der Detektorschaltung (50) und der Verzögerungsschaltung (34) verbunden ist, die durch ein Setzsignal gesetzt wird und die durch ein Ausgangssignal der Verzögerungsschaltung (34) rückgesetzt wird.

Revendications

1. Convertisseur numérique-analogique destiné à comparer des données numériques (DD) à N bits qui doivent être converties avec une valeur numérique de référence changeant pendant une période de conversion pour produire des impulsions d'une durée d'impulsions correspondant à une valeur des données à N bits en fonction des résultats de la comparaison, et pour filtrer les impulsions afin d'obtenir une sortie continue, ledit convertisseur comportant: un dispositif (10) générateur d'une série de valeurs numériques pour compter des impulsions d'une fréquence prédéterminée (CK) afin de produire plusieurs séries de valeurs numériques qui doivent être comparées avec les données numériques pendant une période de conversion, chacune desdites séries produites pendant la période de conversion ayant une pondération différente, et un dispositif (12) de comparaison de N bits connectée audit dispositif (10) générateur de séries de valeurs numériques pour comparer séquentiellement chacune desdites plusieurs séries de valeurs numériques avec les données numériques de manière à émettre un nombre d'impulsions dans une période de conversion dont le nombre correspond au nombre des séries de valeurs numériques, caractérisé en ce que ledit dispositif (10) générateur de séries de valeurs numériques comporte un compteur binaire (16) à n bits (n+1<N) pour compter les impulsions de la fréquence prédéterminée afin de produire séquentiellement des nombres binaires; un circuit de détection (22) qui est connecté audit compteur binaire (16) à n bits qui détecte si un comptage du compteur binaire (16) à n bits a atteint un premier et un second nombre prédéterminés, et qui émet une impulsion de comptage (CP) quand le comptage dudit compteur binaire (16) à n bits atteint le premier nombre prédéterminé et émet un signal de verrouillage (LP) quand le comptage dudit compteur binaire (16) à n bits atteint le second nombre prédéterminé; et un compteur binaire (18) à (N−n) bits qui est connecté audit circuit de détection (22) et qui incrémente un comptage d'une unité quand l'impulsion de comptage (CP) sst reçue; ledit compteur binaire (16) à n bits délivrant à sa sortie les bits les plus significatifs du (N−n+1) ème au Nème bit dudit dispositif de comparaison (12) à N bits, et le contenu du compteur binaire (18) à (N−n) bits étant fourni dans un ordre inverse de signification aux bits depuis le moins significatif jusqu'au (N−n)ème dudit dispositif de comparaison à N bits.

2. Convertisseur numérique-analogique selon la revendication 1, caractérisé en ce que ledit dispositif (10) générateur de séries de valeurs numériques comporte un circuit de verrouillage (20) à (N−n) bits qui est connecté audit circuit de détection (22) et audit compteur binaire (18) à (N−n) bits et qui verrouille un comptage dudit compteur binaire (18) à (N−n) bits en réponse au signal de verrouillage.

3. Convertisseur numérique-analogique selon la revendication 1, caractérisé en ce que ledit dispositif de comparaison (12) à N bits comporte un premier comparateur (24) pour comparer le contenu des bits depuis le moins significatif jusqu'au (N−n)ème; un circuit de verrouillage (28) qui est connecté audit comparateur (24) et audit circuit de détection (22) et qui verrouille une sortie dudit premier comparateur (24) en réponse au signal de verrouillage; et un second comparateur (26) qui est connecté audit circuit de verrouillage (28) et qui compare le contenu des bits les plus significatifs du (N−n+1)ème au Nème et qui produit une sortie de comparaison avec une priorité sur une sortie dudit circuit de verrouillage (28).

4. Convertisseur numérique-analogique selon la revendication 1 ou 2, caractérisé en ce que ledit circuit de détection (50) détecte également si un contenu dudit compteur binaire (16) à N bits a atteint un troisième

nombre prédéterminé et qui émet un signal de mise en place quand le contenu dudit compteur binaire (16) à n bits atteint la troisième valeur prédéterminée.

5. Convertisseur numérique-analogique selon la revendication 4, dépendant de la revendication 2, caractérisé en ce que ledit dispositif de comparaison (12) comporte un comparateur (30) destiné à comparer le contenu inversé dudit circuit de verrouillage (20) avec les (N−n) bits inférieurs des données numériques à N bits, un circuit à coincidence (32) destiné à détecter une coincidence entre le contenu dudit compteur (16) à n bits avec les n bits supérieurs des données numériques à N bits; un circuit à retard (34) qui est connecté audit comparateur (30) et audit circuit à coincidence (32) et qui retarde une sortie dudit circuit à coincidence (32) d'une période des impulsions de la fréquence prédéterminée (CK) en réponse à une sortie dudit comparateur (30); et un circuit bistable (46) qui est connecté audit circuit de détection (50) et audit circuit à retard (34) et qui est positionné par le signal de positionnement et qui est ramené au repos par un signal de sortie provenant dudit circuit à retard (34).

6. Convertisseur numérique-analogique selon la revendication 4, dépendant seulement de la revendication 1, caractérisé en ce que ledit dispositif de comparaison comporte un comparateur (30) destiné à comparer le contenu inversé dudit compteur binaire (18) à (N−n) bits avec les (N−n) bits inférieurs des données numériques à N bits; un circuit de verrouillage (28) qui est connecté audit comparateur (30) et audit circuit de détection (50) et qui verrouille une sortie dudit comparateur (30) en réponse au signal de verrouillage; un circuit à coincidence (32) qui détecte une coincidence entre le contenu dudit compteur binaire (16) à n bits avec les n bits supérieurs des données numériques à N bits; un circuit à retard (34) qui est connecté audit circuit de verrouillage (28) et audit circuit à coincidence (32) et qui retarde une sortie dudit circuit à coincidence (32) d'une période des impulsions de la fréquence prédéterminée (CK) en réponse à une sortie dudit circuit de verrouillage (28); et un circuit bistable (46) qui est connecté audit circuit de détection (50) et audit circuit à retard (34), qui est positionné par le signal de positionnement et qui est ramené au repos par un signal de sortie dudit circuit à retard (34).

FIG. 1

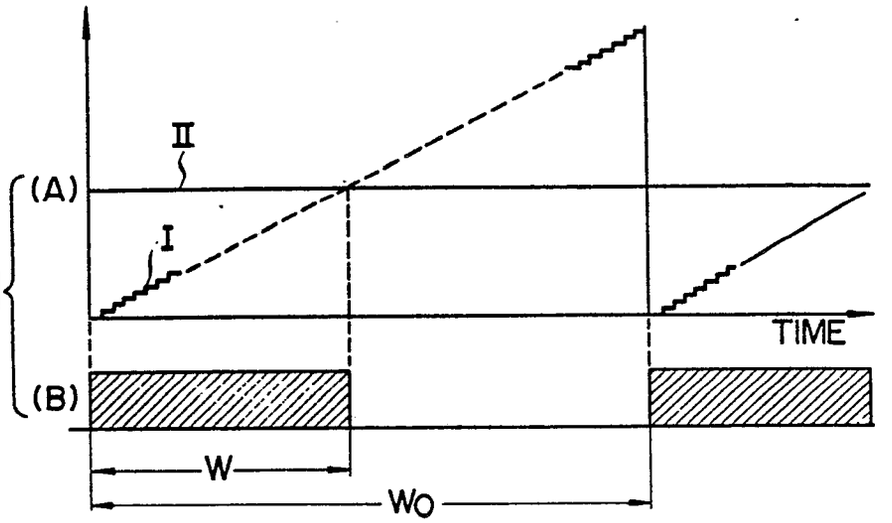


FIG. 2

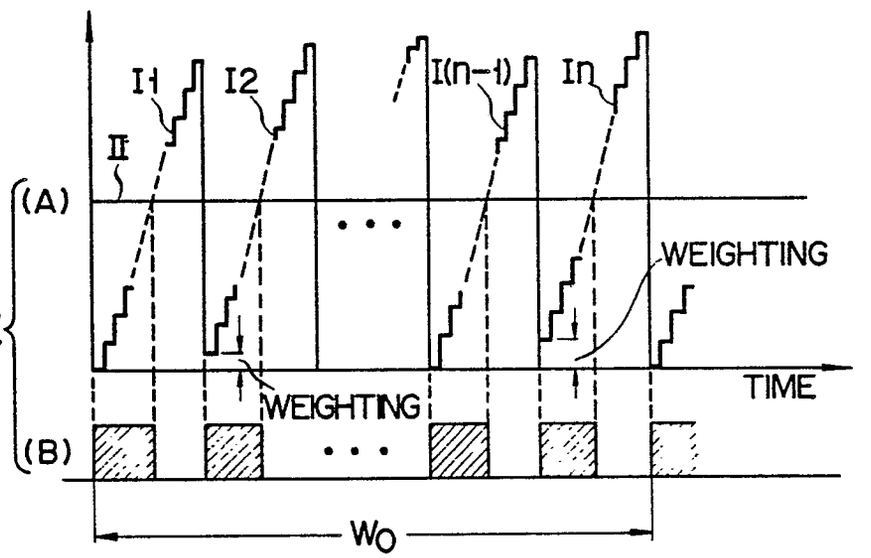


FIG. 3

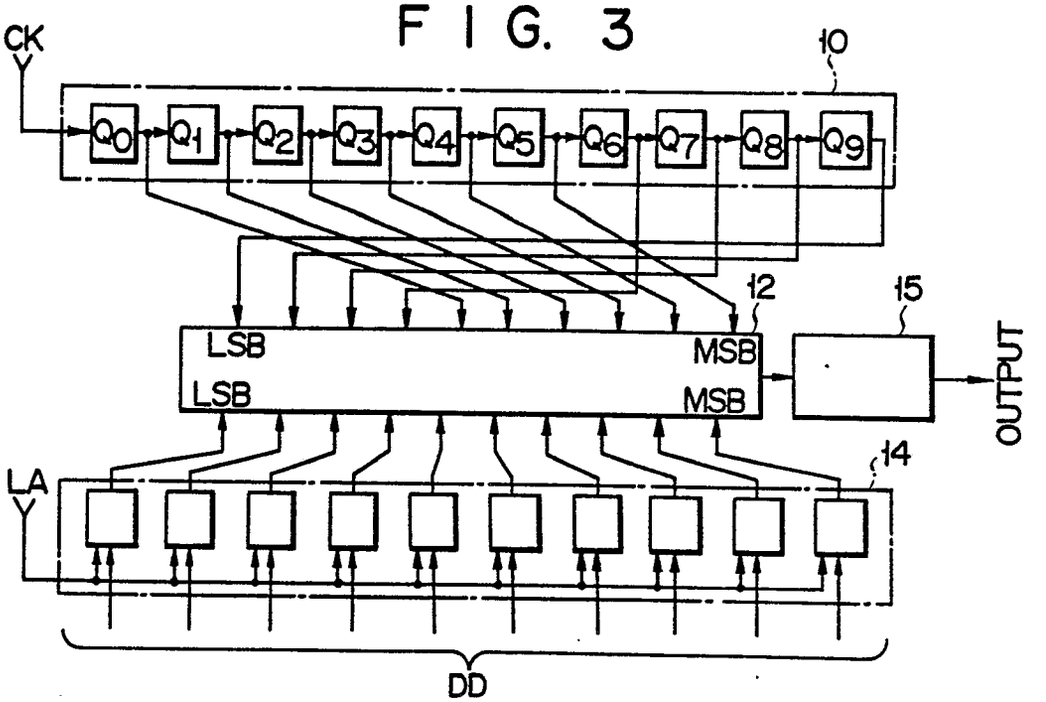
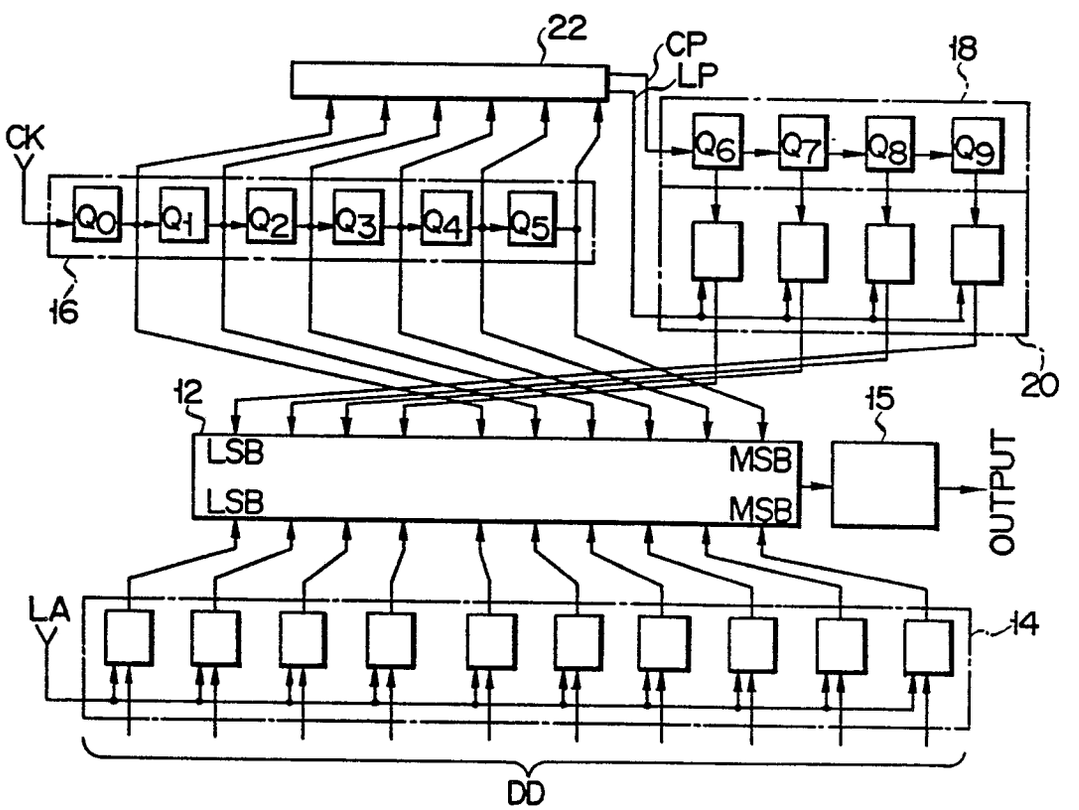

CK
10
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
12
15
LSB
MSB
LSB
MSB
OUTPUT
14
LA
DD

FIG. 5


22
CP
LP
18
CK
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
16
20
12
15
LSB
MSB
LSB
MSB
OUTPUT
LA
14
DD

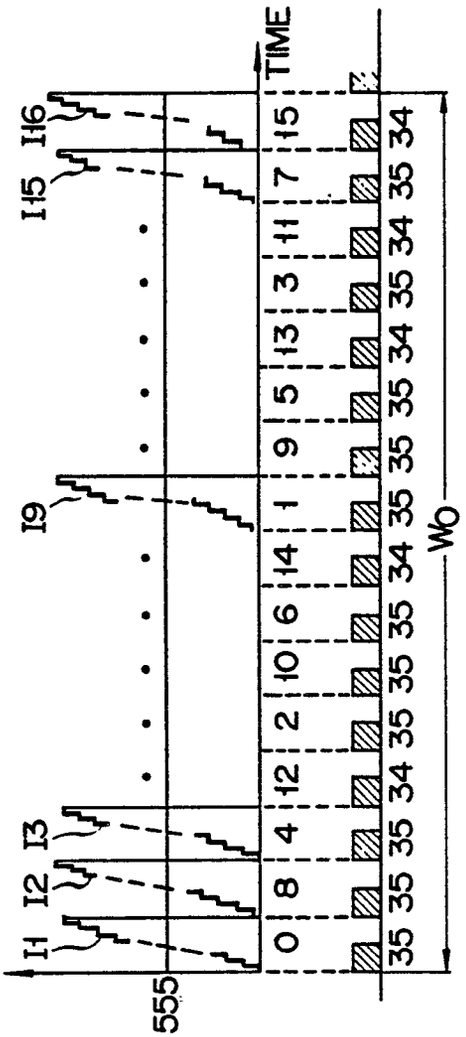

TIME
I1
I2
I3
I9
I15
I16
555
0 8 4 12 2 10 6 14 1 9 5 13 3 11 7 15
35 35 35 34 35 35 35 34 35 35 35 34 35 35 35 34
W0
(A)
(B)

FIG. 4

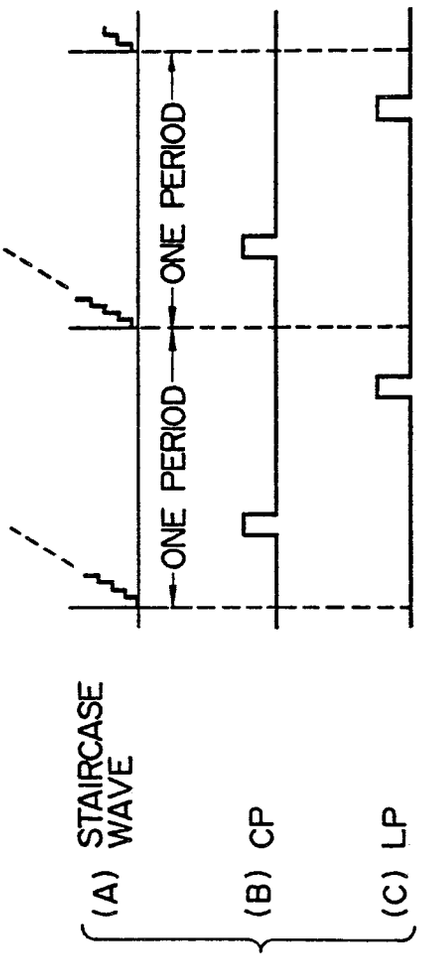

ONE PERIOD
ONE PERIOD
(A) STAIRCASE WAVE
(B) CP
(C) LP

FIG. 6

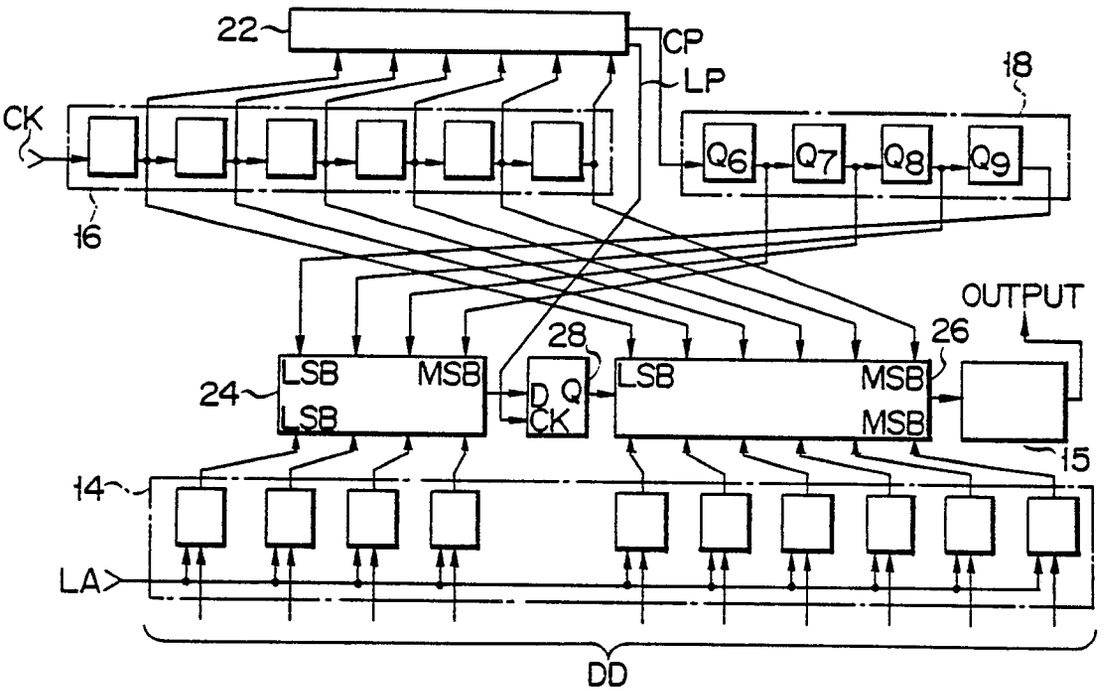

22
CP
LP
18
CK
Q6
Q7
Q8
Q9
16
OUTPUT
28
26
LSB
MSB
24
LSB
D Q
CK
LSB
MSB
MSB
15
14
LA
DD

FIG. 7

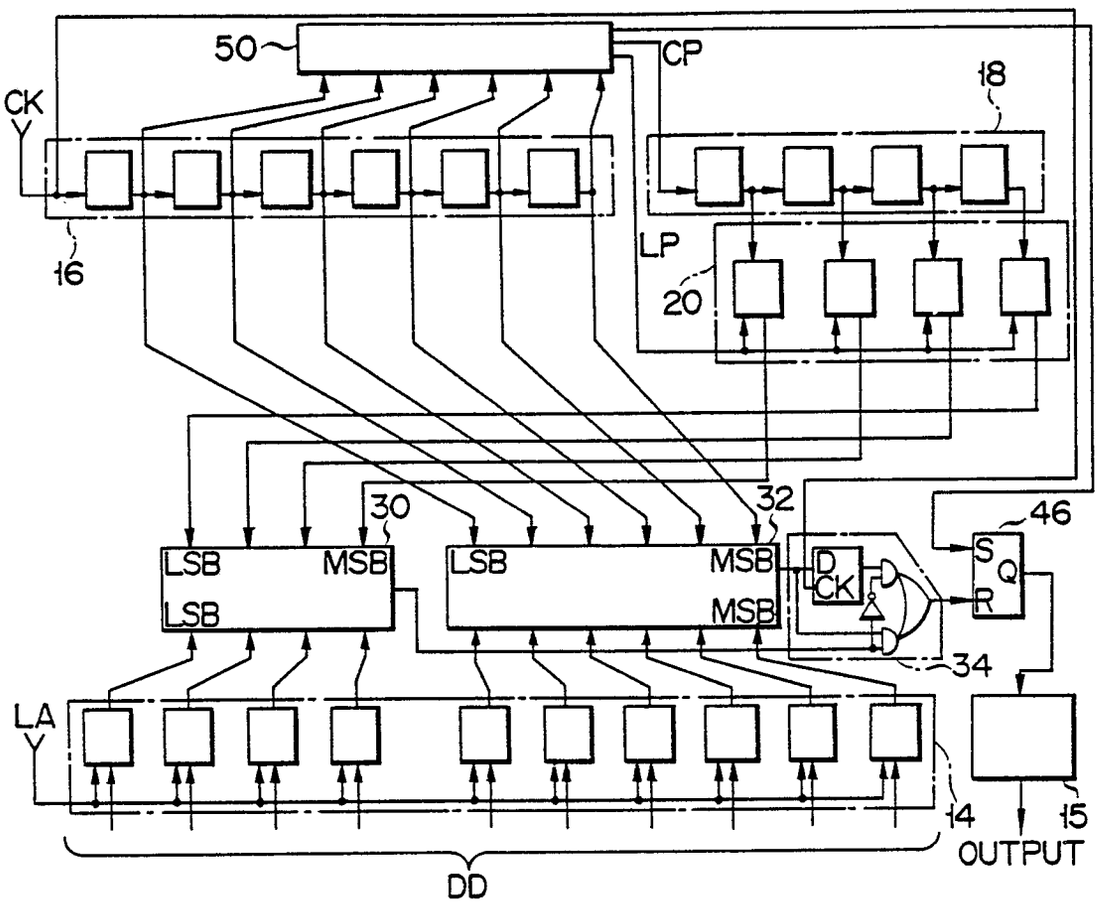

50
CP
18
CK
Y
16
LP
20
30
32
46
LSB
MSB
LSB
MSB
LSB
MSB
LSB
MSB
D
CK
S
Q
R
34
LA
Y
14
15
OUTPUT
DD

FIG. 8

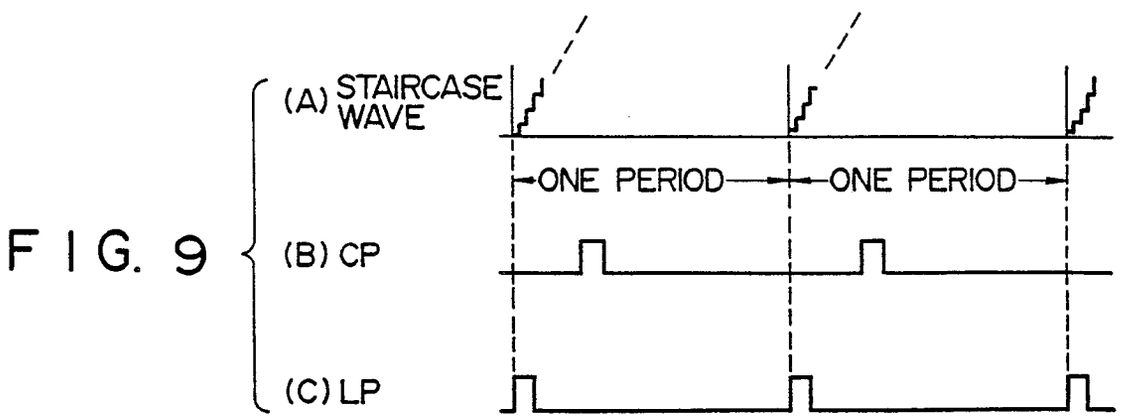
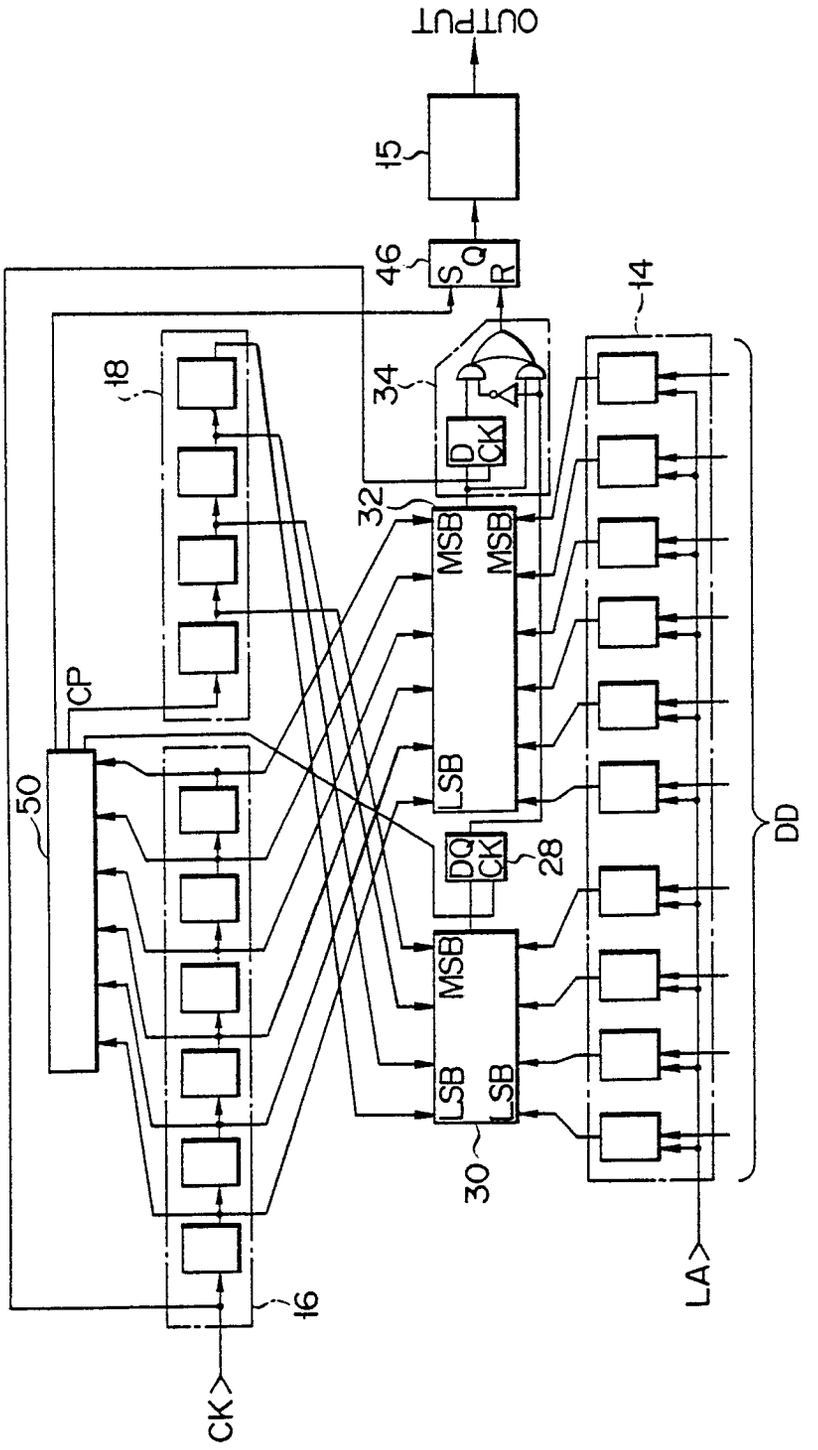

(A) STAIRCASE WAVE
ONE PERIOD
ONE PERIOD
(B) CP
(C) LP

FIG. 9

FIG. 10


OUTPUT
15
46
S
Q
R
14
18
34
D
CK
32
MSB
MSB
LSB
DQ
CK
28
MSB
LSB
LSB
30
DD
CP
50
16
CK>
LA>