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(54) **SPLIT-GATE MOSFET**

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H01L 29/78 (2006.01)
H01L 29/06 (2006.01)

(Continued)

(52) **U.S. Cl.**

CPC ***H01L 29/7813*** (2013.01); ***H01L 29/0642*** (2013.01); ***H01L 29/4236*** (2013.01); ***H01L 29/4238*** (2013.01); ***H01L 29/66734*** (2013.01)

(58) **Field of Classification Search**

CPC H01L 29/7813; H01L 29/0642; H01L 29/4236; H01L 29/4238; H01L 29/66734

See application file for complete search history.

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(57) **ABSTRACT**

A split-gate MOSFET includes first and second epitaxial layers, first, second, and third gates, a gate oxide layer, a trench oxide layer, and a trench implantation region formed on a substrate in order. The second epitaxial layer has a doping concentration greater than that of the first epitaxial layer. A plurality of trenches is in the first and second epitaxial layers. Both the first and second gates are located in each of the trenches in a cell region. The third gates are located in each of the trenches in a terminal region. The third gate closest to the cell region is grounded, and the others are floating. The gate oxide layer is disposed between the first and second gates. The trench oxide layer is located between the first gate and the first epitaxial layer and located between the trench surface and the third gate. The trench implantation

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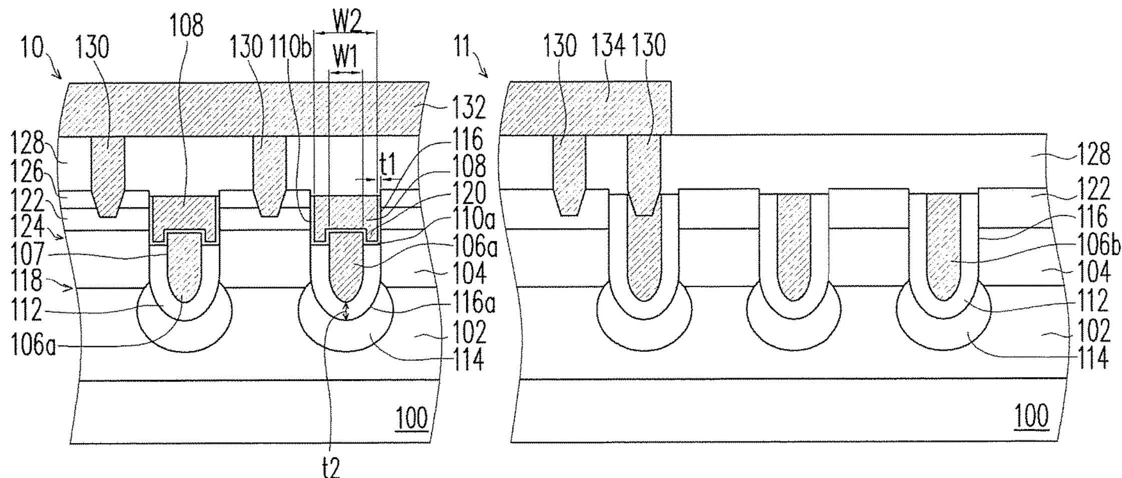

region is located in the first epitaxial layer at the bottom of the trench and has a doping concentration less than that of the first epitaxial layer.

11 Claims, 13 Drawing Sheets

(51) **Int. Cl.**
H01L 29/66 (2006.01)
H01L 29/423 (2006.01)

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FIG. 1

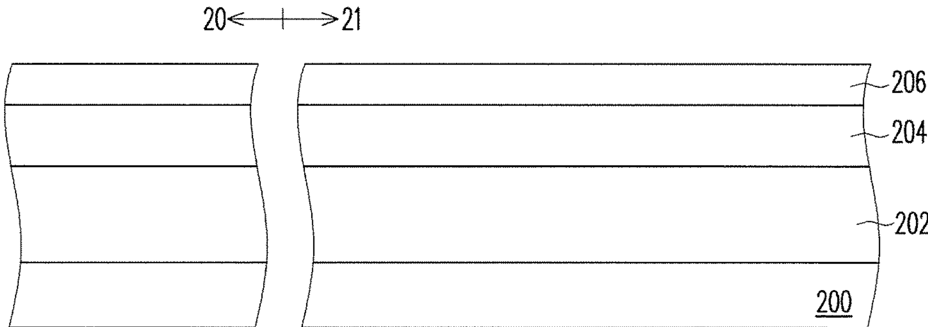

FIG. 2A

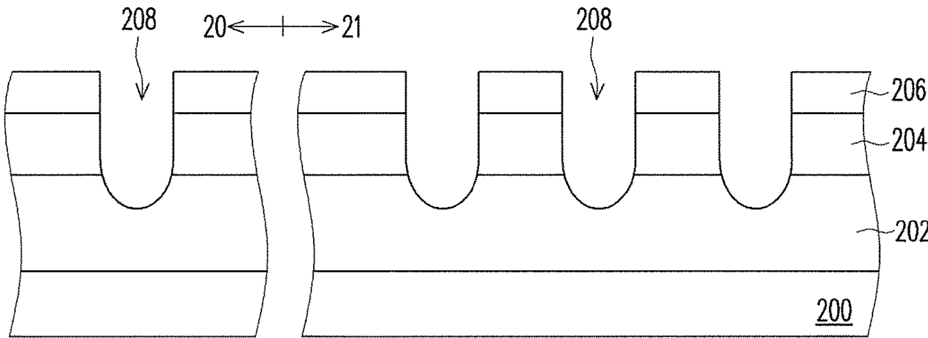

FIG. 2B

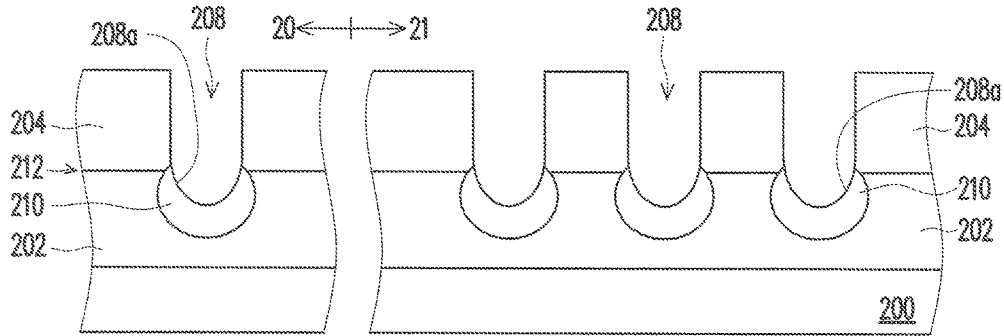

FIG. 2C

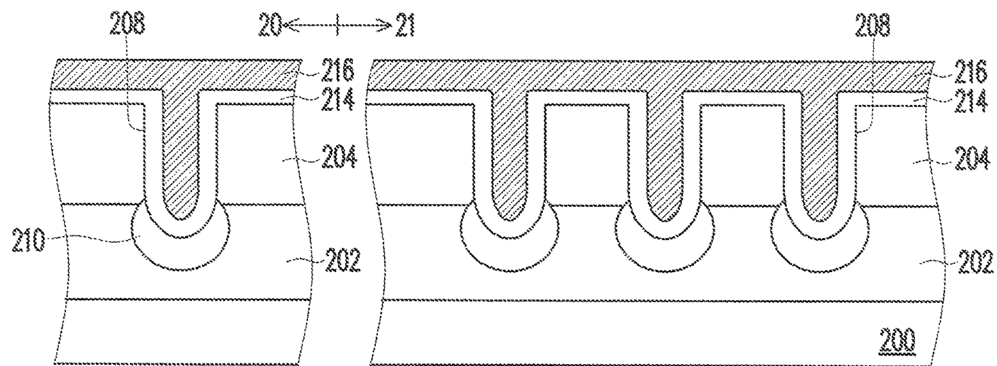

FIG. 2D

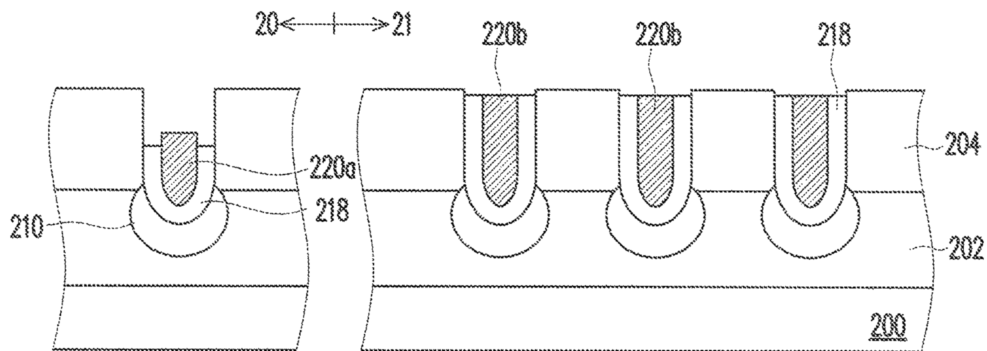

FIG. 2E

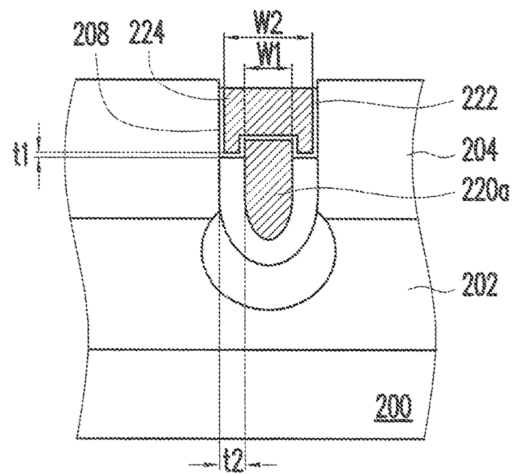

FIG. 2F

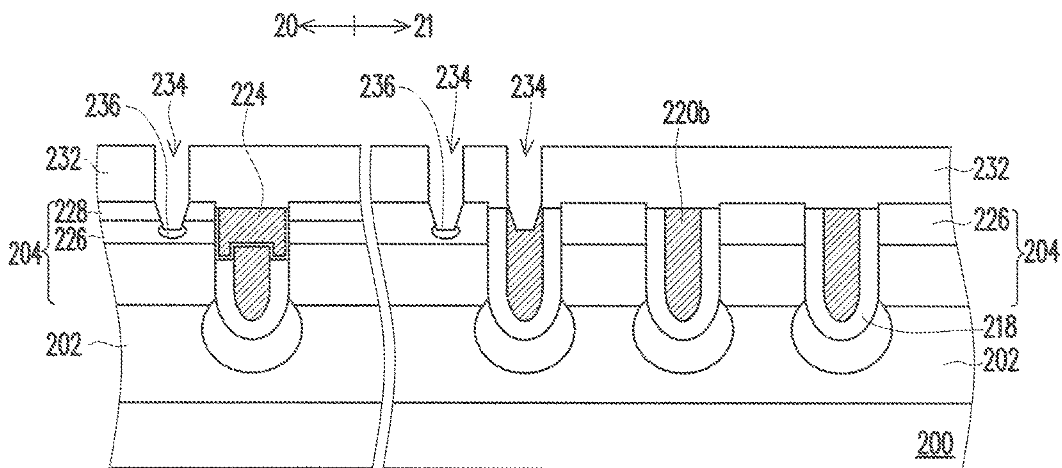

FIG. 2G

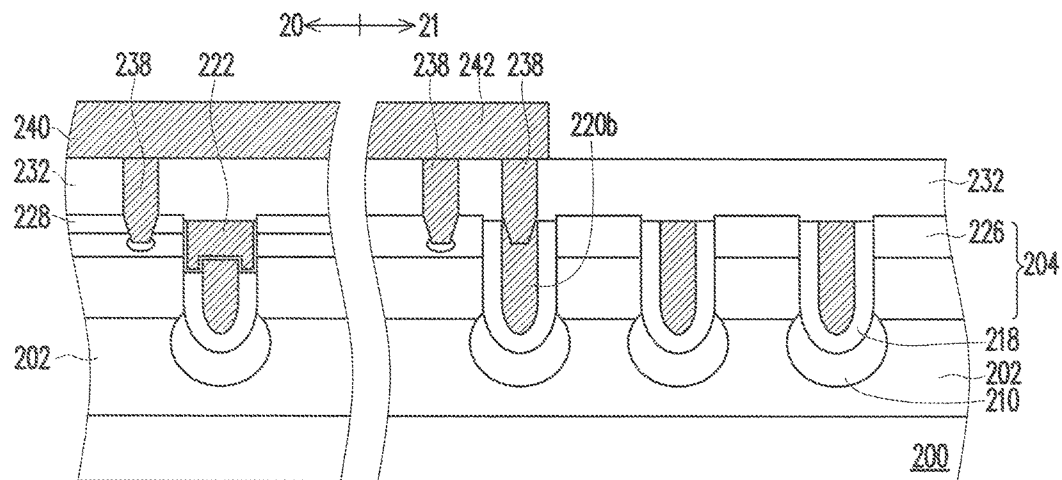

FIG. 2H

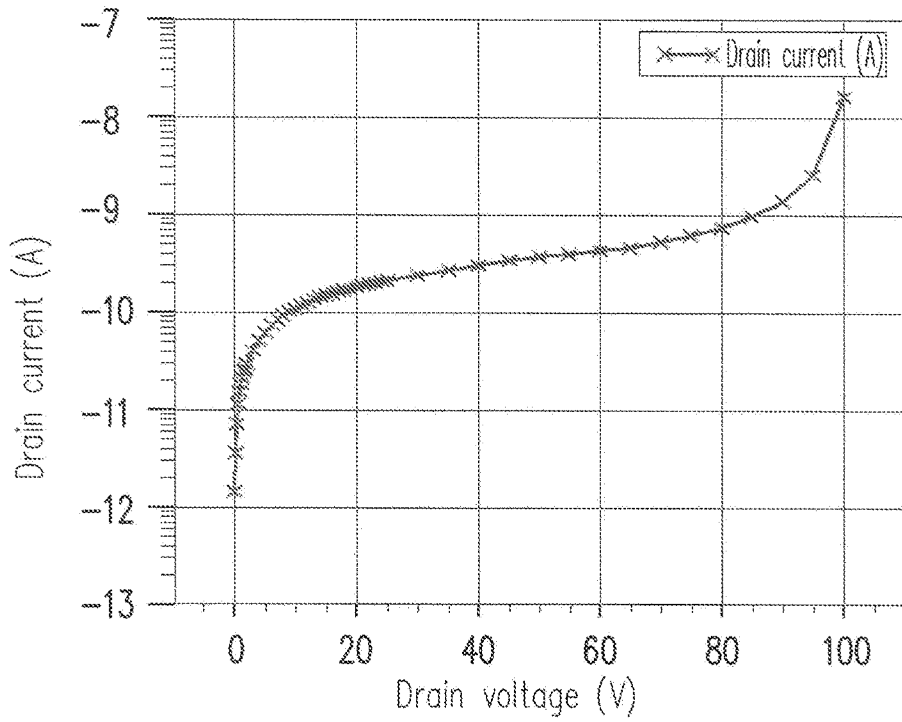

FIG. 3

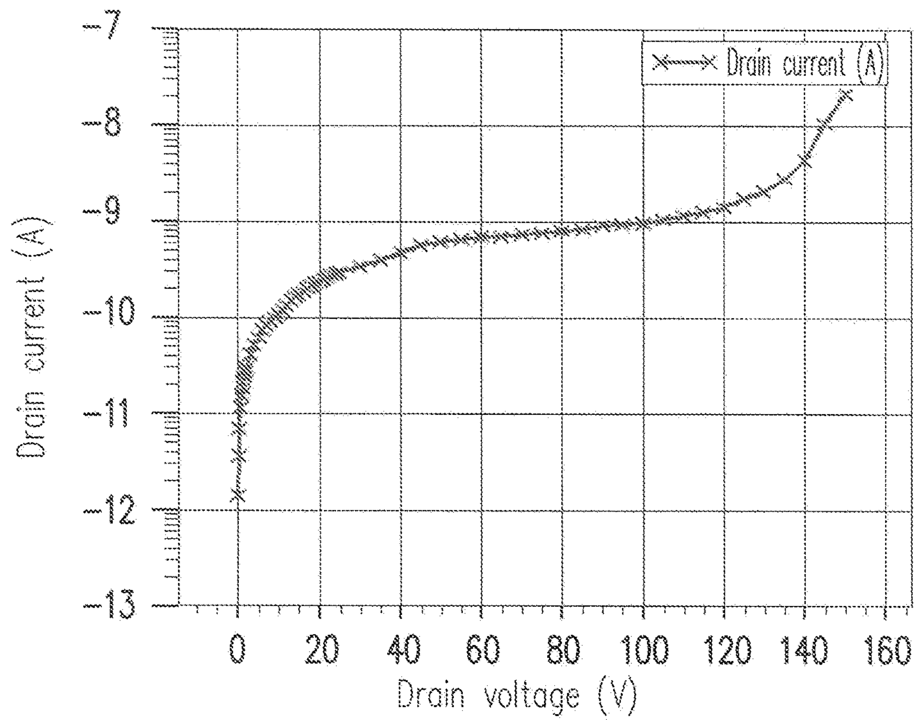

FIG. 4

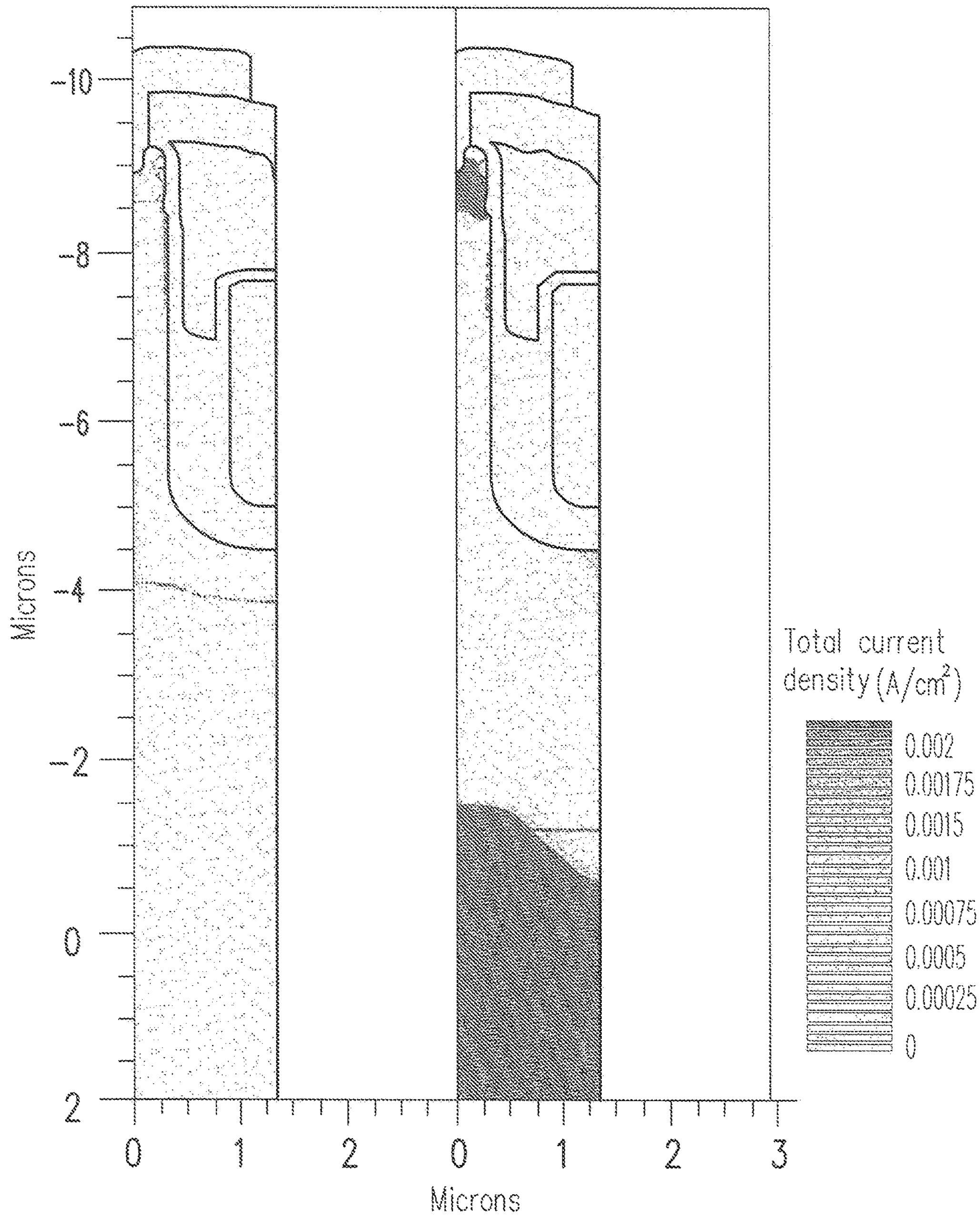

FIG. 5

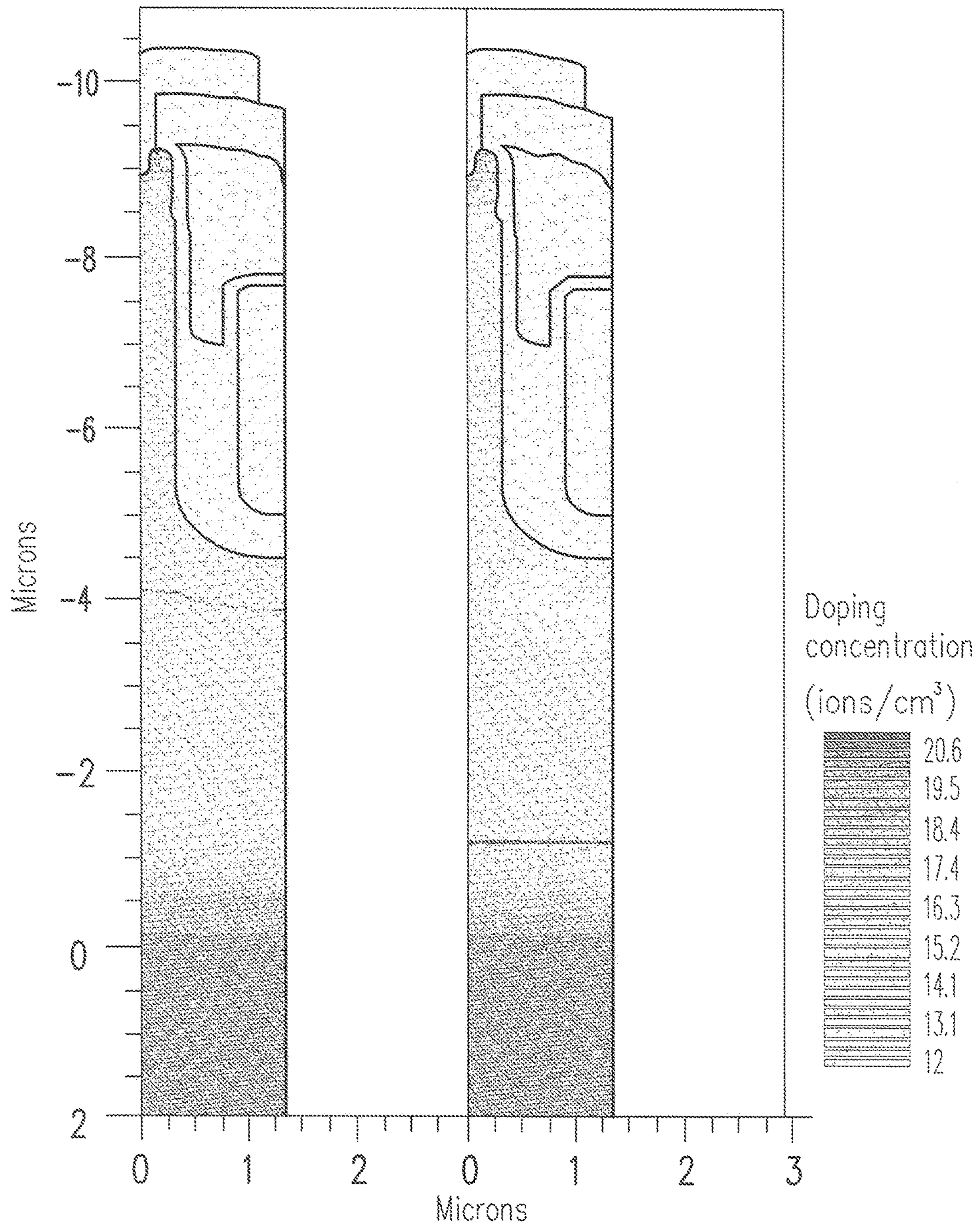

FIG. 6

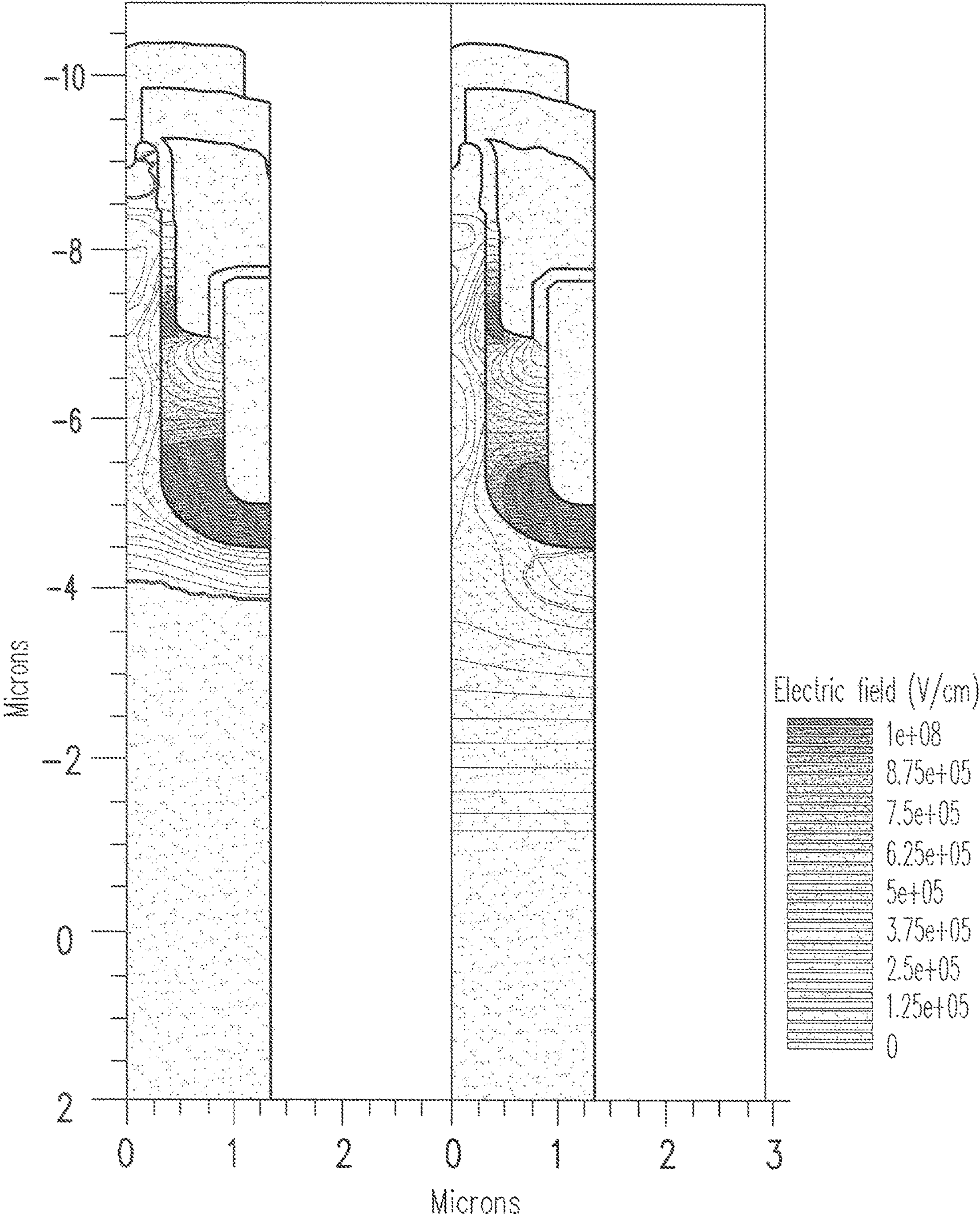

FIG. 7

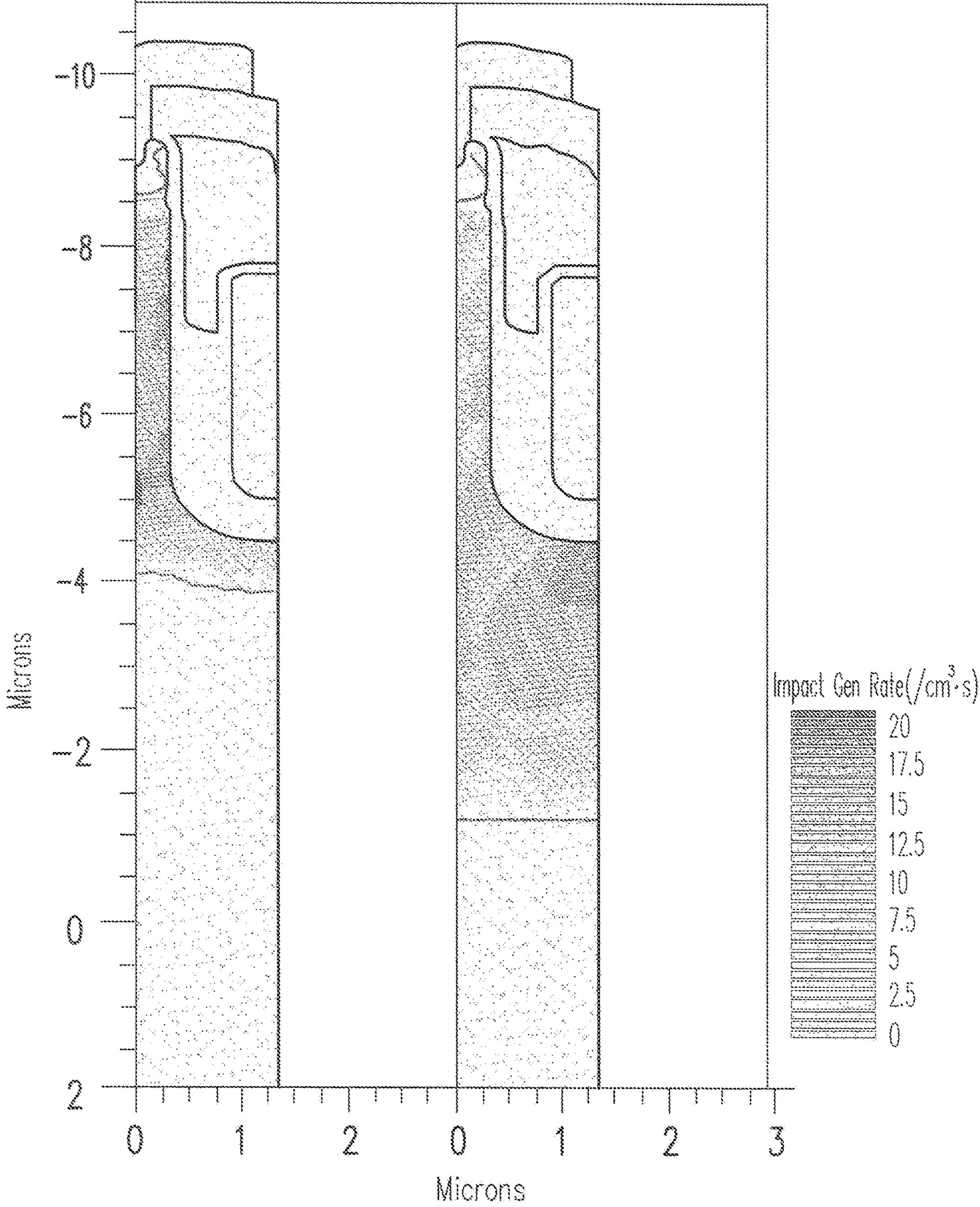

FIG. 8

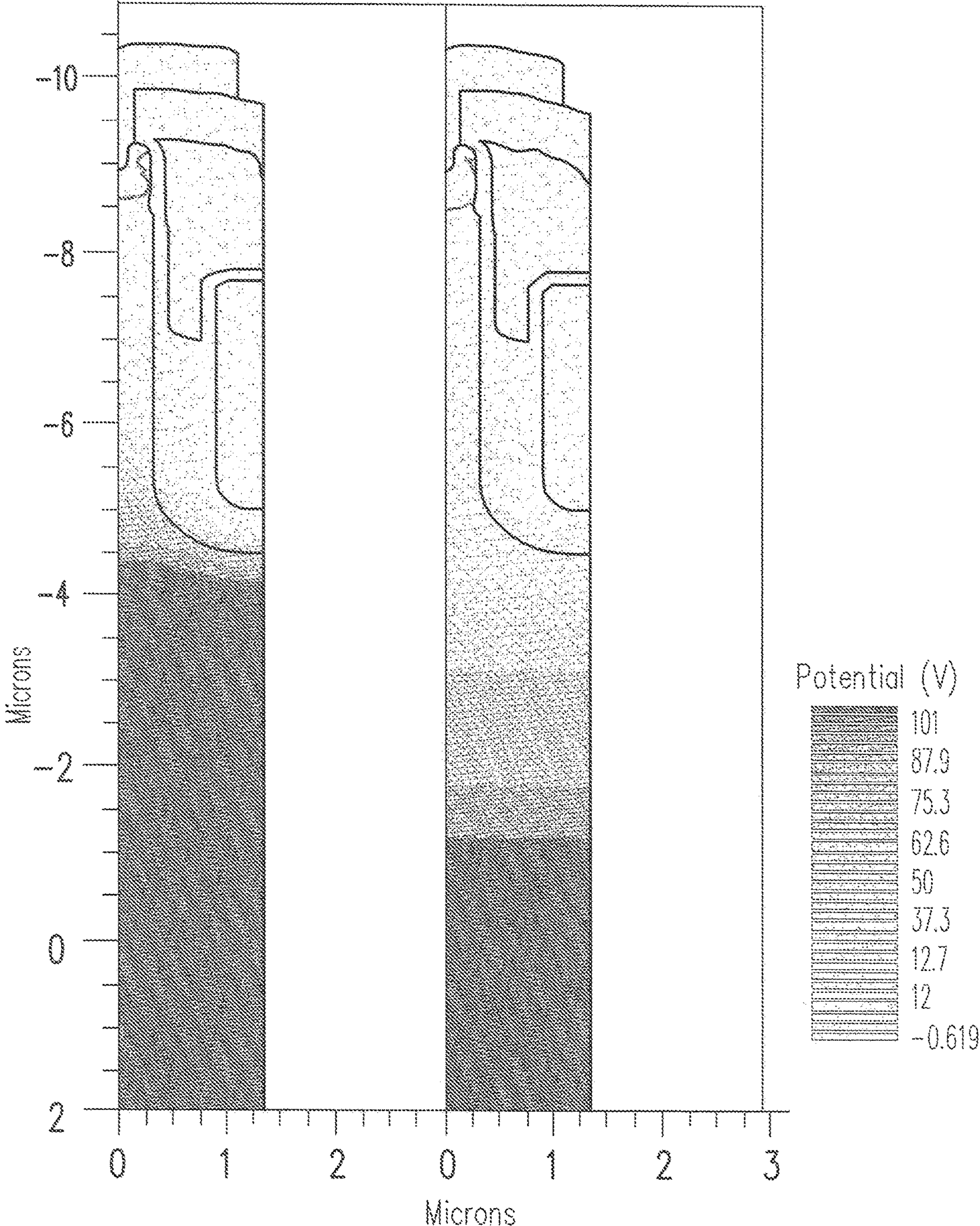

FIG. 9

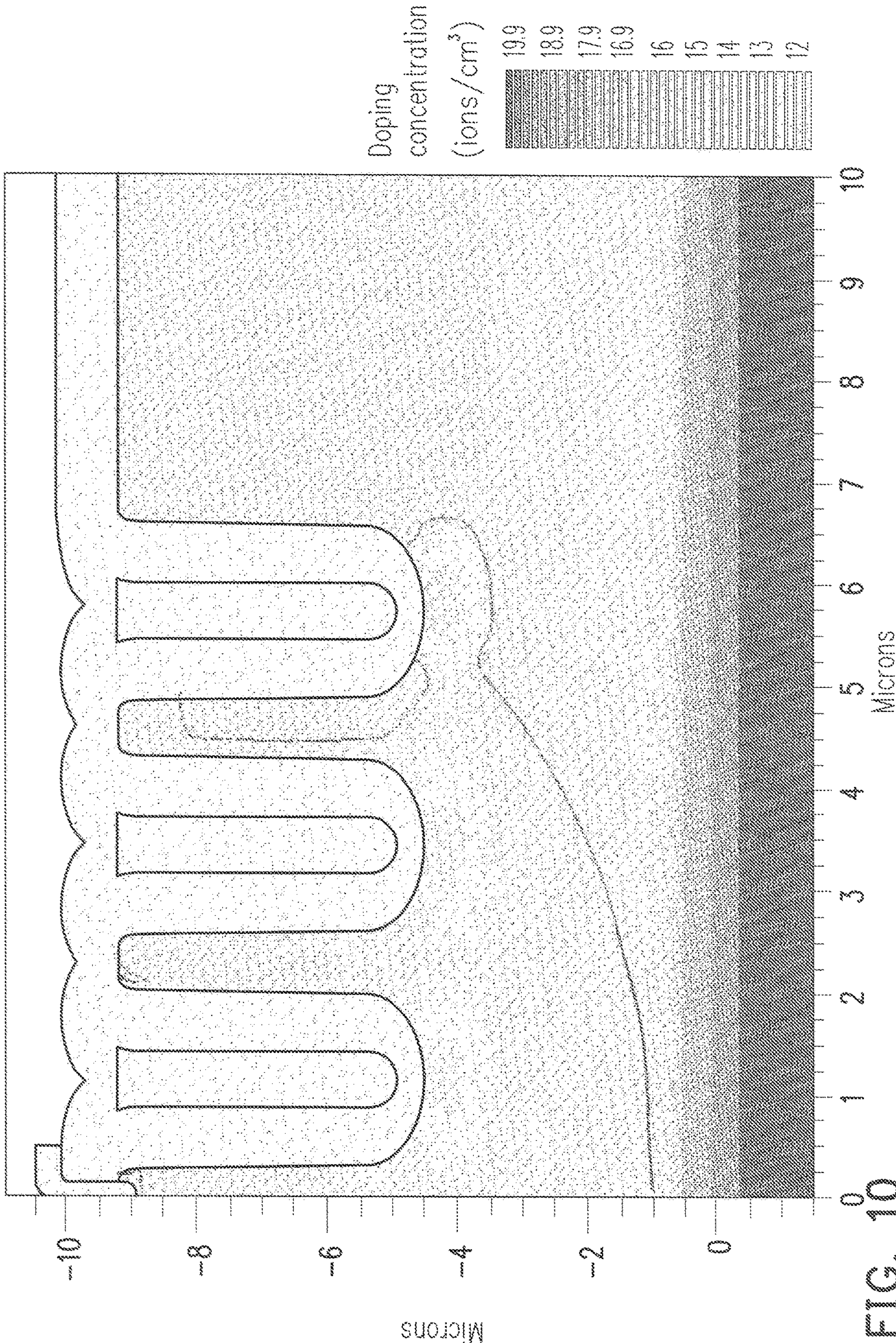

FIG. 10

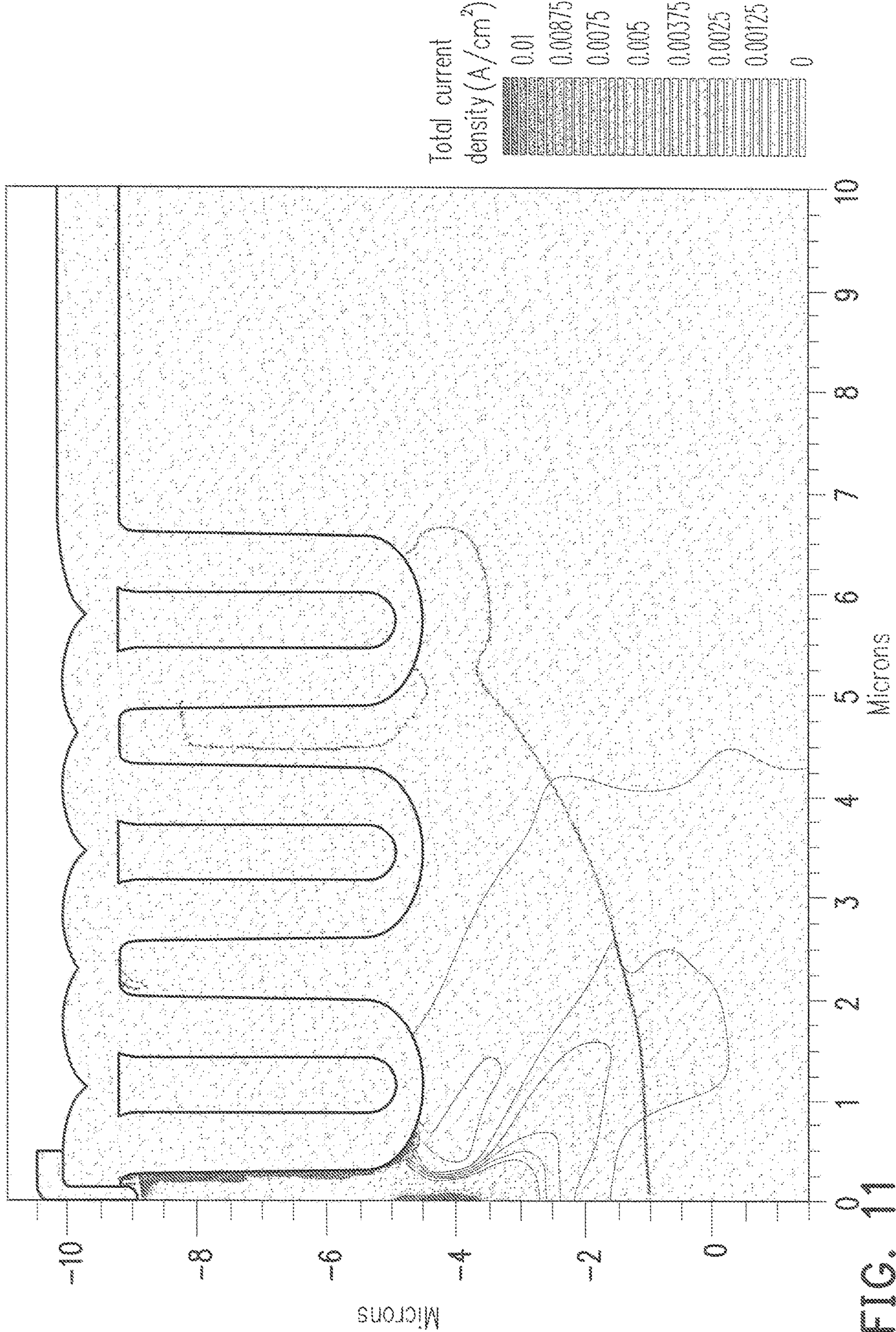

FIG. 11

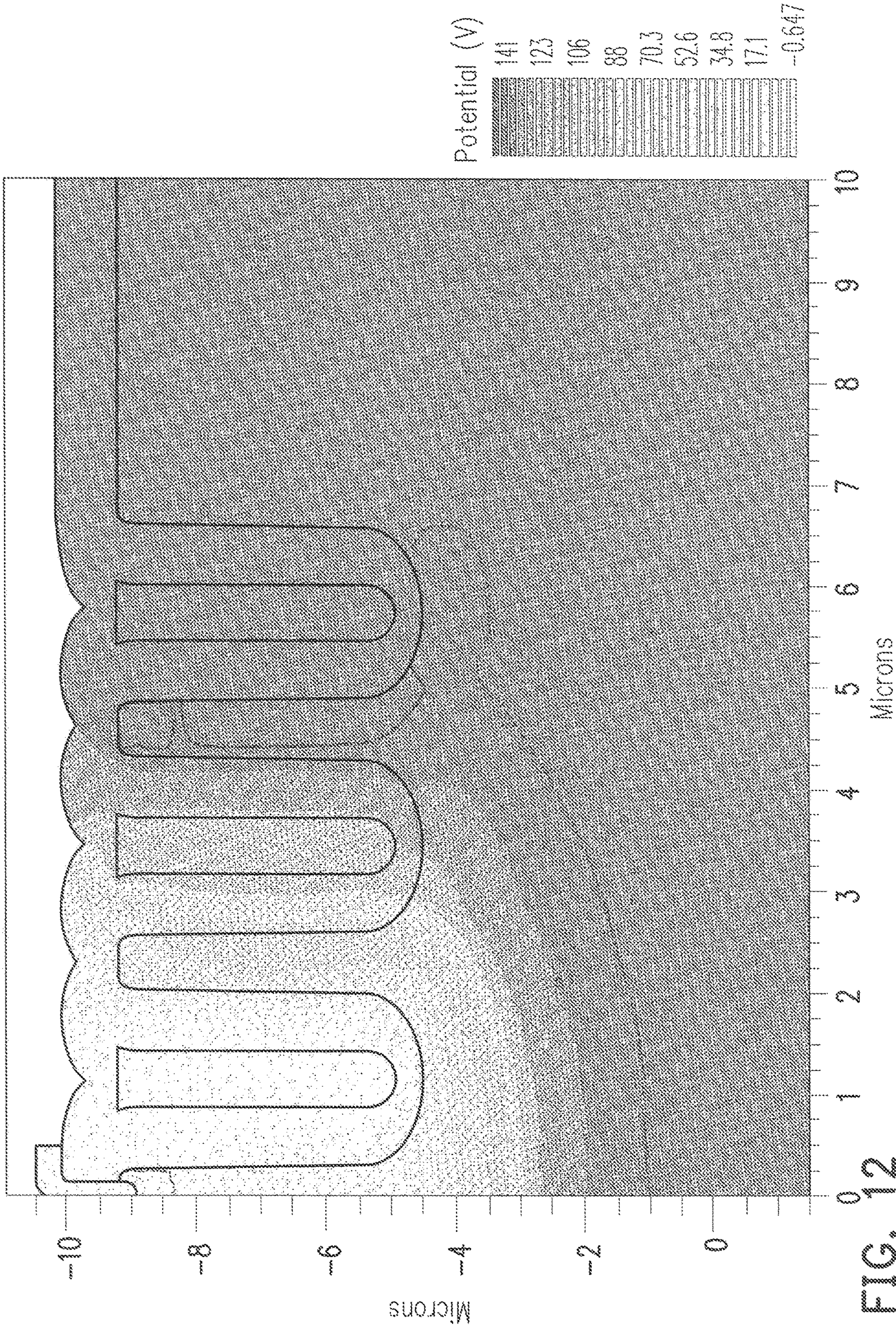

FIG. 12

SPLIT-GATE MOSFET

CROSS-REFERENCE TO RELATED APPLICATION

This application claims the priority benefit of Taiwan application serial no. 105127204, filed on Aug. 25, 2016. The entirety of the above-mentioned patent application is hereby incorporated by reference herein and made a part of this specification.

BACKGROUND OF THE INVENTION

Field of the Invention

The invention relates to a trench MOSFET, and more particularly, to a split-gate MOSFET.

Description of Related Art

The split-gate MOSFET is also referred to as a shielded-gate MOSFET, and the structure thereof divides the gate structure in a trench MOSFET into two electric potentials by isolating via an inter-poly-dielectric (IPD) layer. The gate located above is used for forming a channel of the MOSFET, and the gate located below is electrically coupled to a source potential via a metal interconnect for the generation of two-dimensional charge balance under blocking operation, and excessive gate-to-source capacitance in a traditional trench MOSFET is reduced via the IPD layer, so as to reduce switching loss.

However, as the high-voltage application reaches 100 V or above, a trench oxide layer greater than 8000 Angstroms not only significantly increases the cell pitch of the MOSFET, but also increases the cell resistance. Moreover, forming such a thick trench oxide layer is more costly and requires longer cyclical deposition time, and due to thermal oxide growth process, the corners of the trench oxide layer close to the bottom of the trench are thinner, and as a result adverse effects are occurred.

SUMMARY OF THE INVENTION

The invention provides a split-gate MOSFET. The effect of the split-gate MOSFET can be maintained in a high-voltage field.

The split-gate MOSFET of the invention at least has a terminal region and a cell region. The split-gate MOSFET includes a substrate, first and second epitaxial layers, a plurality of first, second, and third gates, a gate oxide layer, a trench oxide layer, and a trench implantation region. The first epitaxial layer is formed on the substrate and has a first doping concentration. The second epitaxial layer is formed on the first epitaxial layer, wherein the second epitaxial layer has a second doping concentration greater than the first doping concentration. A plurality of trenches is in the first and the second epitaxial layers, and the trenches pass through the second epitaxial layer and are extended into the first epitaxial layer. The first and second gates are both located within each of the trenches in the cell region, wherein the second gate is located on the first gate. The third gates are respectively located in each of the trenches in the terminal region, wherein the third gate closest to the cell region is grounded and the rest of the third gates are floating gates. The gate oxide layer is located between the first and second gates and located between the second gate and the second epitaxial layer. The trench oxide layer is located between the first gate and the first epitaxial layer and located between the surface of the trench and the third gate in the terminal region. The trench implantation region is located in the first epitaxial layer at the bottom of each of the trenches in the cell region and the terminal region, wherein the trench implantation region has a third doping concentration less than the first doping concentration.

In an embodiment of the invention, the trench implantation region can cover the bottom of each of the trenches.

In an embodiment of the invention, the interface of the first and second epitaxial layers can be adjacent to the trench implantation region.

In an embodiment of the invention, the interface of the first and second epitaxial layers can be in contact with the trench implantation region.

In an embodiment of the invention, the thickness of the gate oxide layer can be less than the thickness of the trench oxide layer.

In an embodiment of the invention, the width of the second gate can be greater than the width of the first gate.

In an embodiment of the invention, the second gate can further include an extending portion extended to the sidewall of the first gate.

In an embodiment of the invention, the conductive state of the first and second epitaxial layers is, for instance, n-type.

In an embodiment of the invention, the split-gate MOSFET can further include a p-type well on the second epitaxial layer.

In an embodiment of the invention, the interface of the p-type well and the second epitaxial layer can be adjacent to the gate oxide layer between the first and second gates.

In an embodiment of the invention, the third gate closest to the cell region and the p-type well in the cell region are equipotential.

Based on the above, in the invention, via two epitaxial layers having different doping concentrations and the implantation region at the bottom of each trench, the width of the depletion region for high-voltage application can be maintained and the resistance of the split-gate MOSFET can be reduced at the same time. Moreover, maximum electric field at the corners of the trench can also be released.

In order to make the aforementioned features and advantages of the disclosure more comprehensible, embodiments accompanied with figures are described in detail below.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention.

FIG. **1** is a cross-sectional schematic of a split-gate MOSFET according to an embodiment of the invention.

FIG. **2**A to FIG. **2**H are cross-sectional schematics of the manufacturing process of a split-gate MOSFET according to another embodiment of the invention.

FIG. **3** is a current-voltage curve of the drain of simulation target 2.

FIG. **4** is a current-voltage curve of the drain of simulation target 1.

FIG. **5** is a graph of the distribution of total current density of simulation target 1 and simulation target 2.

FIG. **6** shows graphs of the distribution of doping concentration of simulation target 1 and simulation target 2.

FIG. **7** shows graphs of the distribution of electric field of simulation target 1 and simulation target 2.

FIG. **8** shows graphs of impact generation rate of simulation target 1 and simulation target 2.

FIG. **9** shows graphs of the distribution of potential of simulation target 1 and simulation target 2.

FIG. **10** is a graph of the distribution of doping concentration of simulation target 3.

FIG. **11** is a graph of the distribution of total current density of simulation target 3.

FIG. **12** is a graph of the distribution of potential of simulation target 3.

DESCRIPTION OF THE EMBODIMENTS

The figures in the following embodiments are intended to more comprehensively describe the exemplary embodiments of the inventive concept, but the invention can still be implemented in many different forms, and the invention should not be construed as limited to the recited embodiments. In the figures, for clarity, the relative thickness and location of film layers, regions, and/or structural devices may be reduced or enlarged. Moreover, in the present specification, "first", "second", "third" . . . etc. are used to describe different regions, film layers, and/or blocks, but such terms are only intended to differentiate a region, film layer, or block from another region, film layer, or block. Therefore, a first region, film layer, or block discussed below can be referred to as a second region, film layer, or block without compromising the teaching of the embodiments.

FIG. **1** is a cross-sectional schematic of a split-gate MOSFET according to an embodiment of the invention.

Referring to FIG. **1**, the split-gate MOSFET of the present embodiment at least has a cell region **10** and a terminal region **11** including a substrate **100**, a first epitaxial layer **102**, a second epitaxial layer **104**, a first gate **106***a*, a second gate **108**, a third gate **106***b*, gate oxide layers **110***a* to *b*, a trench oxide layer **112**, and a trench implantation region **114**. In particular, the first epitaxial layer **102** is formed on the substrate **100**, and the first epitaxial layer **102** has a first doping concentration; the second epitaxial layer **104** is formed on the first epitaxial layer **102**, wherein the second epitaxial layer **104** has a second doping concentration greater than the first doping concentration sufficient to reduce the resistance of the cell region **10** of the split-gate MOSFET such that the turn-on current (RD_{SON}) may be reduced. The conductive type of the first epitaxial layer **102** and the second epitaxial layer **104** is, for instance, n-type. A plurality of trenches **116** is in the first epitaxial layer **102** and the second epitaxial layer **104**, and the trenches **116** pass through the second epitaxial layer **104** and are extended in the first epitaxial layer **102**. The first gate **106***a* and the second gate **108** are both located within the trenches **116** of the cell region **10**, wherein the second gate **108** is located on the first gate **106***a*. The third gates **106***b* are respectively located in each of the trenches **116** in the terminal region **11**, wherein the third gate **106***b* closest to the cell region **10** is grounded (GND), and the rest of the third gates **106***b* are floating gates. The first gate **106***a* and the third gate **106***b* are preferably formed by the same deposition process, and therefore the same reference numerals are used in the figure to represent gates located at different regions. In an embodiment, the number of the trench **116** having the third gate **106***b* in the terminal region **11** is, for instance, 2 to 4, but the number can be increased as needed. Moreover, the gate oxide layer **110***a* is located between the first gate **106***a* and the second gate **108** and the gate oxide layer **110***b* is located between the second gate **108** and the second epitaxial layer **104**, the gate oxide layers **110***a* and **110***b* are generally the same film layer formed by the same process, and two reference numerals are adopted here to represent gate oxide layers located at different regions. The trench oxide layer **112** is located between the first gate **106***a* and the first epitaxial layer **102** and located between the surface of the trench **116** and the third gate **106***b* in the terminal region **11**.

Referring further to FIG. **1**, the trench implantation region **114** is located in the first epitaxial layer **102** of a bottom **116***a* of each of the trenches **116**, wherein the trench implantation region **114** has a third doping concentration, and the third doping concentration is less than the first doping concentration of the first epitaxial layer **102**. In the case that the first and second epitaxial layers **102** and **104** are n-type, in the trench implantation region **114**, the doping concentration of the first epitaxial layer **102** of the bottom **116***a* of the trench **116** is generally reduced by implanting a dopant (such as boron) having the opposite conductive type (p-type). Since the trench implantation region **114** for which the doping concentration is reduced has a greater resistance, if the trench implantation region **114** in the cell region **10** can cover the bottom **116***a* of each of the trenches **116**, then the release of maximum electric field at the corners of the trench can be facilitated. Moreover, an interface **118** of the first epitaxial layer **102** and the second epitaxial layer **104** can be in contact with the trench implantation region **114** or slightly higher than the trench implantation region **114**. In the present embodiment, a thickness t**1** of the gate oxide layers **110***a* to *b* is generally less than a thickness t**2** of the trench oxide layer **112**, and since the first doping concentration of the first epitaxial layer **102** is low enough and does not need to be the same as the second doping concentration of the second epitaxial layer **104**, a width of a depletion region for high-voltage application can be maintained, and the thickness t**2** of the trench oxide layer **112** does not need to be increased due to the application of high-voltage field. As a result, the cell pitch of the cell region **10** of the split-gate MOSFET can be reduced and therefore higher breakdown voltage (BVDSS) can be achieved. A width w**2** of the second gate **108** can be greater than a width w**1** of the first gate **106***a* as shown in FIG. **1**, or the two can be the same. When the width w**2** of the second gate **108** is greater than the width w**1** of the first gate **106***a*, the second gate **108** can further include an extending portion **120** extended to a sidewall **107** of the first gate **106***a*.

Referring further to FIG. **1**, in the split-gate MOSFET, a p-type well **122** can be further included on the second epitaxial layer **104**, wherein an interface **124** of the p-type well **122** and the second epitaxial layer **104** can be adjacent to the gate oxide layer **110***a* between the first gate **106***a* and the second gate **108**, such as level with or slightly lower or slightly higher than the gate oxide layer **110***a*. The p-type well **122** in the terminal region **11** is located between the trenches **116**. Moreover, a source doped region **126** of the cell region **10** of the general split-gate MOSFET can be electrically connected to a conductive layer **132** above via vias **130** located in an insulation layer **128**, wherein the conductive layer **132** is, for instance, a metal layer. The surface of the first epitaxial layer **102** is not formed in the substrate **100** on the drain portion of the cell region **10** of the split-gate MOSFET, which is prior art and is not repeated herein. Moreover, the third gate **106***b* in the terminal region **11** closest to the cell region **10** and the p-type well **122** in the cell region **10** can be equipotential, and therefore, as shown in FIG. **1**, the effect of equipotential of the third gate **106***b* and the p-type well **122** can be achieved via the vias **130**

located in the insulation layer **128** and the conductive layer **134** above the vias **130**. However, the invention is not limited thereto, and other designs can also be adopted to achieve the effect.

FIG. **2**A to FIG. **2**H are cross-sectional schematics of the manufacturing process of a split-gate MOSFET according to another embodiment of the invention.

Referring to FIG. **2**A, a first epitaxial layer **202** is first simultaneously formed on a substrate **200** of a cell region **20** and a terminal region **21**, and then a second epitaxial layer **204** is formed, wherein the processes of the first epitaxial layer **202** and the second epitaxial layer **204** are similar, wherein a bigger difference is that the doping concentration of the second epitaxial layer **204** is greater than the doping concentration of the first epitaxial layer **202**. Next, an entire mask layer **206** is formed to cover the second epitaxial layer **204**.

Then, referring to FIG. **2**B, the mask layer **206** is patterned to expose the portion in which a trench **208** is to be formed, and then the mask layer **206** is used as an etch mask. The etching passes through the second epitaxial layer **204** and continues in the first epitaxial layer **202** to form the trench **208**.

Next, referring to FIG. **2**C, a trench implantation step is performed to form a trench implantation region **210** in the first epitaxial layer **202** of a bottom **208***a* of each of the trenches **208**. If the first epitaxial layer **202** is n-type, then a p-type dopant (such as boron) is used in the trench implantation step to reduce the concentration of a portion of the first epitaxial layer **202**. Therefore, the doping concentration of the trench implantation region **210** is less than the doping concentration of the first epitaxial layer **202**. In the present embodiment, an interface **212** of the first and second epitaxial layers **202** and **204** is in contact with the trench implantation region **210**, but the invention is not limited thereto. Then, the mask layer **206** shown in FIG. **2**B can be removed.

Next, referring to FIG. **2**D, thermal oxidation is performed to form an oxide layer **214** on the surface exposed by the first and second epitaxial layers **202** and **204** (i.e., the surface of the trench **116**), and then a conductive layer **216** is comprehensively deposited on the substrate **200**.

Next, referring to FIG. **2**E, the conductive layer **216** of FIG. **2**D can be first planarized via CMP to expose the oxide layer **214** of FIG. **2**D, and then a portion of the oxide layer is removed by wet etching to leave the portion used as the trench oxide layer **218**, wherein the height of the trench oxide layer **218** of the cell region **20** can be made less than the height of the trench oxide layer **218** of the terminal region **21** by, for instance, controlling the length of the etching time and using an etch mask (not shown). Next, the exposed portion of the conductive layer is removed to respectively obtain a first gate **220***a* and a third gate **220***b*. When the first gate **220***a* is slightly protruding as shown in the figure, the subsequently-formed structure can cover the top of the first gate **220***a*.

Next, referring to FIG. **2**F, a gate oxide layer **222** and a second gate **224** are formed on the surface of the trench **208** of the cell region and on the first gate **220***a* in the trench **208**, and the manufacturing methods of the gate oxide layer **222** and the second gate **224** are as shown in the method of FIG. **2**D to FIG. **2**E. A thickness t**1** of the gate oxide layer **222** is generally less than a thickness t**2** of the trench oxide layer **218**, and a width w**2** of the second gate **224** can be greater than a width w**1** of the first gate **220***a*.

Next, referring to FIG. **2**G, a p-type well **226** is comprehensively formed on the surface of the second epitaxial layer **204** of the cell region **20** and the terminal region **21** via a plurality of doping steps. The doping steps are, for instance, a first p-type doping step in which the dose is low and the energy is low, a second p-type doping step in which the dose is medium and the energy is medium, and a third p-type doping step in which the dose is high and the energy is high. Next, an n-type doping step can be additionally performed in the cell region **20** to form a source doped region **228**, and a drain doped region (not shown) can also be formed on the other side of the substrate **200**. Next, an insulation layer **232** is formed to cover the entire cell region **20** and the terminal region **21**, and a plurality of via openings **234** passing through the insulation layer **232** is formed, wherein the via openings **234** in the cell region **20** can further pass through the source doped region **228** and be extended to the p-type well **226**, and the via openings **234** in the terminal region **21** can be further extended to the p-type well **226** or extended to the third gate **220***b* closest to the cell region **20**. Next, a p+ doped region **236** can be optionally formed in the via openings **234**.

Lastly, referring to FIG. **2**H, vias **238** are formed in the via openings **234**, and then conductive layers **240** and **242** connected to the vias **238** are formed on the insulation layer **232**, wherein the conductive layers **240** and **242** can be metal layers.

To verify the effects of the invention, several simulation experiments are provided below, but the scope of the invention is not limited to the following experiments.

Simulation target 1: the cell region of the split-gate MOSFET of the invention, wherein the thickness of the first epitaxial layer is about 4.5 microns and the phosphorous dopant amount is 7e15 ions/cm^2; the thickness of the second epitaxial layer is about 5 microns and the phosphorous dopant amount is 3.1e16 ions/cm^2; the boron dopant amount of the trench implantation region is 5e12 ions/cm^2.

Simulation target 2: the cell region of the split-gate MOSFET of a control group, wherein the trench implantation region of simulation target 1 is omitted, and only one epitaxial layer having a thickness of about 9.5 microns and a phosphorous dopant amount of 3.1e16 ions/cm^2 is included, and the rest are all the same as simulation target 1.

Simulation target 3: the terminal region of the split-gate MOSFET of the invention having 3 trenches, and the gate closest to the cell region and the p-type well are equipotential, and the rest of the gates are floating gates. The other parameters are the same as those of simulation target 1.

Simulation Results

FIG. **3** is a current-voltage curve of the drain of simulation target 2, and FIG. **4** is a current-voltage curve of the drain of simulation target 1. It can be known from the comparison of FIG. **3** and FIG. **4** that, the split-gate MOSFET of the invention can be applied in a voltage field of 100 V or above.

The left side of FIG. **5** is a graph of the distribution of total current density of simulation target 2, and the right side of FIG. **5** is a graph of the distribution of total current density (unit: A/cm^2) of simulation target 1. It can be known from FIG. **5** that, the current density of the split-gate MOSFET of the invention is higher.

The left side of FIG. **6** is a graph of the distribution of doping concentration of simulation target 2, and the right side of FIG. **6** is a graph of the distribution of doping concentration of simulation target 1 (unit: ions/cm^3) (the numeric value in FIG. **6** is the value of n of 10^n). It can be seen from FIG. **6** that, the bottom of the trench of the split-gate MOSFET of the invention has a region having lower doping concentration, and the doping concentration of

the epitaxial layer in the periphery of the trench is higher than the doping concentration of the epitaxial layer below the trench.

The left side of FIG. **7** is a graph of the distribution of electric field of simulation target 2, and the right side of FIG. **7** is a graph of the distribution of electric field of simulation target 1. It can be known from FIG. **7** that, the split-gate MOSFET of the invention can prevent high potential at the corners of the trench.

The left side of FIG. **8** is a graph of impact generation (Gen) rate of simulation target 2, and the right side of FIG. **8** is a graph of impact generation rate of simulation target 1. It can be known from FIG. **8** that, the impact generation rate of the split-gate MOSFET of the invention is more uniform.

The left side of FIG. **9** is a graph of the distribution of potential of simulation target 2, and the right side of FIG. **9** is a graph of the distribution of potential of simulation target 1. It can be known from FIG. **7** that, the split-gate MOSFET of the invention can withstand a higher electric potential.

FIG. **10** is a graph of the distribution of doping concentration of simulation target 3 (the numeric value in FIG. **10** is the value of n of 10^n). It can be seen from FIG. **10** that, the bottom of the trench of the split-gate MOSFET of the invention has a region having lower doping concentration, and the doping concentration of the epitaxial layer close to the periphery of the trench is higher than the doping concentration of the epitaxial layer below the trench.

FIG. **11** is a graph of the distribution of total current density of simulation target 3. It can be known from FIG. **11** that, the current density of the split-gate MOSFET of the invention is gradually reduced from the terminal region toward the edge.

FIG. **12** is a graph of the distribution of potential of simulation target 3. It can be known from FIG. **12** that, the field of the terminal region of the split-gate MOSFET of the invention is reduced and extended to the edge, and withstands an electric potential reaching 150 V or above.

Based on the above, in the invention, the width of the depletion region for high-voltage application is maintained via the epitaxial layer having low doping concentration, and the resistance of the split-gate MOSFET is reduced via an epitaxial layer having high doping concentration, and at the same time, maximum electric field at the corners of the trench can be released in the implantation region having doping concentration at the bottom of the trench. Therefore, the split-gate MOSFET of the invention can achieve the effect of low on-resistance, application in a high voltage field of 100 V or above can be achieved without increasing the thickness of the trench oxide layer, the thickness of the trench oxide layer can be thin, and an additional lithography process is not needed.

Although the invention has been described with reference to the above embodiments, it will be apparent to one of ordinary skill in the art that modifications to the described embodiments may be made without departing from the spirit of the invention. Accordingly, the scope of the invention is defined by the attached claims not by the above detailed descriptions.

What is claimed is:

1. A split-gate MOSFET at least having a terminal region and a cell region, comprising:

a substrate;

a first epitaxial layer formed on the substrate, wherein the first epitaxial layer has a first doping concentration;

a second epitaxial layer formed on the first epitaxial layer, wherein the second epitaxial layer has a second doping concentration greater than the first doping concentration, a plurality of trenches is in the first epitaxial layer and the second epitaxial layer, and the plurality of trenches pass through the second epitaxial layer and is extended into the first epitaxial layer;

a plurality of first gates respectively located within the plurality of trenches in the cell region;

a plurality of second gates respectively located within the plurality of trenches on the first gate in the cell region;

a plurality of third gates respectively located in the plurality of trenches in the terminal region, wherein the third gate closest to the cell region is grounded, and the rest of the plurality of third gates are floating gates;

a gate oxide layer located between the first gate and the second gate and located between the second gate and the second epitaxial layer;

a trench oxide layer located between the first gate and the first epitaxial layer and located between a surface of the plurality of trenches and the third gate in the terminal region; and

a trench implantation region located in the first epitaxial layer at a bottom of each of the plurality of trenches in the terminal region and the cell region, wherein the trench implantation region has a third doping concentration less than the first doping concentration.

2. The split-gate MOSFET of claim **1**, wherein the trench implantation region covers the bottom of each of the plurality of trenches.

3. The split-gate MOSFET of claim **1**, wherein an interface of the first epitaxial layer and the second epitaxial layer is adjacent to the trench implantation region.

4. The split-gate MOSFET of claim **1**, wherein an interface of the first epitaxial layer and the second epitaxial layer is in contact with the trench implantation region.

5. The split-gate MOSFET of claim **1**, wherein a thickness of the gate oxide layer is less than a thickness of the trench oxide layer.

6. The split-gate MOSFET of claim **1**, wherein a width of the second gate is greater than a width of the first gate.

7. The split-gate MOSFET of claim **1**, wherein the second gate further comprises an extending portion extended to a sidewall of the first gate.

8. The split-gate MOSFET of claim **1**, wherein a conductive state of the first epitaxial layer and the second epitaxial layer is n-type.

9. The split-gate MOSFET of claim **8**, further comprising a p-type well located on the second epitaxial layer.

10. The split-gate MOSFET of claim **9**, wherein an interface of the p-type well and the second epitaxial layer is adjacent to the gate oxide layer between the first gate and the second gate.

11. The split-gate MOSFET of claim **9**, wherein the third gate closest to the cell region and the p-type well in the cell region are equipotential.

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