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(71) Applicant: **THE HONG KONG UNIVERSITY OF SCIENCE AND TECHNOLOGY** [CN/CN]; Clear Water Bay, Kowloon, Hong Kong (CN).

(72) Inventors: **CHEN, Jing**; Tower 6, 6 B, Senior Staff Quarter, The Hong Kong University of Science, and Technology, Clear Water Bay, Kowloon, Hong Kong (CN). **TANG, Gaofei**; 2/F, 98A, Tai Po Tsai Village, Clear Water Bay Road, Kowloon, Hong Kong (CN).

(74) Agent: **TEE & HOWE INTELLECTUAL PROPERTY ATTORNEYS**; CHEN, Yuan, 10th Floor, Tower D, Minsheng Financial Center, 28 Jianguomennei Avenue, Dongcheng District, Beijing 100005 (CN).

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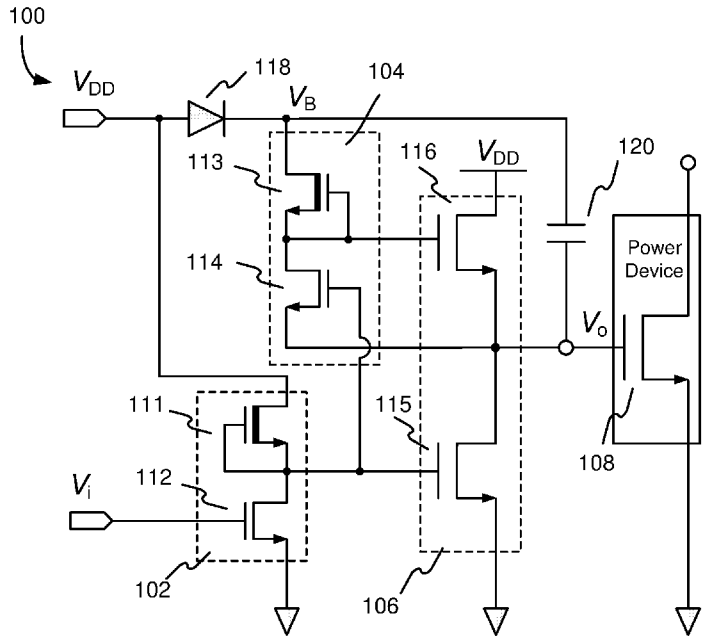

FIG. 1

(57) Abstract: A self-bootstrap integrated gate driver circuit with high driving speed, enhanced driving capability and rail-to-rail output. A capacitor (120) and a diode (118) are used with a first inverter (102) coupled to a control signal input terminal, a second inverter (104) coupled to the first inverter (102), a push-pull circuit (106) comprising a pull-up transistor (116) and a pull-down transistor (115) and a power device comprising a power device transistor (108) with a gate. The control signal input at one state controls the first inverter (102) to a first output state, turns on the pull-down transistor (115) to discharge the gate of the power device transistor (108), turns off the power device and charges the capacitor (120) through the diode (118). The control signal input in another state controls the first inverter (102) to a second output state, turns off the pull-down transistor (115) and turns on the pull-up transistor (116) via the capacitor (120) to turn on the power device.

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POWER DEVICE WITH INTEGRATED GATE DRIVER

CROSS REFERENCE TO RELATED APPLICATION

[0001] This application claims priority to U.S. Provisional Patent Application number 62/391,554, filed on May 4, 2016, entitled: "GaN POWER DEVICE WITH INTEGRATED GATE DRIVER," the entirety of which application is hereby incorporated herein by reference.

TECHNICAL FIELD

[0002] This disclosure generally relates to power semiconductor devices, including a gate driver integrated with a power device.

BACKGROUND

[0003] Gallium nitride (GaN)-based semiconductor devices are generally known for having high breakdown voltage, high switching speed and low on-resistance characteristics. For example, GaN-based lateral heterojunction (e.g. AlGaN/GaN) devices have shown promise as the core power switching devices in high-performance power conversion systems.

[0004] While discrete GaN power devices have already shown better performance than conventional silicon power devices, the peripheral control / driving modules are mainly implemented with a separate silicon-based integrated circuit (IC), leading to a Si-driver/GaN-switch hybrid driving solution. With such a hybrid solution, the inter-chip bonding wires or interconnects on a printed circuit board would present

significant parasitic inductances / capacitances, which tend to degrade the circuit performance under high-frequency switching operations.

[0005] A two-stage gate driver integrated with a GaN power device has been realized previously. However, the circuit topology of this device has a number of adverse issues, including that the source current drops quickly with increased output voltage, as a result of the reduced gate-to-source voltage of one of the enhancement-mode transistors in the buffer stage when the load is being charged up; the charging process severely slows down when the source current becomes very small as the gate-to-source voltage approaches the device's threshold voltage. Another issue with this circuit is that the amplitude of the output voltage is smaller than the supply voltage, raising the possibility that power devices driven with this circuit cannot be fully turned on. The problem is even more severe when the gate driver is integrated with a power device with a larger threshold voltage. Using a larger supply voltage in the gate driver circuit may alleviate this problem, but would result in a larger gate voltage stress on some of the gate driver's inverter transistors and the corresponding larger power consumption in the driver circuit.

SUMMARY

[0006] This Summary is provided to introduce a selection of representative concepts in a simplified form that are further described below in the Detailed Description. This Summary is not intended to identify key features or essential features of the claimed subject matter, nor is it intended to be used in any way that would limit the scope of the claimed subject matter.

[0007] Briefly, one or more aspects of the technology described herein are directed towards an integrated circuit comprising a bootstrap circuit comprising a capacitor and a diode, a first inverter circuit coupled to a control signal input terminal, a second inverter circuit coupled to the first inverter circuit, a push-pull circuit comprising a pull-up transistor and a pull-down transistor and a power device comprising a power device transistor with a gate. In response to the control signal input terminal controlling the first inverter to a first output state, the pull-down transistor turns on, to discharge the gate of the power device, turn off the power device and charge the capacitor through the diode. In response to the control signal input terminal controlling the first inverter to a second output state, the pull-down transistor turns off and the pull-up transistor turns on via the capacitor to turn on the power device.

[0008] Other advantages may become apparent from the following detailed description when taken in conjunction with the drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] The technology described herein is illustrated by way of example and not limited in the accompanying figures in which like reference numerals indicate similar elements and in which:

[0010] FIG. 1 is an example block diagram representation of a gate driver circuit comprising a bootstrap capacitor and diode integrated with a power device, according to one or more example implementations.

[0011] FIG. 2 is an example block diagram representation of the circuit of FIG. 1 showing current flow during a discharging process, according to one or more example implementations.

[0012] FIG. 3 is an example block diagram representation of the circuit of FIG. 1 showing current flow during a charging process, according to one or more example implementations.

[0013] FIG. 4A is a graphical representation that plots relative source currents of a bootstrap gate driver circuit and a non-bootstrap gate driver circuit versus output voltage, according to one or more example implementations.

[0014] FIG. 4B is a graphical representation that plots relative output voltage amplitudes of a bootstrap gate driver circuit and a non-bootstrap gate driver circuit, according to one or more example implementations.

[0015] FIG. 5 is an example block diagram representation of an alternative bootstrap gate driver circuit having an additional inverter stage, according to one or more example implementations.

[0016] FIG. 6 is an example block diagram representation of an alternative bootstrap gate driver circuit having enable logic, according to one or more example implementations.

[0017] FIG. 7 is an example block diagram representation of an alternative bootstrap gate driver circuit having separate charging and discharging gate loops, according to one or more example implementations.

[0018] FIG. 8A is a block diagram representation of an example setup for evaluating driving capability of the bootstrap gate driver circuit, according to one or more example implementations.

[0019] FIG. 8B is a graphical representation demonstrating the driving capability of the circuit of FIGS. 1 – 3 when used with the example setup of FIG. 8A, according to one or more example implementations.

[0020] FIG. 9A is an example representation of schematic waveforms of the bootstrap gate driver circuit, according to one or more example implementations.

[0021] FIG. 9B is a graphical representation of the current versus voltage for a bootstrap gate driver circuit relative to a non-bootstrap gate driver circuit, according to one or more example implementations.

[0022] FIG. 10 is a graphical representation of measured voltage waveforms with a five-megahertz pulse width modulated input signal to the circuit of FIGS. 1 – 3, according to one or more example implementations.

[0023] FIG. 11A is a block diagram representation of an example setup for inputting a 25-megahertz input signal to the circuit of FIGS. 1 – 3, according to one or more example implementations.

[0024] FIG. 11B shows measured voltage waveforms with the example setup of FIG. 11A, according to one or more example implementations.

[0025] FIG. 12 is a block diagram representation of an example bootstrap gate driver circuit with resistive-load switching, according to one or more example implementations.

[0026] FIG. 13 is a representation of the switching waveforms of the bootstrap gate driver circuit with resistive-load switching of FIG. 12, according to one or more example implementations.

DETAILED DESCRIPTION

[0027] Various aspects of the technology described herein are generally directed towards a bootstrap circuit that may be integrated with a power device. For example, the integration of the circuit for driving a gallium nitride (GaN) power device effectively reduces parasitic parameters, while also increasing the charging speed relative to other gate drivers. Further, the amplitude of the output voltage of the self-bootstrap gate driver circuit described herein can reach the supply voltage rail, providing rail-to-rail driving signal.

[0028] As will be understood, one example usage of such a circuit includes a DC/DC converter. The circuit may be used in power conversion systems with high switching frequencies (up to a few hundreds of megahertz), and for example may be used in switch-mode power supplies, UPS (uninterrupted power supplies), data centers, motor drives and the like.

[0029] In one or more implementations, GaN-based power devices with an integrated gate driver are described herein. Such an integrated circuit features enhancement-mode GaN power device that operate with high-voltage blocking capability (e.g. 100~1,000 V between source and drain) and an integrated gate driver circuit that operates under a relatively low supply voltage (e.g. 5 to 10 V). The various components, including transistors, diode, capacitor and/or resistors may be integrated in the gate driver circuit on a GaN-on-Si platform. The GaN-based gate

drive circuit, when monolithically integrated with GaN power devices, benefits from significantly reduced parasitic effects and consequently improved switching performance. The gate drive circuit described herein employs a self-bootstrap scheme, providing for the amplitude of the generated drive signal able to reach the supply voltage of the gate driver to achieve rail-to-rail output, enhanced driving capability and fast charging speed relative to other circuits.

[0030] It should be understood that any of the examples herein are non-limiting. For example, a number of circuits are shown with field effect transistors, but it is understood that these are only examples. As such, the technology described herein is not limited to any particular implementations, embodiments, aspects, concepts, structures, functionalities or examples described herein. Rather, any of the implementations, embodiments, aspects, concepts, structures, functionalities or examples described herein are non-limiting, and the technology may be used in various ways that provide benefits and advantages in switching concepts in general.

[0031] Moreover, the numerous techniques of the present application are described with particular reference example implementations. For simplicity and clarity of illustration, the drawing figures illustrate various general manners of construction, and some descriptions and/or details of well-known features and techniques may be omitted to avoid unnecessarily obscuring the description. Additionally, elements in the drawing figures are not necessarily drawn to scale, some areas or elements may be expanded to help improve understanding. Still further, the terms “first,” “second,” “third,” “fourth,” and the like may be used for distinguishing between similar elements and not necessarily for describing a particular sequential or chronological order. It is to be understood that the terms so used are interchangeable. Furthermore, the terms “comprise,” “include,” “have,” and any variations thereof, are intended to cover

non-exclusive inclusions, such that a process, method, article, apparatus, or composition that comprises a list of elements is not necessarily limited to those elements, but may include other elements not expressly listed or inherent to such process, method, article, apparatus, or composition.

[0032] It is contemplated and intended that the design of the controlling portion in the present application can be applied to other heterostructures such as InAlN/GaN, AlN/GaN, or other semiconductor materials, including a silicon device, a silicon carbide device, a gallium nitride device or a gallium arsenide device; for clarity, the examples are based on an AlGaN/GaN-on-Si platform. However, these are only non-limiting examples, and many variations to modify the design to make other combinations and forms of such designs are generally able to be employed.

[0033] In general, and as represented in the example implementation of FIG. 1, a self-bootstrap type integrated gate driver 100 comprises an input (first) inverter stage 102, a logic (second inverter) stage 104 and a push-pull stage 106 generally directed towards charging and discharging a load stage, shown as a power device 108. The power device 108 may be integrated with the gate driver 100 on the same chip. As will be understood, the transistors 111 – 116, along with a diode 118 and a capacitor 120, provide a gate drive circuit with enhanced driving capability, higher driving speed and rail-to-rail output.

[0034] In FIG. 1, the exemplified input inverter stage 102 comprises a depletion-mode transistor 111 and an enhancement-mode transistor 112, which translate and reshape the input signal V_i for use by the subsequent logic stage 104 and a pull-down transistor 115 of the push-pull stage 106. As can be seen, the source terminals of the transistor 112 and the pull-down transistor 115 are tied together to

achieve the same logic '0' reference between the inverter stage 102 and the pull-down transistor 105.

[0035] The exemplified logic stage 104 comprises a depletion-mode transistor 113 and an enhancement-mode transistor 114, which form the second inverter that inverts the signal from the input inverter stage 102 to control a pull-up transistor 116 of the push-pull stage 106. The source terminals of the transistor 114 and the pull-up transistor 116 are tied together to achieve the same logic reference between the logic stage (second inverter) 104 and the pull-up transistor 116. Thus, the transistors 115 and 116 form the push-pull stage 106 that charges and discharges the load stage (power device) 108.

[0036] In general, the diode 108 and capacitor 109 form a bootstrap circuit to provide power supply for the logic stage (second inverter) 104 and the pull-up transistor 116. More particularly, the operation of the gate driver is shown in FIG. 2 (discharging process) and FIG. 3 (charging process).

[0037] In the discharging process shown in FIG. 2, when the input signal V_i is at a logic '0' state, the pull-down transistor 115 is fully turned on by the current flow from V_{DD}, whereby the power device 108 (its gate) is turned off. In this state, the bootstrap capacitor 120 is charged by the supply voltage V_{DD} through the bootstrap diode 118, until V_B is V_{DD}-V_{DB} (where V_{DB} is the turn-on voltage of the bootstrap diode 108). When charged, the capacitor 120 serves as the power supply for the second inverter 104 formed by the transistors 113 and 114.

[0038] In the charging process shown in FIG. 3, when the input signal V_i is a logic '1' state and V_i' is at a logic '0' state, the pull-down transistor 115 is turned off and the logic stage (second inverter) 104 formed by transistors 113 and 114 outputs a logic

'1' state. Note that the voltage levels of logic '0' / '1' for the logic stage (second inverter) 104 are V_o / V_B, whereas the voltage levels of logic '0' / '1' for the input (first) inverter stage 102 are GND / V_{DD}.

[0039] Because the voltage across the bootstrap capacitor 120 (V_B - V_o) can be kept near (V_{DD} - V_{DB}), the gate-to-source voltage V_{GSU} of the pull-up transistor 116 is kept at (V_{DD} - V_{DB}), whereby in general the pull-up transistor 116 is always on during the charging process and V_o is rapidly charged to V_{DD}, achieving rail-to-rail output.

[0040] FIG. 4A is a graphical representation that plots the source current I_{source} of the gate driver 100 (FIGS. 1 - 3) during circuit operation. As can be seen by the solid line in FIG. 4A, the source current I_{source} of the gate driver is kept at a high level during the charging process, in contrast to the dashed line which drops quickly for a gate driver circuit without the bootstrap technology described herein. Further, the gate driver 100 of FIGS. 1 – 3 rapidly charges the power device transistor's gate to a voltage of V_{DD}; the solid line in FIG. 4B shows the amplitude of gate driver's output voltage under different V_{DD} supply voltages. Indeed, the gate driver 100 of FIGS. 1 – 3 provides rail-to-rail output as a result of the nearly constant gate-to-source voltage V_{GSU} of the pull-up transistor 116 during the charging process. A gate driver circuit without the bootstrap technology (the dashed line in FIG. 4B) suffers some voltage loss at the output terminal, because the gate-to-source voltage V_{GSU} of a similar pull-up transistor may be larger than its threshold voltage.

[0041] FIG. 5 shows an alternative implementation of a bootstrap gate driver circuit 200, which may be integrated with an (e.g., GaN) power device 208. In the alternative implementation FIG. 5, inverting output is featured. The basic topology of this alternative implementation comprises a first inverter stage with ground as logic '0'

formed by transistors 222 and 223, a second inverter stage with a ground terminal as logic '0' formed by transistors 211 and 212, a third inverter stage with V_o as logic '0' formed by transistors 213 and 214, and a push-pull buffer stage formed by transistors 215 and 216. Also shown are the bootstrap components comprising a bootstrap diode 218 and a bootstrap capacitor 220.

[0042] Any of the gate driver circuits 100 (FIGS. 1-3), 200 (FIG. 5), 300 (FIG. 6, described below) and 400 (FIG. 7, described below) may use similar underlying technologies. Using the circuit 200 of FIG. 5 as an example, the depletion-mode transistors 211, 213 and 222 may be achieved by Schottky-gated high electron mobility transistors (HEMTs) or metal-insulator-semiconductor HEMTs with gate dielectric between the gate metal and semiconductor. The enhancement-mode transistors 212, 214, 215, 216 and 223 may be achieved by different gate structures, such as *p*-type gate, fluorine-plasma treated gate or partially/fully recessed gate. The bootstrap diode 218 may be a Schottky barrier diode (SBD), comprising ohmic metal as the cathode and Schottky metal as the anode. Alternatively, the diode 218 may be achieved by a lateral field effect rectifier (L-FER), comprising an enhancement-mode device with its gate and source tied together as the anode, and the drain terminal as the cathode. The turn-on voltage of the bootstrap diode 218 V_{DB} needs to be such that V_B-V_o (=V_{DD}-V_{DB}) is sufficient to act as the power supply of the inverter formed by the transistors 213 and 214 and pull-up transistor 216.

[0043] The bootstrap capacitor 220 may be achieved by a metal-insulator-metal (MIM) capacitor, a *p*-type gate capacitor or a metal-insulator-semiconductor (MIS) capacitor. Further, the MIM capacitor, *p*-type gate capacitor and MIS capacitor could be paralleled together to achieve a larger capacitance density. Similar to FIGS. 1 - 3, the capacitor 220 is charged when the pull-down transistor 215 is turned on and

V_o is low. The capacitance value needs to store sufficient charge to turn on the pull-up transistor 216 when the V_i input terminal is at the logic low state and the pull-down transistor 215 is turned off.

[0044] FIG. 6 shows another alternative implementation of a bootstrap gate driver circuit 300 including an enable terminal *EN*, which provides a non-inverting output with an enable function. The basic topology of the circuit 300 comprises a NAND logic gate stage with ground terminal as logic '0' formed by transistors 311, 312 and 330, an inverter stage with V_o as logic '0' formed by transistors 313 and 314, a push-pull buffer stage formed by transistors 315 and 316. The bootstrap circuit comprises a bootstrap diode 318 and a bootstrap capacitor 320. As can be seen from the logic, only when the enable terminal *EN* is at the logic high state is the enhancement-mode transistor 330 turned on; in this state, the gate driver may drive the power device 308, such as to with a pulse width modulation signal or the like received at the input terminal V_i.

[0045] FIG. 7 shows another alternative implementation of a bootstrap gate driver circuit 300 that may be integrated with an (e.g., GaN) power device 408. FIG. 7 shows a non-inverting output with separate charging and discharging loops at the gate driver's output terminal V_o. The basic topology of FIG. 7 comprises a first inverter stage with ground terminal as logic '0' formed by transistor 411 and 412, a second inverter stage with V_o as logic '0' formed by transistors 413 and 414, a push-pull buffer stage formed by transistors 415 and 416. The bootstrap components comprise a bootstrap diode 418 and a bootstrap capacitor 420. A resistor 440 is in the charging loop and a resistor 411 is in the discharging loop. The resistors 410 and 411 may be achieved by 2-DEG (2-dimensional electron gas) channel resistor that is intrinsically formed at the AlGaN/GaN interface.

[0046] FIG. 8A shows a measurement setup to exemplify the driving capability of one gate driver circuit with a bootstrap scheme, e.g., the gate driver circuit 100 FIG. 1. The resistor 880 is ten ohms and the capacitor load 882 is 200 pF. FIG. 8B shows the rise time t_r (2.8 nanoseconds) and the fall time t_f (1.6 nanoseconds) for an output drive waveform. As can be seen, the gate driver 100 provides higher driving capability, faster turn-on process and rail-to-rail output; (by way of comparison, a similar circuit without the bootstrap scheme has a significantly larger rise time t_r of 8.8 nanoseconds, a fall time t_f of 1.6 nanoseconds and an output signal with only 4.5-volt amplitude when the power supply is 6.0 volt).

[0047] FIG. 9A shows schematic waveforms of the gate driver circuit 100 (FIG. 1), in which the discharging process corresponds to V_i = '0', and the charging process corresponds to V_i = '1'. As can be seen, during the discharging process, the output of the gate driver is 0 V and the voltage drop (V_B-V_o) across the bootstrap capacitor 120 may be charged to (V_{DD}- V_{DB}); During the charging process, the gate-to-source voltage V_{GSU} of pull-up transistor 116 can be kept near (V_{DD}-V_{DB}) as a result of the stable voltage drop across the bootstrap capacitor, whereby the amplitude of V_o can reach up to V_{DD}.

[0048] FIG. 9B shows a source current I_{source} comparison of the circuit 100 of FIGS. 1 – 3 (the dashed, dotted line) versus a non-bootstrap driver circuit (the dashed line) plotted with the *I-V* curves (the solid line) of the pull-up transistor 116. As can be seen, for the circuit 100 with a bootstrap scheme, the source current I_{source} remains at a high level during the charging process, in contrast to the rapid drop of other schemes. The bootstrap gate driver design is able to charge the power device's gate to voltage of V_{DD}.

[0049] Turning to high frequency operation, FIG. 10 shows the measured voltage waveforms of the implementation of FIGS. 1 - 3 when the input pulse width modulation is five megahertz and V_{DD} is 6.0 volts. The voltage drop across the bootstrap capacitor 120 is approximately 4.5 volts for the turn-on voltage of bootstrap diode 118 is approximately 1.5 volts. The voltage V_B may be elevated to approximately 10.5 volts when V_o is charged up to 6.0 volts.

[0050] FIGS. 11A and 11B demonstrate that the gate driver circuit 100 with the bootstrap scheme works properly under a 25-MHz high frequency input pulse width modulation signal generated by a ring oscillator.

[0051] FIG. 12 shows resistive-load switching, with a load 1240 in the form of an external twenty-ohm resistor. The voltage HV is sixty volts in this example. FIG. 13 shows the voltage waveforms during one test with a switching frequency of five megahertz.

[0052] As can be seen, there is provided a gate driver circuit with a self-bootstrap technology comprising a diode and capacitor. The gate driver circuit has low parasitic inductance, high operation frequency, a convenient control method and high compatibility between peripheral circuits and power devices. Indeed, the gate driver circuit operates appropriately at high frequencies on the order of (at least) 5 to 25 MHz, and operates appropriately under resistive load. The gate driver circuit may be integrated with a power device, e.g., fabricated on the same chip, without the need of a hybrid driving solution.

[0053] One or more aspects are directed towards a gate driver comprising an output terminal coupled to a power device, the gate driver comprising a first transistor comprising a first gate terminal electrically in contact with a first source

terminal, and a first drain terminal electrically in contact with a power supply, and a second transistor comprising a second gate terminal electrically coupled to an input terminal, a second drain terminal electrically in contact with the first source terminal of the first transistor, and a second source terminal electrically in contact with ground. Further aspects comprise a third transistor comprising a third gate terminal electrically in contact with a third source terminal, and a third drain terminal, a diode comprising an anode electrically in contact with the power supply and a cathode electrically in contact with the third drain terminal of the third transistor, and a fourth transistor comprising a fourth gate terminal electrically in contact with the second drain terminal of the second transistor, a fourth drain terminal electrically in contact with the third source terminal of the third transistor, and a fourth source terminal electrically in contact with the output terminal. Further aspects comprise a fifth transistor comprising a fifth gate terminal electrically in contact with the second drain terminal of the second transistor, a fifth drain terminal electrically coupled to the output terminal, and a fifth source terminal electrically in contact with ground, a sixth transistor comprising a sixth gate terminal electrically in contact with the fourth drain terminal of the fourth transistor, a sixth drain terminal electrically in contact with the power supply, and a sixth source terminal electrically in contact with the output terminal, and a capacitor electrically connected between the cathode of the diode and the output terminal.

[0054] The power device may comprise a power device transistor comprising a power device transistor gate terminal electrically connected to the output terminal, a power device transistor drain terminal electrically coupled to a high voltage node, and a power device transistor source terminal electrically in contact with ground.

The power device transistor drain terminal may be electrically coupled to the high voltage node via a load.

[0055] The second gate terminal electrically coupled to the input terminal may be electrically in contact with the input terminal. The fifth drain terminal electrically coupled to the output terminal may be electrically in contact with the output terminal.

[0056] The first transistor may comprise a first depletion-mode transistor and the third transistor may comprise a second depletion-mode transistor. The second transistor may comprise a first enhancement-mode transistor, the fourth transistor may comprise a second enhancement-mode transistor, the fifth transistor may comprise a third enhancement-mode transistor and the sixth transistor may comprise a fourth enhancement-mode transistor.

[0057] Aspects may comprise an inverter stage comprising seventh and eighth transistors. The seventh transistor may comprise a seventh gate terminal electrically in contact with a seventh source terminal, and a seventh drain terminal electrically in contact with the power supply. The eighth transistor may comprise an eighth gate terminal electrically in contact with the input terminal, the drain terminal of the eighth transistor electrically in contact with the seventh source terminal of the seventh transistor, and an eighth source terminal electrically in contact with ground. The second gate terminal of the second transistor may be electrically coupled to the input terminal by being electrically in contact with the seventh drain terminal of the seventh transistor.

[0058] Other aspects may comprise a seventh transistor comprising a seventh drain terminal electrically in contact with the first source terminal of the first transistor, a seventh gate terminal electrically in contact with an enable terminal, and a seventh

source terminal electrically in contact with the second drain terminal of the second transistor.

[0059] Still other aspects may comprise a first resistor connected between the output terminal and the power device and a second resistor connected between the drain terminal of the fifth transistor and the power device. The fifth drain terminal may be electrically coupled to the output terminal via the second resistor and the first resistor.

[0060] At least one of the first, second, third, fourth, fifth or sixth transistors may comprise a silicon device, a silicon carbide device, a gallium nitride device or a gallium arsenide device.

[0061] One or more aspects are directed towards an integrated circuit comprising a bootstrap circuit comprising a capacitor and diode, a first inverter circuit coupled to a control signal input terminal, a second inverter circuit coupled to the first inverter circuit, a push-pull circuit comprising a pull-up transistor and a pull-down transistor and a power device comprising a power device transistor with a gate. In response to the control signal input terminal controlling the first inverter to a first output state, the pull-down transistor turns on to discharge the gate of the power device transistor, turn off the power device and charge the capacitor through the diode. In response to the control signal input terminal controlling the first inverter to a second output state, the pull-down transistor turns off and the pull-up transistor turns on via the capacitor to turn on the power device.

[0062] The first inverter circuit, the second inverter circuit, the push-pull circuit and the power device may comprise respective gallium nitride devices. Aspects may comprise at least one resistor, wherein, in response to the pull-down transistor being

turned on, the gate of the power device transistor is discharged through the at least one resistor.

[0063] The first inverter circuit further may comprise an enable transistor coupled to an enable signal input terminal, the enable signal input terminal configured to be controlled to a disabled state that prevents the first inverter from being controlled to the second output state or to be controlled to an enabled state that allows the first inverter to be controlled to the second output state.

[0064] One or more aspects are directed towards signaling a first inverter stage with a first control voltage to charge a capacitor through a diode coupled to a power supply, turn off a power device and, in a discharging operation, discharge a transistor gate of the power device through a pull-down transistor. Aspects comprise signaling the first inverter stage with a second control voltage to couple the capacitor to a pull-up transistor gate to turn on a pull-up transistor and, in a charging operation, turn on the power device.

[0065] The signaling of the first inverter stage with the first control voltage and the signaling of the first inverter stage with a second control voltage may comprise driving the first inverter stage with a high frequency on and off signal. Other aspects may comprise controlling an enable signal state to a first state that disables the signaling of the first inverter stage with the second control voltage, or to a second state that enables the signaling of the first inverter stage with the second control voltage.

CONCLUSION

[0066] While the invention is susceptible to various modifications and alternative constructions, certain illustrated implementations thereof are shown in the drawings and have been described above in detail. It should be understood, however, that there is no intention to limit the invention to the specific forms disclosed, but on the contrary, the intention is to cover all modifications, alternative constructions, and equivalents falling within the spirit and scope of the invention.

[0067] In addition to the various implementations described herein, it is to be understood that other similar implementations can be used or modifications and additions can be made to the described implementation(s) for performing the same or equivalent function of the corresponding implementation(s) without deviating therefrom. Accordingly, the invention is not to be limited to any single implementation, but rather is to be construed in breadth, spirit and scope in accordance with the appended claims.

WHAT IS CLAIMED IS:

1. A system, comprising:

a gate driver comprising an output terminal coupled to a power device, the gate driver comprising:

a first transistor comprising a first gate terminal electrically in contact with a first source terminal, and a first drain terminal electrically in contact with a power supply;

a second transistor comprising a second gate terminal electrically coupled to an input terminal, a second drain terminal electrically in contact with the first source terminal of the first transistor, and a second source terminal electrically in contact with ground;

a third transistor comprising a third gate terminal electrically in contact with a third source terminal, and a third drain terminal;

a diode comprising an anode electrically in contact with the power supply and a cathode electrically in contact with the third drain terminal of the third transistor;

a fourth transistor comprising a fourth gate terminal electrically in contact with the second drain terminal of the second transistor, a fourth drain terminal electrically in contact with the third source terminal of the third transistor, and a fourth source terminal electrically in contact with the output terminal;

a fifth transistor comprising a fifth gate terminal electrically in contact with the second drain terminal of the second transistor, a fifth drain terminal electrically coupled to the output terminal, and a fifth source terminal electrically in contact with ground;

a sixth transistor comprising a sixth gate terminal electrically in contact with the fourth drain terminal of the fourth transistor, a sixth drain terminal electrically in contact with the power supply, and a sixth source terminal electrically in contact with the output terminal; and

a capacitor electrically connected between the cathode of the diode and the output terminal.

2. The system of claim 1, wherein the power device comprises a power device transistor comprising a power device transistor gate terminal electrically connected to the output terminal, a power device transistor drain terminal electrically coupled to a high voltage node, and a power device transistor source terminal electrically in contact with ground.

3. The system of claim 1, wherein the power device transistor drain terminal is electrically coupled to the high voltage node via a load.

4. The system of claim 1, wherein the second gate terminal electrically coupled to the input terminal is electrically in contact with the input terminal.

5. The system of claim 1, wherein the fifth drain terminal electrically coupled to the output terminal is electrically in contact with the output terminal.

6. The system of claim 1, wherein the first transistor comprises a first depletion-mode transistor and the third transistor comprises a second depletion-mode transistor.

7. The system of claim 1, wherein the second transistor comprises a first enhancement-mode transistor, the fourth transistor comprises a second enhancement-mode transistor, the fifth transistor comprises a third enhancement-mode transistor and the sixth transistor comprises a fourth enhancement-mode transistor.

8. The system of claim 1, further comprising an inverter stage comprising seventh and eighth transistors, the seventh transistor comprising a seventh gate terminal electrically in contact with a seventh source terminal, and a seventh drain terminal electrically in contact with the power supply, and the eighth transistor comprising an eighth gate terminal electrically in contact with the input terminal, the drain terminal of the eighth transistor electrically in contact with the seventh source terminal of the seventh transistor, and an eighth source terminal electrically in contact with ground.

9. The system of claim 8, wherein the second gate terminal of the second transistor is electrically coupled to the input terminal by being electrically in contact with the seventh drain terminal of the seventh transistor.

10. The system of claim 1, further comprising a seventh transistor comprising a seventh drain terminal electrically in contact with the first source terminal of the first transistor, a seventh gate terminal electrically in contact with an enable terminal, and a seventh source terminal electrically in contact with the second drain terminal of the second transistor.

11. The system of claim 1, further comprising a first resistor connected between the output terminal and the power device and a second resistor connected between the drain terminal of the fifth transistor and the power device.

12. The system of claim 11, wherein the fifth drain terminal is electrically coupled to the output terminal via the second resistor and the first resistor.

13. The system of claim 1, wherein at least one of the first, second, third, fourth, fifth or sixth transistors comprises a silicon device, a silicon carbide device, a gallium nitride device or a gallium arsenide device.

14. A system, comprising an integrated circuit, the integrated circuit comprising:

a bootstrap circuit comprising a capacitor and diode;

a first inverter circuit coupled to a control signal input terminal;

a second inverter circuit coupled to the first inverter circuit;

a push-pull circuit comprising a pull-up transistor and a pull-down transistor;

a power device comprising a power device transistor with a gate;

wherein, in response to the control signal input terminal controlling the first inverter to a first output state, the pull-down transistor turns on to discharge the gate of the power device transistor, turn off the power device and charge the capacitor through the diode, and

wherein, in response to the control signal input terminal controlling the first inverter to a second output state, the pull-down transistor turns off and the pull-up transistor turns on via the capacitor to turn on the power device.

15. The system of claim 14, wherein the first inverter circuit, the second inverter circuit, the push-pull circuit and the power device comprise respective gallium nitride devices.

16. The system of claim 14, further comprising at least one resistor, wherein, in response to the pull-down transistor being turned on, the gate of the power device transistor is discharged through the at least one resistor.

17. The system of claim 14, wherein the first inverter circuit further comprises an enable transistor coupled to an enable signal input terminal, the enable signal input terminal configured to be controlled to a disabled state that prevents the first inverter from being controlled to the second output state or to be controlled to an enabled state that allows the first inverter to be controlled to the second output state.

18. A method, comprising:

signaling a first inverter stage with a first control voltage to charge a capacitor through a diode coupled to a power supply, turn off a power device and, in a discharging operation, discharge a transistor gate of the power device through a pull-down transistor; and

signaling the first inverter stage with a second control voltage to couple the capacitor to a pull-up transistor gate to turn on a pull-up transistor and, in a charging operation, turn on the power device.

19. The method of claim 18, wherein the signaling of the first inverter stage with the first control voltage and the signaling of the first inverter stage with a second

control voltage comprises driving the first inverter stage with a high frequency on and off signal.

20. The method of claim 18, further comprising, controlling an enable signal state to a first state that disables the signaling of the first inverter stage with the second control voltage, or to a second state that enables the signaling of the first inverter stage with the second control voltage.

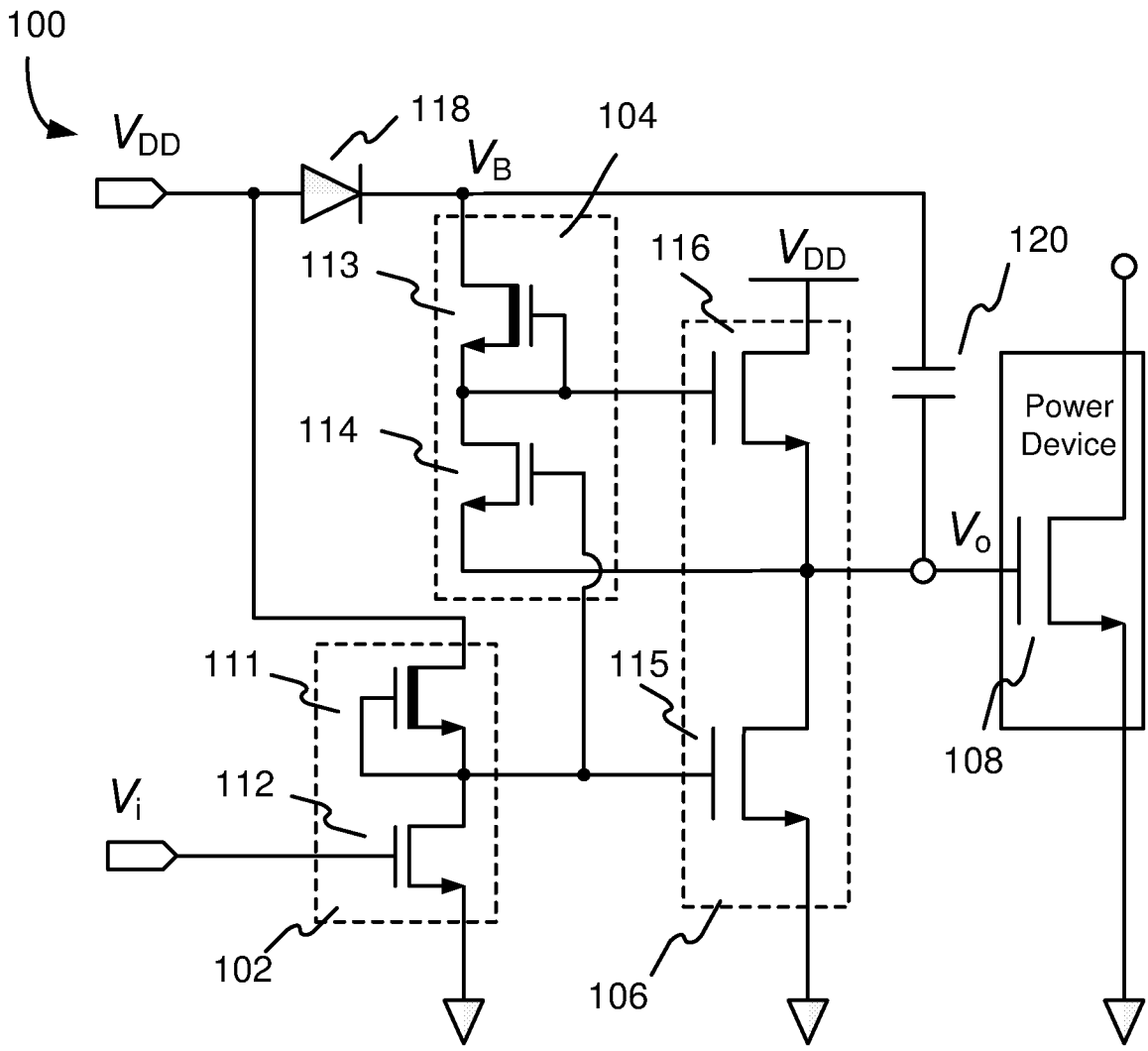
100
V_{DD}
118
V_B
104
113
116
V_{DD}
120
114
Power Device
V_o
111
115
108
V_i
112
102
106

FIG. 1

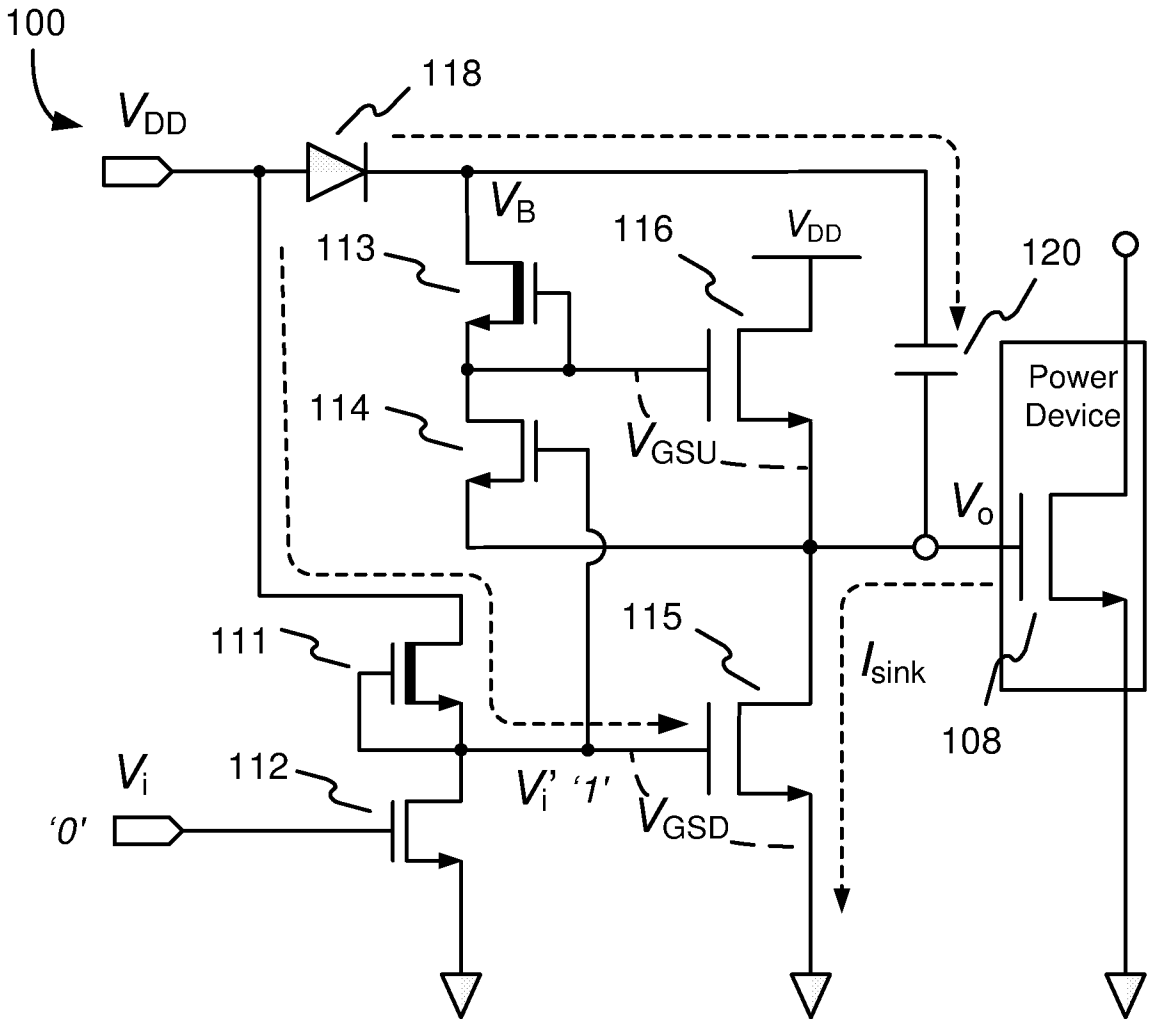
100
V_{DD}
118
V_B
116
V_{DD}
113
120
Power Device
114
V_{GSU}
V_o
111
115
I_{sink}
108
V_i
'0'
112
V_i' '1'
V_{GSD}

FIG. 2

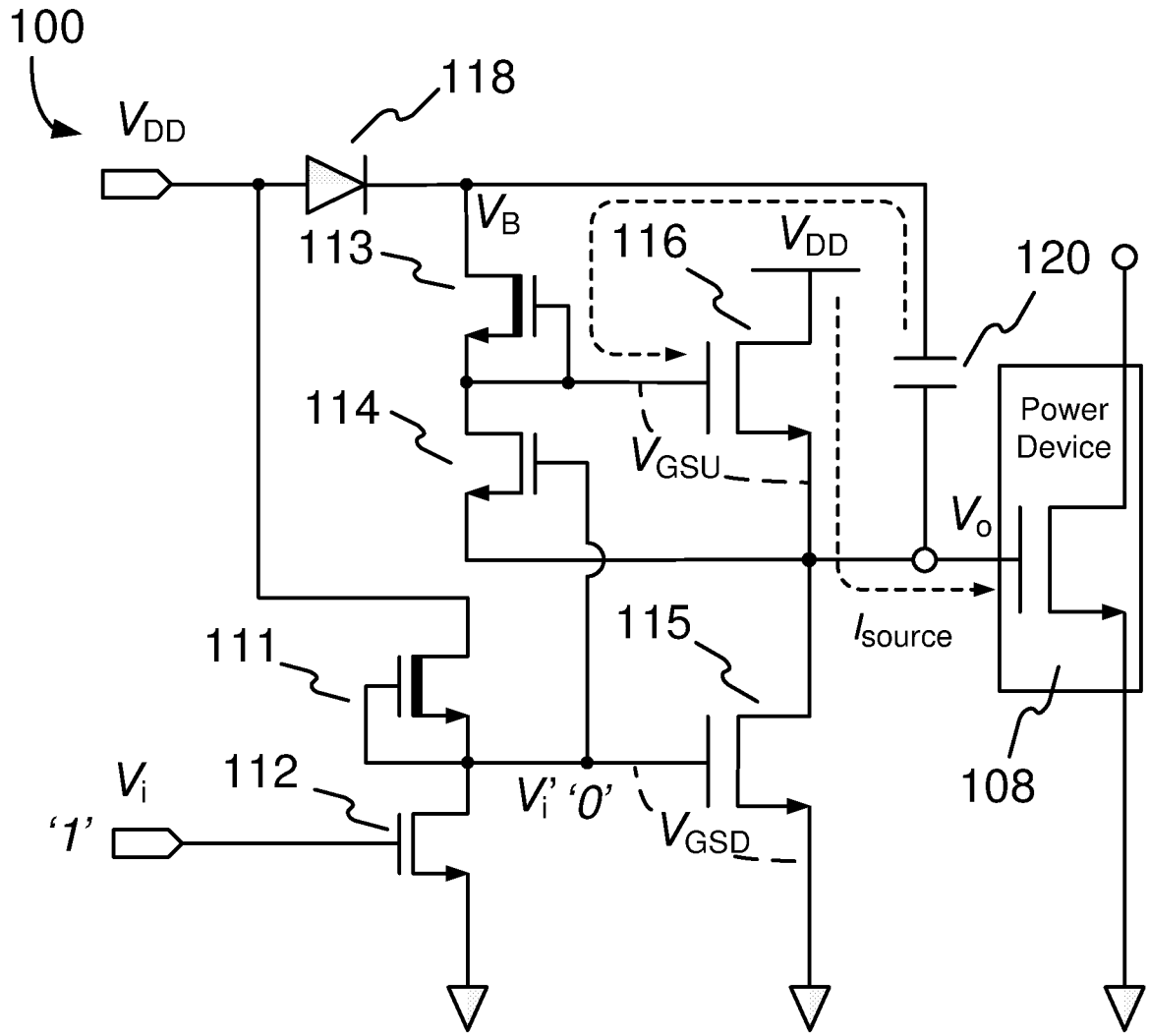
100
118
V_{DD}
V_B
113
116
V_{DD}
120
114
V_{GSU}
Power Device
V_o
I_{source}
111
115
112
V_i
'1'
V_i '0'
V_{GSD}
108

FIG. 3

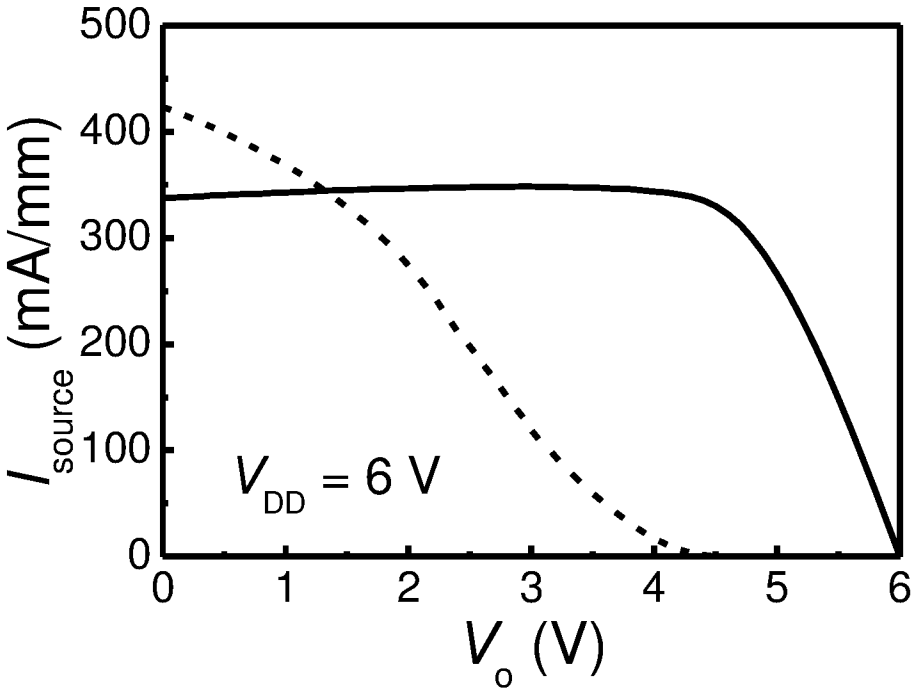
500
400
300
200
100
0
I_{source} (mA/mm)
V_{DD} = 6 V
0
1
2
3
4
5
6
V_o (V)

FIG. 4A

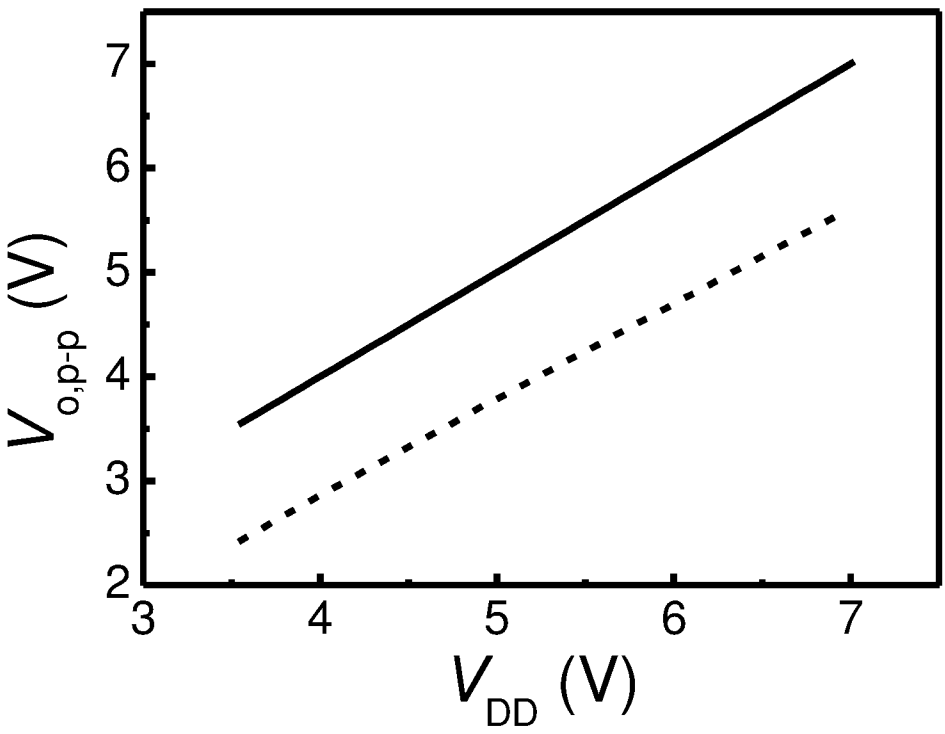
7
6
5
4
3
2
$V_{o,p-p}$ (V)
3
4
5
6
7
V_{DD} (V)

FIG. 4B

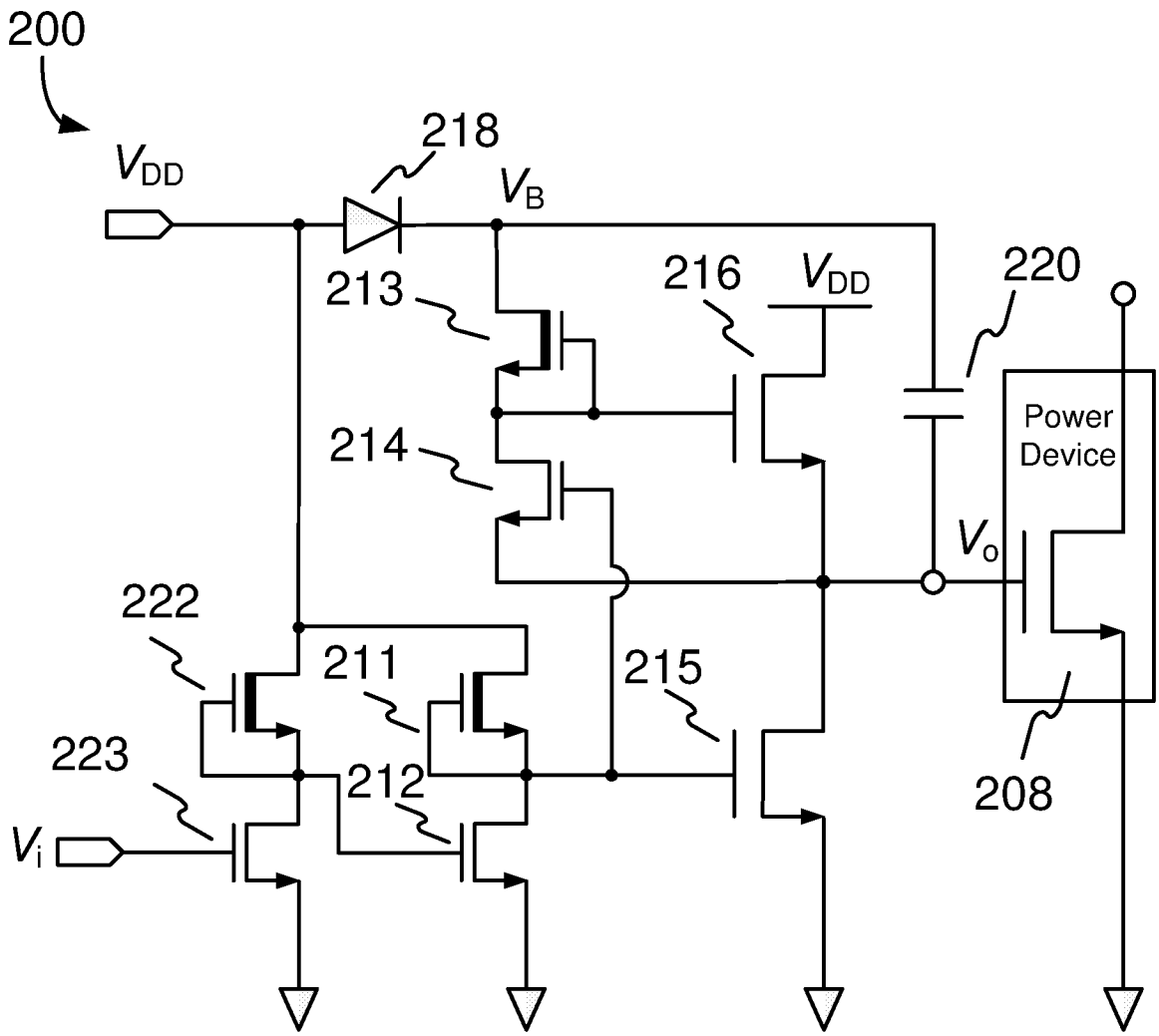
200
218
V_{DD}
V_B
213
216
V_{DD}
220
214
Power
Device
V_o
222
211
215
223
212
V_i
208

FIG. 5

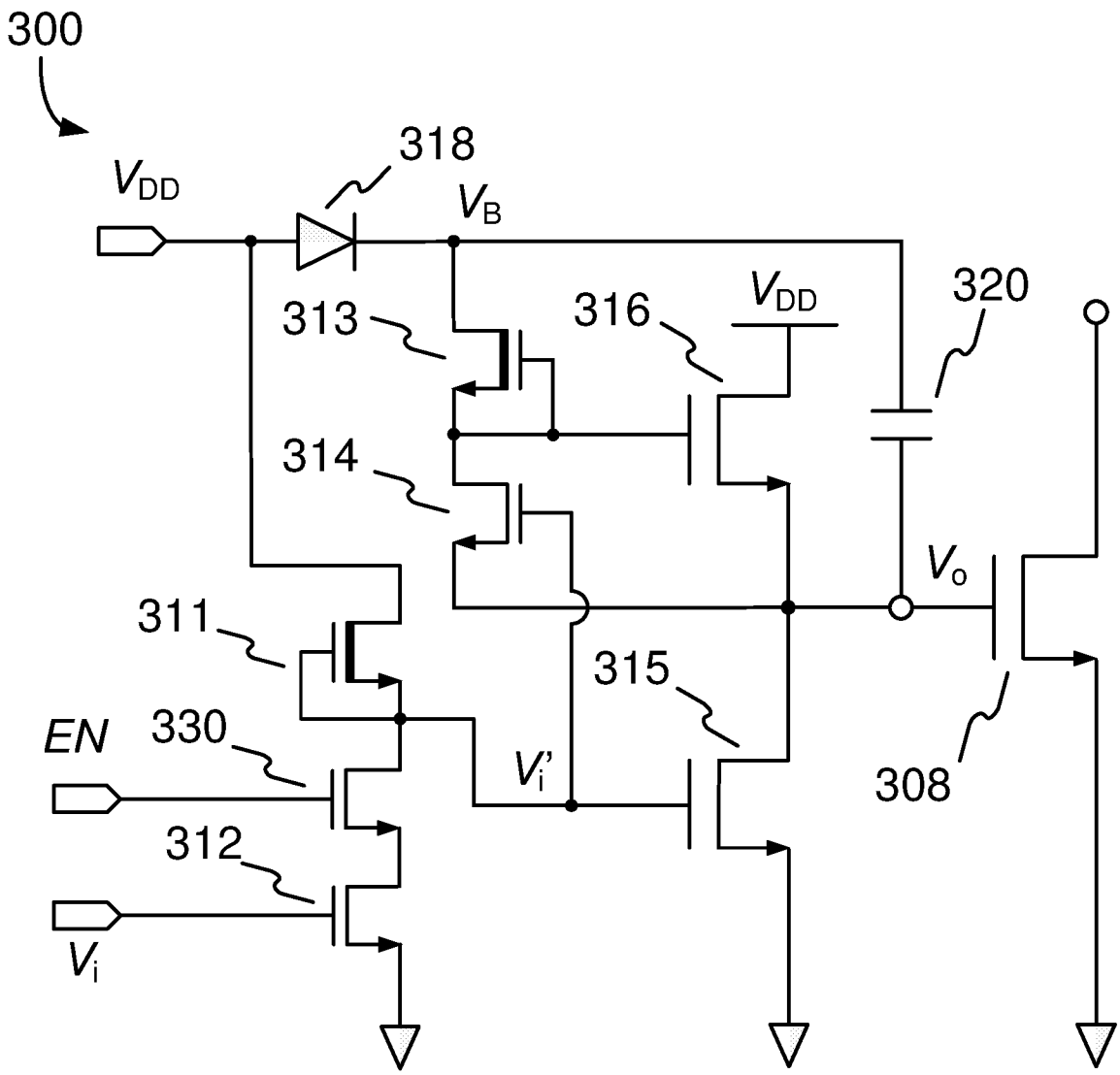

FIG. 6

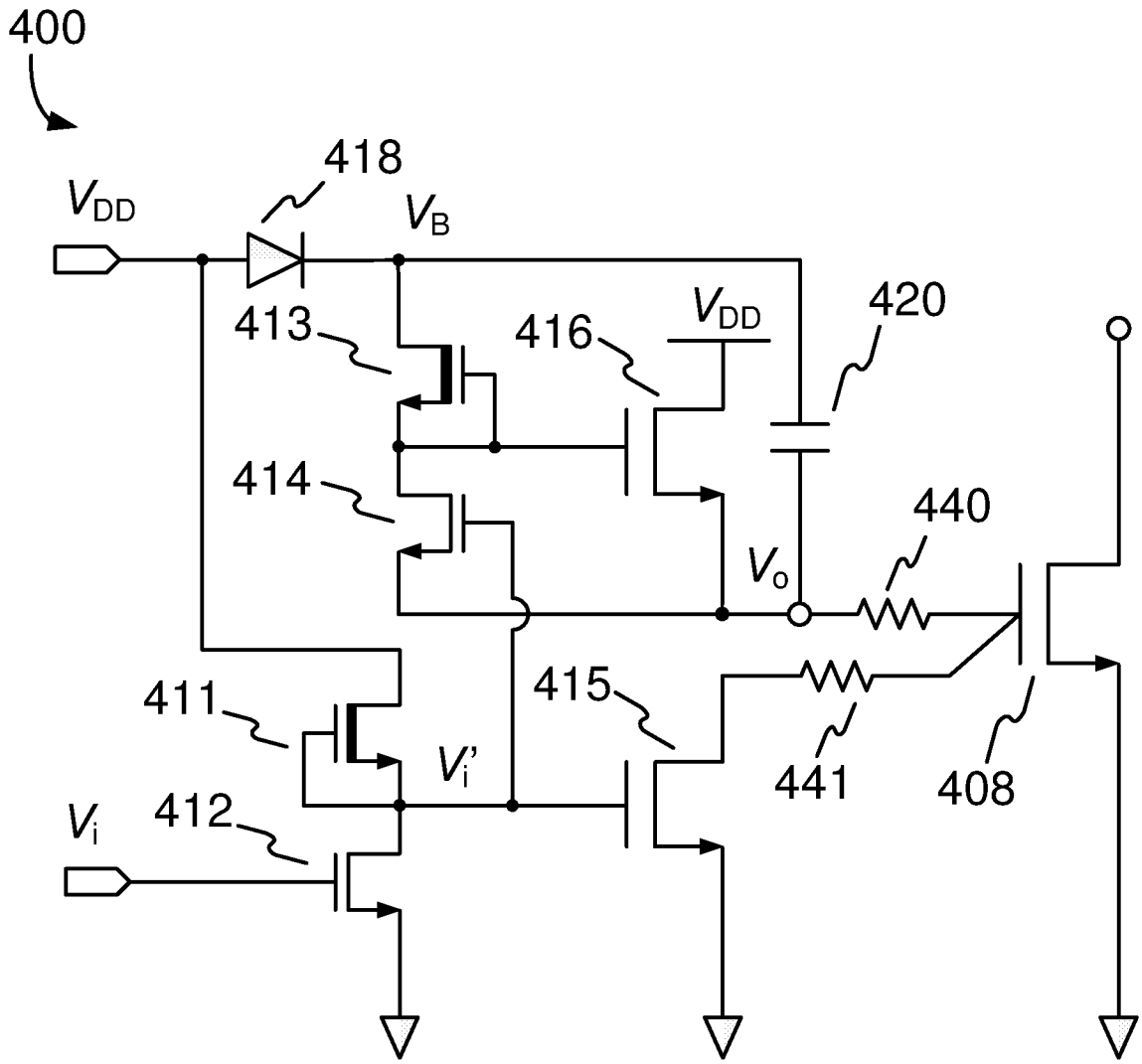
400
418
V_{DD}
V_B
413
416
V_{DD}
420
414
440
V_o
411
415
V_i'
441
408
V_i
412

FIG. 7

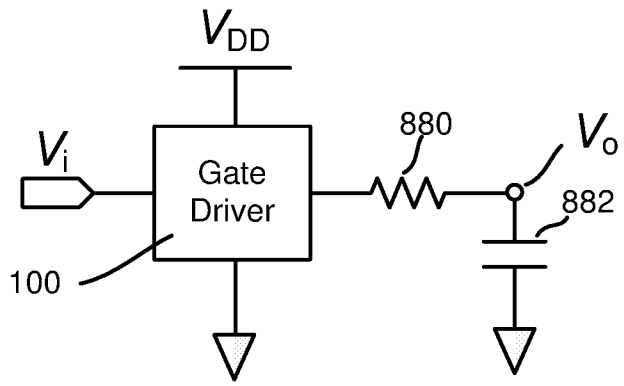
V_{DD}
V_i
Gate
Driver
880
V_o
882
100

FIG. 8A

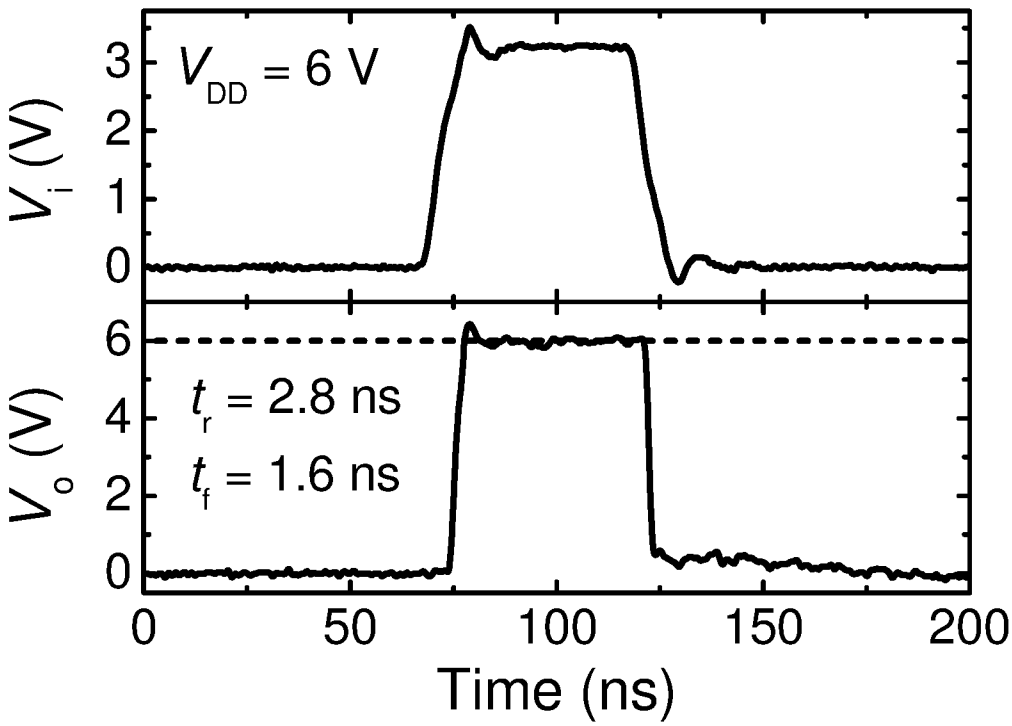
V_{DD} = 6 V
V_i (V)
V_o (V)
t_r = 2.8 ns
t_f = 1.6 ns
0
1
2
3
4
6
0
50
100
150
200
Time (ns)

FIG. 8B

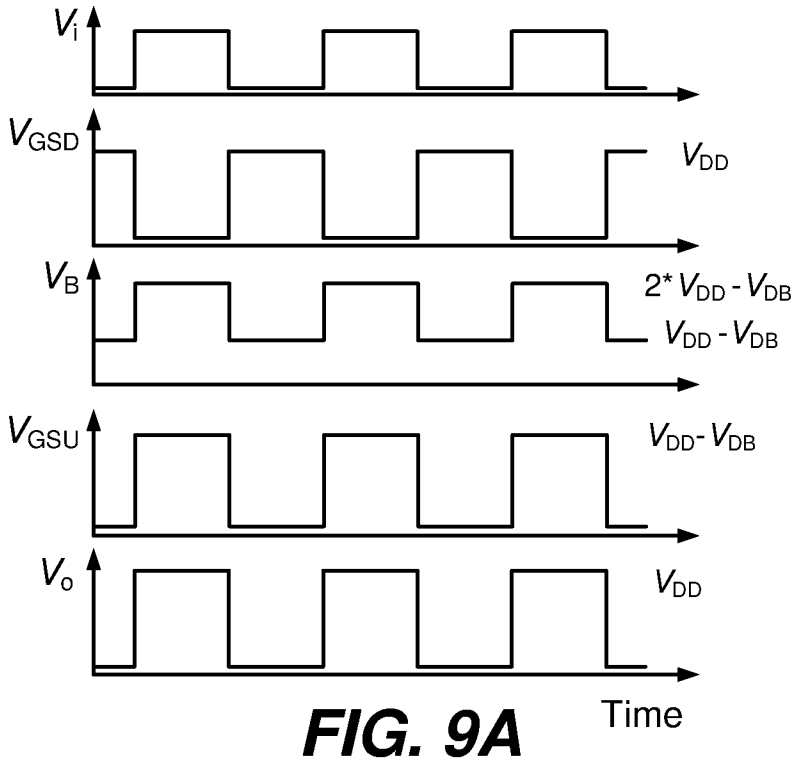
V_i
V_{GSD}
V_{DD}
V_B
$2^*V_{DD}-V_{DB}$
$V_{DD}-V_{DB}$
V_{GSU}
$V_{DD}-V_{DB}$
V_o
V_{DD}
Time

FIG. 9A

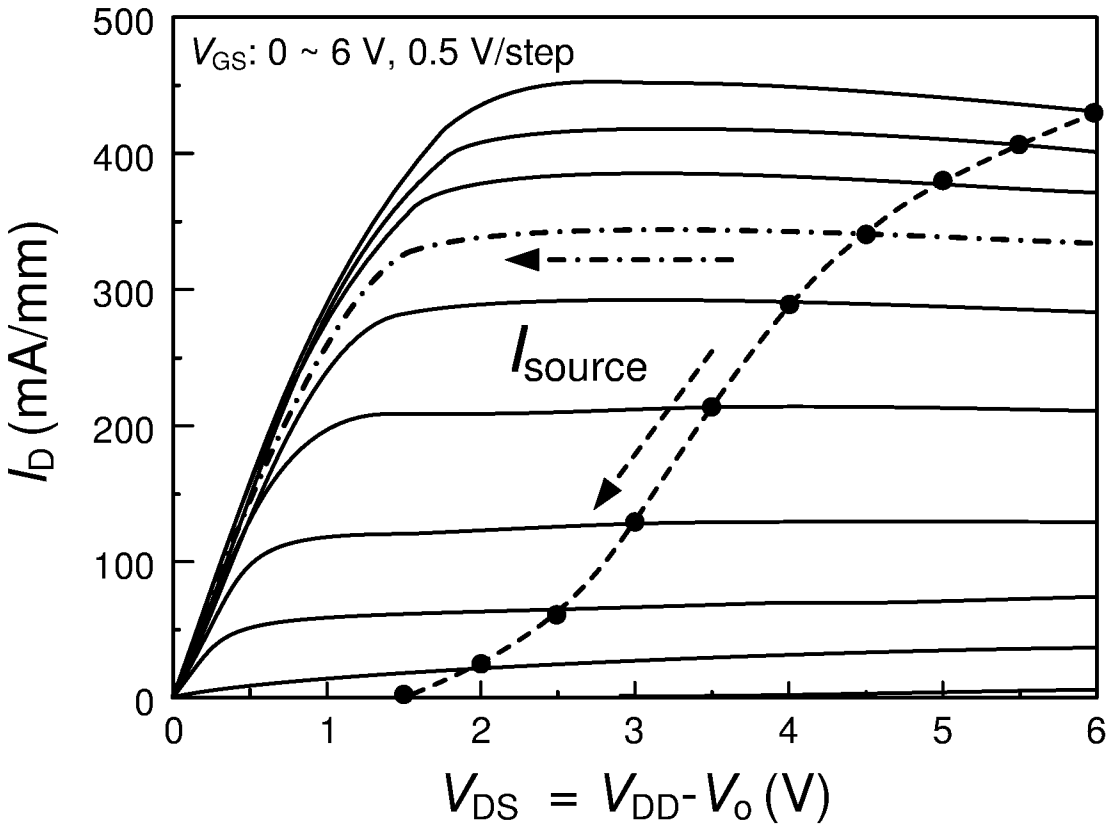
V_{GS}: 0 ~ 6 V, 0.5 V/step
I_{source}
I_D (mA/mm)
500
400
300
200
100
0
0
1
2
3
4
5
6
$V_{DS} = V_{DD}-V_o$ (V)

FIG. 9B

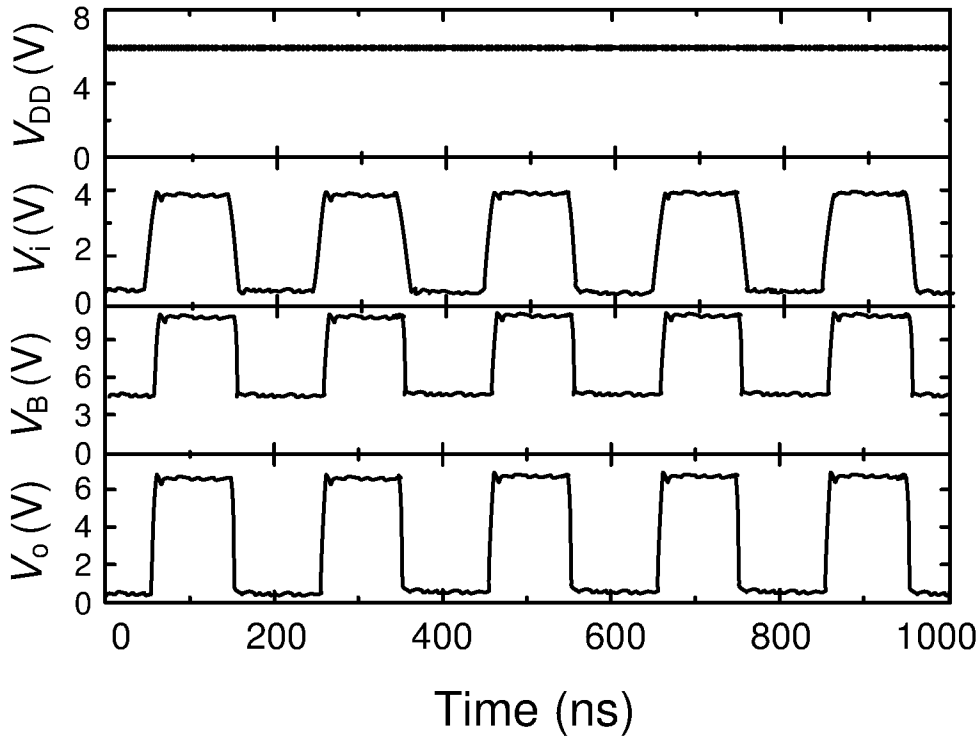
8
4
0
V_{DD} (V)
4
2
0
V_i (V)
9
6
3
0
V_B (V)
6
4
2
0
V_o (V)
0
200
400
600
800
1000
Time (ns)

FIG. 10

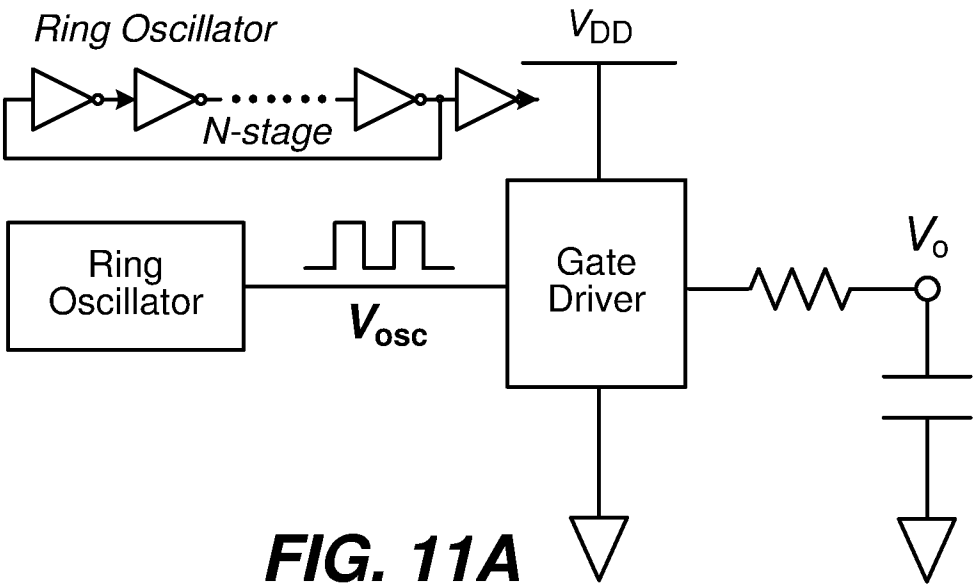

FIG. 11A

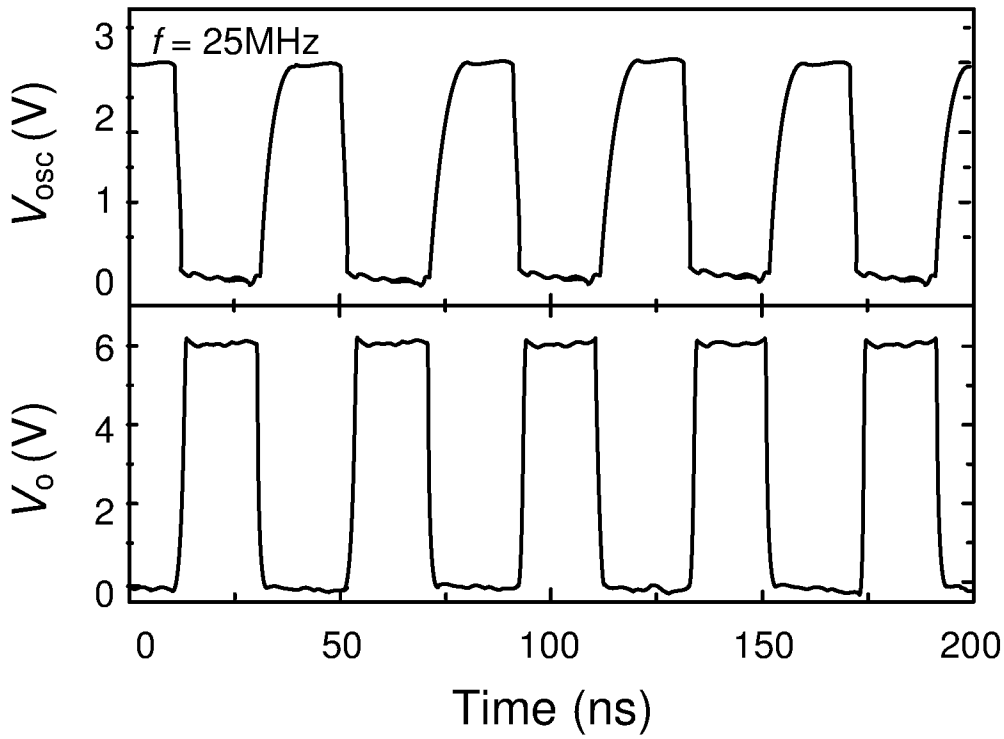

FIG. 11B

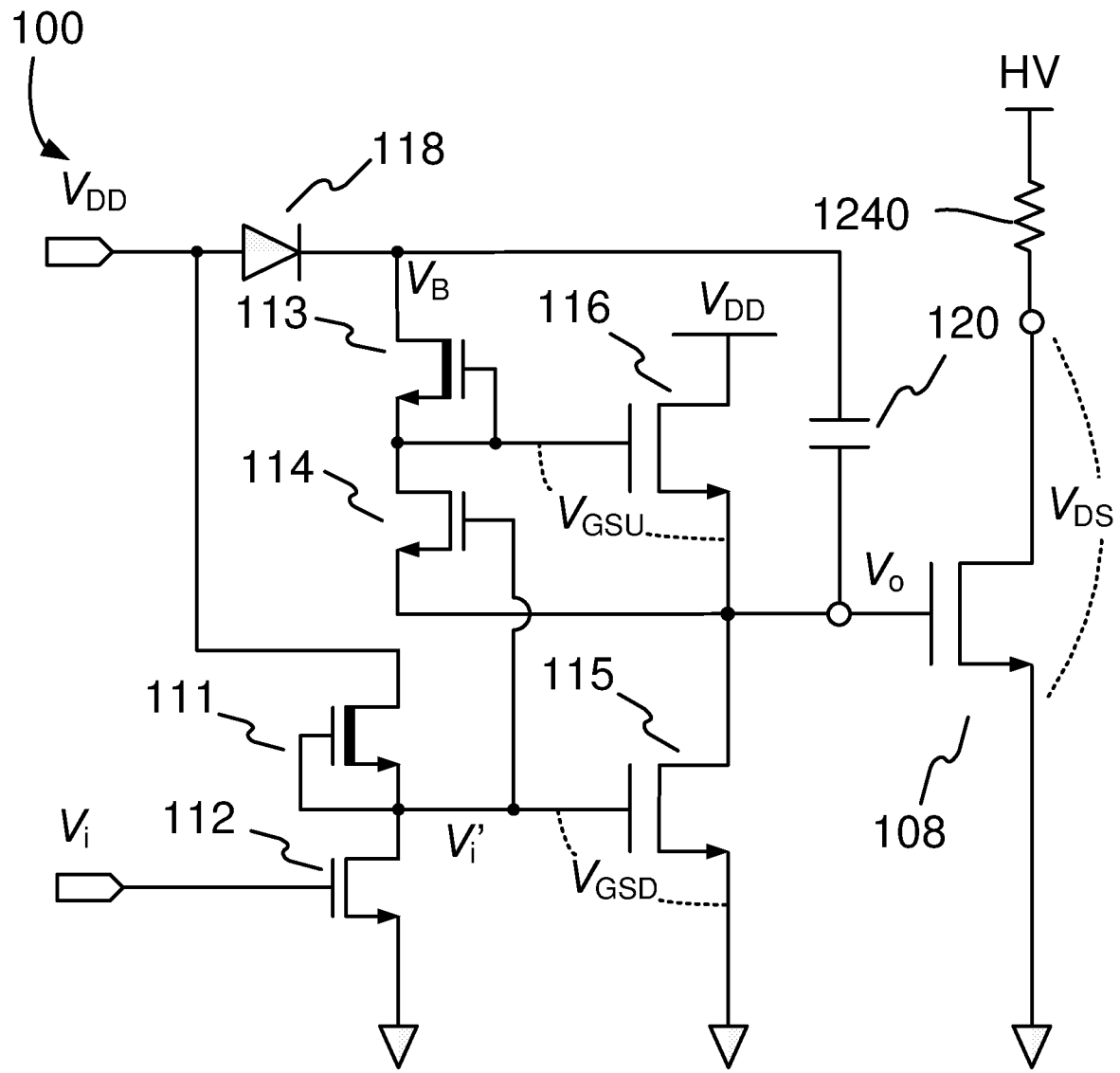
100
HV
118
V_{DD}
1240
V_B
113
116
V_{DD}
120
114
V_{GSU}
V_{DS}
V_o
115
111
108
V_i
112
V_i'
V_{GSD}

FIG. 12

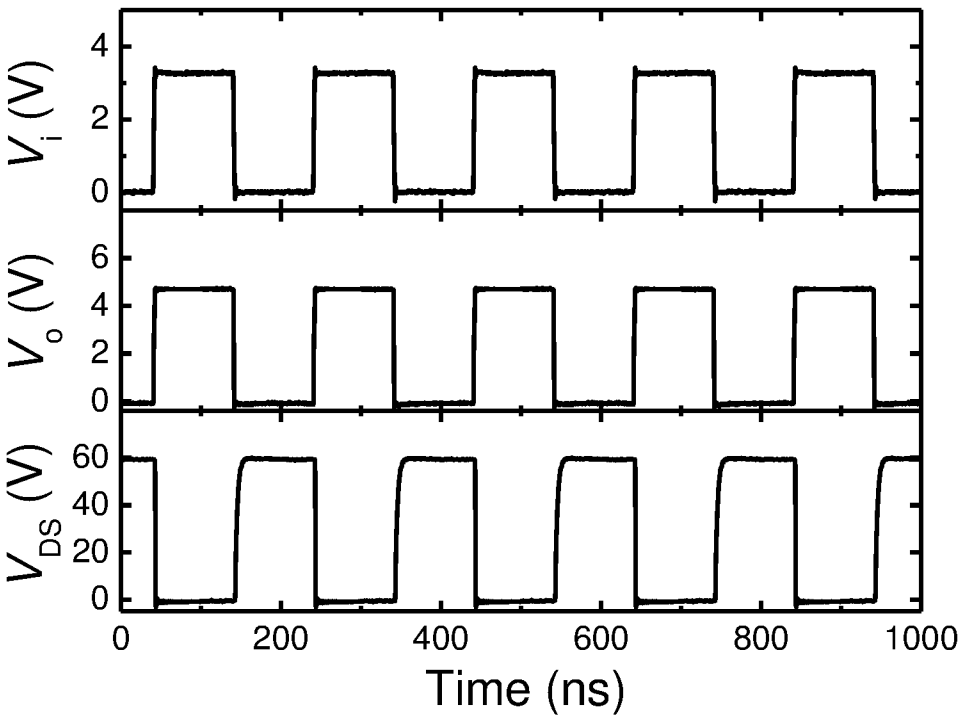

FIG. 13

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2017/082833

A. CLASSIFICATION OF SUBJECT MATTER

H02M 1/08(2006.01)i; H03K 17/687(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H02M; H03K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNPAT,EPODOC,WPI,CNKI: gate,driv+,voltage+,bootstrap+,circuit,diode+,pull, push,inverter,capaci+,transistor+,discharg+, charg+,source,drain,switch+

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	CN 103532353 A (UNIV. SHANDONG) 22 January 2014 (2014-01-22) description, paragraphs [0035]-[0043] and figures 2-3	1-20
A	CN 101771345 A (DONGBU HITEK CO., LTD.) 07 July 2010 (2010-07-07) the whole document	1-20
A	CN 101977046 A (UNIV. XIDIAN) 16 February 2011 (2011-02-16) the whole document	1-20
A	US 2002140501 A1 (GOYHENETCHE, PHILIPPE ET AL.) 03 October 2002 (2002-10-03) the whole document	1-20
A	US 2015171833 A1 (KONKUK UNIVERSITY INDUSTRIAL COOPERATION CORP. ET AL.) 18 June 2015 (2015-06-18) the whole document	1-20
A	US 2016013730 A1 (SAMSUNG ELECTRONICS CO., LTD.) 14 January 2016 (2016-01-14) the whole document	1-20

☐ Further documents are listed in the continuation of Box C. ☑ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
17 July 2017	**04 August 2017**

Name and mailing address of the ISA/CN	Authorized officer
STATE INTELLECTUAL PROPERTY OFFICE OF THE P.R.CHINA **6, Xitucheng Rd., Jimen Bridge, Haidian District, Beijing 100088** **China**	**WANG,Xueting**
Facsimile No. **(86-10)62019451**	Telephone No. **(86-10)62413263**

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2017/082833

Patent document cited in search report			Publication date (day/month/year)	Patent family member(s)			Publication date (day/month/year)
CN	103532353	A	22 January 2014	None			
CN	101771345	A	07 July 2010	TW	201025862	A	01 July 2010
				US	2010164593	A1	01 July 2010
				KR	20100078400	A	08 July 2010
				KR	101606400	B1	25 March 2016
				US	8054123	B2	08 November 2011
CN	101977046	A	16 February 2011	None			
US	2002140501	A1	03 October 2002	US	6469567	B1	22 October 2002
US	2015171833	A1	18 June 2015	KR	20150069317	A	23 June 2015
US	2016013730	A1	14 January 2016	KR	20160009115	A	26 January 2016