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(54) **THIN SILICON CIRCUITS AND METHOD FOR MAKING THE SAME**

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(57) **ABSTRACT**

An apparatus including a circuit substrate comprising a single crystal semiconductor layer having a smallest dimension reduced; and circuit devices formed in the single crystal layer.

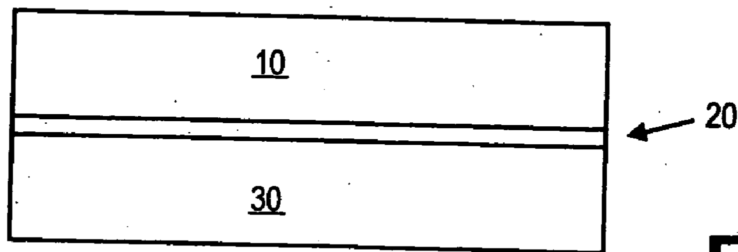

FIG. 1

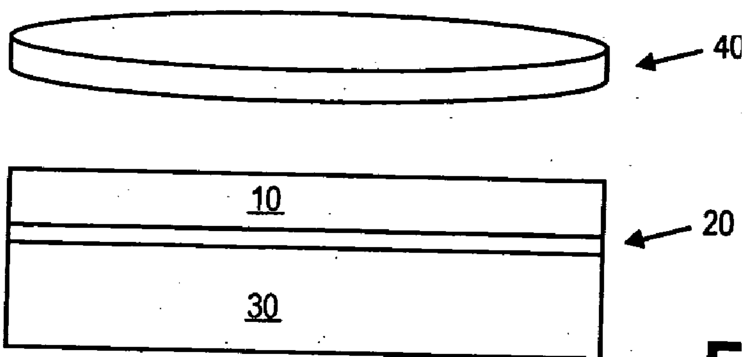

FIG. 2

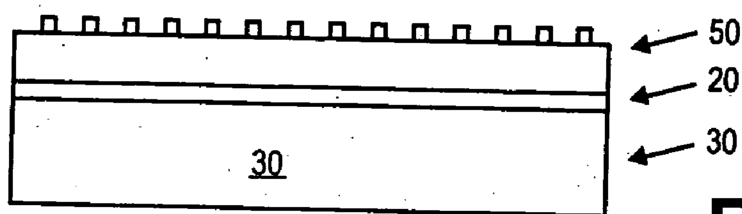

FIG. 3

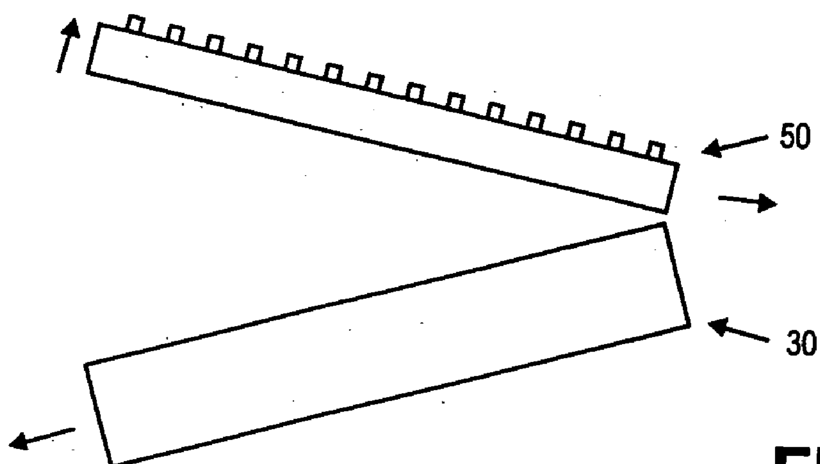

FIG. 4

FIG. 5

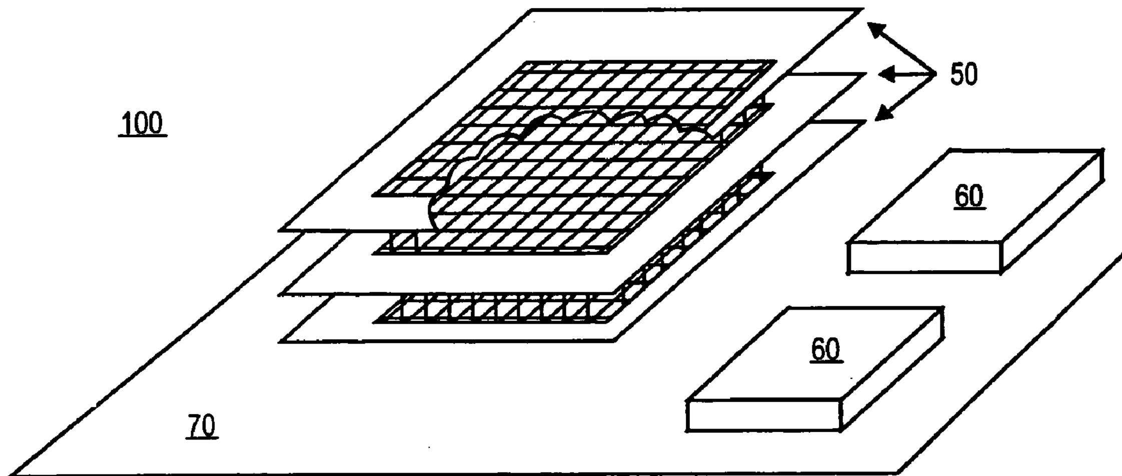

FIG. 6

THIN SILICON CIRCUITS AND METHOD FOR MAKING THE SAME

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application is a Divisional of co-pending U.S. patent application Ser. No. 09/751,626, filed Dec. 27, 2000, which is Continuation-In-Part of co-pending U.S. patent application Ser. No. 09/607,252, filed Jun. 30, 2000.

FIELD OF THE INVENTION

[0002] The invention generally relates to semiconductor based products and more particularly to the fabrication and design of integrated circuit structures.

BACKGROUND OF THE INVENTION

[0003] A typical integrated circuit consists of a substrate on which devices are formed in and/or on the substrate. Such devices include for example transistors and capacitors that may be interconnected with one another and/or communicate with an external source.

[0004] One common approach to making an integrated circuit is to fabricate the circuit as part of a wafer such as a semiconductor wafer on which multiple integrated circuits are formed simultaneously. Fabricating these circuits at the wafer level allows similar circuits to be formed at one time which tends to make the fabrication process more efficient. Once formed the wafer is singulated into individual dies or chips. Currently, single crystal silicon wafers are up to 300 mm or 12 inches in diameter and about 750 microns thick. A 300 mm diameter wafer needs to be about 750 microns thick to avoid problems with breakage during processing and warpage of the wafer.

[0005] There are currently applications for semiconductor integrated circuits that require die (device) thickness of substantially less than 750 microns. In order to conserve space in packaging, and to increase memory density in a given area, such as flash memory circuits, an emerging technology is to stack integrated circuits one on top of another. In these situations, it would be beneficial to have circuit thicknesses of less than 100 microns.

[0006] Currently, these requirements are being met by processing the circuits using a 750 micron thick wafer and then thinning the unused portion of the silicon wafer to reduce the thickness to a more suitable number of approximately 25 to 100 microns. The thinning technique is typically chemical-mechanical polishing or grinding. The difficulty of the current method is that the thinning is done after the devices and circuits have been processed into the wafer, and thus contributes to loss of circuits through damage to the wafer.

[0007] An improved minimum thickness integrated circuit and a method of making a minimum thickness wafer is needed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] The features, aspects, and advantages of the invention will become more thoroughly apparent from the following detailed description, appended claims, and accompanying drawings in which:

[0009] **FIG. 1** is a schematic, cross-sectional side view of an oxidized single crystal semicoductor layer bonded to a support substrate in accordance with an embodiment of the invention.

[0010] **FIG. 2** is a schematic, cross-sectional side view of a grinding or polishing used to thin the single crystal layer of **FIG. 1**.

[0011] **FIG. 3** shows the structure of **FIG. 1** after the integrated circuit devices are manufactured (or fabricated) in the thinned single crystal layer.

[0012] **FIG. 4** shows the structure of **FIG. 3** and illustrates the separation of the thinned single crystal layer from the support substrate.

[0013] **FIG. 5** is a drawing of the thinned single crystal layer separated from the support substrate with integrated circuits introduced thereon and ready for subsequent dicing and stacking.

[0014] **FIG. 6** shows a schematic top perspective view of stacked structure containing more than one integrated circuit on a thinned single crystal layer.

DETAILED DESCRIPTION OF THE INVENTION

[0015] A method and apparatus are disclosed. According to one aspect of the invention, the method comprises coupling a single crystal layer to the surface of a support substrate such as a support substrate of a crystalline or polycrystalline material. At the interface of the single crystal and the support substrate there may be a differentially removable material, such as an oxide (e.g. silicon dioxide). In a further aspect, the method includes thinning the single crystal layer and forming circuit devices on the thinned layer. In a still further aspect, the thinned layer having devices formed thereon is separated from the support substrate. In this regard, the method describes a process for the manufacture of thin semiconductor products. Thus, in one embodiment of the invention, a composite substrate of a single crystal semiconductor material and polycrystalline semiconductor material may replace existing 750 micron thick monolithic single crystal wafers, epitaxial silicon wafers, or silicon on insulator structures, as a durable integrated circuit device substrate suitable for typical integrated circuit process operations.

[0016] In the following description, for the purposes of explanation, numerous specific details are set forth in order to provide a thorough understanding of the invention. It will be apparent, however, to one skilled in the art that the invention may be practiced without some of these specific details. The following description and accompanying drawings provide various examples for the purposes of illustration. However, these examples should not be construed in a limiting sense as they are merely intended to provide examples of the invention rather than to provide an exhaustive list of all possible implementations of the invention.

[0017] Reference will now be made to drawings wherein like structures will be provided with like reference designations. In order to show the structures of the invention most clearly, the drawings included herein are diagrammatic representations of integrated circuit structures. Thus, the actual appearance of the fabricated structures, for example in a photomicrograph, may appear different while still incorporating the essential structures of the invention. Moreover the drawings show only the structures necessary to understand the invention. Additional structures known in the art have not been included to maintain the clarity of the drawings.

[0018] FIGS. **1-5** illustrate a technique for forming thin semiconductor products according to an embodiment of the invention.

[0019] **FIG. 1** shows a composite structure consisting of single crystal semiconductor layer **10** oxidized and bonded through differentially removable material **20** to support substrate **30**. Support substrate **30** is for example, single crystal or polycrystalline silicon. Substrate **30** may have a diameter similar to a semiconductor wafer diameter (e.g. on the order of six inches to 12 inches). Support substrate **30** has a thickness sufficient to support a single crystal layer through integrated circuit processing operations. A suitable thickness for support substrate **30** to permit conventional wafer processing with respect to the composite structure is on the order of 750 microns. Prior to forming the composite structure, the surface of support substrate **30** may be polished flat such as by a chemical-mechanical polish.

[0020] Polycrystalline silicon substrates suitable as support substrate **30** may be manufactured by casting ingots of silicon followed by slicing the ingots into wafers, and polishing the resulting wafers. In one example, a polycrystalline material is cast in a mold for a large size cast. From the cast, 200 mm, 300 mm, or greater cylindrical ingots are drilled and the ingots are used to form the support substrate of the composite wafer. Since the cast mold primarily determines the diameter of the wafer, the increased wafer diameter size from, for example, 200 mm to 300 mm, or greater may be produced without relying upon the development of new ingot casting tools. The focus of this discussion is forming composite wafers of diameters of 200 mm, 300 mm, or greater, in keeping with the current trends in the industry. It is to be appreciated that, where desired, smaller diameter wafers may also be formed according to the methods described herein.

[0021] In one embodiment, overlying the surface of support substrate **30** is differentially removable material **20**. In the example where support substrate **30** and single crystal layer **10** are each a semiconductor material such as silicon, differentially removable material is silicon dioxide (SiO_2) thermally grown or deposited (e.g. by plasma enhanced chemical vapor deposition (PECVD)) to a thickness of, for example, about one micron. Alternatively, the differentially removable layer can be one of silicon nitride and phosphorous or boron doped glass (PBSG).

[0022] Overlying differentially removable material **20** on the surface of support structure **30** is single crystal layer **10**. Single crystal layer **10** is, for example, a semiconductor material suitable for forming devices therein or thereon. In one embodiment, single crystal layer **10** is introduced to a thickness on the order of 25 to 100 microns.

[0023] In one embodiment, the single crystal layer is introduced by thermally bonding a single crystal wafer to an oxidized single or polycrystalline wafer and polishing down the top single crystal layer to a thickness of 25 to 100 microns.

[0024] **FIG. 2** illustrates the composite structure being thinned such as through a polish (grinding) or chemical-mechanical polish using polishing pad and slurry **40**. In one embodiment, single crystal layer **10** may be thinned to a thickness of less than 100 microns. At this point single crystal silicon wafer is attached to a support substrate **30**. The composite structure protects thinned single crystal layer **10** from damage from warping or breakage during subsequent circuit processing.

[0025] **FIG. 3** shows the integrated circuit introduced onto the thinned single crystal layer **10** of the composite structure. In this embodiment, integrated circuits **50** are fabricated in and/or on the thinned single crystal layer. Conventional processing techniques may be used to introduce the integrated circuit into the thin single crystal silicon layer, because of the support given by the substrate.

[0026] Following circuit processing to form, for example, a plurality of integrated circuit dies or chips, **FIG. 4** shows thin single crystal layer **10** having integrated circuits **50** fabricated therein and thereon being removed from the support substrate **30**. In the example where differentially removable layer **20** is SiO_2, thinned single crystal layer **10** may be separated from the composite structure by selectively etching differentially removable layer **20** that bonded the two of them together. Once separated, support substrate **30** can then be discarded or reused along with another single crystal silicon layer.

[0027] **FIG. 5** shows thinned single crystal layer **10** that has the integrated circuit devices **50** introduced therein. Thinned single crystal layer **10** has a thickness in this embodiment, on the order of less than 100 microns. At this point, thinned single crystal layer **10** may be singulated into individual integrated circuit dies or chips.

[0028] **FIG. 6** is a top perspective view of a stack of memory circuits on thinned single crystal layers **50** formed according to the techniques described herein. Memory circuits **50** are stacked one on top of another over an area of circuit board **70** and isolated from one another by, for example, a dielectric material (not shown). Vias and interconnects are disposed between the different layers of memory circuits to communicate, for example, between each other, or between circuits on circuit board **70**.

[0029] Stacking integrated circuits in, for example, a vertical or y-direction one on top of the other such as is shown in **FIG. 6** conserves space in packaging and increases device density. To conserve y-direction space this requires that the stacked circuits be fabricated into very thin silicon. An example of desired stacking of integrated circuits is memory circuits where the available number of memory circuits can be greatly expanded (e.g. doubled, tripled etc.) by stacking memory circuits over a given area of memory board. Applications for this type of packaging include, but are not limited to, cell phones and other mobile appliance applications that require the packing of the high density of elements in a small volume.

What is claimed is:

1. An apparatus comprising:

a circuit substrate comprising a single crystal semiconductor layer having a smallest dimension reduced; and

circuit devices formed in the single crystal layer.

2. The apparatus of claim 1, wherein the circuit substrate is formed as part of a composite structure comprising a removable support substrate.

3. The apparatus of claim 2, wherein the junction between the single crystal semiconductor layer and the removable support structure is an oxide.

4. The apparatus of claim 1, wherein the circuit devices form integrated circuits that interact with other electrical devices off the single crystal layer.

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