Nov. 17, 1970 A. I. KLAYMAN ET AL 3,541,266

BANDWIDTH COMPRESSOR AND EXPANDER

Original Filed Oct. 22, 1965 10 Sheets-Sheet 1

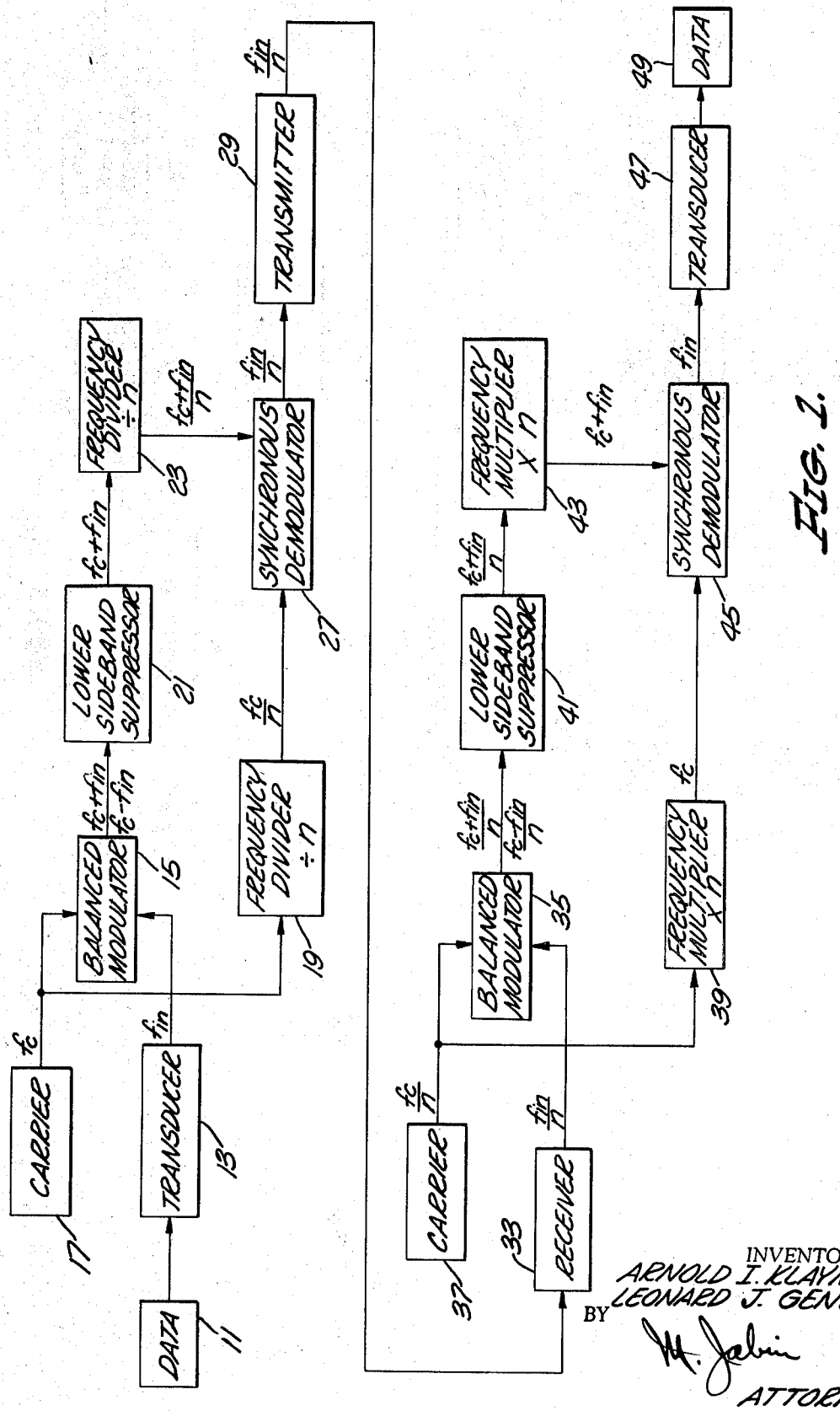

FIG. 1.

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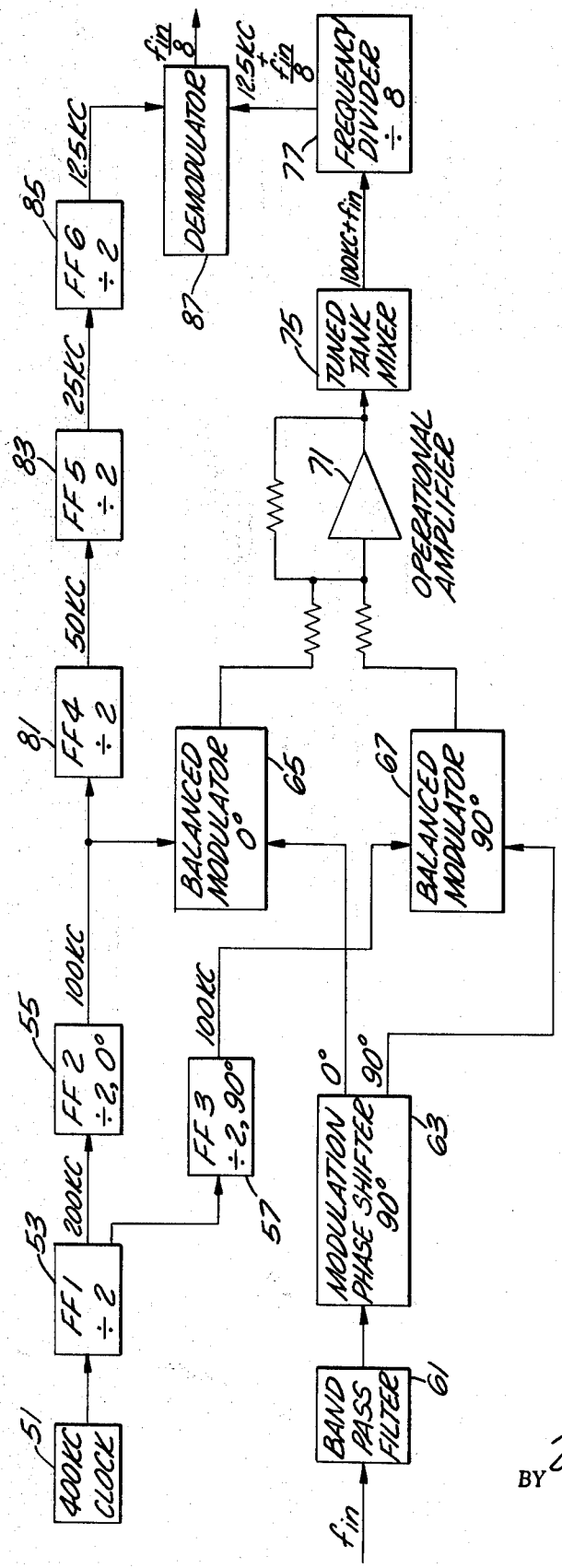

FIG. 2.

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BANDWIDTH COMPRESSOR AND EXPANDER

Original Filed Oct. 22, 1965 10 Sheets-Sheet 3

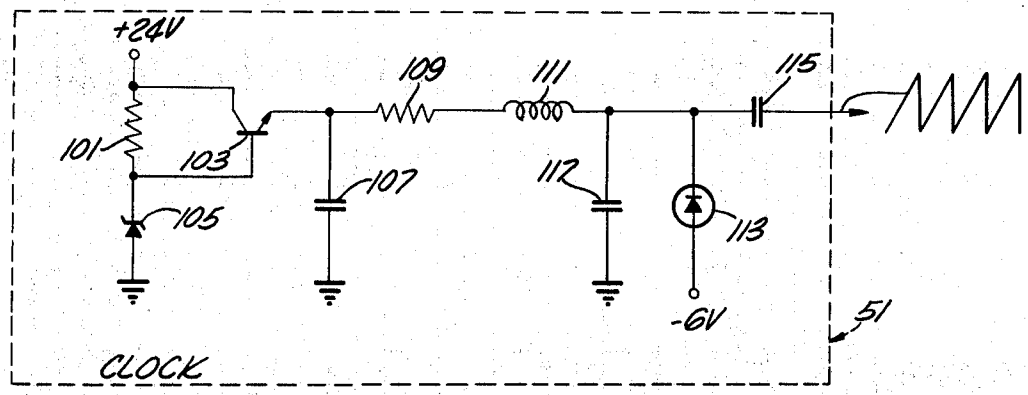

FIG. 3.

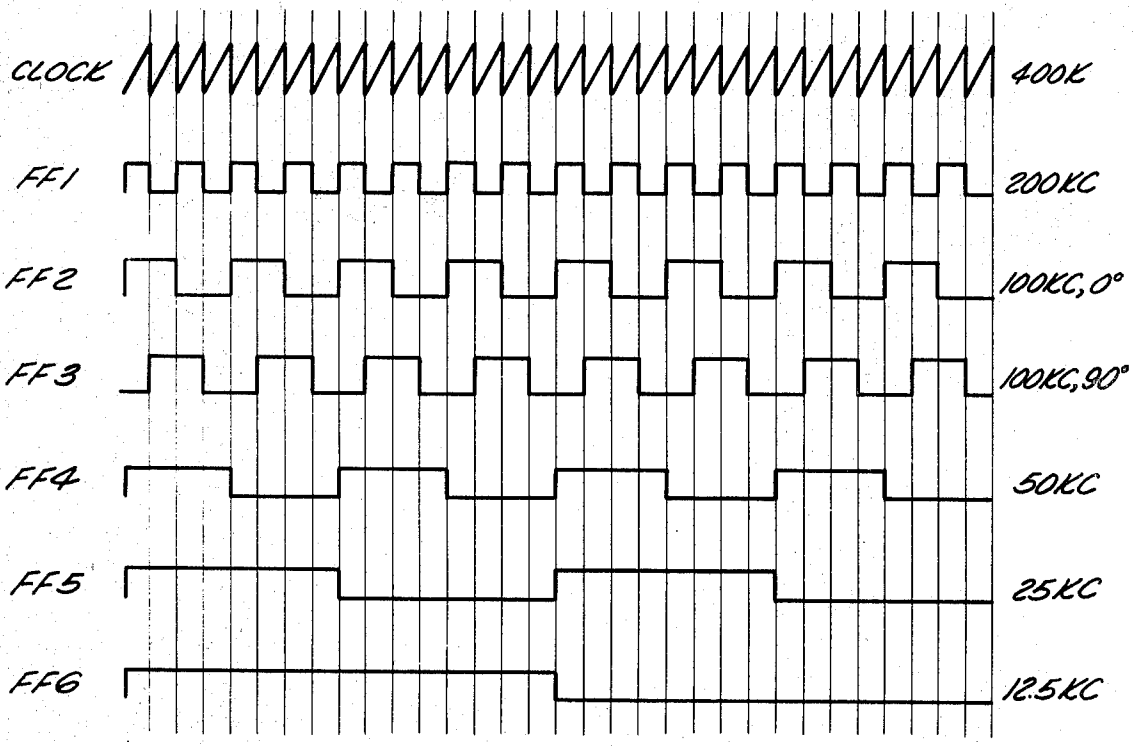

FIG. 4.

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Original Filed Oct. 22, 1965 10 Sheets-Sheet 4

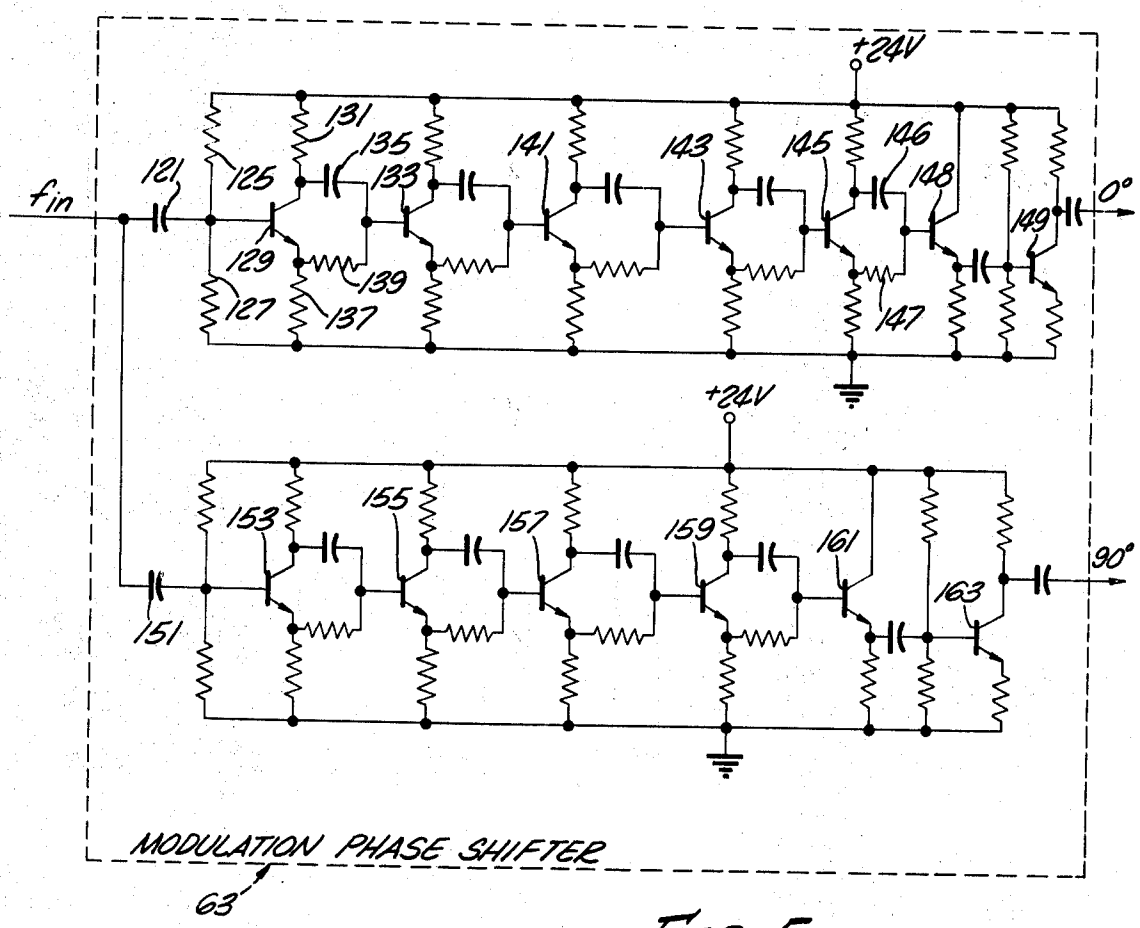

FIG. 5.

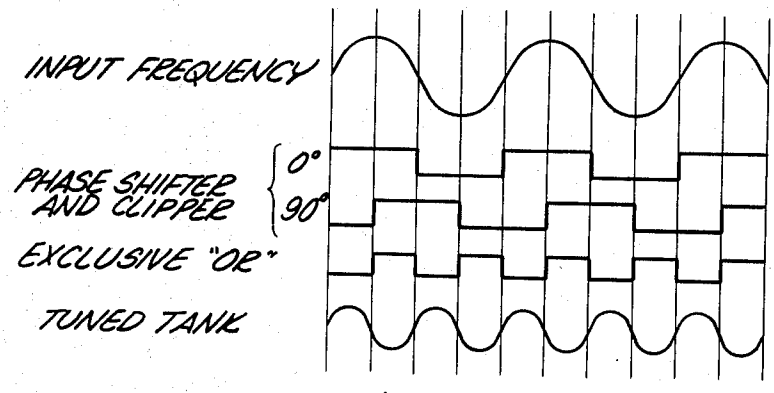

FIG. 12.

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BANDWIDTH COMPRESSOR AND EXPANDER

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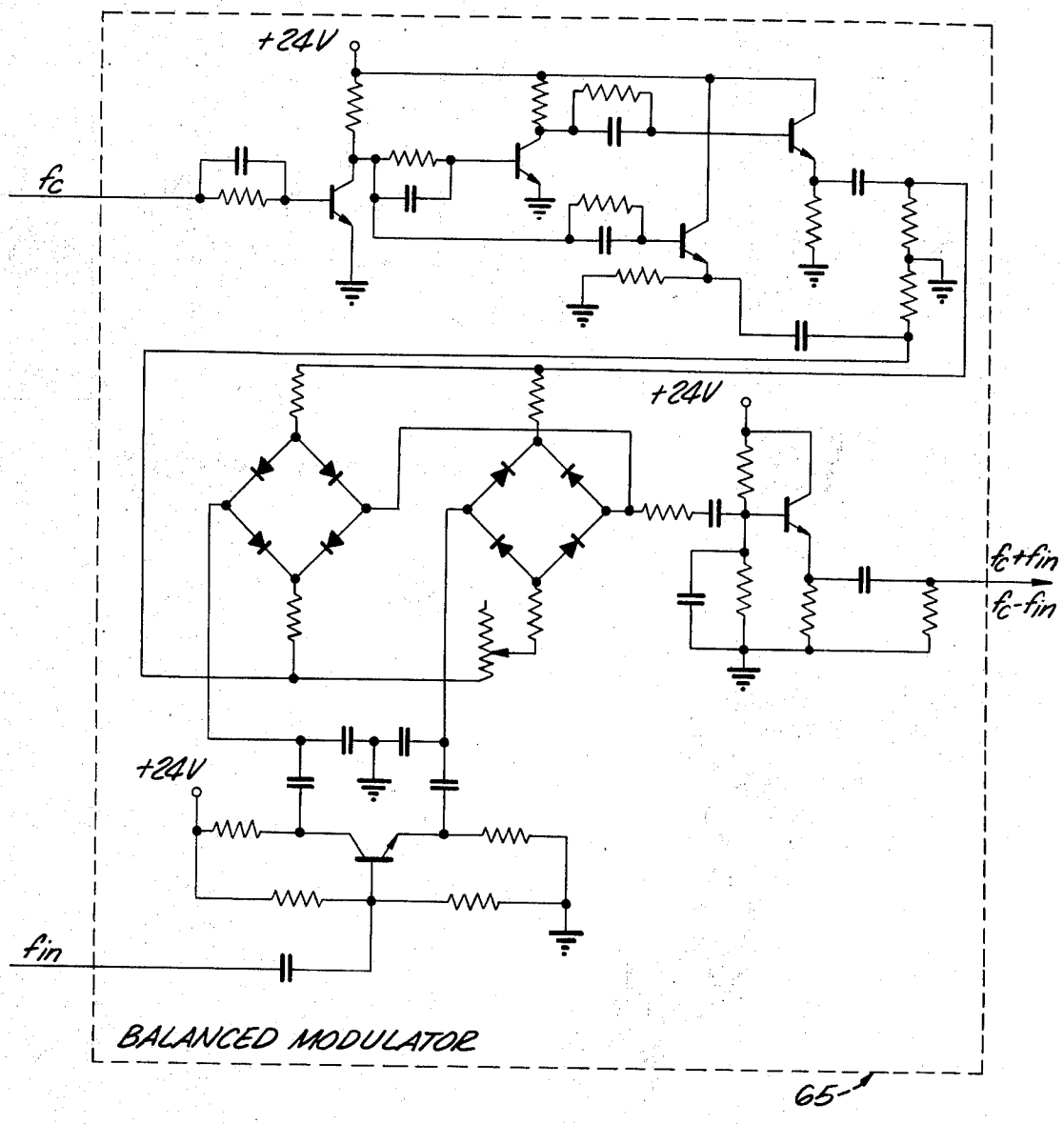

FIG. 6.

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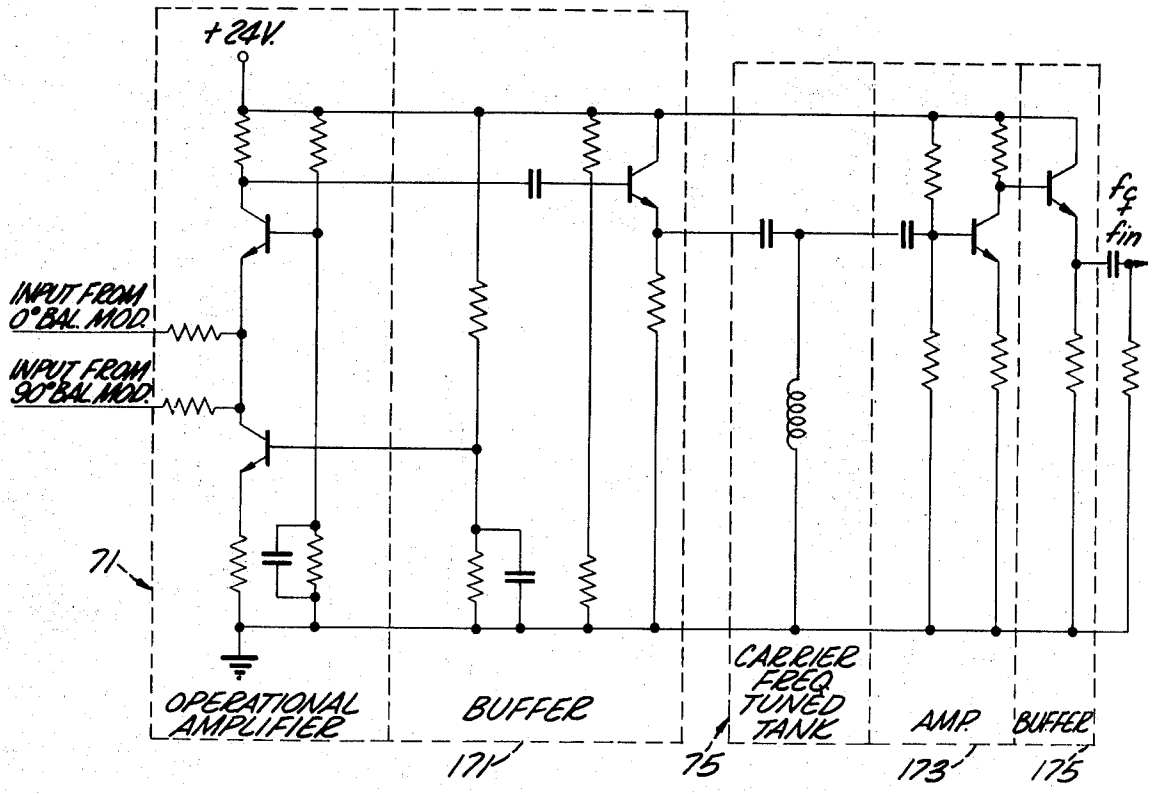

FIG. 7.

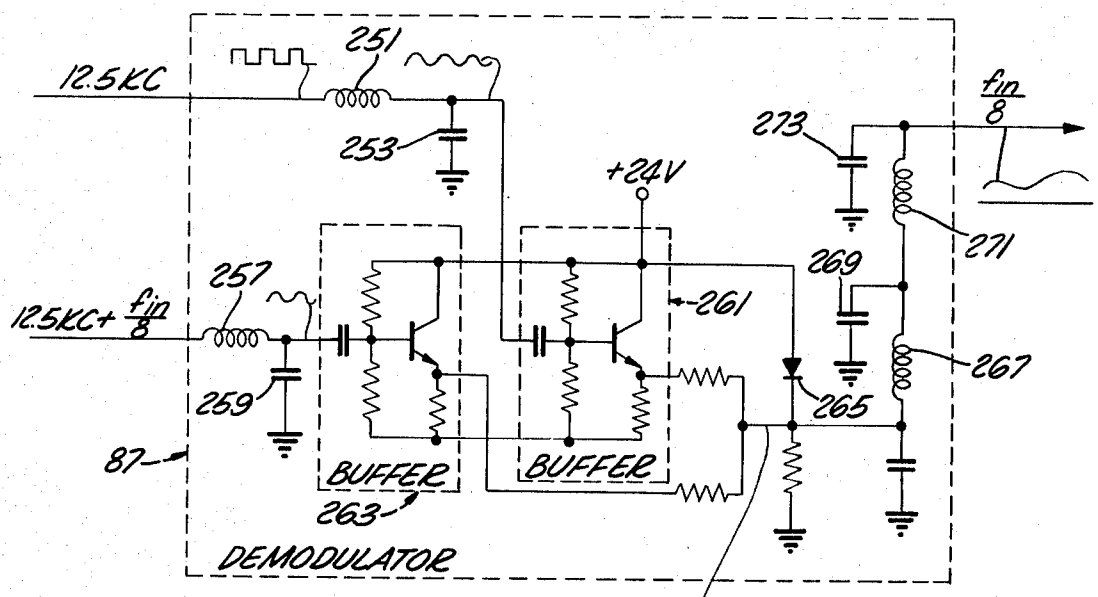

FIG. 9.

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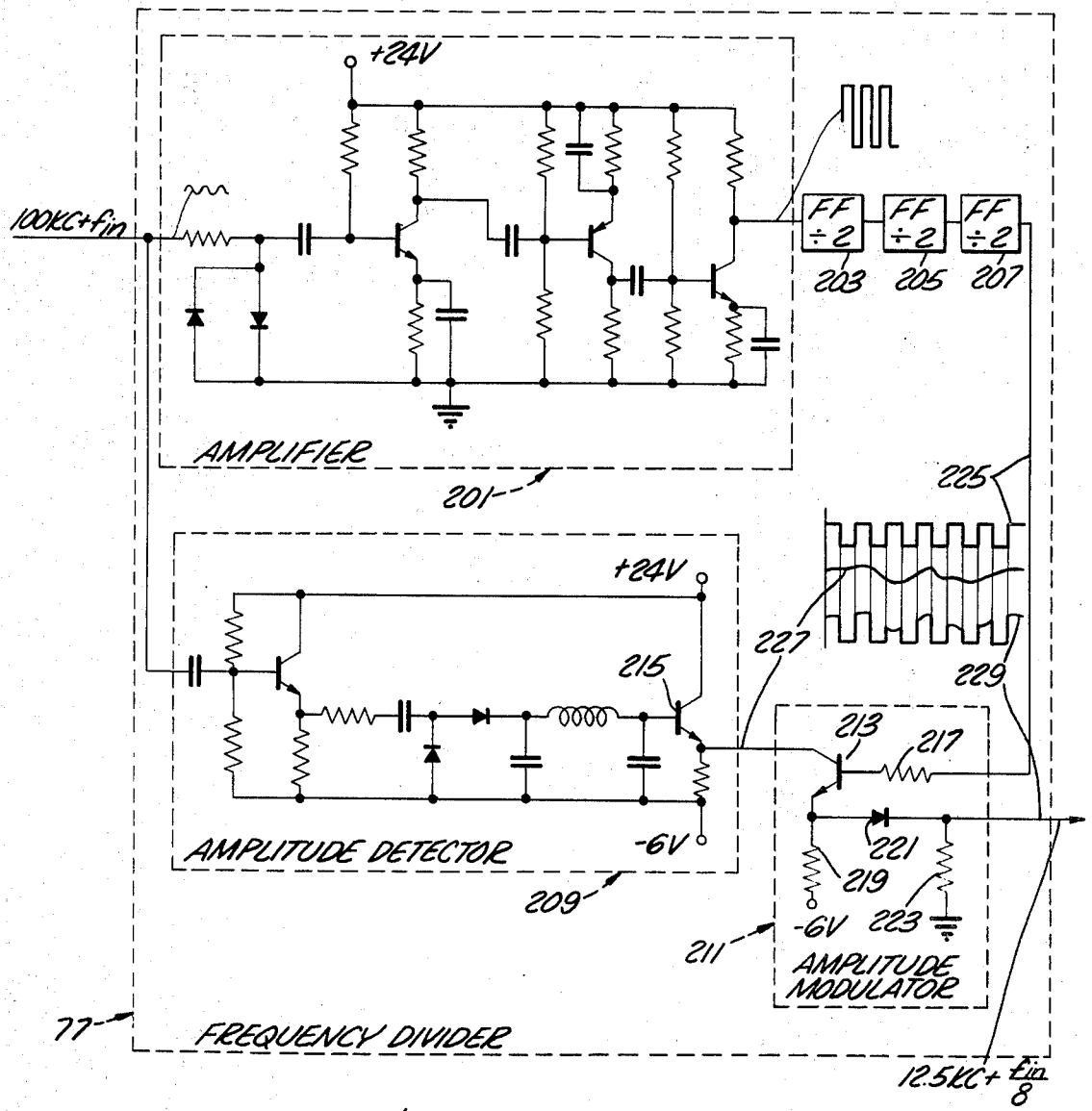

FIG. 8.

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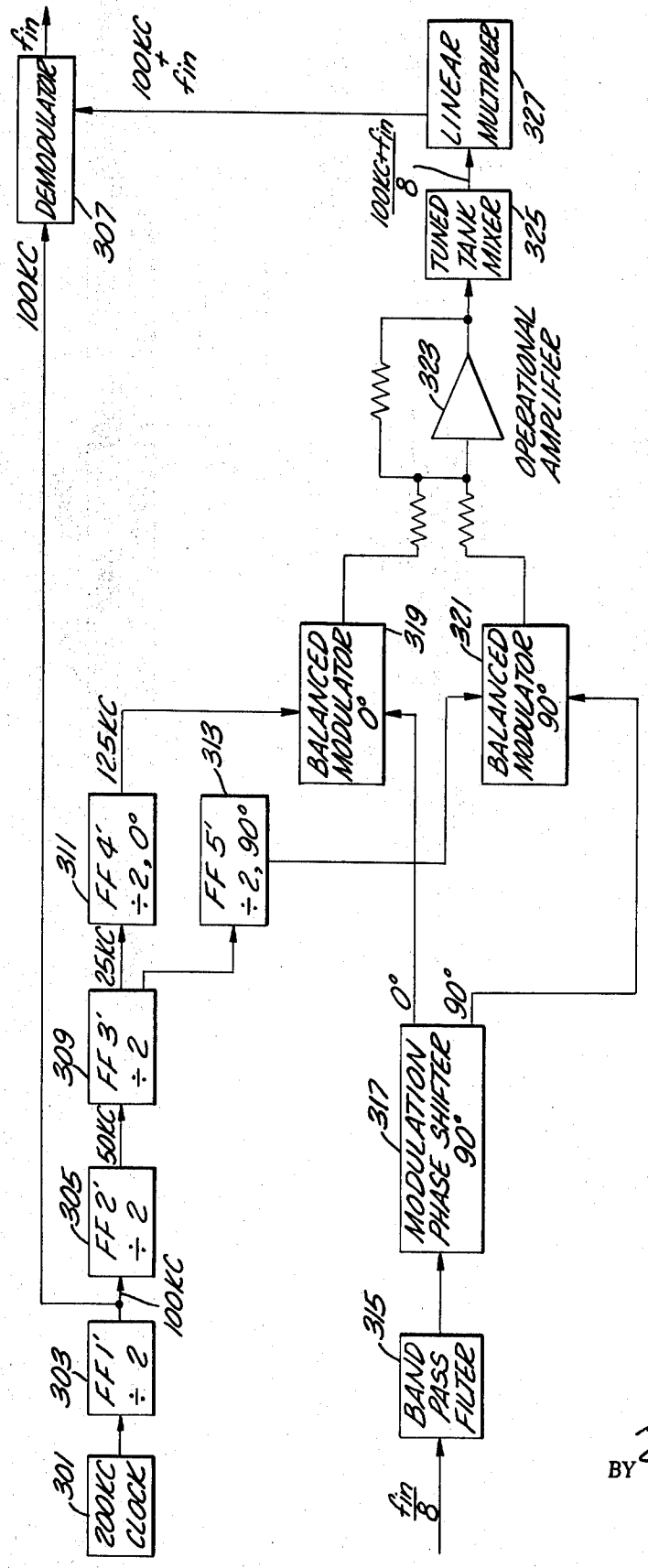

FIG. 10.

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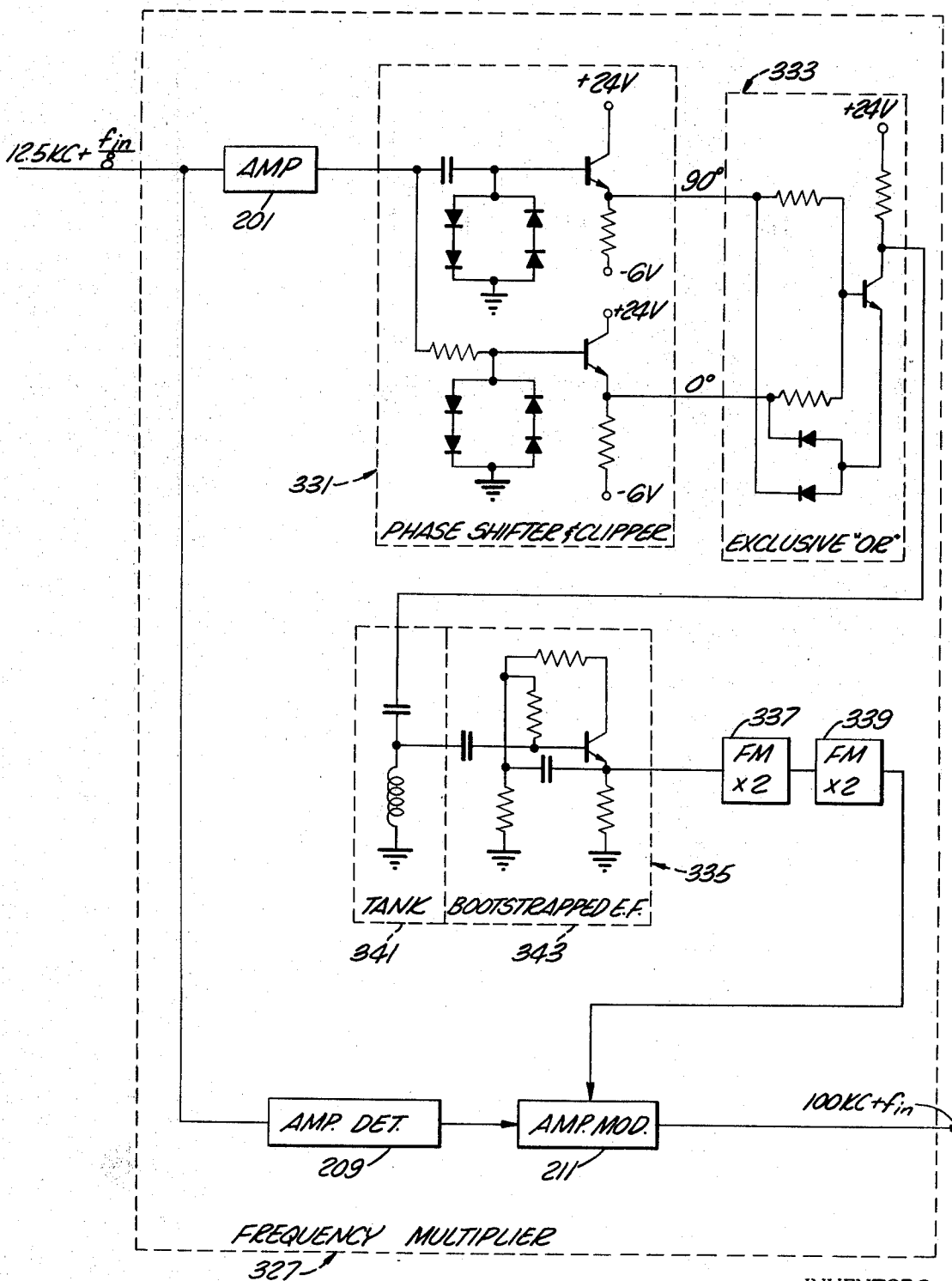

FIG. 11.

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BANDWIDTH COMPRESSOR AND EXPANDER

Original Filed Oct. 22, 1965 10 Sheets-Sheet 10

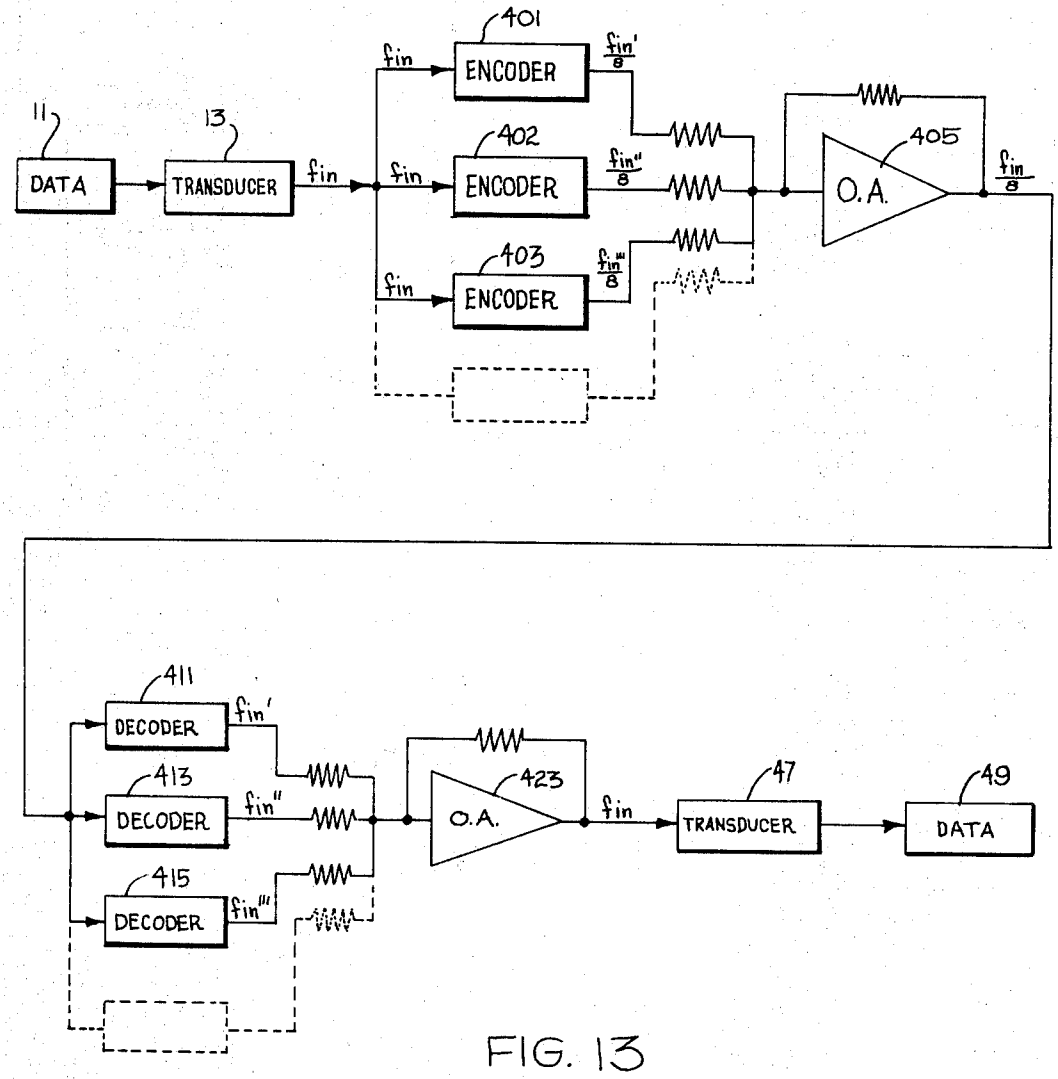

FIG. 13

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Patented Nov. 17, 1970

3,541,266

BANDWIDTH COMPRESSOR AND EXPANDER

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Continuation of application Ser. No. 508,635, Oct. 22, 1965, which is a continuation-in-part of application Ser. No. 474,243, July 23, 1965. This application Sept. 30, 1968, Ser. No. 763,989

Int. Cl. H04b 1/66

U.S. Cl. 179—15.55 7 Claims

ABSTRACT OF THE DISCLOSURE

An electronic system is disclosed for the transmission of high-bandwidth intelligence over a low-bandwidth communication channel by means of frequency compression and expansion. A bandwidth compressor is used to lower all frequency components by a given amount, and the bandwidth expander conversely raises all frequency components by the same amount. A plurality of encoders and decoders are tuned in successive stages over the whole frequency spectrum utilized by the data being transmitted.

The present invention is a continuation of application Ser. No. 508,635, filed Oct. 22, 1965 now abandoned, which was a continuation-in-part of application Ser. No. 474,243 now abandoned, entitled Bandwidth Compressor and Expander, filed in the names of the same inventors on July 23, 1965, and assigned to the same assignee.

The present invention relates to electronic circuits, and more particularly to bandwidth compressor and expander circuits.

In the field of electronic communications, telephone, telegraph, teletype, facsimile, radio, television, and any other transmission of data, it is desirable to use as little of the available frequency spectrum as possible, while still transmitting all of the desired information.

The reason for this is simply that the less space in the spectrum that must be used to transmit a given amount of information, the more room will be available for additional channels of communication. For instance, a common telephone speech channel covers the frequency range of from approximately 300 to 3,000 cycles per second. With bandwidth compression, this could be cut in half, or to one-tenth, or even greater and still transmit the same information. In other words, two to ten or more phone conversations could conceivably be carried in the channel space normally required by just one. This philosophy can be extended to all forms of electronic communications previously mentioned plus the fields of hi-fi, stereo, electronic organs and other musical instruments, etc. Television channels consume an enormous amount of channel space. Use of a bandwidth compressor would provide space for many more television channels and make video tape recording much simpler and less costly.

A typical electronic communication channel involves a data input source, an input transducer, a transmitter, a receiver, and an output transducer. If the data being transmitted is the spoken human voice, the input transducer could be a microphone, the transmitter could be a radio transmitter, the receiver could be a radio receiver, and the output transducer could be a loudspeaker, which finally completes the channel by turning the electrical impulses back into the original acoustical data.

If, after the entering data is converted to equivalent electrical impulses by the transducer, these impulses are altered by an encoder, the data can still be processed at the receiver by providing a decoder which performs the exact opposite function of the encoder. In the case of a bandwidth compressor the encoder is a device which instantaneously lowers all frequency components entering it by a given amount and the decoder conversely raises all frequency components entering it by the same amount. For example, let us say that a 1000 cycle per second sine wave is being transmitted and it is desired to compress the bandwidth by ½. The encoder would therefore have an output of 500 cycles per second for an input of 1000 cycles per second and the decoder would have an output of 1000 cycles per second for an input of 500 cycles per second. A second requirement is that the amplitude throughout the system must be preserved. In a practical system, the encoder and decoder must operate over the whole frequency spectrum which is being utilized by the data being transmitted. The band width reduction capability should be as high a ratio as is possible depending on system requirements. The example given above of 2 to 1 reduction should only be construed as an example and could just as well have been some other ratio.

It is an object of the present invention, therefore, to provide a bandwidth compressor and expander circuit.

It is yet another object of the present invention to provide a circuit for the transmission of high-bandwidth intelligence over a low-bandwidth communication channel by frequency compression and expansion.

According to one embodiment of the present invention, a bandwidth compressor and expander circuit comprises an encoder which feeds a carrier frequency and the input intelligence to a balanced modulator and then divides the resulting upper sideband frequency by a constant. The carrier frequency is divided by the same constant and the two divided frequencies are fed to a demodulator. The result is that the bandwidth of the input intelligence is compressed.

After being transmitted and received, the compressed intelligence is supplied to a decoder where it is fed to a balanced modulator along with the carrier frequency which has been divided by the same constant. The resulting upper sideband frequency is then multiplied by the same constant and is fed with the original carrier frequency to a demodulator. The result is a reconstruction of the original input intelligence.

The features of the present invention which are believed to be novel are set forth with particularity in the appended claims. The present invention, both as to its organization and manner of operation, together with further objects and advantages thereof, may best be understood by reference to the following description, taken in connection with the accompanying drawings, in which:

FIG. 1 is a block diagram of a bandwidth compressor and expander circuit according to the present invention.

FIG. 2 is a block diagram of an encoder useful in the circuit of FIG. 1.

FIG. 3 is a schematic diagram of the clock shown in FIG. 2.

FIG. 4 shows the waveforms of the outputs of the flip-flop shown in FIG. 2.

FIG. 5 is a schematic diagram of the modulation phase shifter shown in block form in FIG. 2.

FIG. 6 is a schematic diagram of the balanced modulator shown in block form in FIG. 2.

FIG. 7 is a schematic diagram showing the operational amplifier of FIG. 2 in detail.

FIG. 8 is a schematic diagram of the frequency divider shown in block form in FIG. 2.

FIG. 9 is a schematic diagram of the demodulator shown in block form in FIG. 2.

FIG. 10 is a block diagram of a decoder useful in the circuit of FIG. 1 with the encoder shown in FIG. 2.

FIG. 11 is a schematic diagram of the frequency multiplier shown in block form in FIG. 10.

FIG. 12 is a synchrogram showing the waveforms present in the frequency multiplier of FIG. 11.

FIG. 13 is a block diagram of a system utilizing the present invention.

Turning now to the drawings, FIG. 1 shows data source **11** connected to transducer **13**, which supplies the modulating frequency, f_{in}, to balanced modulator **15**. Carrier **17** supplies the carrier frequency, f_c, to balanced modulator **15** and to frequency divider **19**. The output of balanced modulator **15** is supplied to lower-sideband suppressor **21**, the output of which, f_c+f_{in}, is supplied to frequency divider **23**. The outputs of frequency dividers **19** and **23** are fed to synchronous demodulator **27**, the output of which, f_{in}/n, where n represents any constant, is supplied to transmitter **29**.

When a low frequency is made to amplitude modulate a higher frequency, several new frequency components are produced. In addition to the carrier frequency and the modulating frequency there are also produced sidebands which contain the sum and difference frequencies. For example, if the carrier frequency is 100 kc. (kilocycles) and the modulating frequency is 2 kc. then the frequencies present are 100 kc., 2 kc., 102 kc., and 98 kc. If the modulation is accomplished in a balanced modulator it is possible to suppress the carrier frequency leaving only the sideband frequencies of 102 kc. and 98 kc. It is further possible to suppress either one of the sideband frequencies while leaving the other one intact.

If the lower sideband of 98 kc. is suppressed by a filter or other means, then the remaining frequency is 102 kc. This represents the carrier (100 kc.) plus the modulating frequency (2 kc.). We now have translated the frequency we wish to operate on to a higher frequency domain. If we now divide the 102 kc. frequency by a constant such as 2, the result is 51 kc. By dividing the carrier frequency of 100 kc. by 2 also, and feeding both the 51 kc. and 50 kc. to a synchronous demodulator, there is produced an output frequency of 1 kc. This constitutes a division of the input intelligence by 2, or a bandwidth compression of ½.

The output of transmitter **29** is received by receiver **33**, the output of which is connected to balanced modulator **35**. Carrier **37** supplies a carrier frequency, f_c/n, to balanced modulator **35** and to frequency multiplier **39**. The output of balanced modulator **35** is supplied to lower sideband suppressor **41**, the output of which, $(f_c+f_{in})/n$, is supplied to frequency multiplier **43**. The outputs of frequency multipliers **39** and **43** are fed to synchronous demodulator **45**, the output of which, f_{in}, is supplied to transducer **47**, which supplies the output intelligence as data **49**.

There can thus be seen how the encoder portion of FIG. 1, comprising carrier **17**, balanced modulator **15**, lower sideband suppressor **21**, frequency dividers **19** and **23**, and synchronous demodulator **27**, corresponds to the decoder portion comprising carrier **37**, balanced modulator **35**, lower sideband suppressor **41**, frequency multipliers **39** and **43**, and synchronous demodulator **45**. The preceding comments on expansion apply also as well to compression, except for obvious differences. The frequency of the output intelligence will be equal to that of the input intelligence.

FIG. 2 is a block diagram showing an encoder that could be substituted for the encoder portion of the circuit shown in FIG. 1 and illustrates a system that could be used to generate a frequency division of eight times.

Clock **51** is connected to flip-flop **53** (FF1), which is in turn connected to flip-flop **55** (FF2) and flip-flop **57** (FF3). All the flip-flops shown in FIG. 2 divide by 2, by way of example only, and the output of flip-flop **57** is 90° out of phase with the output of flip-flop **55**. Since clock **51** generates a 400 kc. output, by way of example only, the outputs of flip-flops **55** and **57** are 100 kc. each and 90° out of phase with each other.

The input intelligence, f_{in}, representing the voice or music, etc., is received by band pass filter **61**, which allows the desired frequency band to pass through modulation

phase shifter **63**, so as to produce two outputs which are 90° out of phase with respect to each other. The carrier frequency of 100 kc. and f_{in} which are at 0° are supplied to balanced modulator **65**, and the carrier frequency of 100 kc. and f_{in} which are at 90° are supplied to balanced modulator **67**. The outputs of modulators **65** and **67** are fed to operational amplifier **71** and then to tank mixer **75**, which is tuned so as to pass through a frequency equal to the upper sideband of 100 kc.$+f_{in}$, which is supplied to frequency divider **77**.

The 100 kc. output of flip-flop **55** is also supplied to flip-flop **81** (FF4), and then in turn passes through flip-flops **83** (FF5) and **85** (FF6). The resulting frequency is ⅛ the carrier frequency of 100 kc., or 12.5 kc. In the example being described, frequency divider **77** divides by 8, and the output therefrom of 12.5 kc.$+f_{in}/8$ is supplied to demodulator **87**, which also receives the output from flip-flop **85**. The output of demodulator **87** will be $f_{in}/8$, which can then be supplied to a transmitter as shown in FIG. 1.

The encoder shown in FIG. 2 will operate over the desired frequency spectrum and be capable of dividing by eight times. For simplicity, the majority of the system has been designed with integrated micrologic circuits.

The phasing method of generating single sideband frequencies which was used requires that the carrier frequency of 100 kc. be generated with both the 0° and 90° phase relationships, and also that the modulation have both the 0° and 90° phases. Digital techniques are used at the carrier frequencies for accuracy of phases and division.

FIG. 3 shows the clock circuit, which is a thyristor relaxation oscillator, in detail. One end of resistor **101** is connected to a source of positive potential and to the collector of NPN transistor **103**. The other end of resistor **101** is connected to the cathode of Zener diode **105** and to the base of transistor **103**. The anode of diode **105** is grounded, and the emitter of transistor **103** is grounded through capacitor **107**. The emitter of transistor **103** is also connected to resistor **109**, which is in series with coil **111**. The other end of coil **111** is connected to thyristor **113**, capacitor **115** and to ground through capacitor **117**. The output from capacitor **115** is the sawtooth wave shown in FIG. 3 and has a peak of 3 volts, which is fed to flip-flop **53**.

All the flip-flops are integrated binary bistable multivibrator ones such as those manufactured by Fairchild Camera and Instrument Corporation. The flip-flop **53** divides the 400 kc. clock frequency by 2, and generates both the true term and its complement. Since the true term is fed to flip-flop **55** and the complement term is fed to flip-flop **57**, the outputs of FF2 and FF3 are 90° apart.

FIG. 4 is a synchrogram showing the described relationships between the waveforms of the clock output and FF1–FF6.

FIG. 5 shows the circuit details of modulation phase shifter **63**. The output of band pass filter **61** is fed to capacitor **121**. The other terminal of capacitor **121** is connected to transistor bias resistors **125** and **127** and to the base of NPN transistor **129**. The other end of resistor **125** is connected to a source of positive potential, and the other end of resistor **127** is grounded. The collector of transistor **129** is connected to the source of positive potential through resistor **131** and to the base of transistor **133** through capacitor **135**. The emitter of transistor **129** is connected to ground through resistor **137** and to the base of transistor **133** through resistor **139**. Transistor **133** is similarly connected to the base of transistor **141**, which is similarly connected to the base of transistor **143**, which is similarly connected to the base of transistor **145**, making a total of 5 stages, with each stage operating as a phase inverter. The collector and emitter of transistor **145** are connected through capacitor **146** and resistor **147**, respectively, to the base of transistor **148**, which is connected as an emitter follower to act as a low impedance

source to the base of transistor **149**, which serves as a normalizing amplifier to bring the signal level up to the desired level. The 90° phase shifted output is taken from the collector of transistor **149**.

The output of band pass filter **61** is also fed to capacitor **151**, the other end of which is connected to the base of transistor **153**, as was capacitor **121** connected to transistor **129**. Transistor **153** is connected to the base of transistor **155**, as was transistor **129** connected to transistor **133**. Transistor **155** is connected in turn to the base of transistor **157** as was transistor **133** connected to transistor **141**. Transistor **157** is similarly connected to transistor **159**, making a total of 4 phase-inverter stages. The last stage is similarly connected to transistor **161** of an emitter follower and then to transistor **163** of a normalizing amplifier. The 0° output is taken from the collector of transistor **163**.

One of the essential requirements of phase shifter **63** is that it must maintain the 90° phase shift for the entire range of frequencies over which the system is to be operated. To accomplish this, the phase shifter **63** has two legs, each having a plurality of phase-inverter stages followed by an emitter follower and then by a normalizing amplifier. One leg has one less phase-inverter stage than does the other leg, to achieve the 90° phase shift. The values of the components for each stage are selected so that each stage will cover different but overlapping frequency ranges.

FIG. 6 shows the circuit details of balanced modulator **65** into which the 0° carrier and the 0° modulation are fed. The 90° carrier and the 90° modulation are fed into balanced modulator **67**, which is identical to modulator **65**.

FIG. 7 shows the circuit details of the portion of FIG. 2 between the outputs of balanced modulators **65** and **67** and the input to frequency divider **77**. The outputs of both balanced modulators are connected to an operational amplifier which performs the addition of the two signals which are 90° out of phase with respect to each other. The added signals are fed to a high Q tank circuit where they are combined. The combination of the 0° and 90° modulation at this point are such as to cancel the carrier and the lower sideband, retaining only the information contained in the upper sideband.

Buffer **171** is an emitter follower circuit and is used as a buffer because it has a high input impedance and a low output impedance. Buffer **171** is a part of the operational amplifier block **71**, as far as function is concerned. Amplifier **173** and buffer **175** amplify and buffer the output of the tank circuit and are part of the tuned tank mixer block **75**, as far as function is concerned.

FIG. 8 shows the circuit details of the digital divider circuit used to divide the upper single sideband eight times, by way of example. The upper single sideband frequency in the described example is the sum of 100 kc. and the modulation. The amplitude of the single sideband is dependent upon the amplitude of the modulation.

Amplifier **201** of frequency divider **77** is a high gain amplifier whose output stage swings into saturation for all input amplitudes, that is, for the minimum signal input. Amplifier **201** generates a constant voltage output pulse equal in frequency to the incoming single sideband. Flip-flops **203**, **205**, and **207** are binary flip-flops that divide the output of amplifier **201** by 2 for each stage. Thus, the three stages shown divide the single sideband frequency by eight. The divided single sideband frequency is then use to modulate the envelope frequency component.

The envelope or amplitude detector **209** detects the modulation envelope by rectifying the single sideband and filtering it to arrive at the amplitude of the single sideband. The amplitude detector **209** generates an output equal to the amplitude of the single sideband input. This output voltage is used as the collector voltage of an emitter follower circuit whose base is driven by the output of flip-flop **207**.

Thus, in FIG. 8, the collector of transistor **213** of envelope or amplitude modulator **211** is connected to the emitter of transistor **215** of amplitude detector **209**. The base of transistor **213** is connected through resistor **217** to the output of flip-flop **207**, and the emiter of transistor **213** is connected to a −6 volt power supply through resistor **219** and to the anode of germanium diode **221**. The cathode of diode **221** is connected to ground through resistor **223** and supplies the output of amplitude modulator **211**.

The base of transistor **213** is driven on and off by the flip-flop divider. The emitter voltage of transistor **213**, however, can never be greater than its collector voltage. The emitter, therefore, will be driven on and off by flip-flop **207**, and its voltage will be whatever the collector voltage is. Amplitude modulator **211** chops the amplitude envelope at the divided frequency.

Waveform **225** shown in FIG. 8 represents the output from flip-flop **207**, waveform **227** represents the output of amplitude detector **209**, and waveform **229** represents the output of frequency divider **77**, which in the example described is 12.5 kc.+$f_{in}/8$. Thus, the upper single sideband of 100 kc.+f_{in} has been divided 8 times linearly, while retaining its amplitude information. In addition, the 100 kc. carrier has been divided 8 times as the output of flip-flop **85** in FIG. 2. To demodulate the divided single sideband, it is necessary merely to mix the divided single sideband and the divided carrier.

FIG. 9 shows the circuit details of demodulator **87**. The square wave inputs of $f_c/8$ and $(f_c+f_{in})/8$ are converted to sine waves in the tank circuits formed by coil **251** and capacitor **253**, and by coil **257** and capacitor **259**, respectively, for mixing purposes. The sine waves are then buffered by buffers **261** and **263**, respectively, to isolate the tanks from each other. Diode **265** removes the bottom portion of the envelope, and the filters formed by coil **267** and capacitor **269**, and by coil **271** and capacitor **273** remove the carrier, leaving only the modulation, having a frequency of $f_{in}/8$.

FIG. 10 is a block diagram corresponding to FIG. 2 and shows a decoder that could be substituted for the decoder portion of the circuit shown in FIG. 1. Clock **301** is connected to flip-flop **303** (FF1′), which is connected to flip-flop **305** (FF2′) and to demodulator **307**. The output of flip-flop **305** is connected to flip-flop **309** (FF3′) which is in turn connected to flip-flops **311** (FF4′) and **313** (FF5′). The output of flip-flop **311** is 90° out of phase with the output of flip-flop **313**. Since clock **301** generates a 200 kc. output, the outputs of flip-flops **311** and **313** are 12.5 kc. each and 90° out of phase with each other.

The input intelligence, $f_{in}/8$, is received by band pass filter **315**, and is then passed through modulation phase shifter **317**, so as to produce two outputs which are 90° out of phase with respect to each other. The outputs of flip-flop **311** and modulation phase shifter **317** (0°) are supplied to balanced modulator **319**, and the outputs of flip-flop **313** and modulation phase shifter **317** (90°) are supplied to balanced modulator **321**. The outputs of modulators **319** and **321** are fed to operational amplifier **323** and then to tank mixer **325**, which is tuned so as to pass through only a frequency equal to the upper sideband of 12.5 kc.+f_{in}/n which is supplied to linear multiplier **327**. The output of multiplier **327** is supplied to demodulator **307**. Since the 100 kc. output of flip-flop **303** is also supplied to demodulator **307**, the output thereof will be f_{in}, which is the reconstructed original modulation.

The block diagram of the frequency expander utilizes substantially the same blocks or circuits as does the frequency compressor, except that the blocks are interconnected to generate multiplication instead of division. The only block that is significantly different, therefore, is linear multiplier **327**.

FIG. 11 shows the schematic diagram of multiplier **327** in detail. It can be seen from FIG. 11 that the amplifier

201, amplitude detector 209 and amplitude modulator 211 are identical in both frequency divider 77 and frequency multiplier 327. In fact, the only difference between the divider 77 and multiplier 327 is that the 3 flip-flop stages 203, 205 and 207 of the former are replaced by 3 series-connected multiplier stages in the latter. Each multiplier stage has a phase shifter and clipper 331, the 0° and 90° outputs of which are connected to an exclusive "OR" circuit 333, the output of which is connected to a tuned-tank circuit 335. This multiplier stage is followed by two identical multiplier stages 337 and 339. The phase shifter and clipper of the first multiplier stage is connected to the output of amplifier 201, and the output of the third multiplier stage 339 is connected to amplitude modulator 211.

Phase shifter and clipper 331 has two outputs 90° out of phase with each other, and each of which has been clipped into a square wave. The output of exclusive "OR" circuit 333 is supplied to tank section 341 of tuned tank 335. The output of tank section 341 is supplied to bootstrapped emitter follower section 343 of tuned tank 335. The output of bootstrapped emitter follower section 343 is fed to the next multiplier stage 337.

FIG. 12 shows the relationships between the various waveforms present within frequency multiplier 327. It can be seen from FIG. 12 that the output of each multiplier stage is doubled in frequency and 90° out of phase with its input. Thus, with the 3 multiplier stages of frequency multiplier 327, the output thereof will be multiplied by 8 and in phase with the input thereto.

A divider or a multiplier circuit will work only at the specific frequency to which it is tuned. A band of frequencies will not be linearly divided or multiplied. In the described system, however, the divider and multiplier are operating on the carrier, and not upon the information directly. The information is a part of the carrier, it is true, but the information causes the carrier to deviate in frequency less than from 1 to 3%. A small deviation such as that in the carrier frequency can be accepted by the divider or multiplier circuit without difficulty. Thus, the system shown in FIG. 1 could not be simplified by merely connecting the frequency divider directly to the output of the transducer and the frequency multiplier directly to the output of the receiver. The wide band of frequencies that would then be fed directly to the divider and multiplier would make the system inoperative.

FIG. 13 is a block diagram of the frequency compressor and expander showing the entire system for a compression of eight times, by way of example only. Data source 11 is the information, speech, music, etc. to be compressed. The transducer 13 converts the speech, music, etc. into the electrical frequency equivalent, f_{in}. Each of the encoders 401, 402 and 403 is the same as the encoder shown in FIG. 2 and is a bandwidth compressor for a compression of eight times, except as will be described. Each encoder is capable of dividing only those frequencies that are sinusoidal and cross zero, and that range of mixed frequencies whose highest beat frequency is not greater than the lowest resulting divided frequency. Thus, for a data range of 300 to 3000 c.p.s., to divide by 8, resulting in a lowest divided frequency of 37.5 c.p.s., the encoder for the first band would be tuned to 300 to 337.5 c.p.s. The second encoder would be tuned to 337.5 to (337.5+337.5/8) c.p.s. Each additional encoder would be tuned in successive ⅛ octave stages. For a division by 4, the incoming information would be channelled into ¼ octave bands, for a division of 2, into ½ octave bands. The incoming data may contain frequencies far in excess of the frequency coverage of any one band. Thus, as many bands as are required to cover the data frequency range may be adjacently spaced to provide coverage of the full data frequency range. Each band of frequencies is fed to an identical encoder, except that the band pass filter 61 of each encoder is tuned to the proper band. The required number of encoders are summed together in an operational amplifier 405 through summing resistors. The output of amplifier 405 is then $f_{in}/8$ for the example being described.

The compressed data frequency $f_{in}/8$, representing a bandwidth compression of 8 times, is then transmitted via telephone, radio, etc. to the bandwidth expander. The bandwidth expander decodes the compressed frequency $f_{in}/8$ back to the original frequency f_{in}. Each decoder 441, 413 and 415 is the same as the decoder shown in FIG. 10, except for the frequencies to which its band pass filter is tuned, and can accept frequencies that are sinusoidal and cross zero. For the described example, $f_{in}/8$ must be separated into ⅛ octave bands. The ⅛ octave band of each decode must coincide with one of the encoder bands divided by eight. For example, the lowest ⅛ octave band in the expander will be 37.5 c.p.s. to 37.5+37.5/8, or 37.5 c.p.s. to about 42.18 c.p.s. Each additional decoder would be tuned in successive ⅛ octave stages.

The required number of adjacent bands are then summed together in an operational amplifier 423 to reproduce f_{in}. Transducer 47 is then utilized to supply the output intelligence as data 49.

While particular embodiments of the present invention have been shown and described, it will be obvious to those skilled in the art that changes and modifications may be made without departing from this invention in its broader aspects, and, therefore, the aim in the appended claims is to cover all such changes and modifications as fall within the true spirit and scope of this invention.

We claim:

1. A bandwidth compressor comprising:
(a) a clock generator coupled to a plurality of flip-flop circuits having first and second outputs 90° out of phase with respect to each other,
(b) a modulation phase shifter adapted for converting input intelligence into first and second outputs 90° out of phase with respect to each other,
(c) a first balanced modulator coupled to said first output of said flip-flop circuits and to said first output of said modulation phase shifter,
(d) a second balanced modulator coupled to said second output of said flip-flop circuits and to said second output of said modulation phase shifter,
(e) an operational amplifier coupled to the outputs of said first and second balanced modulators,
(f) a tuned-tank mixer circuit coupled to the output of said operational amplifier, the output of said tuned-tank mixer circuit being a single sideband frequency,
(g) a first frequency divider circuit coupled to the output of said tuned-tank mixer and dividing said single sideband frequency by a constant,
(h) a second frequency divider circuit coupled to said first output of said flip-flop circuits and dividing it by said constant, and
(i) a demodulator coupled to the outputs of said first and second frequency dividers and generating therefrom an output having a frequency equal to that of said input intelligence divided by said constant.

2. A bandwidth expander comprising:
(a) a clock generator coupled to a plurality of flip-flop circuits having first and second outputs 90° out of phase with respect to each other,
(b) a modulation phase shifter adapted for converting input intelligence into first and second outputs 90° out of phase with respect to each other,
(c) a first balanced modulator coupled to said first output of said flip-flop circuits and to said first output of said modulation phase shifter,
(d) a second balanced modulator coupled to said sec-

ond output of said flip-flop circuits and to said second output of said modulation phase shifter,

(e) an operational amplifier coupled to the outputs of said first and second balanced modulators,

(f) a tuned-tank mixer circuit to the output of said operational amplifier, the output of said tuned-tank mixer circuit being a single sideband frequency,

(g) a frequency multiplier circuit coupled to the output of said tuned-tank mixer and multiplying said single sideband frequency by a constant, and

(h) a demodulator coupled to the output of said frequency multiplier and to a carrier having a frequency equal to that of said first output of said flip-flop circuits multiplied by said constant, and generating therefrom an output having a frequency equal to that of said input intelligence multiplied by said constant.

3. A bandwidth compressor and expander comprising:

(a) first means for generating first and second carriers each having a first frequency and being 90° out of phase with respect to each other,

(b) a first modulation phase shifter adapted for converting input intelligence having a second frequency into first and second outputs 90° out of phase with respect to each other,

(c) a first balanced modulator coupled to said first carrier and to said first output of said modulation phase shifter,

(d) a second balanced modulator coupled to said second carrier and to said second output of said modulation phase shifter,

(e) a first operational amplifier coupled to the outputs of said first and second balanced modulators,

(f) a first tuned-tank mixer circuit coupled to the output of said first operational amplifier, the output of said first tuned-tank mixer circuit being a single sideband having a third frequency,

(g) a first frequency divider circuit coupled to the output of said tuned-tank mixer and dividing said third frequency by a constant,

(h) a second frequency divider circuit coupled to said first carrier and dividing it by said constant,

(i) a first demodulator coupled to the outputs of said first and second frequency dividers and generating therefrom an output having a fourth frequency equal to that of said input intelligence divided by said constant,

(j) second means for generating third and fourth carriers, each having a fifth frequency equal to said first frequency divided by said constant and 90° out of phase with respect to each other,

(k) a second modulation phase shifter adapted for converting the output of said demodulator into first and second outputs 90° out of phase with respect to each other,

(l) a third balanced modulator coupled to said third carrier and to said first output of said second modulation phase shifter,

(m) a fourth balanced modulator coupled to said fourth carrier and to said second output of said second modulation phase shifter,

(n) a second operational amplifier coupled to the outputs of said third and fourth balanced modulators,

(o) a second tuned-tank mixer circuit coupled to the output of said operational amplifier, the output of said second tuned-tank mixer being a simple sideband having a sixth frequency,

(p) a first frequency multiplier circuit coupled to the output of said second tuned tank mixer and multiplying said sixth frequency by said constant,

(q) a second frequency multiplier circuit coupled to said third carrier and multiplying it by said constant, and

(r) a second demodulator coupled to the outputs of said first and second frequency multipliers and generating therefrom an output having said second frequency.

4. A circuit as defined in claim 3 in which said first frequency divider circuit comprises:

(a) a high-gain amplifier,

(b) an amplitude detector coupled to the input of said amplifier,

(c) a plurality of series-connected flip-flop circuits coupled to the output of said amplifier, and

(d) an amplitude modulator coupled to the outputs of said amplitude detector and said flip-flop circuits.

5. A circuit as defined in claim 4 in which said amplitude modulator comprises a transistor having its collector coupled to the output of said amplitude detector, its base coupled to the output of said flip-flop circuits, and its emitter coupled to the anode of a diode, the output of said amplitude modulator being coupled to the cathode of said diode.

6. A circuit as defined in claim 3 in which said first frequency multiplier circuit comprises:

(a) a high-gain amplifier,

(b) an amplitude detector coupled to the input of said amplifier,

(c) a plurality of series-connected stages coupled to the output of said amplifier, each of said stages comprising a phase shifter and clipper circuit, an exclusive "OR" circuit coupled to the output of said phase shifter and clipper circuit, and a tuned-tank circuit coupled to the output of said exclusive "OR" circuit, and

(d) an amplitude modulator coupled to the outputs of said amplitude detector and said plurality of series-connected stages.

7. A circuit as defined in claim 3 in which said first modulation phase shifter comprises:

(a) a first leg having a plurality of phase-inverter stages, an emitter follower coupled to the output of said plurality of phase-inverter stages, and a normalizing amplifier coupled to the output of said emitter follower, and

(b) a second leg having a plurality of phase-inverter stages, an emitter follower coupled to the output of said plurality of phase-inverter stages of said second leg, and a normalizing amplifier coupled to the output of said emitter follower of said second leg, the quantity of said phase-inverter stages in said first and second legs being unequal, and in each of said legs the components of each phase-inverter stage having different values such that said stages operate at different but overlapping frequency ranges.

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