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(71) Applicants (for all designated States except US): **ADVANCED MICRO DEVICES, INC.** [US/US]; One AMD Place, Mail Stop 68, P.O. Box 3453, Sunnyvale, CA 94088-3453 (US). **AMD FAB 36 LIMITED LIABILITY COMPANY & CO. KG** [DE/DE]; Wilschdorfer Landstrasse 101, 01109 Dresden (DE).

(72) Inventors; and

(75) Inventors/Applicants (for US only): **KRONHOLZ, Stephan** [DE/DE]; Weinbergstrasse 18, 01129 Dresden (DE). **NAUMANN, Andreas** [DE/DE]; Louisenstr. 61, 01099 Dresden (DE). **BEERNINK, Gunda** [DE/DE]; Fichtenstrasse 1, 01097 Dresden (DE).

(74) Agent: **PFAU, Anton, K.**; Grünecker, Kinkeldey, Stockmair & Schwanhäusser, Leopoldstrasse 4, 80802 München (DE).

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(57) Abstract: The growth rate in a selective epitaxial growth process for depositing a threshold adjusting semiconductor alloy, such as a silicon/germanium alloy, may be enhanced by performing a plasma assisted etch process prior to performing the selective epitaxial growth process. For example, a mask layer may be patterned on the basis of the plasma assisted etch process, thereby simultaneously providing for a superior device topography during the subsequent growth process. Hence, the threshold adjusting material may be deposited with enhanced thickness uniformity, thereby reducing overall threshold variability.



# **REDUCTION OF THICKNESS VARIATIONS OF A THRESHOLD ADJUSTING SEMICONDUCTOR ALLOY BY REDUCING PATTERNING NON-UNIFORMITIES PRIOR TO DEPOSITING THE SEMICONDUCTOR ALLOY**

## **FIELD OF THE PRESENT DISCLOSURE**

Generally, the present disclosure relates to sophisticated integrated circuits including advanced transistor elements that comprise highly capacitive gate structures including a metal containing electrode and a high-k gate dielectric of increased permittivity compared to gate dielectrics, such as silicon dioxide and silicon nitride.

## **DESCRIPTION OF THE PRIOR ART**

The fabrication of advanced integrated circuits, such as CPUs, storage devices, ASICs (application specific integrated circuits), and the like, requires a large number of circuit elements to be formed on a given chip area according to a specified circuit layout, wherein field effect transistors represent one important type of circuit elements that substantially determine performance of the integrated circuits. Generally, a plurality of process technologies are currently practiced, wherein for many types of complex circuitry including field effect transistors, MOS technology is currently one of the most promising approaches due to the superior characteristics in view of operating speed and/or power consumption and/or cost efficiency. During the fabrication of complex integrated circuits using, for instance, MOS technology, millions of transistors, e.g., n-channel transistors and/or p-channel transistors, are formed on a substrate including a crystalline semiconductor layer. A field effect transistor, irrespective of whether an n-channel transistor or a p-channel transistor is considered, typically comprises so-called pn-junctions that are formed by an interface of highly doped regions, referred to as drain and source regions, with a slightly doped or non-doped region, such as a channel region, disposed adjacent to the highly doped regions. In a field effect transistor the conductivity of the channel region, i.e., the drive current capability of the conductive channel, is controlled by a gate electrode formed adjacent to the channel region and separated therefrom by a thin insulating layer. The conductivity of the channel region upon formation of a conductive channel due to the application of an appropriate control voltage

to the gate electrode, depends on the dopant concentration, the mobility of the charge carriers, and – for a given extension of the channel region in the transistor width direction – on the distance between the source and drain regions, which is also referred to as channel length. Hence, in combination with the capability of rapidly creating a conductive channel below the insulating layer upon application of the control voltage to the gate electrode, the conductivity of the channel region substantially affects the performance of MOS transistors. Thus, as the speed of creating the channel, which depends on the conductivity of the gate electrode, and the channel resistivity substantially determine the transistor characteristics, the scaling of the channel length - and associated therewith the reduction of channel resistivity and reduction of gate resistivity – is a dominant design criterion for accomplishing an increase in the operating speed of the integrated circuits.

Presently, the vast majority of integrated circuits is fabricated on the basis of silicon due to the substantially unlimited availability thereof, the well-understood characteristics of silicon and related materials and processes and the experience gathered over the last 50 years. Therefore, silicon will likely remain the material of choice in the foreseeable future for circuit generations designed for mass products. One reason for the importance of silicon in fabricating semiconductor devices, has been the superior characteristics of a silicon/silicon dioxide interface that allows reliable electrical insulation of different regions from each other. The silicon/silicon dioxide interface is stable at high temperatures and thus, allows the performance of subsequent high temperature processes, as are required for example for anneal cycles to activate dopants and to cure crystal damage without sacrificing the electrical characteristics of the interface.

For the reasons pointed out above, silicon dioxide is preferably used as a gate insulation layer in field effect transistors that separates the gate electrode, frequently comprised of polysilicon or other metal containing materials, from the silicon channel region. In steadily improving device performance of field effect transistors, the length of the channel region has continuously been decreased to improve switching speed and drive current capability. Since the transistor performance is controlled by the voltage supplied to the gate electrode to invert the surface of the channel region to a sufficiently high charge density for providing the desired drive current for a given supply voltage, a certain degree of

capacitive coupling, provided by the capacitor formed by the gate electrode, the channel region and the silicon dioxide disposed therebetween, has to be maintained. It turns out that decreasing the channel length requires an increased capacitive coupling to avoid the so-called short channel behavior during transistor operation. The short channel behavior may lead to an increased leakage current and to a pronounced dependence of the threshold voltage on the channel length. Aggressively scaled transistor devices with a relatively low supply voltage and thus reduced threshold voltage may suffer from an exponential increase of the leakage current while also requiring enhanced capacitive coupling of the gate electrode to the channel region. Thus, the thickness of the silicon dioxide layer has to be correspondingly decreased to provide for the required capacitance between the gate and the channel region. For example, a channel length of approximately  $0.08\mu\text{m}$  may require a gate dielectric made of silicon dioxide as thin as approximately  $1.2\text{nm}$ . Although generally usage of high speed transistor elements having an extremely short channel may be restricted to high speed applications, whereas transistor elements with a longer channel may be used for less critical applications, such as storage transistor elements, the relatively high leakage current caused by direct tunneling of charge carriers through an ultra thin silicon dioxide gate insulation layer may reach values for an oxide thickness in the range of  $1\text{-}2\text{nm}$  that may no longer be compatible with requirements for performance driven circuits.

Therefore, replacing silicon dioxide, or at least a part thereof, as the material for gate insulation layers has been considered, particularly for extremely thin silicon dioxide gate layers. Possible alternative dielectrics include materials that exhibit a significantly higher permittivity so that a physically greater thickness of a correspondingly formed gate insulation layer nevertheless provides for a capacitive coupling that would be obtained by an extremely thin silicon dioxide layer. Commonly, a thickness required for achieving a specified capacitive coupling with silicon dioxide is referred to as capacitance equivalent thickness (CET). Thus, at a first glance, it appears that simply replacing the silicon dioxide with high-k materials is a straight forward way to obtain a capacitance equivalent thickness in the range of  $1\text{nm}$  and less.

It has been thus suggested to replace silicon dioxide with high permittivity materials such as tantalum oxide ( $\text{Ta}_2\text{O}_5$ ) with a  $k$  of approximately 25, strontium titanium oxide ( $\text{SrTiO}_3$ ) having a  $k$  of approximately 150, hafnium oxide ( $\text{HfO}_2$ ),  $\text{HfSiO}$ , zirconium oxide ( $\text{ZrO}_2$ ), and the like.

When advancing to sophisticated gate architecture based on high- $k$  dielectrics additionally, transistor performance may also be increased by providing an appropriate conductive material for the gate electrode so as to replace the usually used polysilicon material, since polysilicon may suffer from charge carrier depletion at the vicinity of the interface to the gate dielectric, thereby reducing the effective capacitance between the channel region and the gate electrode. Thus, a gate stack has been suggested in which a high- $k$  dielectric material provides for enhanced capacitance even at a less critical thickness compared to a silicon dioxide layer, while additionally maintaining leakage currents at an acceptable level. On the other hand metal containing non-polysilicon material, such as titanium nitride, aluminum oxide and the like, may be formed so as to directly connect to the high- $k$  dielectric material, thereby substantially avoiding the presence of a depletion zone. Since typically a low threshold voltage of the transistor, which represents the voltage at which a conductive channel forms in the channel region, is desired to obtain the high drive currents, commonly the controllability of the respective channel requires sophisticated lateral dopant profiles and dopant gradients, at least in the vicinity of the pn-junctions. Therefore, so-called halo regions are usually formed by ion implantation in order to introduce a dopant species whose conductivity type corresponds to the conductivity type of the remaining channel and semiconductor region so as to "reinforce" the resulting pn-junction dopant gradient after the formation of respective extension and deep drain and source regions. In this way, the threshold voltage of the transistor significantly determines the controllability of the channel, wherein a significant variance of the threshold voltage may be observed for reduced gate lengths. Hence, by providing an appropriate halo implantation region the controllability of the channel may be enhanced, thereby also reducing the variance of the threshold voltage, which is also referred to as threshold roll off, and also reducing significant variations of transistor performance with a variation in gate length. Since the threshold voltage of the transistors is significantly affected by the work function of the gate material that is in contact with the gate dielectric material, an appropriate adjustment of the effective work function with respect to the conductivity type of the transistor under consideration has to be guaranteed.

For example, appropriate metal-containing gate electrode materials such as titanium nitride, aluminum oxide and the like may frequently be used, wherein the corresponding work function may be adjusted so as to be appropriate for one type of transistor, such as n-channel transistors, while p-channel transistors may require a different work function and thus a differently treated metal containing electrode material in order to obtain the desired threshold voltage. In this case, complex and sophisticated manufacturing regimes may be required so as to provide different gate electrode materials in order to comply with the requirements of different transistor types. For this reason it has also been proposed to appropriately adjust the threshold voltage of transistor devices by providing a specifically designed semiconductor material at the interface between the high-k dielectric material and the channel region of the transistor device, in order to appropriately "adapt" the band gap of the specifically designed semiconductor material to the work function of the metal-containing gate electrode material, thereby obtaining the desired low threshold voltage of the transistor under consideration. Typically, a corresponding specifically designed semiconductor material, such as silicon/germanium and the like, may be provided by an epitaxial growth technique, which may also present an additional complex process step, which however may provide for reduced overall process complexity compared to the provision of the different metal-containing gate electrode materials or which may provide for increased flexibility in obtaining appropriate transistor characteristics.

It turns out, however, that the manufacturing sequence for providing the threshold adjusting semiconductor alloy may have a significant influence on threshold variability across an active region, as will be explained in more detail with reference to Figs 1a to 1f.

Fig 1a schematically illustrates a cross-sectional view of a semiconductor device 100 comprising a substrate 101, above which is formed a silicon-containing semiconductor material 103 having an appropriate thickness for forming therein and thereabove transistor elements. In the example shown, a buried insulating layer 102, for instance in the form of a silicon dioxide material, is positioned between the substrate 101 and the silicon-containing semiconductor layer 103. Moreover, an isolation structure 104, such as a shallow trench isolation, is formed in the semiconductor layer 103 so as to define a first crystalline "active" region 103a and a second active region 103b. In this context, an

active region is to be understood as a semiconductor material in which an appropriate dopant profile is to be created in order to form pn junctions for one or more transistor elements. In the example shown, the first active region 103a may correspond to one or more p-channel transistors while the second active region 103b may correspond to one or more n-channel transistors. Furthermore, in the manufacturing stage shown, a silicon dioxide mask layer 105 is formed above the first and second active regions 103a, 103b while typically the silicon dioxide material of the layer 105 may not be formed on the isolation structure 104, since typically the material of the layer 105 may be formed as a thermal oxide material.

The semiconductor device 100 as illustrated in Fig 1a may typically be formed on the basis of the following process techniques. First, the isolation structure 104 is formed on the basis of well-established lithography, etch, deposition, planarization and anneal techniques in which, for instance, a trench is formed in the semiconductor layer 103 on the basis of a lithography process, which is subsequently filled with an appropriate insulating material such as silicon dioxide, silicon nitride and the like. After removing any excess material further processing is typically continued by performing implantation sequences using an appropriate mask regime in order to introduce the appropriate dopant species for the active regions 103a, 103b. It should be appreciated that, although sophisticated planarization techniques may typically be used during the formation of the isolation structure 104, nevertheless a more or less pronounced surface topography may be obtained after the above-described process sequence so that the material of the active regions 103a, 103b may extend above the surface 104s of the isolation structure 104. Thereafter, the silicon dioxide 105 may be formed, for instance by oxidation on the basis of appropriately selected process parameters in order to obtain a desired thickness of the layer 105, which may act as a growth mask during the further processing of the semiconductor device 100. That is, as previously discussed, the active region 103a has to be exposed prior to performing a selective epitaxial growth process for depositing a silicon/germanium alloy that may provide for the required band gap offset or threshold voltage adjustment for responding p-channel transistors to be formed in and above the active region 103a.

Fig 1b schematically illustrates the semiconductor device in a further advanced manufacturing stage in which a resist mask 106 is formed above the second active region 103b. The resist mask may be formed by lithography techniques in accordance

with similar recipes as may also be used for the masking regime when introducing the corresponding well dopant species into the active regions 103a, 103b. Thus, after patterning the resist mask 106, the active region 103a is exposed to a wet chemical etch ambient 107, which may be performed on the basis of hydrofluoric acid (Hf), which may efficiently remove silicon dioxide selectively to silicon material. Thus, the exposed portion of the mask layer 105 is effectively removed wherein, however, the previously created surface topography with respect to the regions 103a, 103b and the isolation structure 104 may typically be maintained or may be even further increased. Next, a further wet chemical etch process is typically performed so as to remove the resist mask 106 on the basis of well-established etch recipes wherein, depending on the chemistry used, the resulting surface topography may further be increased.

Fig 1c schematically illustrates the semiconductor device 100 after the above-described process sequence and prior to actually depositing the silicon/germanium alloy on the exposed active region 103a. As illustrated, the moderately pronounced surface topography may result in the exposure of a horizontal surface portion 103h and also of a substantially vertical surface portion 103v, wherein both portions may act as deposition surface areas during the subsequent epitaxial growth process.

Fig 1d schematically illustrates the semiconductor device 100 during a selective epitaxial growth process 108 in which process parameters are selected in accordance with well-established recipes such that a significant material deposition may be restricted to the exposed surface areas 103h, 103v, while a material deposition on dielectric surface areas, such as the isolation structure 104 and the silicon dioxide mask layer 105 may be negligible. Consequently, during the selective epitaxial growth process 108 a silicon/germanium alloy 109 may selectively be formed on the active region 103a, wherein the surface portions 103h, 103v may act as a template material. For instance, in sophisticated applications the silicon/germanium alloy 109 may have to be provided with a desired target thickness, for instance of approximately 10 nm, when a germanium concentration of approximately 25 atomic percent is used. It should be appreciated that the material composition of the silicon/germanium alloy 109 as well as the thickness thereof may have a significant influence on the finally obtained threshold voltage and thus the finally obtained transistor characteristics. Though the material composition may be controlled with a high degree of accuracy, a significant degree of threshold variability may be observed in completed semiconductor devices, which is believed to be caused

by a thickness variation in the silicon/germanium alloy. Without intending to restrict the present disclosure to any theory, it is nevertheless assumed that a difference of growth rate may occur during the deposition process 108, which may have its origin in the different crystallographic orientations of the exposed surface areas 103h, 103v. That is, as illustrated in Fig 1d, the semiconductor layer 103 may be provided as a crystalline material having a surface orientation (100) while a transistor length direction and width directions are typically aligned with respect to the crystallographic (110) direction. Consequently, in particular at the area in the vicinity of the isolation structure 104, in which the surface portion 103v may have a substantially (110) orientation and in the area of a corresponding rounded portion 103r, other crystallographic directions may be present, thereby resulting in an increased growth rate compared to central portions having substantially the (100) orientation. As a consequence, a thickness 109p at the periphery of the active region 103a may be greater compared to a thickness 109c in the centre of the active region 103a, thereby possibly resulting in a threshold variability across the active region 103a.

Fig 1e schematically illustrates the semiconductor device 100 in a further advanced manufacturing stage. As illustrated, one or more p-channel transistors are formed in and above the active region 103a on the basis of respective silicon/germanium alloys, which may be referred to as alloys 109c, 109p since these materials may have a different thickness, as previously explained with reference to Fig 1d. Furthermore, an n-channel transistor 150b is formed in and above the active region 103b. The transistors 150a, 150b comprise an electrode structure 151 including a gate insulation layer 151b, comprising a high-k dielectric material, as is previously explained. Furthermore, a metal-containing electrode material, such as aluminum oxide, titanium nitride and the like, may be formed on the gate insulation layer 151b, followed by a further electrode material, such as polysilicon 151c. As illustrated, in the p-channel transistors 150a the gate insulation layers 151b are formed on the corresponding silicon/germanium alloys 109c, 109p, respectively, so that a threshold voltage of the transistors 150a, ie. the voltage at which a conductive channel forms in a channel region 153, may be determined by the characteristics of the alloys 109c, 109p and the materials 151b and 151a in combination with the corresponding characteristics of drain and source regions 154, which may also be formed on the basis of sophisticated dopant profiles, as previously explained. On the other hand, the band gap configuration of the channel region 153 of the n-channel transistor 150b is appropriate for the corresponding materials 151b, 151a of the

transistor 150b. Thus, in this configuration, although the silicon/germanium alloy may be formed on the basis of a specifically selected target thickness, which may result in substantially the same threshold voltages for transistors 150a, the previously occurring deposition non-uniformity may thus contribute to a corresponding difference in transistor characteristics, even if the remaining manufacturing processes for forming the gate electrode structure 151 and the drain and source regions 154 may be performed with a high degree of process uniformity.

Fig 1f schematically illustrates a cross-sectional view in order to depict a p-channel transistor, such as one of the transistors 150a of Fig 1e, along a transistor width direction. Thus, as illustrated, the gate electrode structure 151 may extend across the entire active region 103a and may also be formed above a portion of the isolation structure 104. Due to the deposition non-uniformities previously described, the silicon/germanium alloy 109 may comprise the peripheral portion 109p and the central portion 109c, which may thus differ in thickness, as discussed above. Consequently, also within a single transistor element a pronounced thickness variation of the silicon/germanium alloy may exist so that an overall threshold voltage may be obtained that may be difficult to be predicted due to the varying thickness of the silicon/germanium alloy 109. Moreover, for a difference in transistor width of various active regions, a further pronounced threshold variability may occur since for an increased overall transistor width the etch effect EDTE at the isolation structure 104 may be less pronounced compared to a transistor active region having a reduced width. Consequently, the dependence of the threshold on the transistor width may be significantly increased due to the thickness variation of the silicon/germanium material, even within a single transistor element, thereby contributing to a significant overall device variability, which may not be compatible with performance requirements of sophisticated semiconductor devices.

In view of the situation described above, the present disclosure relates to methods and semiconductor devices in which threshold voltage adjustment may be accomplished on the basis of a semiconductor alloy while avoiding or at least reducing the effects of one or more of the problems identified above.

## SUMMARY OF THE PRESENT DISCLOSURE

Generally, the present disclosure provides methods and semiconductor devices in which threshold variability may be reduced by enhancing the surface topography of active semiconductor regions prior to performing a selective epitaxial growth process. To this end, material of the active region under consideration may be removed in a highly controllable manner so as to significantly reduce the growth rate variability during the subsequent epitaxial growth process. For this purpose, in some illustrative embodiments, plasma assisted etch recipes may be used, for instance in the context of patterning growth mask thereby obtaining reduced pronounced surface topography, which may thus provide for enhanced uniformity during the epitaxial growth process.

One illustrative method disclosed herein comprises forming a mask layer on a first silicon-containing crystalline semiconductor regions and a second silicon-containing crystalline semiconductor region, wherein the first and second silicon-containing semiconductor regions are laterally separated by an isolation region. The method further comprises removing the mask layer selectively from the first silicon-containing crystalline semiconductor region while maintaining the mask layer on the second silicon-containing crystalline semiconductor region. Furthermore, the first silicon-containing crystalline semiconductor region is recessed and a threshold adjusting semiconductor alloy is selectively formed on the recessed first silicon-containing crystalline semiconductor region. The method further comprises forming a first electrode structure of a first transistor above the threshold adjusting semiconductor alloy and forming a second gate electrode structure of a second transistor above the second silicon-containing crystalline semiconductor region.

A still further illustrative method disclosed herein comprises exposing a surface of an active semiconductor region that is laterally enclosed by an isolation structure wherein any exposed surface areas of the exposed surface have substantially the same crystalline orientation. Moreover, the method comprises forming a threshold adjusting semiconductor material on the exposed surface by performing a selective epitaxial growth process. Finally, the method comprises forming a gate electrode structure of a transistor on the threshold adjusting semiconductor material wherein the gate electrode structure comprises a high-k dielectric material and a metal-containing electrode material formed on the the high-k dielectric material.

One illustrative semiconductor device disclosed herein comprises an active silicon-containing semiconductor region and an isolation structure laterally enclosing the active silicon-containing semiconductor region, wherein the isolation structure has a first edge and a second edge that define a width of the active silicon-containing semiconductor region. The semiconductor device further comprises a threshold adjusting semiconductor alloy formed on the active silicon-containing semiconductor region and extending from the first edge to the second edge and having a thickness with a variation of approximately 5 percent or less. Moreover, the semiconductor device comprises a gate electrode structure comprising a high-k gate insulation layer and a metal-containing electrode material that is formed on the high-k gate insulation layer.

## BRIEF DESCRIPTION OF THE DRAWINGS

Further embodiments of the present disclosure are defined in the appended claims and will become more apparent with the following detailed description when taken with reference to the accompanying drawings, in which:

Figs 1a – 1d schematically illustrate cross-sectional views during various manufacturing stages in selectively forming a silicon/germanium alloy on an active region of a p-channel transistor according to conventional strategies;

Figs 1e and 1f schematically illustrate cross-sectional views of transistor elements formed on the basis of the preceding conventional process strategy, thereby obtaining a pronounced threshold voltage variability, which is believed to be caused by a non-uniformity of growth rates;

Figs 2a and 2b schematically illustrate cross-sectional views of a semiconductor device during the deposition and patterning of a mask material wherein the patterning may be accomplished on the basis of a plasma assisted etch process according to illustrative embodiments;

Fig 2c schematically illustrates the semiconductor device during the manufacturing phase in which a certain degree of material removal and thus

recessing of the active region may be accomplished, thereby enhancing surface topography prior to selective epitaxial growth process according to further illustrative embodiments;

Figs 2d and 2e schematically illustrate cross-sectional views of the device during further manufacturing steps for forming a threshold adjusting semiconductor alloy according to illustrative embodiments;

Fig 2f schematically illustrates a top view of the semiconductor device after the epitaxial growth of the threshold adjusting semiconductor alloy; and

Figs 2g and 2h schematically illustrate cross-sectional views of the semiconductor device in a very advanced manufacturing stage in which sophisticated gate electrode structures including a high-k gate insulation material may be formed on the basis of the threshold adjusting semiconductor alloy having a reduced degree of thickness variability according to still further illustrative embodiments.

## DETAILED DESCRIPTION

While the present disclosure is described with reference to the embodiments as illustrated in the following detailed description as well as in the drawings, it should be understood that the following detailed description as well as the drawings are not intended to limit the subject matter disclosed herein to the particular illustrative embodiments disclosed, but rather the described illustrative embodiments merely exemplify the various aspects of the present disclosure, the scope of which is defined by the appended claims.

BasicallyAs one example, the present disclosure provides semiconductor devices and techniques in which sophisticated gate electrode structures may be formed in an early manufacturing stage on the basis of a high-k dielectric material and a metal-containing electrode material. The threshold voltage of one type of transistor may therefore be adjusted by providing an appropriate semiconductor material in the channel region of the corresponding transistors, which may be

accomplished by manufacturing process techniques with enhanced uniformity, thereby reducing the threshold variability compared to conventional strategies, as previously described. For this purpose, the surface topography of the exposed active region may be enhanced in order to use the number of different crystallographic orientations, which may typically be present at the edge of active regions when a more or less pronounced surface topography has been generated during the preceding manufacturing processes. That is, by removing material of the exposed active region in a highly controllable manner, that is, in some illustrative embodiments, on the basis of a plasma assisted etch process, a certain degree of recessing may be accomplished, thereby also reducing the amount of undesired surface areas, such as substantially vertical surface or sidewall portions at the periphery of the exposed active region. Consequently, the influence of undesired crystallographic orientations on the growth rate during the selective epitaxial growth process may be reduced thereby reducing the difference in thickness between central areas and peripheral areas of the epitaxially grown semiconductor material. It should be appreciated that the term 'thickness variability or uniformity' as used herein may be defined on the basis of thickness of the semiconductor alloy in the centre of an active region under consideration and by determining a percentage of a deviation from this "reference" thickness at the periphery of the active region. For instance, a thickness of 10 nm at the centre of the active region and a thickness of 12 nm at the periphery thereof may correspond to a thickness variability of 20 percent.

In some illustrative embodiments disclosed herein the highly controllable material removal in the active region may be accomplished during a plasma assisted etch process for patterning a mask layer, thereby maintaining a high degree of process efficiency with respect to the conventional strategy as previously described. For example, silicon nitride may be used as an efficient mask material which may efficiently be etched on the basis of plasma assisted etch chemistries using chlorine or fluorine-based recipes, as are well-established in the art. In other illustrative embodiments, an additional material removal may be applied, if desired, for instance on the basis of well controllable wet chemical etch processes and the like. Consequently, based on the previous plasma assisted etch process, any desired degree of recessing may be applied without

contributing to pronounced growth uniformities, as is typically caused in conventional strategies.

With reference to Figs 2a – 2j further illustrative embodiments will now be described in more detail, wherein also reference may be made to Figs 1a – 1f, if required.

Fig 2a schematically illustrates a cross-sectional view of a semiconductor device 200 comprising a substrate 201 and a silicon-containing semiconductor region 203, which may be in a substantially crystalline state. Furthermore, in some illustrative embodiments, as is for instance shown in Fig 2a, at least a portion of the device 200 may be formed on the basis of an SOI architecture in which a buried insulating layer 202 is positioned between the substrate 201 and the semiconductor layer 203. It should be appreciated, however, that the principles disclosed herein may also readily be applied to a bulk configuration in which the buried insulating layer 202 may be omitted, at least in some device areas of the semiconductor device 200. Furthermore, an isolation structure 204, such as a shallow trench isolation, may be provided in the semiconductor layer 203, thereby defining the first active region 203a and a second active region 203b. As previously explained with reference to the device 100, the active regions 203a, 203b may comprise a basic dopant profile for defining the conductivity type of corresponding transistors still to be formed in and above the active regions 203a, 203b. In one illustrative embodiment the active region 203a may represent an n-doped region in order to form one or more p-channel transistors therein. Similarly, the active region 203b may represent the active region of one or more n-channel transistors. In the following, a manufacturing sequence will be described in which a threshold adjusting semiconductor alloy may selectively be formed on the active region 203a in order to provide for a corresponding threshold voltage for one or more transistors to be formed therein. It should be appreciated, however, that also corresponding mechanisms for adjusting the threshold voltage may be applied to any transistor to be formed in and above the active region 203b or to both active regions 203a, 203b, depending on the overall device and process requirements. Furthermore, in the manufacturing stage shown, a mask layer 205 may be formed above the active regions 203a, 203b with an appropriate thickness, for instance with a thickness in the range of

approximately 10 nm or less. In one illustrative embodiment the mask layer 205 may be comprised of silicon nitride which may be formed in a highly controllable manner on the basis of well-established deposition recipes. In other illustrative embodiments, the mask layer 205 may be comprised of other materials, which may selectively be removed with respect to material of the active region 203a and the isolation structure 204 by using a plasma assisted etch recipe. For instance, silicon carbide, nitrogen-containing silicon carbide and the like represent appropriate materials that may be used for forming the mask layer 205.

The semiconductor device 200 may be formed on the basis of well-established process techniques, as also previously described with reference to the device 100, when the active regions 230a, 230b and the isolation structure 204 are considered. As previously discussed, during the corresponding manufacturing sequence, a more or less pronounced surface topography may be generated. Thereafter, the mask layer 205 may be formed on the basis of a deposition process 215, such as a thermally activated CVD (chemical vapour deposition) process, a plasma assisted deposition process and the like. It should be appreciated that a plurality of deposition recipes are well-established in the art so as to form a material layer, such as silicon nitride, silicon carbide and the like, with a desired thickness in the above-specified range with a high degree of uniformity.

Fig 2b schematically illustrates the semiconductor device 200 in a further advanced manufacturing stage. As illustrated, an etch mask 206, such as a resist mask, is formed in such a manner that the mask layer 205 above the active region 203b may be covered, while the portion of the mask layer 205 formed above the active region 203a may be exposed to a plasma assisted etch ambient 217. As previously explained, the etch mask 206 may be formed on the basis of well-established photolithography techniques. Thereafter, the plasma assisted ambient of the etch process 217 may be established, for instance on the basis of appropriate etch recipes and process parameters, wherein a plurality of chlorine and fluorine-based chemistries are available for silicon nitride, silicon carbide and the like, in a selective manner with respect to the isolation structure 204 and the material of the active region 203a. Thus, during the etch process 217 increasingly material of the layer 205 may be removed wherein finally during the

advance of the etch front the active region 203 may be exposed and may also interact with the etch ambient 217, however at a significantly reduced degree compared to the material of the mask layer 205. Consequently, due to the anisotropic nature of the etch process 217, a certain degree of recessing of the active region 203a may be accomplished without contributing to a pronounced corner rounding, as may typically occur on the basis of wet chemical etch recipes, as previously discussed.

Fig 2c schematically illustrates the semiconductor device 200 in a further advanced stage. As illustrated, a certain degree of recessing or thickness reduction, indicated as 203r, may be created thereby enhancing the overall surface topography, ie. reducing the height difference between the surface 203s and the surface 204s of the isolation region 204. As explained with reference to Fig 2e, in some illustrative embodiments the recess 203r may be accomplished on the basis of the etch process 217 (cf. Fig 2b), for instance by appropriately selecting an etch time of the process 217 wherein appropriate values may be obtained on the basis of test runs and the like. In other illustrative embodiments, an additional plasma assisted etch process 217a may be performed after substantially completely removing the exposed portion of the mask layer 205, when the etch behaviour of the material of the active region 203a is considered inappropriate with respect to the etch chemistry of the process 217 of Fig 2b. Also in these embodiments, the recess 203r may be obtained in a highly controllable manner, thereby reducing the height difference between the region 203a and the isolation structure 204, thereby also providing for a reduced degree of variability with respect to crystallographic orientations at the periphery of the active region 203a, as previously explained.

Fig 2d schematically illustrates the semiconductor device 200 when subjected to an etch sequence 218, which may include appropriate etch steps for removing contaminants, such as etch byproducts created during the preceding etch process or processes 217, 217a and which may also include etch steps for removing the etch mask 206 (cf. Fig 2c). For example, the etch sequence 218 may be performed on the basis of hydrofluoric acid (Hf) for cleaning exposed surface areas wherein prior to or after, if desired, a dedicated etch chemistry may be applied so as to remove the etch mask 206 (cf. Fig 2c). In some

illustrative embodiments the etch sequence 218 may further comprise a specific etch step for increasing the degree of recessing, as indicated by 203d, wherein a desired "anisotropic" etch behaviour may be accomplished due to the preceding plasma assisted etch steps. That is, further to the preceding recessing of the material of the active region 203a, a further etch step, even when exhibiting basically an isotropic behaviour, may result in a uniform material removal, even at the vicinity of the isolation structure 204. For example, well-controllable and very selective etch recipes are available, for instance based on tetra methyl ammonium hydroxide (TMAH), which basically represents a chemical agent for etching resist material which, however, may also be used for etching silicon material in higher concentrations at elevated temperature, wherein also a high degree of selectivity with respect to silicon dioxide, silicon nitride and the like may be achieved. Consequently, based on the corresponding etch chemistry a further recessing 230d, if desired, may be accomplished, for instance such that a corresponding thickness of the semiconductor alloy still to be formed, may be compensated for in view of enhancing overall process uniformity.

Fig 2e schematically illustrates the semiconductor device 200 when exposed to a deposition ambient 208, which is appropriately designed so as to selectively deposit a threshold adjusting semiconductor alloy 209 on the active region 203a. For instance, the semiconductor alloy 209 may comprise a silicon/germanium alloy with an appropriate germanium fraction, such as 20 atomic percent or higher, depending on the overall device requirements. As previously explained, the resulting band gap offset obtained by the material 209 may depend on the material composition and the thickness. Hence, for both parameters appropriate target values may be selected in order to obtain the desired threshold voltage. Due to the enhanced surface topography the variability in growth rate during the process 208 may significantly be reduced, thereby obtaining a thickness 209p at the periphery of the active region 203a that may exhibit a significantly reduced degree of deviation from a thickness 209c at the centre. In this respect, the variability in thickness of the material 209 may be approximately 5 percent and less, for instance in some illustrative embodiments a thickness variability of approximately 3 percent and less may be accomplished, while in other cases the variability may be 2 percent and less. It should be appreciated that the thickness variability may be understood in the above-defined sense. Consequently, for

instance for a target thickness of 9 nm of a silicon/germanium alloy having a germanium fraction of 25 atomic percent, the corresponding difference between the peripheral thickness 209p and the central thickness 209c may be less than approximately 0.45 nm, while in other cases an even further enhanced uniformity may be accomplished.

It should be appreciated that other semiconductor alloys may be used if required by corresponding threshold adjusting mechanisms, any such materials may also be provided with enhanced uniformity due to the reduction of a corresponding edge effects during the deposition that may be caused by the difference in growth rate of different crystallographic orientations, as previously explained.

Fig 2f schematically illustrates a top view of the semiconductor device 200 after the deposition of the semiconductor alloy 209 and the removal of the mask layer 205 (cf. Fig 2e). As is evident from Fig 2f, due to the superior thickness uniformity of the semiconductor alloy 209, also an enhanced uniformity may be accomplished along a length direction, indicated as L, and also along a width direction, indicated as W. Consequently, a corresponding threshold variability of transistor elements, which may be formed in and above the active region 203a, may be reduced while also the thickness variability within a single transistor element along the width direction may also be reduced.

Fig 2g schematically illustrates a cross-sectional view of the semiconductor device 200 along the transistor length direction, which in Fig 2g corresponds to the horizontal direction. As illustrated, a plurality of transistors 250a, such as p-channel transistors, may be formed in and above the active regions 203a, while one or more transistors 250b may be formed in and above the active region 203b. The transistors 250a, 250b may have a similar configuration, as previously described with reference to the device 100. That is, the transistors 250a, 250b may comprise a gate electrode structure 251 including a gate insulation layer 251b, a metal-containing electrode material 251a directly formed on the gate insulation layer 251b, followed by a further electrode material 251c, such as a polysilicon material, metal silicide and the like. Moreover, in the transistors 250a, the gate insulation layers 251b may be formed on the threshold adjusting semiconductor alloy 209 so as to obtain a desired threshold voltage or

a channel region 253, which comprises the alloy 209 in the transistors 250a. Due to the superior thickness uniformity of the semiconductor alloy 209, the transistors 250a may exhibit a very similar threshold voltage, thereby contributing to overall uniformity of the device 200 with respect to performance and reliability.

With respect to any manufacturing techniques for forming the transistors 250a, 250b, the appropriate manufacturing regime may be used. The gate electrode structures 251 may be formed by depositing an appropriate gate dielectric, which may comprise conventional dielectrics in combination with high-k materials, followed by the deposition of the metal-containing electrode material 251a, for instance in the form of aluminum oxide, titanium nitride and the like. Thereafter, any further appropriate material, such as polysilicon, may be deposited and subsequently the layer structure may be patterned on the basis of sophisticated lithography techniques. Thereafter, the dopant profiles for drain and source regions 254 may be obtained on the basis of sophisticated implantation techniques, for instance using a sidewall spacer structure 252. Thereafter, the device 200 may be annealed in order to activate dopant and recrystallize implantation induced damage.

Fig 2h schematically illustrates a semiconductor device 200 according to a cross-sectional view along a transistor width direction, which corresponds to the horizontal direction of Fig 2h. For example, the cross-section may be made through one of the transistors 250a when a plurality of transistors are formed in and above the active region 203a. In other cases a single transistor may be formed in and above the active region 203a and the cross-section may be made through the gate electrode structure along the width direction. Thus, the transistor 250a may comprise the threshold adjusting semiconductor alloy 209 on which is to be formed the gate insulation layer 250b, followed by the metal-containing electrode material 251a and the further gate material 251c. Due to the significantly reduced difference in thickness of the semiconductor alloy 209, ie. the thickness values 209p, 209c, may have reduced variability within the above-specified range, the overall threshold voltage of the transistor 250a may be defined with enhanced accuracy and predictability, while at the same time the

dependency of threshold variability from transistor width or transistor devices of different width may significantly be reduced.

As a result, the present disclosure provides semiconductor devices and techniques in which enhanced uniformity of the growth rate of a selective epitaxial growth process may be accomplished so that a threshold adjusting semiconductor alloy may be provided with a significantly reduced thickness variability and reduced variability with respect to material composition at an early manufacturing stage. Thus, sophisticated gate electrode structures comprising a high-k gate dielectric in combination with a metal-containing electrode material may be formed prior to forming drain and source regions, thereby providing for a high degree of compatibility with well-established CMOS techniques.

Further modifications and variations of the present disclosure will be apparent to those skilled in the art in view of this description. Accordingly, this description is to be construed as illustrative only and is for the purpose of teaching those skilled in the art the general manner of carrying out the teaching provided herein. It is to be understood that the forms of the subject matter shown and described herein are to be taken as the presently preferred embodiments.

**CLAIMS****1. A method comprising:**

forming a mask layer on above a first silicon containing crystalline semiconductor region and a second silicon containing crystalline semiconductor region, said first and second silicon containing crystalline semiconductor regions being laterally separated by an isolation region;

removing said mask layer selectively from above said first silicon containing crystalline semiconductor region while maintaining said mask layer on above said second silicon containing crystalline semiconductor region;

recessing reducing a thickness of said first silicon containing crystalline semiconductor region;

forming a threshold adjusting semiconductor alloy selectively on said recessed reduced thickness first silicon containing crystalline semiconductor region;

forming a first gate electrode structure of a first transistor above said threshold adjusting semiconductor alloy; and

forming a second gate electrode structure of a second transistor above said second silicon containing crystalline semiconductor region.

**2. The method of claim 1, wherein forming said first and second gate electrode structures comprises forming a high-k dielectric gate insulation layer and forming a metal containing electrode material on said high-k gate insulation layer.**

**3. The method of claim 1, wherein forming said mask layer comprises forming a silicon nitride layer.**

4. The method of claim 1, wherein removing said mask layer selectively from said first silicon containing crystalline semiconductor region comprises performing a plasma assisted etch process.
5. The method of claim 4, wherein said thickness of said first silicon containing crystalline semiconductor region is recessed reduced during said plasma assisted etch process.
6. The method of claim 3, further comprising performing a wet chemical etch process after removing said mask layer selectively from said first silicon containing crystalline semiconductor region.
7. The method of claim 6, further comprising removing a resist mask used to selectively removing said mask layer.
8. The method of claim 6, wherein said thickness of said first silicon containing crystalline semiconductor region is recessed reduced on the basis of said wet chemical etch process.
9. The method of claim 8, wherein performing said wet chemical etch process comprises using tetra methyl ammonium hydroxide (TMAH).
10. The method of claim 1, wherein forming said threshold adjusting semiconductor alloy comprises performing a selective epitaxial growth process so as to suppress material deposition on said isolation structure and on said mask layer formed above said second silicon containing crystalline semiconductor region.
11. The method of claim 10, wherein said threshold adjusting semiconductor alloy comprises a silicon/germanium alloy.
12. A method comprising: [Great Claim]

exposing a surface of an active semiconductor region that is laterally enclosed by an isolation structure, any exposed surface areas of said exposed surface having substantially the same crystalline orientation;

forming a threshold adjusting semiconductor material on said exposed surface by performing a selective epitaxial growth process; and

forming a gate electrode structure of a transistor on said threshold adjusting semiconductor material, said gate electrode structure comprising a high-k dielectric material and a metal containing electrode material formed on said high-k dielectric material.

13. The method of claim 12, wherein exposing said surface comprises removing material of said active semiconductor region that extends above a surface of said isolation structure.
14. The method of claim 13, wherein removing material of said active semiconductor region comprises performing a plasma assisted etch process.
15. The method of claim 14, further comprising forming a mask layer above said active semiconductor region and selectively removing said mask layer from said active region on the basis of said plasma assisted etch process, while maintaining said mask layer above a further active region.
16. The method of claim 15, wherein said mask layer comprises silicon nitride.
17. The method of claim 15, wherein said mask layer is formed with a thickness of approximately 10 nanometer (nm) or less.
18. The method of claim 14, further comprises performing a wet chemical etch process after exposing said surface.
19. The method of claim 18, wherein said wet chemical etch process is performed on the basis of hydrofluoric acid (HF).

20. The method of claim 12, wherein said threshold adjusting semiconductor material comprises a silicon/germanium alloy.
21. A semiconductor device comprising:
- an active silicon containing semiconductor region;
- an isolation structure laterally enclosing said active silicon containing semiconductor region, said isolation structure having a first edge and a second edge, said first and second edges defining a width of said active silicon containing semiconductor region;
- a threshold adjusting semiconductor alloy formed on said active silicon containing semiconductor region, said threshold adjusting semiconductor region extending from said first edge to said second edge and having a thickness with a variation of approximately 5 percent or less; and
- a gate electrode structure comprising a high-k gate insulation layer and a metal containing electrode material formed on said high-k gate insulation layer.
22. The semiconductor device of claim 21, wherein an average thickness of said threshold adjusting semiconductor alloy is approximately 10 nanometer or less.
23. The semiconductor device of claim 22, wherein said threshold adjusting semiconductor alloy comprises a silicon/germanium alloy with a germanium concentration of approximately 20 atomic percent or more.

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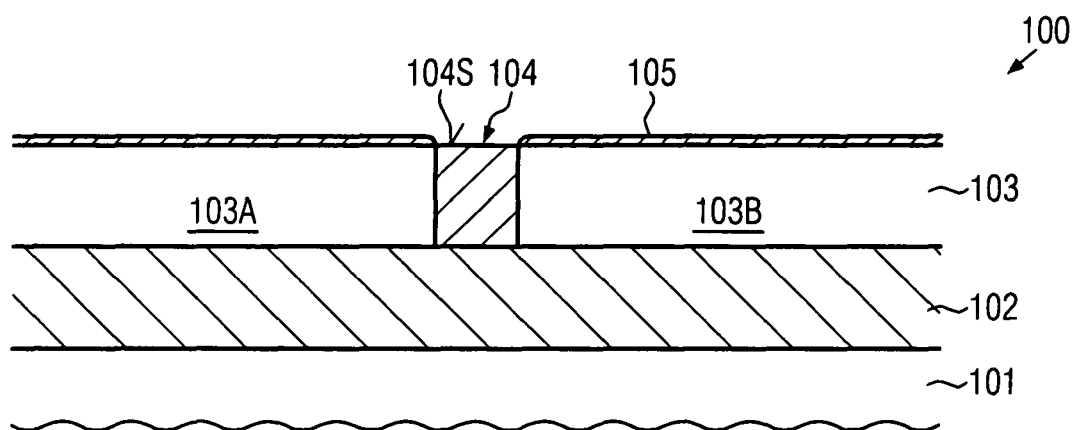


FIG. 1a  
(prior art)

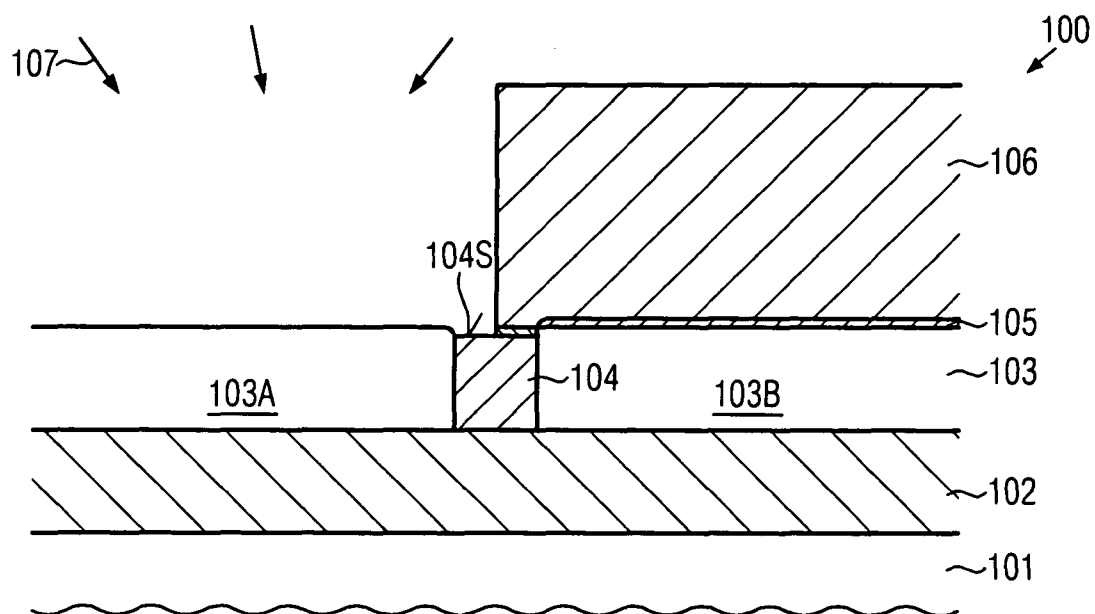


FIG. 1b  
(prior art)

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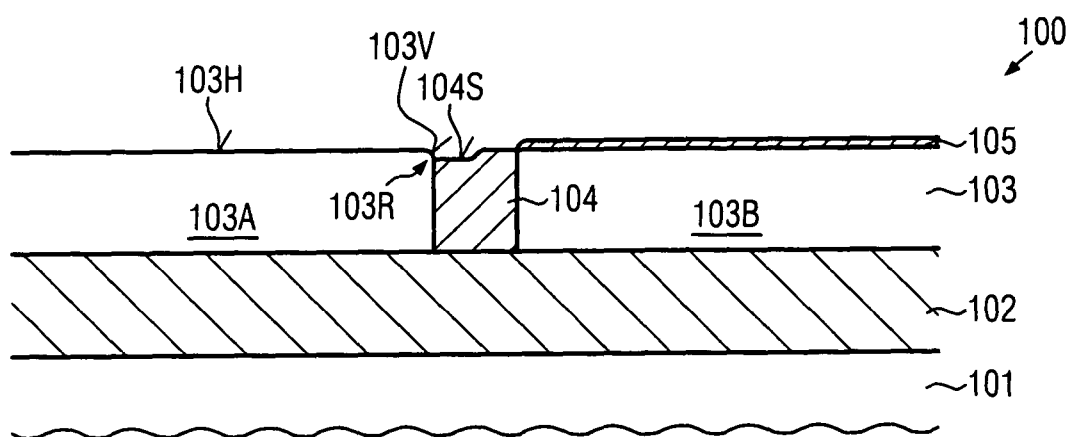


FIG. 1c  
(prior art)

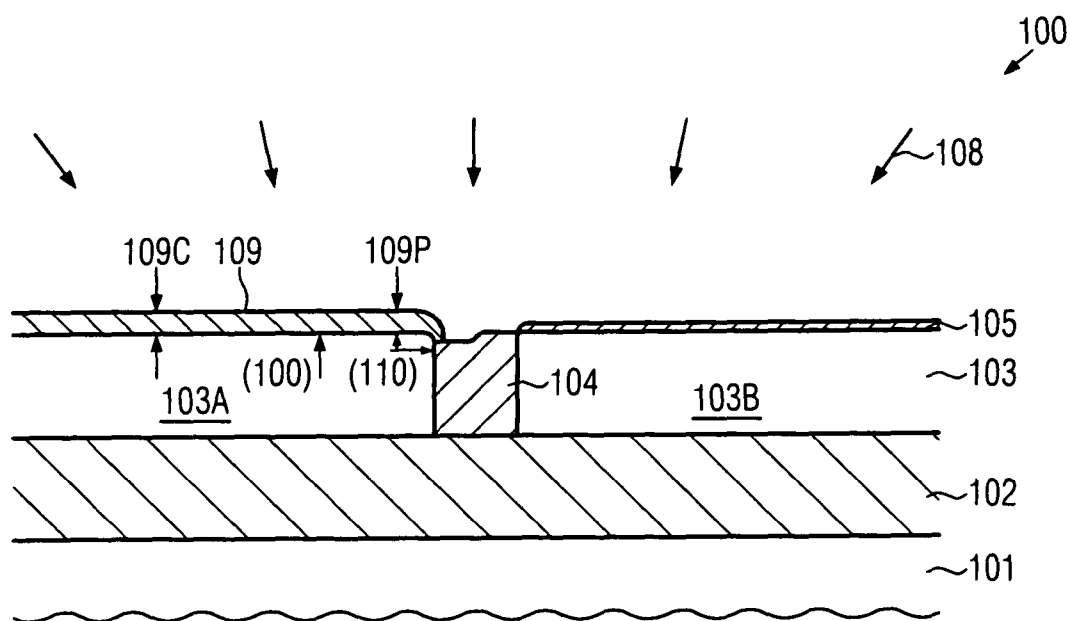


FIG. 1d  
(prior art)

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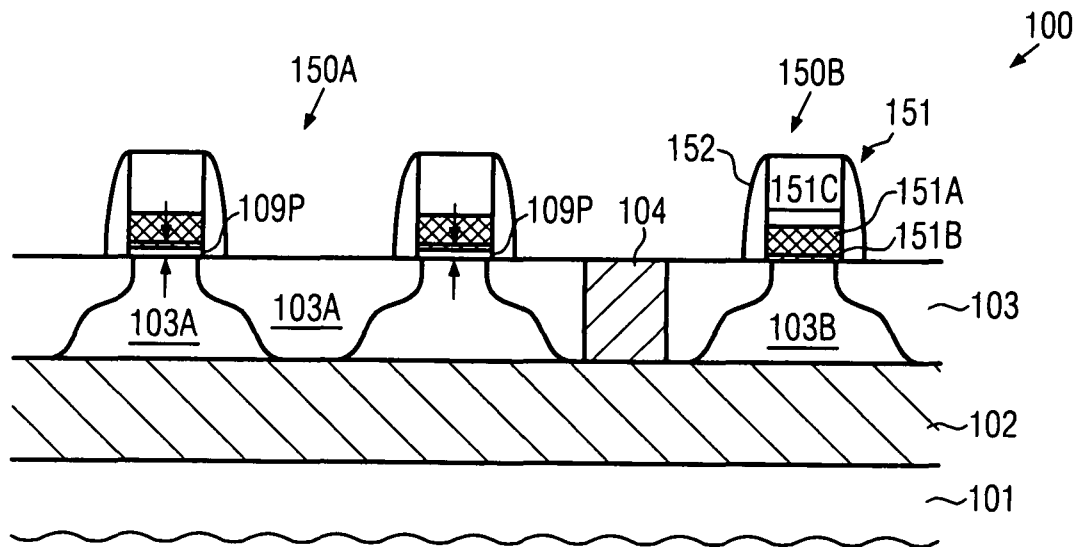


FIG. 1e  
(prior art)

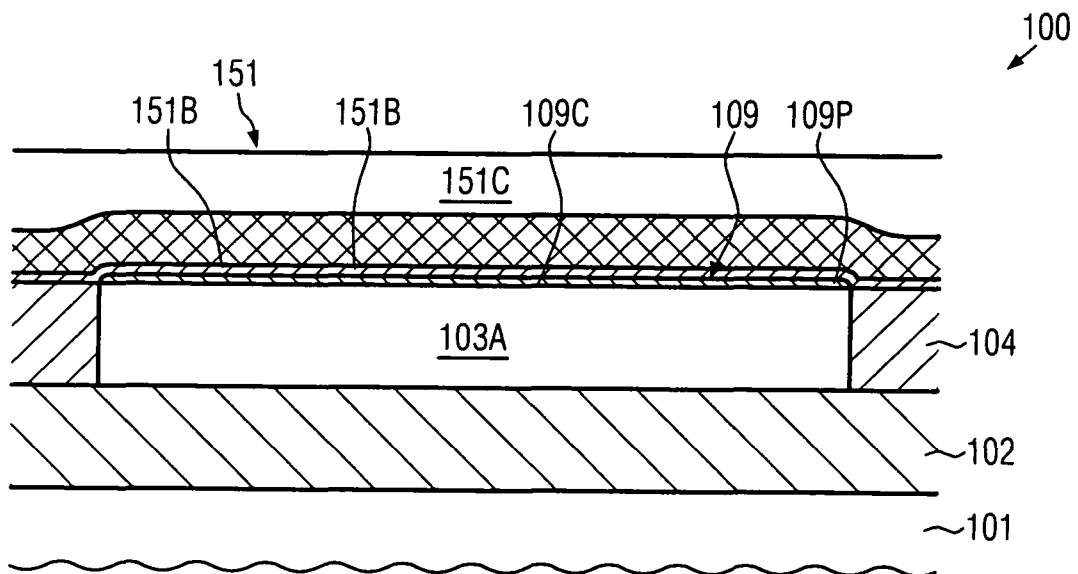


FIG. 1f  
(prior art)

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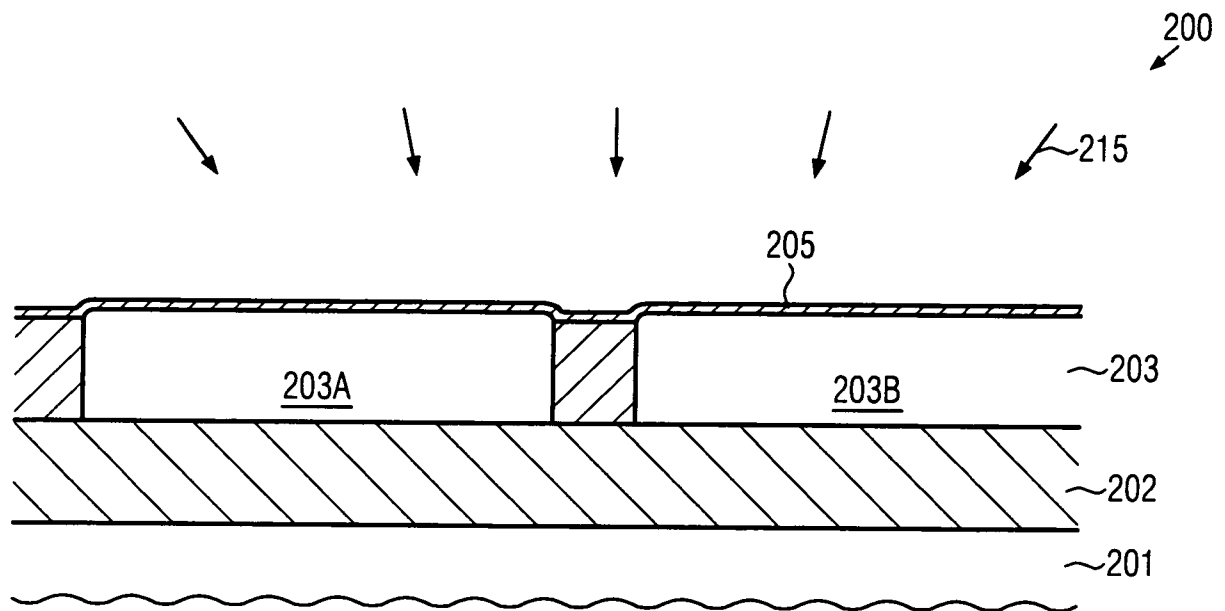


FIG. 2a

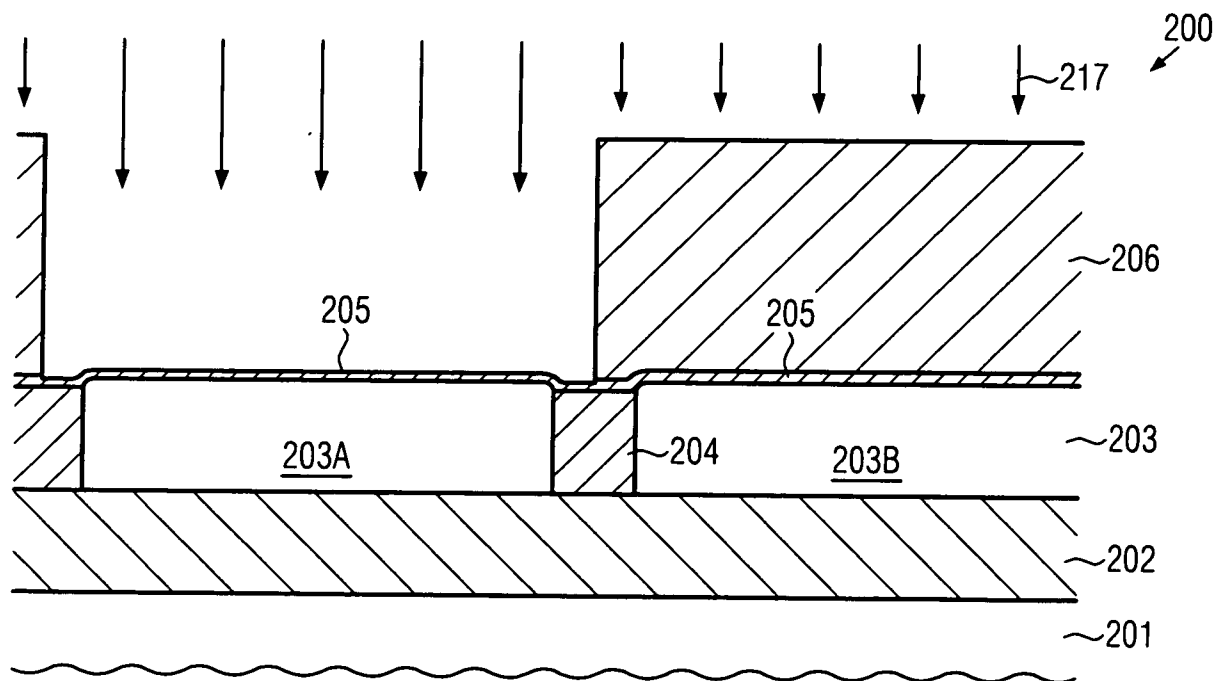


FIG. 2b

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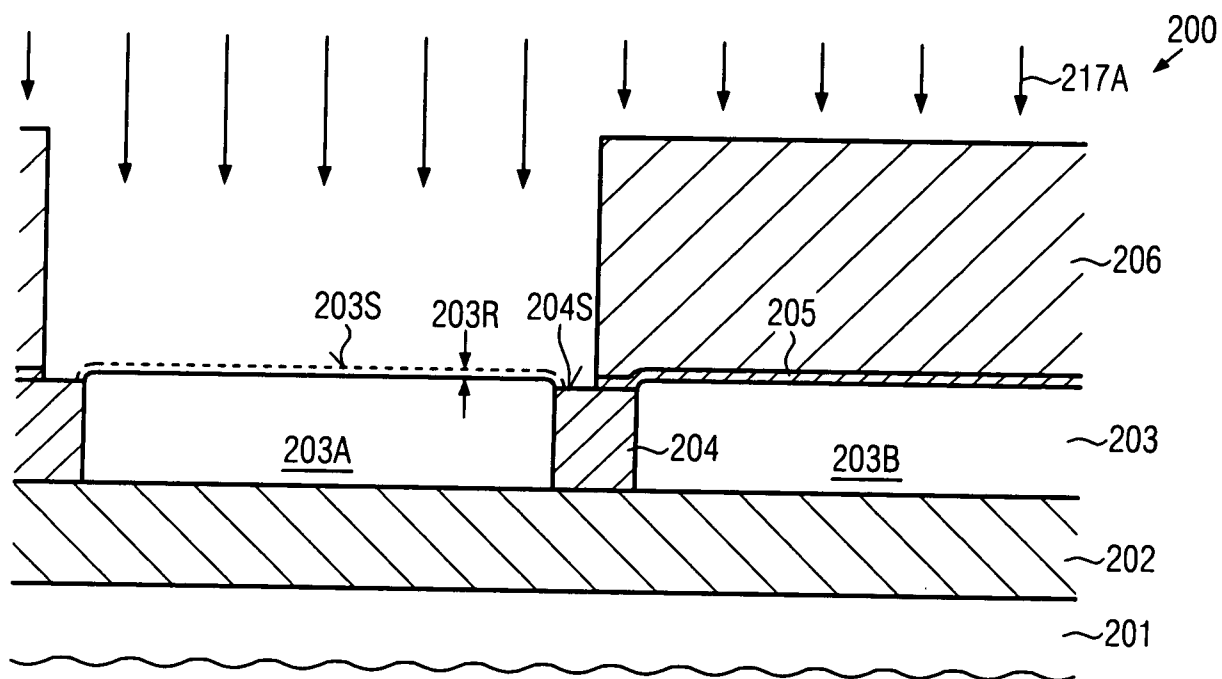


FIG. 2c

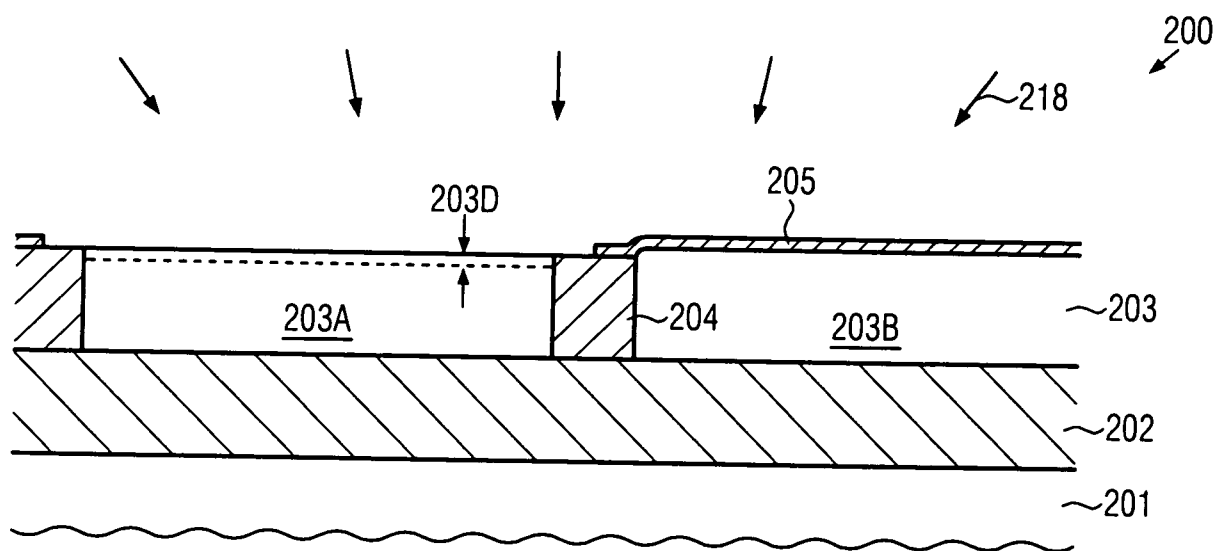


FIG. 2d

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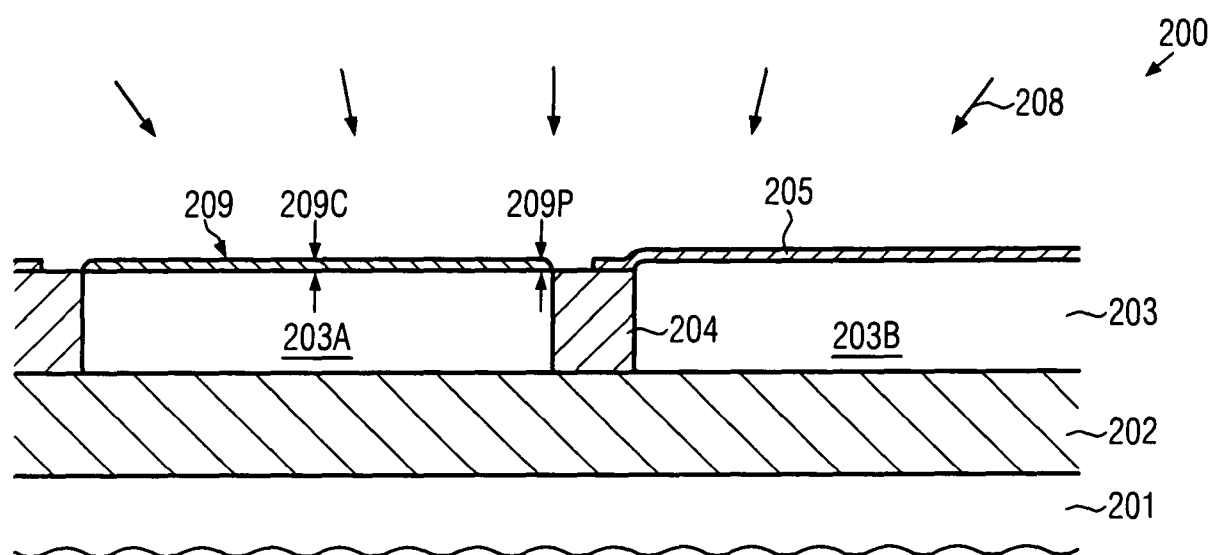


FIG. 2e

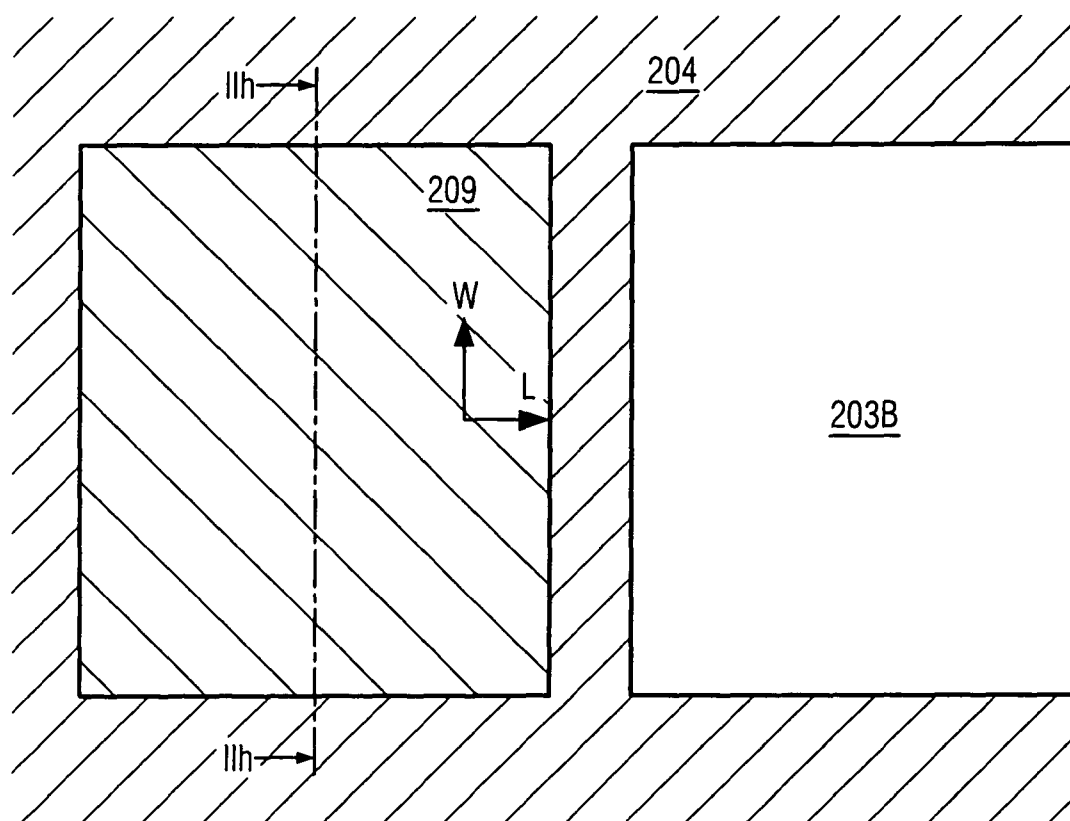


FIG. 2f

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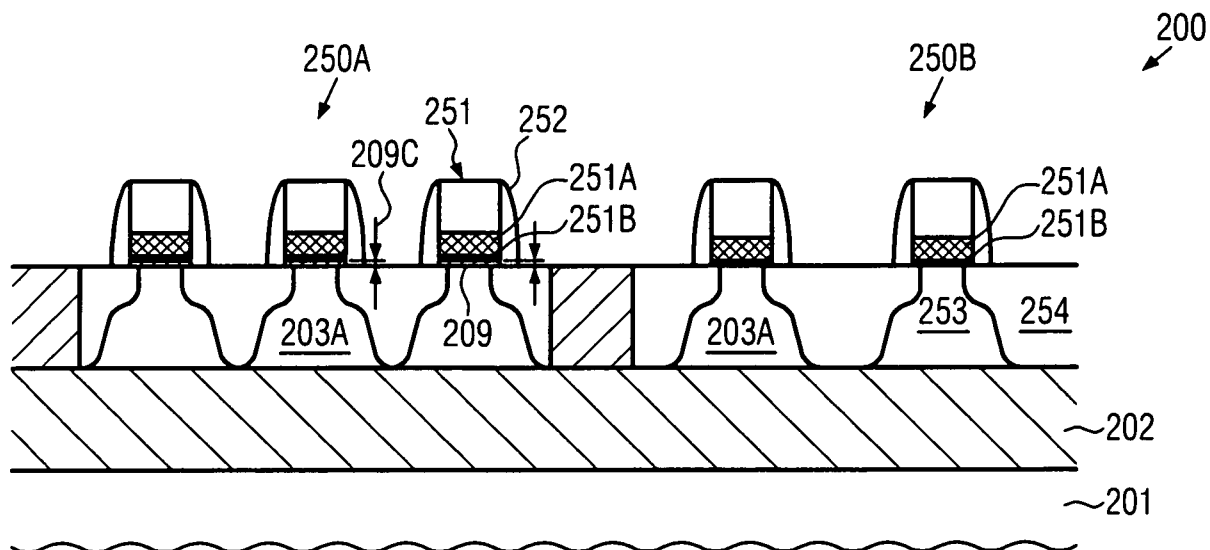


FIG. 2g

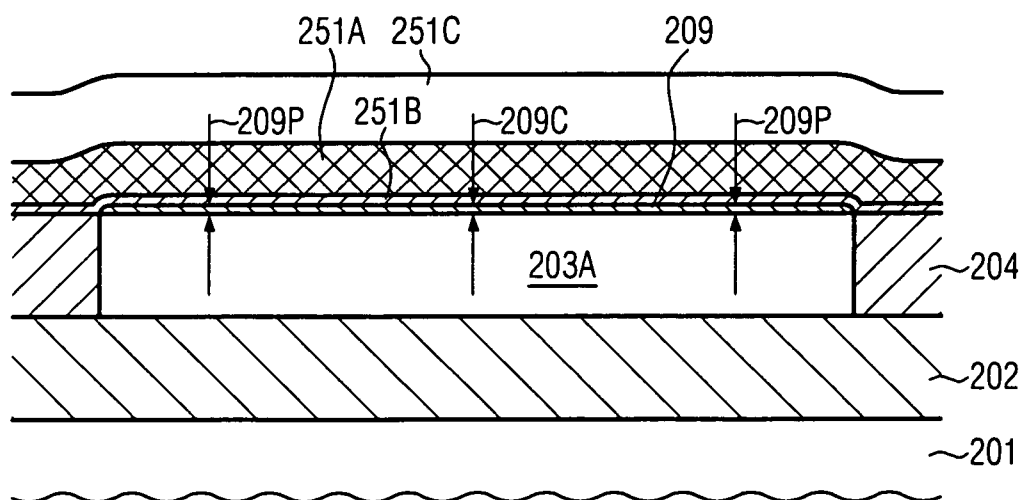


FIG. 2h

# INTERNATIONAL SEARCH REPORT

International application No

PCT/EP2010/000490

## A. CLASSIFICATION OF SUBJECT MATTER

INV. H01L21/8234 H01L21/8238

ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

## B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, INSPEC, IBM-TDB, WPI Data

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category* | Citation of document, with indication, where appropriate, of the relevant passages                                    | Relevant to claim No.   |
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| Y         | abstract; figures 4-10,14A<br>paragraph [0084] - paragraph [0086]                                                     | 3-9,<br>13-19,<br>21-23 |
| Y         | US 2002/001907 A1 (WEON DAE HEE [KR] ET AL) 3 January 2002 (2002-01-03)                                               | 3-9,<br>21-23           |
|           | abstract; claims; figures                                                                                             |                         |
| Y         | WO 2006/083821 A1 (ASM INC [US]; BAUER MATTHIAS [US]; ARENA CHANTAL [US]; BERTRAM RONALD) 10 August 2006 (2006-08-10) | 3-9,<br>21-23           |
|           | abstract; figures<br>table 1                                                                                          |                         |
|           | -----<br>-/--                                                                                                         |                         |

☒ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

\* Special categories of cited documents :

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"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search

20 April 2010

Date of mailing of the international search report

27/04/2010

Name and mailing address of the ISA/

European Patent Office, P.B. 5818 Patentlaan 2  
NL - 2280 HV Rijswijk  
Tel. (+31-70) 340-2040,  
Fax: (+31-70) 340-3016

Authorized officer

Wirner, Christoph

# INTERNATIONAL SEARCH REPORT

International application No

PCT/EP2010/000490

**C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT**

| Category* | Citation of document, with indication, where appropriate, of the relevant passages                                | Relevant to claim No. |
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Information on patent family members

International application No

PCT/EP2010/000490

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