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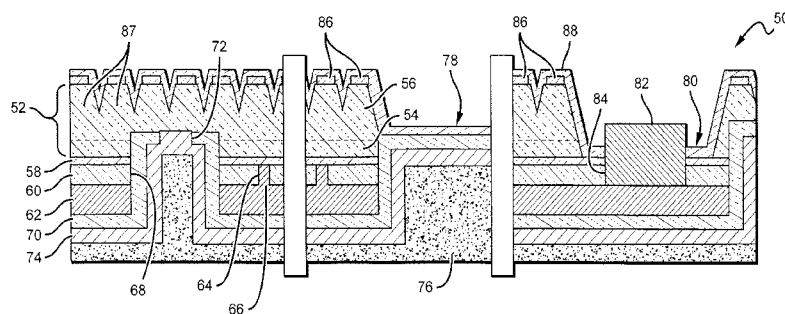


FIG. 4

(57) **Abstract:** The application discloses a LED chip that can result in simpler manufacturing processes using fewer steps. The LED structure can have fewer layers than conventional LED chips with the layers arranged in three different ways for efficient fabrication and operation. The LED chips (50) comprise an active LED structure (52). One option is to have a dielectric reflective layer (60) is included adjacent to one of the oppositely doped layers and a metal reflective layer (62) is on the dielectric reflective layer (60), wherein the dielectric (60) and/or metal (62) reflective layers extend beyond the edge of said active region (52). By extending the dielectric layer, the LED chips can emit with more efficiency by reflecting more LED light to emit in the desired direction. By extending the metal reflective layer beyond the edge of the active region, the metal reflective layer can serve as a current spreading layer and barrier, in addition to reflecting LED light to emit in the desired direction. The other options to simplify the manufacturing is that the LED chips comprise self-aligned and/or self-limiting features that simplify etching processes during fabrication.



HIGH EFFICIENCY LEDS AND METHODS OF MANUFACTURING

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] This invention relates to light emitting diodes, and more particularly to light emitting diodes having high reflectivity mirrors.

Description of the Related Art

[0002] Light emitting diodes (LED or LEDs) are solid state devices that convert electric energy to light, and generally comprise one or more active layers of semiconductor material sandwiched between oppositely doped n-type and p-type layers. When a bias is applied across the doped layers, holes and electrons are injected into the active layer where they recombine to generate light. Light is emitted from the active layer and from all surfaces of the LED.

[0003] For typical LEDs it is desirable to operate at the highest light emission efficiency, and one way that emission efficiency can be measured is by the emission intensity in relation to the input power, or lumens per watt. One way to maximize emission efficiency is by maximizing extraction of light emitted by the active region or active structure of LEDs. For conventional LEDs with a single out-coupling surface, the external quantum

efficiency can be limited by a number of factors, such as total internal reflection (TIR) of light from the LED's emission region. TIR can be caused by the large difference in the refractive index between the LED's semiconductor and surrounding ambient. Some LEDs have relatively low light extraction efficiencies because of the high index of refraction of the substrate compared to the index of refraction for the surrounding material, such as epoxy. This difference results in a small escape cone from which light rays from the active area can transmit from the substrate into the epoxy and ultimately escape from the LED package. Light that does not escape can be absorbed in the semiconductor material or at surfaces that reflect the light.

[0004] Different approaches have been developed to reduce TIR and improve overall light extraction, with one of the more popular being surface texturing. Surface texturing increases the light escape probability by providing a varying surface that allows photons multiple opportunities to find an escape cone. Light that does not find an escape cone can continue to experience TIR, and reflects off the textured surface at different angles until it finds an escape cone. The benefits of surface texturing have been discussed in several articles. [See Windisch et al., Impact of Texture-Enhanced Transmission on High-Efficiency Surface Textured Light Emitting Diodes, Appl. Phys. Lett., Vol. 79, No. 15, Oct. 2001, Pgs. 2316-2317; Schnitzer et al. 30% External Quantum Efficiency From Surface Textured, Thin Film Light Emitting Diodes, Appl. Phys. Lett., Vol 64, No. 16, Oct. 1993, Pgs. 2174-2176; Windisch et al. Light Extraction Mechanisms in High-Efficiency Surface Textured Light Emitting Diodes, IEEE Journal on Selected Topics in

Quantum Electronics, Vol. 8, No. 2, March/April 2002, Pgs. 248-255; Streubel et al. High Brightness AlGaInP Light Emitting Diodes, IEEE Journal on Selected Topics in Quantum Electronics, Vol. 8, No. March/April 2002]. U.S. Patent No. 6,657,236, also assigned to Cree Inc., discloses structures formed on the semiconductor layers for enhancing light extraction in LEDs.

[0005] Another way to increase light extraction efficiency is to provide reflective surfaces that reflect light so that it contributes to useful emission from the LED chip or LED package. In a typical LED package 10 illustrated in FIG. 1, a single LED chip 12 is mounted on a reflective cup 13 by means of a solder bond or conductive epoxy. One or more wire bonds 11 can connect the ohmic contacts of the LED chip 12 to leads 15A and/or 15B, which may be attached to or integral with the reflective cup 13. The reflective cup may be filled with an encapsulant material 16 which may contain a wavelength conversion material such as a phosphor. At least some of the light emitted by the LED at a first wavelength may be absorbed by the phosphor, which may responsively emit light at a second wavelength. The entire assembly is then encapsulated in a clear protective resin 14, which may be molded in the shape of a lens to collimate the light emitted from the LED chip 12. While the reflective cup 13 may direct light in an upward direction, optical losses may occur when the light is reflected. Some light may be absorbed by the reflector cup due to the less than 100% reflectivity of practical reflector surfaces. Some metals can have less than 95% reflectivity in the wavelength range of interest.

[0006] FIG. 2 shows another LED package in which one or more LED chips 22 can be mounted onto a carrier such as a

printed circuit board (PCB) carrier, substrate or submount 23. A metal reflector 24 mounted on the submount 23 surrounds the LED chip(s) 22 and reflects light emitted by the LED chips 22 away from the package 20. The reflector 24 also provides mechanical protection to the LED chips 22. One or more wirebond connections 11 are made between ohmic contacts on the LED chips 22 and electrical traces 25A, 25B on the submount 23. The mounted LED chips 22 are then covered with an encapsulant 26, which may provide environmental and mechanical protection to the chips while also acting as a lens. The metal reflector 24 is typically attached to the carrier by means of a solder or epoxy bond. The metal reflector 24 may also experience optical losses when the light is reflected because it also has less than 100% reflectivity.

[0007] The reflectors shown in FIGs. 1 and 2 are arranged to reflect light that escapes from the LED. LEDs have also been developed having internal reflective surfaces or layers to reflect light internal to the LEDs. FIG. 3 shows a schematic of an LED chip 30 with an LED 32 mounted on a submount 34 by a metal bond layer 36. The LED further comprises a p-contact/reflector 38 between the LED 32 and the metal bond 36, with the reflector 38 typically comprising a metal such as silver (Ag). This arrangement is utilized in commercially available LEDs such as those from Cree® Inc., available under the EZBright™ family of LEDs. The reflector 38 is integral to the LED chip 30 and can reflect light emitted from the LED chip's active region toward the submount back toward the LED's primary emitting surface. The reflector also reflects TIR light back toward the LED's primary emitting surface. Like the metal reflectors above, reflector 38

reflects less than 100% of light and in some cases less than 95%. The reflectivity of a metal film on a semiconductor layer may be calculated from the materials' optical constants using thin film design software such as TFCalc™ from Software Spectra, Inc. (www.sspectra.com).

[0008] Additional LED chips have been developed with internal reflectors, with some of these LED chips also comprising other structures to allow for contacting the active epitaxial structure. Some of these features allow for applying a signal to the active structure of the LED chip through other layers. These structures can include different combinations of conductive features (e.g. layers, contacts and/or vias) and insulating features (e.g. dielectric and/or passivation layers). These features can be included in both vertical and lateral geometry LED chips. The structures can be relatively complex and can involve complex manufacturing processes with some of these structures requiring nine or more major fabrication steps to form the desired build.

SUMMARY OF THE INVENTION

[0009] The present invention relates to simplified chip architectures or chip builds that can result in simpler manufacturing processes using fewer steps. The LED structure can have fewer layers than conventional LED chips with the layers arranged in different ways for efficient fabrication and operation.

[0010] One embodiment of an LED chip according to the present invention comprises an active LED structure comprising an active region between two oppositely doped layers, with the active region emitting light in response to an electrical signal applied to the oppositely doped layer. A first reflective layer is included adjacent to

one of the oppositely doped layers. A second reflective layer is included on the first reflective layer, with the second reflective layer reflecting light not reflected by the first reflective layer and the second reflective layer extending beyond the edge of the active LED structure.

[0011] Another embodiment of an LED chip according to the present invention comprises an active LED structure having an active region between two oppositely doped layers, with the active region emitting light in response to an electrical signal applied to the oppositely doped layer. A dielectric reflective layer is included on one of said oppositely doped layers and extending beyond the edge of the active region. A metal reflective layer is also included on the first dielectric reflective layer.

[0012] One embodiment of a method for forming LED chips comprises depositing active structure epitaxial layers on a wafer. The method also comprises etching different portions of the active structure in a single etch step, wherein the different portions etch at different rates and wherein at least one of the portions is self-limiting to the etch.

[0013] Another embodiment of a method for forming LED chips comprising forming an active structure of epitaxial layers and forming a plurality of reflective layers on said active structure. The method further comprises performing a single etch step to form a self-aligned via hole through the reflective layers to the active structure.

[0014] Still another embodiment of an LED chip according to the present invention comprises an active LED structure comprising an active region between two

oppositely doped layers. A dielectric reflective layer is included adjacent to one of the oppositely doped layers. A metal reflective layer is on the dielectric reflective layer, wherein the dielectric and metal reflective layers extend beyond the edge of said active region.

[0015] These and other aspects and advantages of the invention will become apparent from the following detailed description and the accompanying drawings, which illustrate by way of example the features of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[0016] FIG. 1 is a sectional view of one embodiment of a prior art LED lamp;

[0017] FIG. 2 is a sectional view of another embodiment of a prior art LED lamp;

[0018] FIG. 3 is a sectional view of another embodiment of a prior art LED chip;

[0019] FIG. 4 is a sectional view of one embodiment of an LED chip according to the present;

[0020] FIG. 5 is a top view of one embodiment of an LED chip according to the present invention;

[0021] FIG. 6 is a flow-diagram showing steps in an LED chip fabrication process according to the present invention;

[0022] FIG. 7 is a sectional view of another embodiment of an LED chip according to the present invention;

[0023] FIG. 8 is a flow-diagram showing steps in another LED chip fabrication process according to the present invention;

[0024] FIG. 9 is a sectional view of another embodiment of an LED chip according to the present invention;

[0025] FIG. 10 is a sectional view of layers in an LED chip according to the present invention;

[0026] FIG. 11 is a sectional view of other layers in an LED chip according to the present invention;

[0027] FIG. 12 is a sectional view of another LED chip according to the present invention; and

[0028] FIG. 13 is a sectional view of still another embodiment of an LED chip according to the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0029] The present invention is directed to simplified LED chip structures/builds that can be fabricated using methods with fewer steps, while still providing LED chips with efficient light emission. The present invention is directed to LED chips having internal or integral reflective surfaces/layers arranged to increase the emission efficiency of the emitters. The present invention can be used as a reflector in conjunction with one or more contacts, or can be used as a reflector separate from the contacts.

[0030] The LED chips according to the present invention can comprise an active LED structure. A dielectric reflective layer is included adjacent to one of the oppositely doped layers. A metal reflective layer is on

the dielectric reflective layer, wherein the dielectric and metal reflective layers extend beyond the edge of said active region. By extending the dielectric layer, the LED chips can emit with more efficiency by reflecting more LED light to emit in the desired direction. By extending the metal reflective layer beyond the edge of the active region, the metal reflective layer can serve as a current spreading layer and barrier, in addition to reflecting LED light to emit in the desired direction. The LED chips can also comprise self-aligned and self-limiting features that simplify etching processes during fabrication.

[0031] The dielectric reflective layer can comprise a material with a different index of refraction (IR) than the active LED structure. In most embodiments, the dielectric reflective layer can comprise a layer with an IR that is primarily lower at or near its interface with the active LED structure. Some embodiments of LED chips according to the present invention can also comprise a second reflective layer, metal layer or mirror stack ("mirror stack") that can be on and used in conjunction with the dielectric reflective layer such that light passing through the dielectric reflective layer (e.g. not experiencing TIR) can be reflected by the second reflective layer.

[0032] These internal or integral reflective layers can reduce optical emission losses that can occur by light being emitted in an undesirable direction where it can be absorbed. Light that is emitted from the emitter's active LED structure in a direction away from useful light emission, such as toward the substrate, submount, or metal reflector can be reflected by the first reflective layer. The reflective surfaces can be

positioned to reflect this light so that it emits from the LED chip in a desirable direction.

[0033] The dielectric reflective layer can comprise many different materials, with some embodiments comprising a dielectric material such as SiO₂. It is understood that many other materials can be used with refractive indexes that are lower or higher, with the preferred having an IR that up to approximately 50% smaller than the LED's active structure material. In other embodiments the IR of the dielectric reflective layer can be up to approximately 40% smaller than the active structure material, while in other embodiments it can be up to approximately 30% smaller.

[0034] Many conventional LEDs can rely primarily on a metal reflector layer made of different material such as Ag or Au. As described above, there can be losses with each reflection off metal reflectors, and these losses can be significant particularly for light making multiple passes and reflections in the LED. There are no optical losses in light reflected by TIR, so that when more light is reflected using TIR instead of a metal material, the emission efficiency of the LED can increase.

[0035] Different embodiments of emitters according to the present invention can also utilize other structures, layers or features that allow for efficient and reliable LED operation. In some embodiments, a current spreading layer can be included in proximity to the reflective layer to provide for spreading of current into the one or more layers of the active LED structure. In other embodiments, materials can be included to provide for reliable adhesion between different layers, such as between the low IR layer and the metal reflective layer.

Different embodiments of the invention also provide conductive via or path arrangements that provide conductive paths through insulating layers such as the reflective/dielectric layer. Some of these features allow for an electric signal to pass through the dielectric reflective layer along the vias so that the dielectric material layer can be used as an internal layer.

[0036] Conventional LED chips can have relatively complex structures that allow for these internal reflector arrangements while at the same time allowing for contacting the active structure with different contact and via arrangements. These complex structures can also lead to relatively complex manufacturing processes. The LEDs according to the present invention comprise simplified LED structures that allow for simplified manufacturing processes. As described in more detail below, some embodiments can comprise a dielectric reflective layer and single layer that can serve as a mirror/barrier/current spreading layer. The LED structure can also comprise a thin contact layer to the p-side of the active structure (e.g. GaN). The thin contact layer can comprise many materials such as ITO and can have a thickness of less than 1000Å.

[0037] In some embodiments, the LED structure can be further simplified by having a plurality of front side layers self-aligned to the active area mesa edges. (all etched in one etch step). This results in fewer etching steps for formation of features such as vias. The manufacturing of the LED structure can be further simplified by the backside mesas (or streets) and light extraction features being formed in one etch step as described below. This is particularly useful for structures that require differing etch times for the

mesas and the light extraction features. In some embodiments, one that requires less etch time can be self-limiting to allow for additional etch time for the other features.

[0038] In some embodiments the dielectric layer mentioned above can comprise many different materials, with some embodiments comprising SiO₂. LED structures with hybrid dielectric mirror consisting of a SiO₂ layer with a single mirror/barrier/current spreading layer and thin ITO p-contact (<1000Å) can be self-aligned to the active area mesas. The SiO₂ layer can serve as both a reflective element and junction passivation layer.

[0039] In some embodiments, the external p-contact can then be formed on the mirror stack by etching through layers down to the mirror stack. In these embodiments, having the mirror layer extend out past the mesa for p-contacting instead of the light absorbing barrier layer used in the conventional structures can reduce light absorption.

[0040] The present invention is described herein with reference to certain embodiments but it is understood that the invention can be embodied in many different forms and should not be construed as limited to the embodiments set forth herein. In particular, dielectric reflective layer can comprise many different material layers and can have many different thicknesses beyond those described herein. The dielectric layer is described herein as a layer of one material, such as a particular dielectric, but it is understood that it can comprise many different materials, and in some embodiments it can comprise more than one layer. The dielectric layer can also be in many different locations on different LED

chips beyond those described herein, and can be used on different devices beyond solid state emitters. Furthermore, the first reflective layer can be provided with or without conductive structures to allow electrical signals to pass through. It is understood that LED chips according to the present invention can also utilize single layer dielectric layers in conjunction with other reflectors such as metal reflective layers or DBR layers. The first reflective layer is arranged to maximize the amount of light reflected by TIR, while at the same time maintaining a simple, efficient and cost effective reflecting system.

[0041] It is also understood that when an element such as a layer, region or substrate is referred to as being "on", "adjacent" or "in proximity" to another element, it can be directly on the other element or intervening elements may also be present. Furthermore, relative terms such as "inner", "outer", "upper", "above", "lower", "beneath", and "below", and similar terms, may be used herein to describe a relationship of one layer or another region. It is understood that these terms are intended to encompass different orientations of the device in addition to the orientation depicted in the figures.

[0042] Although the terms first, second, etc. may be used herein to describe various elements, components, regions, layers and/or sections, these elements, components, regions, layers and/or sections should not be limited by these terms. These terms are only used to distinguish one element, component, region, layer or section from another region, layer or section. Thus, a first element, component, region, layer or section discussed below could be termed a second element, component, region, layer or

section without departing from the teachings of the present invention.

[0043] Embodiments of the invention are described herein with reference to cross-sectional view illustrations that are schematic illustrations of embodiments of the invention. As such, the actual thickness of the layers can be different, and variations from the shapes of the illustrations as a result, for example, of manufacturing techniques and/or tolerances are expected. Embodiments of the invention should not be construed as limited to the particular shapes of the regions illustrated herein but are to include deviations in shapes that result, for example, from manufacturing. A region illustrated or described as square or rectangular will typically have rounded or curved features due to normal manufacturing tolerances. Thus, the regions illustrated in the figures are schematic in nature and their shapes are not intended to illustrate the precise shape of a region of a device and are not intended to limit the scope of the invention.

[0044] The present invention is described herein with reference to light emitting diodes (LED or LEDs) or LED chips, but it is understood that it is equally applicable to other solid-state emitters. It is further understood that the present invention can be used in many different LED chips beyond those described herein. The components can have different shapes and sizes beyond those shown and different numbers of LEDs can be included.

[0045] FIG. 4 and 5 show one embodiment of an LED chip 50 according to the present invention that is arranged with a simplified structure that allows for simplified fabrication. Although the present invention is described with reference to fabrication of a single LED chip it is

understood that the present invention can also be applied to wafer level LED fabrication, fabrication of groups of LEDs, or fabrication of packaged LED chips. The wafer or groups of LEDs can then be separated into individual LED chips using known singulation or dicing methods. The present invention can also be used in different LEDs having different geometries, such lateral geometry or vertical geometry. The present invention can also be used in LEDs compatible with flip-chip mounting as well as those that are arranged for non flip-chip mounting. The different embodiments of the present invention are particularly applicable to fabricating devices having many of the same features as the as the LED chips available from Cree, Inc. under their EZ, WZ and/or DA product family designation.

[0046] The LED chip 50 can comprise an LED active region or structure 52 that can have many different semiconductor layers arranged in different ways. The fabrication and operation of LEDs and their active structure are generally known in the art and only briefly discussed herein. The layers of the active structure 52 can be fabricated using known processes with a suitable process being fabrication using MOCVD. The LED chip 50 comprises an active structure 52 having a p-type layer 54, n-type layer 56 and an active region between the two. It is understood that additional layers and elements can also be included in the active structure 52, including but not limited to buffer, nucleation, contact and current spreading layers as well as light extraction layers and elements. The active layer can comprise single quantum well (SQW), multiple quantum well (MQW), double heterostructure or super lattice structures.

[0047] The active structure 52 can be fabricated from different material systems, with preferred material systems being Group-III nitride based material systems. Group-III nitrides refer to those semiconductor compounds formed between nitrogen and the elements in the Group III of the periodic table, usually aluminum (Al), gallium (Ga), and indium (In). The term also refers to ternary and quaternary compounds such as aluminum gallium nitride (AlGaN) and aluminum indium gallium nitride (AlInGaN). In one embodiment, the n- and p-type layers are gallium nitride (GaN) and the active layer comprises InGaN. In alternative embodiments the n- and p-type layers may be AlGaN, aluminum gallium arsenide (AlGaAs) or aluminum gallium indium arsenide phosphide (AlGaInAsP) and related compounds.

[0048] The active structure 52 can be formed on a growth substrate (not shown) and the growth substrate can be made of many materials such as sapphire, silicon carbide, aluminum nitride (AlN), GaN, with a suitable substrate being a 4H polytype of silicon carbide, although other silicon carbide polytypes can also be used including 3C, 6H and 15R polytypes. Silicon carbide has certain advantages, such as a closer crystal lattice match to Group III-nitrides than sapphire and results in Group III-nitride films of higher quality. Silicon carbide also has a very high thermal conductivity so that the total output power of Group-III nitride devices on silicon carbide is not limited by the thermal dissipation of the substrate (as may be the case with some devices formed on sapphire). SiC substrates are available from Cree Research, Inc., of Durham, North Carolina and methods for producing them are set forth in the scientific literature as well as in U.S. Patents, Nos. Re. 34,861; 4,946,547;

and 5,200,022. In the embodiment shown, the growth substrate has been removed, but in other embodiments all or a portion of the substrate can remain, with some of these embodiments having textured portions to enhance light extraction.

[0049] Different embodiments of the active structure can emit different wavelengths of light depending on the composition of the active layer and n- and p-type layers. In some embodiments, the active structure emits a blue light in the wavelength range of approximately 450 to 460nm. The LED chip 50 can also be covered with one or more conversion materials, such as phosphors, such that at least some of the light from the LED passes through the one or more phosphors and is converted to one or more different wavelengths of light. In one embodiment, the LED chip emits a white light combination of light from the LED's active structure and light from the one or more phosphors. In other embodiments, a remote phosphor can be provided that is in the path emitted from the LED chip 50 to convert the light remotely from the LED chip 50.

[0050] "Front side" fabrication discussed herein refers to fabrication of those layers adjacent the p-type layer 54, and in the embodiment shown would be those layers arranged below the active structure 50. In this embodiment front side also refers to the side opposite the LED chips primary emission surface. "Back side" fabrication then generally refers to fabrication on the side opposite the front side fabrication.

[0051] As mentioned above, the LED chip 50 can comprise a simplified/hybrid mirror arrangement that allows for simplified fabrication of the LED chip 50. In some embodiments, the hybrid mirror can comprise current

spreading layer 58 on the p-GaN, a dielectric reflective layer (e.g. SiO₂) 60 and a mirror stack (single mirror/barrier/current spreading layer) 62 on the dielectric layer 60. It is understood, however, that other embodiments can comprise many different simplified/hybrid mirrors arranged in different ways. In some embodiments, these front side layers can be self-aligned to the active area mesa edges. Stated differently, and as more fully described below, these layers (in addition to others) can be etched to one step to the epitaxial material, which can simplify the overall fabrication process.

[0052] The spreading layer 58 can be on the active structure 52 in a location to aid in current spreading into the p-type layer. In the embodiment shown the current spreading layer 58 can cover some or the entire p-type layer and in some embodiments the current spreading layer 58 helps spread current from a p-type contact 64 across the surface of the p-type layer. This helps to provide improved current spreading across the p-type layer with a corresponding improvement in current injection from the p-type layer to the active region.

[0053] The current spreading layer 58 can comprise many different materials and is typically a transparent conductive oxide such as indium tin oxide (ITO) or a metal such as platinum (Pt), although other materials can also be used. The current spreading layer 58 can have many different thicknesses, with the present invention having a thickness small enough to minimize absorption of light from the active structure that passes through the current spreading layer. In some embodiments, the current spreading layer 58 comprising ITO, and can have thicknesses less than 1000 angstroms (Å). In still other

embodiments it can have a thickness less than 700Å, while other embodiments can have a thickness less than 500Å. Still other embodiments can have a thickness in the range of 50 to 300Å, with some of these embodiments having a current spreading layer with a thickness of approximately 200Å. The current spreading layer 58 as well as the reflective layers described below can be deposited using known methods. It is understood that in embodiments where current spreading is not a concern, the LED chips can be provided without a current spreading layer.

[0054] The dielectric reflective layer 60 that in the embodiment shown is formed on the current spreading layer 58 with current spreading layer between the dielectric layer 60 and active structure 52. It is understood, however, that in other embodiments the dielectric reflective layer 60 can be formed directly on the active structure 52, while in other embodiments other layers can be between the active structure 52 and the dielectric layer 60. The dielectric layer 60 can comprise many different materials and preferably comprises a material that presents an index of refraction (IR) step between the material comprising the active structure 52. Stated differently, the dielectric layer 60 can have an IR that is smaller than the active structure to promote total internal reflection (TIR). Light that experiences TIR is reflected without experiencing absorption or loss, and TIR allows for the efficient reflection of active structure light so that it can contribute to useful or desired LED chip emission.

[0055] The dielectric reflective layer 60 can comprise a material having an IR less than 2.3, while other embodiments can have an IR less than 2.15. In still other embodiments the IR can be less than 2.0. Many different

materials can be used and in some embodiments the dielectric layer 60 can comprise SiO_2 . It is understood that other dielectric materials can be used such as SiN , Si , Ge , MgOx , MgNx , ZnO , SiNx , SiOx , AlN , and alloys or combinations thereof. The dielectric layer 60 can also comprise a plurality of different layers. In some embodiments the dielectric layer can comprise a SiO_2 layer with one or more layers of different material. In some embodiments a TiO_2 layer can be used with a SiO_2 layer. In still other embodiments the dielectric layer can comprise multiple layers in the form of a distributed Bragg reflector (DBR).

[0056] Some Group III nitride materials, such as GaN , can have an IR of approximately 2.4, and SiO_2 has an IR of approximately 1.46. Embodiments with an active LED structure 52 comprising GaN and that also comprises a SiO_2 dielectric layer, can have a sufficient IR step between the two to allow for efficient TIR of light at the junction between the two. GaN material of the active structure 52 has an IR of 2.4 and the SiO_2 material of the dielectric reflective layer 60 has an IR of 1.46. This represents a difference in IR between the two of approximately 39%. The dielectric reflective layer 60 can have different thicknesses depending on the type of material, with some embodiments having a thickness of at least 0.2 microns (μm). In some of these embodiments it can have a thickness in the range of 0.2 to $0.7\mu\text{m}$, while in some of these embodiments it can be approximately $0.5\mu\text{m}$ thick.

[0057] As mentioned above, the LED chips 50 according to the present invention can also utilize a second reflective layer, referred to above as mirror stack 62, to reflect light that does not experience TIR at the

junction with the dielectric reflective layer 60 and passes through the dielectric reflective layer 60. The mirror stack 62 can comprise many different materials such as Ag, Au, Al, or combinations thereof, and can comprise multiple layers. In the embodiment shown, the mirror stack 62 can at least partially comprise Ag, with other embodiments comprising a layer that is substantially all Ag. Different embodiments according to the present invention can also comprise an adhesion layer (not shown) between the dielectric reflective layer 60 and the metal stack 62 to promote adhesion between the two. Many different materials can be used for the adhesion layer, such as TiO, TiON, TiO₂, TaO, TaON, Ta₂O₅, AlO or combinations thereof, with a preferred material being TiON. The adhesion layer can have many different thicknesses from just a few Å to thousands of Å. The thickness of the adhesion layer and the material used should minimize the absorption of light passing to minimize losses of light reflecting off the metal layer 62.

[0058] The LED chip 50 further comprises dielectric layer holes (p vias holes) 64 that can pass through the dielectric reflective layer 60, to the current spreading layer 58. The holes 64 can be filled when the mirror stack 62 is deposited and the metal layer material can form dielectric layer vias 66 to the current spreading layer 58. As described in more detail below, the vias 66 provide a conductive path through the reflective layer 60, with the electrical signal originating from the p-contact, passing through the mirror stack 62, through the vias 66, and to the current spreading layer 58.

[0059] The holes 64 can be formed using many known processes such as conventional etching processes or

mechanical processes such as microdrilling. The holes 64 can have many different shapes and sizes, with the holes 64 in the embodiment shown having a circular cross-section with a diameter of less than 20 μ m. In some embodiments, the holes can have a diameter of approximately 8 μ m, with others having a diameter down to 1 μ m. Adjacent holes 64 can be less than 100 μ m apart, with the embodiment shown having a spacing of 30 μ m spacing from edge to edge. In still other embodiments, the vias can have a spacing of as low as 10 μ m or less. It is understood that the holes 64 (and resulting vias 100) can have cross-sections with different shapes such as square, rectangular, oval, hexagon, pentagon, etc. In other embodiments the holes are not uniform size and shapes and there can be different or nonuniform spaces between adjacent holes.

[0060] In other embodiments different structures can be used to provide a conductive path between the p-contact and the current spreading layer. Instead of holes an interconnected grid can be formed through the dielectric reflective layer 60, with a conductive material then being deposited in the grid to form the conductive path through the composite layer. The grid can take many different forms, with portions of the grid interconnecting at different angles in different embodiments. An electrical signal applied to the grid can spread throughout and along the interconnected portions. It is further understood that in different embodiments a grid can be used in combination with holes, while other embodiments can provide other conductive paths. In some embodiments one or more conductive paths can run outside the LED chip's active layer such as along a side surface of the LED chip.

[0061] An n-type via hole 68 can be formed through the mirror stack 62, dielectric reflective layer 60 and the current spreading layer 58, the p-type layer 54 and to the n-type layer 56. In the embodiment shown, formation of the via hole 68 can take place in a single etch step. This is referred to as layers being "self-aligned." A front side passivation layer 70 can then be included on the inside surface of the via hole 66, and can continue to cover the exposed bottom surface of the mirror stack 62. The passivation layer 70 can protect and provide electrical insulation between layers and can comprise many different materials, such as a dielectric material. A contact hole 72 can be formed through the passivation layer 70 to the n-type layer 56.

[0062] A conductive layer can be included that forms n-type layer via 74 which can be on the surface of the via hole 68 and on the passivation layer 70. The via 74 passes through the mirror stack 62, dielectric reflective layer 60, current spreading layer 58, p-type layer 54, and the passivation hole 72 to make contact with the n-type layer 56. In this arrangement, an electrical signal applied to the via 74 is conducted to the n-type layer 56. The via 74 can be made of many different conductive materials, such as a metal. With some via embodiments comprising a layer of metal, such as Al, covering the passivation layer in the hole 66 and continuing on the passivation layer and covering the mirror stack 62. A bond layer 76 can then be included on the via metal layer 74.

[0063] As mentioned above, the back side processing refers to processing of the LED chip 50 on the side opposite the dielectric reflective layer 60 and mirror stack 62. When fabricating LED chips at the wafer level,

the epitaxial layers are continuous. Mesas or streets are then formed through the epitaxial layers to form the active structures for the individual LEDs. Many different formation methods can be used, such as etching.

[0064] In fabrication of the LED chips at the wafer level, a first "street" 78 is formed between adjacent ones of the LED chips. In the embodiment shown, front side passivation layer 70 and conductive layer 74 extend beyond the edge of the LED structure 52 and to cover the first street 78. A bond pad area (i.e. second street) 80 is also formed between the LED chips 50 in a location for the p-contact 82. In some embodiments, the bond pad area 80 can be formed in one or more corners of the LED chip 50. In this embodiment, the current spreading layer 58, the dielectric reflective layer 60, and the mirror stack 62 extend into the bond pad area 80 (not the first street 78). A p-contact hole 84 is formed through the current spreading layer 58 and the dielectric reflective layer 60, to expose the mirror stack 62. The p-contact is included in the p-contact hole 80 and in contact with the mirror stack 62 and current spreading layer 58.

[0065] During operation, an electrical signal applied to the p-contact spreads primarily to the metal layer 62, through the vias 66, and to the current spreading layer 58 where it spreads into the p-type layer 54. An electrical signal applied to the conductive layer 68 conducts to the n-type layer 56.

[0066] One or more layers of the surfaces of the active structure 52 can also be textured using different methods such as known etching or grinding methods. In conventional LED fabrication processes, the street and texturing can take place in separate fabrication steps.

In embodiments according to the present invention, the street and texturing processes can take place in the same step, simplifying the overall fabrication process.

[0067] In one embodiment according to the present invention, the backside processing can comprise forming a first backside passivation layer 86 on the top surface of the n-type layer. Portions of the first back side passivation layer can then be formed an array of features that help define the texturing pattern in the n-type layer 56. In some embodiments, the first passivation layer 86 can be etched to form a pattern such as an array of features (e.g. circles or dots), with the dots serving as a mask for etching to the textured features. The dots can be in a predefined pattern, which can result in textured features 87 (i.e. truncated cones) that are substantially the same size, or can be in a random pattern, which can result in textured features that vary in size.

[0068] In embodiments according to the present invention, the n-type layer 56 can be etched between the features of the patterned passivation layer 82, with some embodiments utilizing a wet chemical etch. This can cause etching along a crystal plane of the semiconductor layer comprising the n-type layer 56. As shown, this etching continues until the bottoms of each of the truncated cone features intersect with adjacent ones of the truncated cones. This will cause the etching to cease removing material from the n-type layer, with this intersecting being "self-limiting" on the depth of the features. This arrangement and method for forming the textured 87 features is fully described in U.S. Patent Application Serial No. 13/868,361, to Donofrio and assigned to Cree, Inc., the contents of which are incorporated herein.

[0069] During the etching of the n-type layer 56 the first street 78 and the bond pad area 80 can also be etched. The textured features of the n-type layer are self-limiting and once the bottoms of the features intersect, the etching of these features stops, even if the etching material remains. This allows for additional etching time for further removal of epitaxial material in streets 78, 80 while not continuing to remove epitaxial material at the textured features. This allows for one etch process step to be used to etch different features that require different etching time. By one feature being self-limiting, additional time can be used for etching one or more other features, such as the streets.

[0070] Following this etching process, a second back side passivation layer 88 can be included over the active structure 52 and over the streets 78, 80 between the active structures. The first and second back side passivation layers 86, 88 can comprise many different materials and in some embodiments can comprise the same material or different materials. The first back side passivation layer 86 serves primarily as a mask for forming the textured features, while the second back side passivation layer 88 serves primarily to protect the layers below it. Like the front side passivation layer 70 described above, the first and second back side passivation layers can comprise many different materials, such as a dielectric materials.

[0071] The opening can then be formed in the second passivation layer 88, along with the current spreading layer 58 and the dielectric reflective layer 60, to form the p-contact hole 84. The p-contact 80 is formed in the hole 84 and directly on the metal layer 62 for applying an electrical signal to the p-type layer 54 as described

above. The formation of the openings is preferably by an etching process that provide a relatively clean surface on the metal layer 62 and the p-contact 82 should be formed with good sidewall coverage by the current spreading layer 58, dielectric reflective layer 60 and second passivation layer 84, to help prevent metal migration between the layers.

[0072] The LED chip 50 presents a simplified structure that can be fabricated using fewer steps than are used in fabrication of conventional LED chips. FIG. 6 is a flow diagram 90 showing some of the steps used in one embodiment of a fabrication process according to the present invention, with different steps focusing primarily on etching processes. In step one 91 the p reflective layer holes (or p vias holes) 64 can be etched through the dielectric layer 60 to the current spreading layer 58. The holes 64 can be filled when the metal layer 62 is deposited and the metal layer material can form vias 66 to the current spreading layer 58.

[0073] Following deposition of the mirror stack 62, in step two 92, the mirror stack 62, dielectric reflective layer 60 and the current spreading layer and part of the p-type GaN epitaxial material 54 can be etched to form a via hole. As mentioned above, the layers that are etched are "self-aligned" and are etched in a single step. In some conventional LED chips, these layers can be etched in different steps that can result in a more complicated fabrication process.

[0074] Following deposition of the passivation layer 70, in step three 93, the passivation layer 70 can be etched to form passivation layer hole 72 that passes to the n-type layer 56. The conductive via layer 74 fills the

passivation layer hole and forms a contact to the n-type layer 56.

[0075] The first backside passivation layer 86 can be deposited and then formed in to the pattern of features that control formation of the epitaxial materials textured features. In step four 94, the first street 78, the bond pad area 80 and textured features 87 can be formed in the same etching step. As described above, the etching of the textured features 87 can be self-limiting, which causes etching of the textured features 87 to stop while the additional texturing of the streets 78, 80 continues. This self-limiting of the textured features allows for etching of the textured features 87 and streets 78, 80 in one etching step.

[0076] The second backside passivation layer 88 can then be deposited. In step five 95 the p-contact hole 84 can be etched through the second backside passivation layer 88, the current spreading layer 58, and the dielectric reflective layer 60, to the mirror stack 62. The p-contact 82 can then be deposited in the hole 84 and in contact with the mirror stack 62. By having the mirror stack extend out past the mesa, instead of a light absorbing barrier as in some conventional LED chips, light absorption can be reduced.

[0077] LED chips according to the present invention can be arranged in many different ways and can comprise many different layer structures fabricated using different processes. FIG. 7 shows another embodiment of an LED chip 100 that is similar to the LED chip 50 shown in FIGs. 4 and 5 and described above. For the same or similar features or elements the same reference number above from the description of LED chip 50 is used herein with the

understanding that the description above applies to this embodiment.

[0078] The LED chip 100 comprises an active structure 52, comprising a p-type layer 54 and an n-type layer 56, with an active region between the two. The front side of the LED chip 100 comprises a current spreading layer 58 on the p-type layer 54, and a dielectric reflective layer 60 on the current spreading layer 58, with adhesion layers included between additional layers as desired. A mirror stack 62 is included on the dielectric layer 60, with reflective layer vias 66 formed through the dielectric reflective layer 60 and passing from the mirror stack 62, to the current spreading layer 58.

[0079] Also on the front side of the LED chip 100, an n-type via hole 68 is formed through the dielectric reflective layer 60, current spreading layer 58, and p-type layer 54, to the n-type layer 56. The mirror stack 62 is offset from the hole, with the hole in the layers not formed in the self-aligned manner as described above. Furthermore, the dielectric reflective layer 60 is arranged differently than the dielectric reflective layer described above and extends on the inside of the via hole 68, over the surfaces of the p-type and n-type layers 54, 56 that are exposed in the via hole 68. The passivation layer hole 72 extends through the dielectric reflective layer 60 at the top of the via hole 68 to expose a surface of the n-type layer 56 for contacting by the via conductive layer 74. The dielectric reflective layer 60 can also extend into the first street 78 and the bond pad area 80. The front side passivation layer 70 extends into the first street 78 on the reflective layer 60.

[0080] This coverage of the dielectric reflective layer 60 provides for a reflective cup arrangement that help reflect sideways or lateral emitting or trapped light so that it can contribute to useful emission from the LED chip. This can include light that emits directly from the active region in a sideways direction or the light is trapped within the active structure by total internal reflection (TIR). As shown by first light path 102, light emitted along the active region toward the edge of the active structure 52 can be reflected by the upward extending portion of the dielectric reflective layer 60 at the active structure's edge. Similarly and as shown by second light path 104, light emitted toward the via can be reflected by the upward extending portion of the dielectric reflective layer 60 in the via hole 68. This reflective cup arrangement can provide for overall improved emission efficiency for the LED chip 100.

[0081] There are further differences in LED package 100. Unlike the LED package 50, the current spreading layer 58 does not extend into the first street 78 or the bond pad area 80. Instead, it stops at or near the edge of the active structure 52. Furthermore, the dielectric reflective layer 60 does not stop at the edge of the active structure 52 in the bond pad area 80, but instead continues up the edge surface of the current spreading layer 58, the edge of the p-type layer 54 and part of the edge of the n-type layer, and then extends into the bond pad area 80.

[0082] The LED package also comprises first and second backside passivation layers 86, 88, with the first passivation layer 86 arranged for formation of the pattern to dictate the shape and size of the n-type texture features as described above. Like above, the

self-limiting etching of the textured features allows for the same etch step to be used for the formation of the texture features and the first street 78, and the bond pad area 80. The second backside passivation layer 88 is provided as protection over the texture features, first street 78 and bond pad area 80. A p-contact hole 84 can be formed in the bond pad area 80, through the second backside passivation layer 88 and the dielectric reflective layer 60, to expose the top surface of the mirror stack 62. A p-type contact 82 can be formed in the hole 84 and in contact with the mirror stack. Like above, an electrical signal applied to the p-type contact 82 spreads into the mirror stack 62, and is conducted through the vias 66 to the current spreading layer 58 where the signal spreads into the p-type layer 54. An electrical signal applied to the conductive layer 74 is conducted to the n-type layer 56 as described above.

[0083] For LED 100 the dielectric reflective layer 60 can terminate at different points after the active mesa etch. In some embodiments the dielectric reflective layer can extend beyond the edge of the n-GaN into the first street 78 and the bond pad area 80 as shown, while in other embodiments it can terminate between the active mesa step and the edge of the n-GaN. In most embodiments it can be important for the dielectric reflective layer 60 to go past the active area step to form the reflective cup as described above. There can be other considerations regarding how far the layer extends such as the moisture permeability difference between SiO_2 and SiN , where it may be preferred not to have the SiO_2 be continuous across the street. Another SiN (backside passivation) layer is included that would cover the SiO_2 in the streets, but once singulated the edge of the SiO_2 could be exposed. If

some of the SiO₂ of the dielectric reflective is removed in the street, then it would be encapsulated with SiN from both sides.

[0084] The LED chip 100 also presents a simplified structure that can be fabricated using fewer steps than are used in fabrication of conventional LED chips. The LED chip 100 has layers arranged as described above to provide for enhanced light extraction. FIG. 8 is a flow diagram 120 showing some of the steps used in one embodiment of a fabrication process according to the present invention, with different steps focusing primarily on etching processes. Following deposition of the current spreading layer 58, in step one 121 the n-mesa is etched through the current spreading layer 58, through the p-type layer 54 and to n-type layer 56.

[0085] The dielectric layer 60 can then be deposited on over the current spreading layer 58 and over the n-mesa. In some embodiments, the dielectric reflective layer 60 can form a cup as described above and can extend into one or both of the first street 78 and the bond pad area 80. In step two 122, dielectric layer holes 64 can be formed through the dielectric layer using known etching processes.

[0086] In step three 123, the mirror stack can be deposited on the dielectric reflective layer 60, filling the dielectric layer holes to form vias 66. The passivation layer 70 can then be deposited and in step four 124 the passivation layer can be etched to form the n-contact via hole 68. The conductive layer 74 can then be formed over the passivation layer and in contact with the n-type layer 56.

[0087] The first backside passivation layer 86 can then be deposited and etched into its pattern of features. In step five 125, the textured features 87, first street 78 and the bond pad area 80 can be etched in the same step. As described above, the etching of the textured features 87 can be self-limiting, which allows for etching of the textured features and streets even though the street etching can take more time.

[0088] The second backside layer 88 can then be deposited and in step six 126 the second backside passivation layer 88, and the dielectric reflective layer 60 can be etched to the mirror stack 62 and the p-contact 82 can be deposited on the mirror stack 62.

[0089] It is understood that different embodiments can be layers arranged in many different ways beyond those shown in the embodiments above, and can cover different portions of adjacent layers. For example, in the embodiments above, the mirror stack 62 extends into the bond pad area 80 but does not extend beyond the edge of the active region 52 in the first street 78, and does not extend beyond the edge of the n-type via hole 68. However, in other embodiments these and other layers can cover different portions and can extend beyond the areas shown.

[0090] FIG. 9 shows another embodiment of an LED chip 130 according to the present invention that is similar to the LED chip 100 shown in FIG. 6 and described above. The LED chip 130 comprises an active structure 52 having a p-type layer 54 and an n-type layer 56, with an active region between the two. The front side of the LED chip 130 comprises a current spreading layer 58 a dielectric reflective layer 60 on the current spreading layer 58,

with adhesion layers included between additional layers as desired. A mirror stack 62 is included on the dielectric layer 60, with reflective layer vias 66 formed through the dielectric reflective layer 60 and passing from the mirror stack 62, to the current spreading layer 58.

[0091] As with the embodiments above, an n-type via hole 68 is formed through the dielectric reflective layer 60, current spreading layer 58, and p-type layer 54, to the n-type layer 56. Also similar to the embodiments above, the dielectric reflective layer 60 and the mirror stack 62 extend beyond the edge of the active structure 52 in the bond pad area 80 and the dielectric reflective layer extends into the first street 78. However, in this embodiment, the metal stack 62 can extend beyond the edge of the active structure 52 on the dielectric reflective layer 60 and at least partially into the first street 78. The metal stack 62 can also extend with the dielectric layer beyond the edge of the active structure and also to at least partially cover the inner surface of the n-type via hole 68. It is understood that in some embodiments the metal stack 62 should not extend to the n-type GaN layer 56 and should not extend to the edge of the street 80. The mirror stack 62 also should not extend in the n-type via holes to completely cover the dielectric reflective layer 60 in the n-type via holes 68. This allows for efficient and reliable singulation of the devices and allows for etching of the passivation layer hole 72 without contacting the metal stack 62 when depositing the conductive layer 74 on the passivation layer 70.

[0092] This arrangement can provide advantages such as a more efficient cup like reflector that in the

embodiment described above. Both the dielectric layer 60 and the metal stack 62 can contribute to the reflection of light that emits directly from the active region in a sideways direction or light that is trapped within the active structure by total internal reflection (TIR). It is also understood that the metal stack can extend as described herein in embodiments not having the reflect cup arrangement, such as in the embodiment described herein.

[0093] GaN texturing using SiN dots formed from the first backside passivation layer and a self-limiting crystallographic wet etch is described above. Some crystallographic etch is known to etch rapidly through n-GaN but is slow through p-GaN. The LED chip 100 can have an advantage in that the p-GaN has been removed during front side processing (at the n-mesa etch), so the backside etch completes within a relatively short time. For the some prior art devices as well as LED chip 50, the backside etch needs to go through p-GaN, and the etch can consequently take longer and sometimes leaves p-GaN residue that can lower process yield.

[0094] Referring again to the LED chip 50 shown in FIGs. 4 and 5 and described above, the self-aligned mirror stack 62, dielectric reflective layer 60, current spreading layer (ITO), p-type layer and part of n-type layer (GaN), the hole through these layers can be etched by reactive ion etch (RIE) processes, while it is preferred to wet etch Ag mirror stack due to known difficulties performing a clean dry etch of Ag. If an adhesion layer is included and depending on the choice of the adhesion layer, it may be wet or dry etched. The Ag mirror stack wet etch will etch Ag laterally as well as vertically, resulting in an undercut. If the adhesion

layer is a light absorbing metal, the Ag undercut can create an absorbing edge around the Ag periphery, as seen from the dielectric layer side. This is undesirable since it can affect light extraction negatively. It is also undesirable to have an overhanging adhesion layer when depositing the passivation layer over the top because the overhang can prevent conformal coating, leaving gaps in the passivation that can negatively impact reliability.

[0095] Referring now to FIG. 10, to address this issue the present invention provides a process whereby a second wet etch is performed after completing the etch of the Ag mirror stack 62, with the second etch comprising a chemical that etches the adhesion layer 130 but not the Ag mirror stack 62. When this etching process is timed properly, the second etch causes the adhesion layer 130 to etch laterally beyond the mirror stack 62, thus eliminating the absorbing edge around the mirror stack 62. This process also leaves the dielectric reflective layer 60 and current spreading layer 58 aligned in the via hole 68. Many different wet etches can be used to etch Ag, such as commercially available Silver Etchant TFS, Seiver Ethcant 9044 (both from Transese Company, Inc.), and commercially available nitric acid (concentrated or diluted). One example of an adhesion layer material can comprise Ti, which is compatible with Ag. In some embodiments, the Ti layer can be etched with HCl (concentrated or diluted in water).

[0096] For the build structures according to the present invention and as described above with the embodiments shown in FIGs. 4 and 6, the p-contact 82 can be on and connected to the mirror stack 62, with some embodiments having a p-contact on the Ag-side of mirror stack. Before the p-contact 82 is formed, a hole must be formed through

as many as three layers or more. In some embodiments these layers can include the second backside passivation layer 88, the current spreading layer (ITO) 58 and the dielectric layer 60. Typical RIE chemistries for etching dielectrics can tarnish exposed Ag, which may result in a poor electrical contact or inconsistent visual appearance that interferes with automated visual inspection tools. One solution to the problem is to remove the tarnish with immersion into a chemical or by exposing the tarnished surface to a plasma clean, such as N₂ plasma.

[0097] In some embodiments according to the present invention, when depositing the p-contact 82, the exposed mirror stack (Ag) should be encapsulated to prevent metal (Ag) migration during operation. All exposed surfaces of the metal (Ag) should be sealed in during p-contact deposition. There are two elements to this. First, there should be no polymer or impurity deposition on the sidewalls during the RIE etch preceding the p-contact deposition. Second, the p-contact should comprise metals known to be good barrier metals and the deposition of the metals should cover the sidewalls as well as the bottom of the p-contact hole. Examples of suitable RIE etch chemistries include CF₄/O₂ and SF₆/O₂. Referring now to FIG. 11 shows on embodiment p-contact structure 140 that can comprise more than one material, with the p-contact 140 comprising a barrier layer 142 of one material and a bulk material 144 of another. Examples of suitable materials comprise p-contact barrier layer 142 materials include but is not limited to sputtered Ti/Pt, followed by a bulk material comprising 144 comprising evaporated Au. Other embodiments can comprise a barrier layer 142 of sputtered Ti/Ni and a bulk material 144 of evaporated

Ti/Au. Still other embodiments can comprise different combinations of these materials.

[0098] With references again to the embodiments shown in FIGs. 4 and 6, as the structures go through a wafer bonding process there is potential to have voids in the bond layer if the structure topology is too large. For example, the voids under the vias hole 68 or the first street 78 can be too large and result in voids in the bond layer. A solution to this problem can be to planarize the structure prior to wafer bonding. This can be achieved by including a polymer or spin-on-glass on the wafer. FIG. 12 shows an embodiment of an LED chip 160 that is similar to the LED chip 50 shown in FIG. 5 and described above. In this embodiment, a polymer 162 can be included in the voids with the polymer 162 spin-coated, cured, and etched back in the planar regions, just prior to depositing on the bond layer 164. Alternatively, the planarization can be performed between the passivation and the Al layer, between the mirror stack and the passivation, or the planarization polymer can replace passivation. In these embodiments, the polymer can be left intact after cure, or it can be etched back in the planar regions leaving polymer only at step edges.

[0099] FIG. 13 shows another embodiment of an LED chip 150 according to the present invention with a further simplified build. The LED chip 170 can comprise layers and structures similar to LED chip 50 including, but not limited to, the active structure 52, and front side layers such as the current spreading layer 58, mirror stack 62, passivation layer 70, conductive layer 74 and bond layer 76. The backside can also comprise the first street 78, bond pad area 80, p-contact 82, first and second backside passivation layers 86, 88 and textured

features 87. The LED chip 170, however, is simplified by removing the dielectric reflective layer and eliminating the step of forming vias through the reflective layer. This can result in a simplified build process comprising fewer steps, with some embodiments having been fabricated in as little as a 4-step or 4-level build. In some embodiments, removing the reflective layer may result in some reduction in emission efficiency by removal of the dielectric reflective layer, but in some applications these losses may be acceptable.

[00100] In still other embodiments the street and texture features can be etched in two different etching steps as in prior art devices. This can, however, add an additional step to the fabrication process for LED chip 50 and LED chip 100. In still other embodiments the current spreading layer can be removed, in which case the mirror stack can be directly in contact with p-GaN and can be used for spreading current from the p-contact instead of the current spreading layer.

[00101] Although the present invention has been described in detail with reference to certain preferred configurations thereof, other versions are possible. Therefore, the spirit and scope of the invention should not be limited to the versions described above.

WE CLAIM:

1. A light emitting diode (LED) chip, comprising:
an active LED structure comprising an active region between two oppositely doped layers, and said active region emitting light in response to an electrical signal applied to said oppositely doped layer;
a first reflective layer adjacent one of said oppositely doped layers;
a second reflective layer on said first reflective layer, said second reflective layer reflecting light not reflected by said first reflective layer, wherein at least one of said first and said second reflective layers extend beyond the edge of said active LED structure.
2. The LED chip of claim 1, wherein the first reflective layer extends beyond the edge of said active LED structure.
3. The LED chips of claim 1, wherein said second reflective layer extends beyond the edge of said active LED structure.
4. The LED chip of claim 1, wherein both the first and second reflective layers extend beyond the edge of said active LED structure.
5. The LED chip of claim 1, wherein said first reflective layer comprises a dielectric material.
6. The LED chip of claim 1, wherein said first reflective layer comprises SiO₂, SiN, Si, Ge, MgOx, MgNx, ZnO, SiNx, SiOx, AlN and alloys or combinations thereof.

7. The LED chip of claim 1, wherein said second reflective layer comprises a metal.

8. The LED chip of claim 1, wherein said second reflective layer comprises a metal stack.

9. The LED chip of claim 1, further comprising a current spreading layer between said first reflective layer and said active LED structure.

10. The LED chip of claim 1, further comprising a p-contact, wherein said p-contact is on said second reflective layer.

11. The LED chip of claim 7, wherein said p-contact is arranged in a hole through said first reflective layer.

12. The LED chip of claim 1, wherein said first reflective layer extends beyond the edge of one or more layers of said active structure.

13. The LED chip of claim 1, wherein said first reflective layer terminates before the edge of said LED chip.

14. The LED chip of claim 1, wherein said first reflective layer terminates at the edge of said LED chip.

16. The LED chip of claim 1, wherein said first reflective layer terminates between the edge of said active region and the edge of said n-type layer.

17. The LED chip of claim 1, wherein said first and/or second reflective layers form a reflective cup.

18. The LED chip of claim 1, wherein said reflective cup comprises an upward extending portion that reflects emitted laterally in said active structure.

19. The LED chip of claim 1, comprising a self-aligned via hole through said first and second reflectors to said active structure.

20. The LED chip of claim 1, further comprising textured features on said active structure.

21. The LED chip of claim 20, wherein said textured features are self-limiting to an etch.

22. A light emitting diode (LED) chip, comprising:

an active LED structure comprising an active region between two oppositely doped layers, and said active region emitting light in response to an electrical signal applied to said oppositely doped layer;

a dielectric reflective layer on one of said oppositely doped layers and extending beyond the edge of said active region;

a metal reflective layer on said first dielectric reflective layer.

23. The LED chip of claim 22, wherein said dielectric reflective layer extends beyond the edge of said n-type layer.

24. The LED chip of claim 22, wherein said dielectric reflective layer terminates before the edge of said LED chip.

25. The LED chip of claim 22, wherein said dielectric reflective layer terminates at the edge of said LED chip.

26. The LED chip of claim 22, wherein said dielectric reflective layer terminates between the edge of said active region and the edge of said n-type layer.

27. The LED chip of claim 22, wherein said dielectric reflective and/or said metal layer form a reflective cup.

28. The LED chip of claim 22, wherein said metal reflective layer extends beyond the edge of said active structure.

29. The LED chip of claim 28, further comprising a p-contact, wherein said p-contact is on said metal reflective layer.

30. The LED chip of claim 28, wherein said p-contact passes through said dielectric layer and is directly on said metal reflective layer.

31. The LED chip of claim 22, comprising a self-aligned via hole through said dielectric and metal reflective layer to said active structure.

32. The LED chip of claim 22, further comprising self-limiting textured features on said active structure.

33. A method for forming LED chips, comprising:
 depositing active structure epitaxial layers on a wafer;
 etching different portions of said active structure in a single etch step, wherein said different portions

etch at different rates and wherein at least one of said portions is self-limiting to said etch.

34. The method of claim 33, wherein said self-limiting portions comprise textured features on said active structure.

35. The method of claim 33, further comprising forming an array of mask features on said active structure, said etch etching the active structure between said mask features.

36. The method of claim 33, wherein another of said at least one of said portions comprises streets formed between active structure mesas.

37. The method of claim 33, further comprising forming a plurality of reflective layers on said active epitaxial layers.

38. The method of claim 37, further comprising a single etch step to form a self-aligned via hole through said reflective layers to said active structure.

39. The method of claim 33, further comprising forming a plurality of reflective layers on said active epitaxial layers, with one or more of said reflective layers extending beyond the edge of said active structure mesas.

40. The method of claim 39, further comprising forming a contact on one of said reflective layers.

41. The method of claim 39, wherein one or more of said plurality of reflective layers forms a reflective cup.

42. A method for forming LED chips, comprising:
forming an active structure of epitaxial layers;
forming a plurality of reflective layers on said active structure;
performing a single etch step to form a self-aligned via hole through said reflective layers to said active structure.
43. A light emitting diode (LED) chip, comprising:
an active LED structure;
a first reflective layer adjacent said active layer;
a second reflective layer on said first reflective layer, said second reflective layer reflecting light not reflected by said first reflective layer, wherein said first reflective layer extends beyond the active region on a portion of the LED chip.
44. The LED chip of claim 43, wherein said first reflective layer extends beyond the active region on substantially all of the LED chip.
45. The LED chip of claim 43, wherein said second reflective layer extends beyond said active region on a portion of the LED chip.
46. The LED chip of claim 43, wherein said second reflective layer extends beyond said active region on substantially all of the LED chip.
47. The LED chip of claim 46, further comprising a contact on said second reflector.

48. The LED chip of claim 46, wherein said contact passes through said first reflective layer.

49. A light emitting diode (LED) chip, comprising:
an active LED structure;
a plurality of layers on the backside of said active structure;
a via hole on the backside of and into said active LED structure, wherein at least two of said plurality of layers are self-aligned at said via hole.

50. The LED chip of claim 49, wherein said plurality of layers comprises a current spreading layer and a first reflective layer self-aligned at said via hole.

51. The LED chip of claim 49, wherein said first reflective layer comprises a dielectric material.

52. The LED chip of claim 49, wherein said plurality of active layers further comprises a second reflective layer self-aligned at said via hole.

53. The LED chip of claim 52, wherein said second reflective layer comprises a metal.

54. A light emitting diode (LED) chip, comprising:
an active LED structure;
a plurality of layers on the backside of said active structure;
wherein one or more of said plurality of layers self-aligned at more than one location on the backside of said active structure.

55. The LED chip of claim 54, further comprising a via hole, wherein one of said plurality of layers comprises a first layer self-aligned at said via hole and at the edge of said active structure.

56. The LED chip of claim 55, wherein said first layer comprises a current spreading layer.

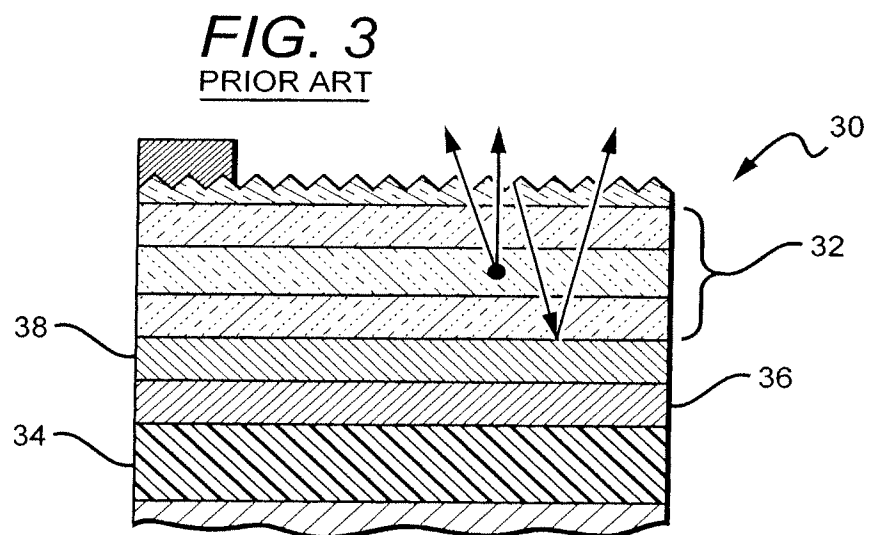
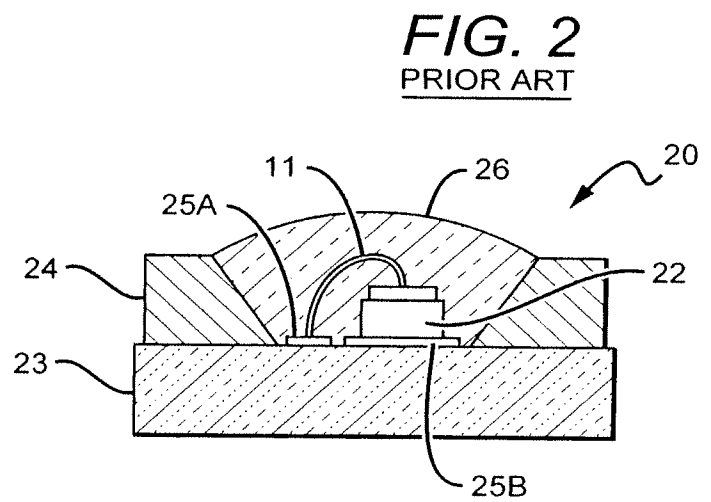
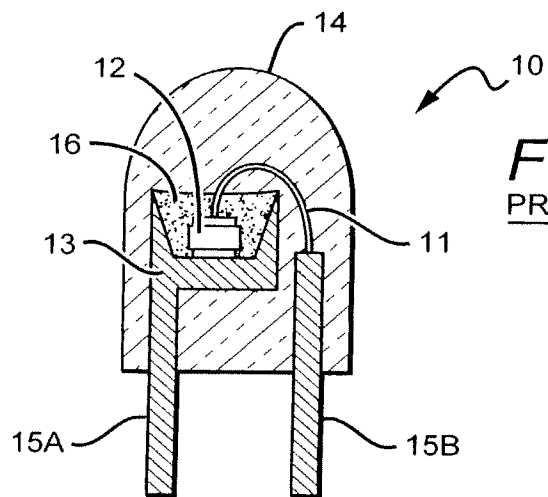
57. The LED chip of claim 55, wherein said plurality of layers further comprises a second layer on said first layer, wherein said second layer is self-aligned at said via hole and/or at the edge of said active structure.

58. The LED chip of claim 57, wherein said second layer comprises a dielectric reflective layer.

59. The LED chip of claim 57, wherein said plurality of layers further comprises a third layer on said second layer, where said third layer is self-aligned at said via hole and/or the edge of said active structure.

60. The LED chip of claim 59, wherein said third layer comprises a metal reflective layer.

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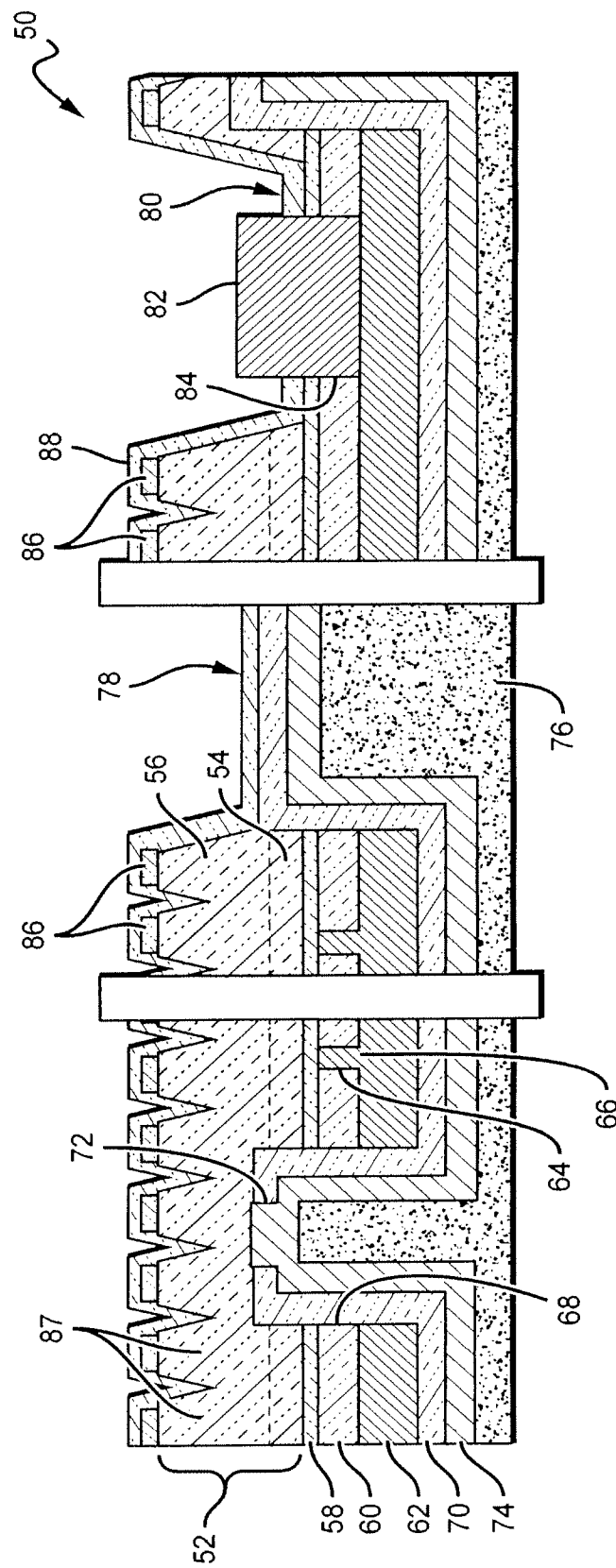


FIG. 4

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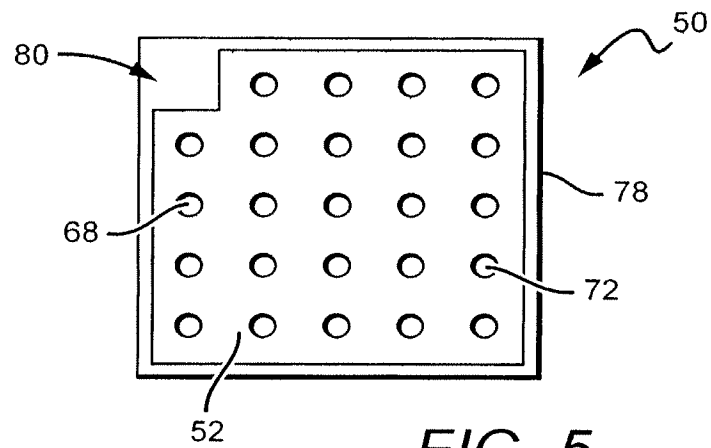


FIG. 5

FIG. 6

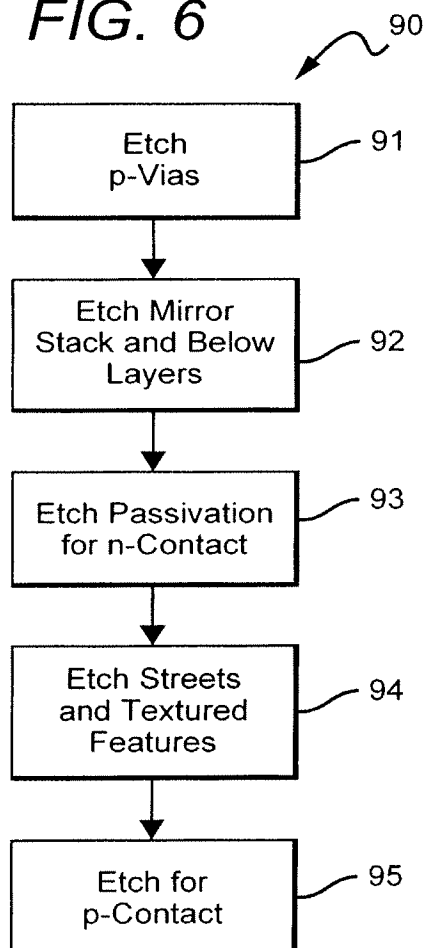
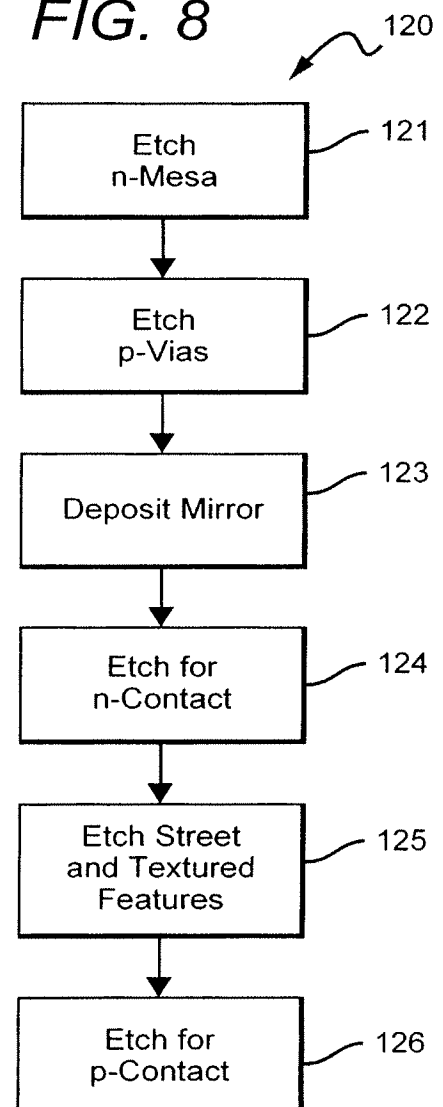


FIG. 8



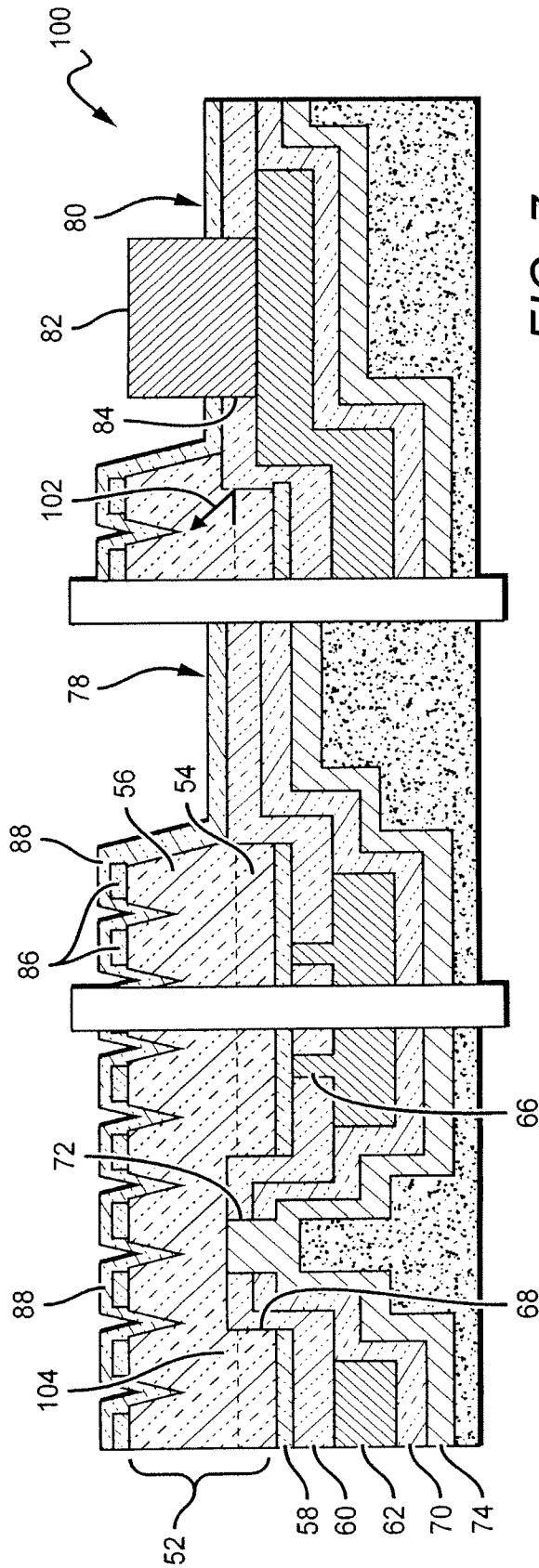


FIG. 7

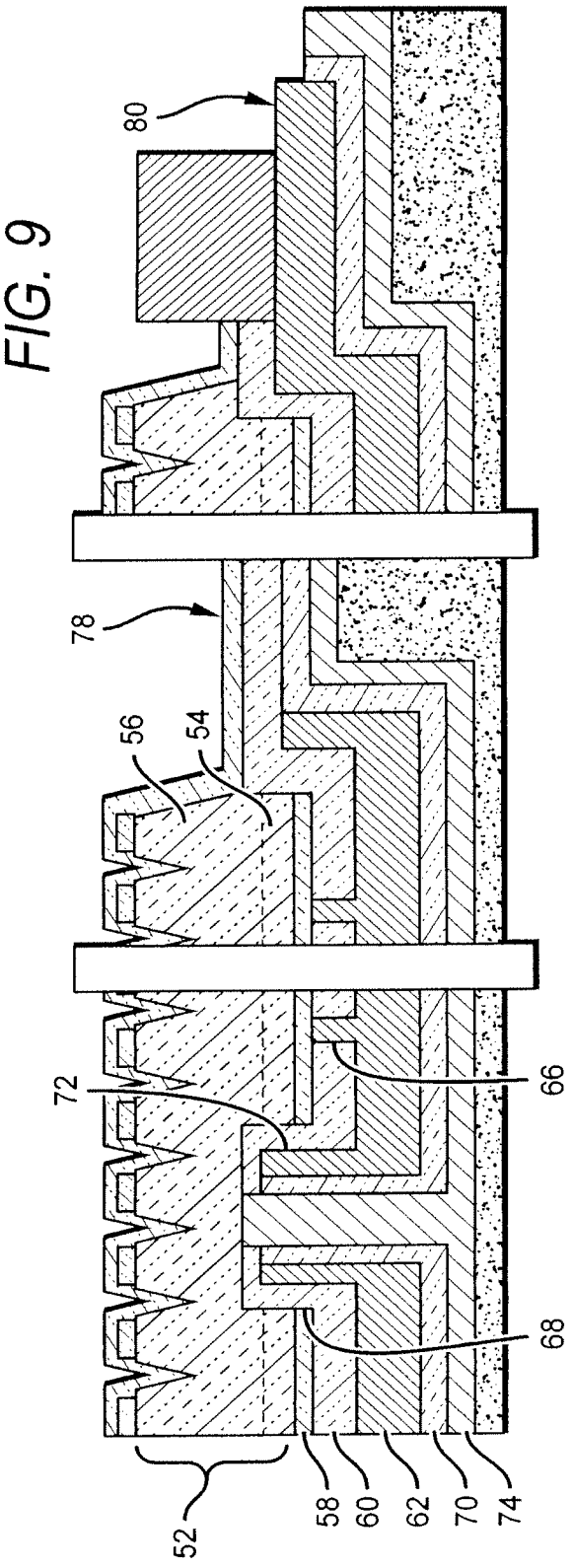


FIG. 9

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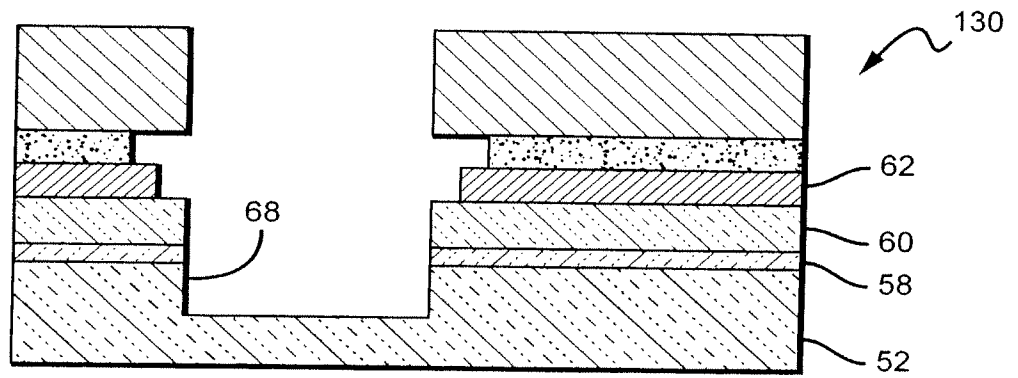
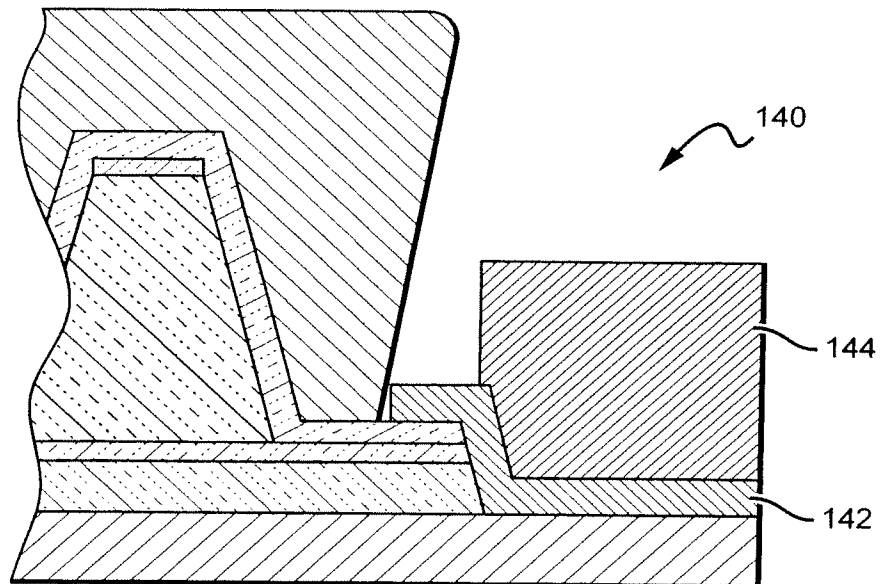
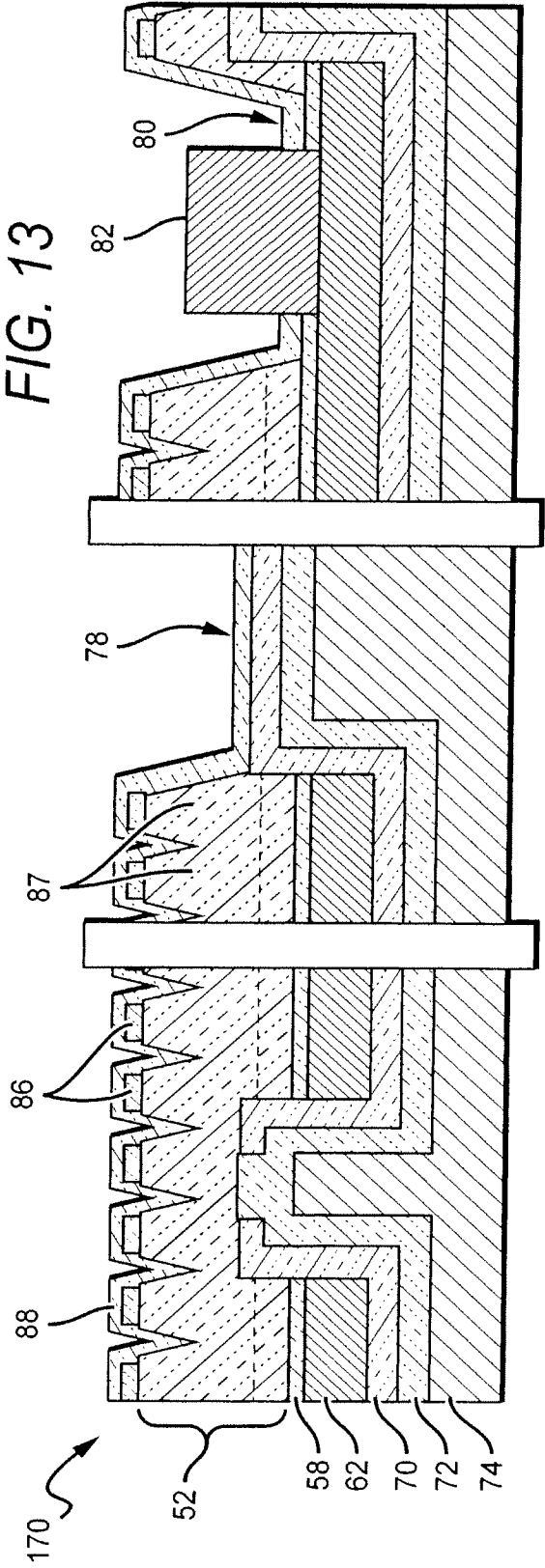
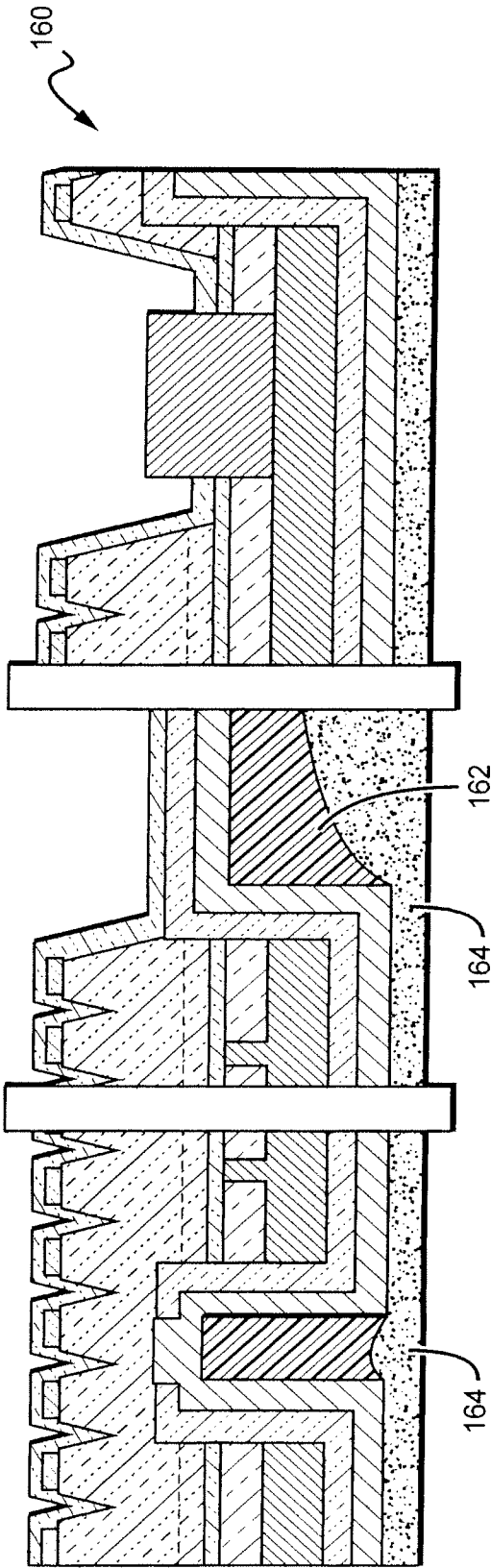


FIG. 10

FIG. 11





INTERNATIONAL SEARCH REPORT

International application No
PCT/US2016/013711

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L33/42 H01L33/46
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EP0-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2006/273335 A1 (ASAHARA HIROKAZU [JP] ET AL) 7 December 2006 (2006-12-07) abstract; figure 1	1
X	----- WO 2012/164456 A1 (KONINKL PHILIPS ELECTRONICS NV [NL]; AKRAM SALMAN [US]; BHAT JEROME CH) 6 December 2012 (2012-12-06) abstract; figures 7,9 paragraph [0026] paragraph [0025] ----- -/-	1,13,22, 24



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

22 March 2016

Date of mailing of the international search report

29/06/2016

Name and mailing address of the ISA/

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Authorized officer

Heising, Stephan

INTERNATIONAL SEARCH REPORT

International application No

PCT/US2016/013711

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	W0 2014/025195 A1 (SEOUL VIOSYS CO [KR]) 13 February 2014 (2014-02-13) abstract; figures 14-17, 30 paragraphs [0081], [0094] -----	1-9, 12-14, 16-18, 22,23, 25-28, 43-47

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2016/013711

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:
2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:
3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of Item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:
4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

1-9, 12-14, 16-18, 22-28, 43-47

Remark on Protest

- ☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
- ☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
- ☐ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1-9, 12-14, 16-18, 22-28, 43-47

directed to a light emitting diode with an active LED structure having reflective layer(s) extending beyond the active LED structure

2. claims: 20, 21, 32-41

directed to a method of fabricating a light emitting diode with an active LED structure having self-limiting features during an etch step.

3. claims: 10, 11, 19, 29-31, 42, 48-60

directed to a light emitting diode with an active LED structure having a self-aligned via hole in the reflective layers formed on the active structure.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/US2016/013711

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2006273335 A1	07-12-2006	CN 1820378 A	16-08-2006
		JP 4976849 B2	18-07-2012
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		DE 112013003931 T5	03-06-2015
		US 2015200230 A1	16-07-2015
		WO 2014025195 A1	13-02-2014
