



**(43) International Publication Date**  
**21 July 2016 (21.07.2016)**

**(51) International Patent Classification:**

|                             |                              |
|-----------------------------|------------------------------|
| <i>H01L 29/78</i> (2006.01) | <i>H01L 29/06</i> (2006.01)  |
| <i>H01L 29/66</i> (2006.01) | <i>H01L 29/739</i> (2006.01) |

**(21) International Application Number:**

PCT/JP2015/006178

**(22) International Filing Date:**

11 December 2015 (11.12.2015)

**(25) Filing Language:**

English

**(26) Publication Language:**

English

**(30) Priority Data:**

2015-005471 15 January 2015 (15.01.2015) JP

(71) Applicants: TOYOTA JIDOSHA KABUSHIKI KAIS-

**HA** [JP/JP]; 1, Toyota-cho, Toyota-shi, Aichi, 4718571 (JP). **DENSO CORPORATION** [JP/JP]; 1-1, Showa-cho, Kariya-shi, Aichi, 4488661 (JP).

(72) Inventors: NISHIMURA, Shinya; c/o TOYOTA

JIDOSHA KABUSHIKI KAISHA, 1, Toyota-cho, Toyota-shi, Aichi, 4718571 (JP). **FUJIWARA, Hirokazu**; c/o

TOYOTA JIDOSHA KABUSHIKI KAISHA, 1, Toyota-cho, Toyota-shi, Aichi, 4718571 (JP). **SOEJIMA, Narumasa**; c/o KABUSHIKI KAISHA TOYOTA CHUO KEN-KYUSHO, 41-1, Yokomichi, Nagakute-shi, Aichi, 4801192 (JP). **TAKEUCHI, Yuichi**; c/o DENSO CORPORATION, 1-1, Showa-cho, Kariya-shi, Aichi, 4488661 (JP).

(74) Agent: KAI-U PATENT LAW FIRM; NAGOYA LU-

CENT TOWER 9F, 6-1, Ushijima-cho, Nishi-ku, Nagoya-shi, Aichi, 4516009 (JP).

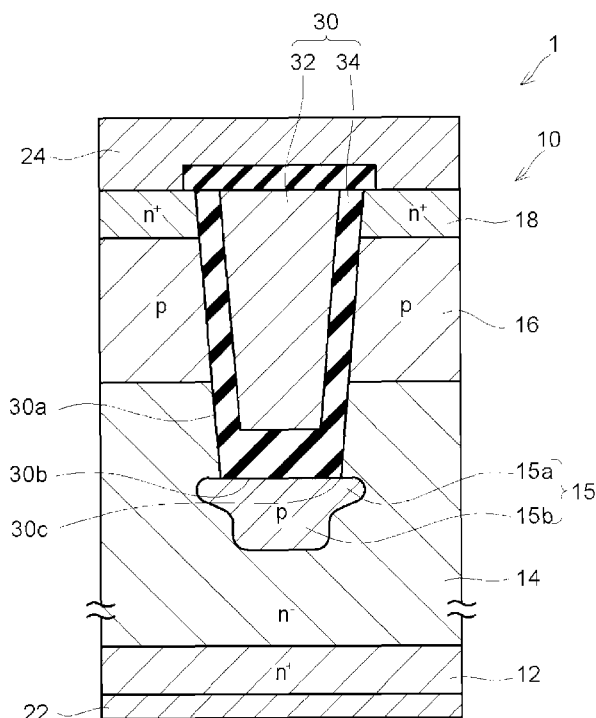
**(81) Designated States** (*unless otherwise indicated, for every*

*kind of national protection available*): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

*[Continued on next page]*

**(54) Title:** SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

FIG. 1



**(57) Abstract:** A semiconductor device includes a p-type semiconductor region in contact with a bottom face of a trench gate, wherein the p-type semiconductor region includes a first p-type semiconductor region containing a first type of p-type impurities and a second p-type semiconductor region containing a second type of p-type impurities. The first p-type semiconductor region is located between the trench gate and the second p-type semiconductor region. In a view along the depth direction, the second p-type semiconductor region is located within a part of the first p-type semiconductor region. A diffusion coefficient of the second type of p-type impurities is smaller than a diffusion coefficient of the first type of p-type impurities.



(84) **Designated States** (*unless otherwise indicated, for every kind of regional protection available*): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE,

SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

**Published:**

— with international search report (*Art. 21(3)*)

## Description

### Title of Invention: SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

#### Technical Field

- [0001] This application claims priority to Japanese Patent Application No. 2015-005471 filed on January 15, 2015, the contents of which are hereby incorporated by reference into the present application.
- [0002] The technique disclosed in the present application relates to a semiconductor device comprising a p-type semiconductor region in contact with a bottom surface of a trench gate, and a method of manufacturing the same.

#### Background Art

- [0003] Patent Literature 1 discloses a semiconductor device including a p-type semiconductor region in contact with a bottom face of a trench gate. The p-type semiconductor region relaxes an electric field applied to the bottom face of the trench gate and improves a withstand voltage of the semiconductor device.

#### Citation List

##### Patent Literature

- [0004] [Patent Literature 1] Japanese Patent Application Publication No. 2006-128507

##### Summary of Invention

- [0005] In conventional techniques, a p-type semiconductor region is formed by forming a trench extending along a depth direction from one of main surfaces of a semiconductor layer, and then irradiating p-type impurities toward the trench. In order to prevent the p-type impurities from being introduced to a side face of the trench when the p-type impurities are irradiated toward the trench, a protective film is formed on the side face of the trench. The p-type impurities are not introduced to an edge part of the bottom face of the trench, and introduced to a central part of the bottom face of the trench due to a thickness of the protective film.
- [0006] It is preferable that the p-type semiconductor region is not only formed under the edge of the bottom face of the trench gate, but also formed at a deeper position under the bottom face of the trench gate in order to relax an electric field applied to the bottom face of the trench gate.
- [0007] In the conventional techniques, a p-type semiconductor region that satisfies these conditions is formed by thermal diffusion of a single type of p-type impurities having a relatively large diffusion coefficient. The p-type semiconductor region formed by such thermal diffusion, however, spreads isotropically and hence spreads along a lateral direction unnecessarily at the deeper position under the bottom face of the trench gate,

resulting in an increase in on-resistance of the semiconductor device.

- [0008] As described above, a configuration required for a p-type semiconductor region is preferably a configuration that the p-type semiconductor region spreads, at a shallower position under the bottom face of the trench gate, along the lateral direction so as to be located under the edge of the bottom face of the trench gate, whereas the p-type semiconductor region spreads, at the deeper position under the bottom face of the trench gate, along a depth direction, with its spreading along the lateral direction being suppressed, in other words, a T-shape configuration in cross section as a whole. It is, however, difficult for a p-type semiconductor region formed with a single type of p-type impurities having a relatively large diffusion coefficient, to have such configuration.
- [0009] The present specification provides a technique that improves both of a withstand voltage and an on-resistance in a semiconductor device that comprises a p-type semiconductor region in contact with a bottom face of a trench gate.
- [0010] A semiconductor device disclosed in the present specification comprises a trench gate and a p-type semiconductor region. The trench gate extends from one of main surfaces of a semiconductor layer along a depth direction. The p-type semiconductor region is in contact with a bottom face of the trench gate. The p-type semiconductor region includes a first p-type semiconductor region containing a first type of p-type impurities and a second p-type semiconductor region containing a second type of p-type impurities. The first p-type semiconductor region is located between the trench gate and the second p-type semiconductor region. In a view along the depth direction, the second p-type semiconductor region is located within a part of the first p-type semiconductor region. A diffusion coefficient of the second type of p-type impurities is smaller than a diffusion coefficient of the first type of p-type impurities.
- [0011] In the above-described semiconductor device, the p-type semiconductor region is formed with two types of p-type impurities having different diffusion coefficients. The first p-type semiconductor region that contains a first type of p-type impurities having a relatively large diffusion coefficient is formed at a shallower position under the bottom face of the trench, and the second p-type semiconductor region that contains the second type of p-type impurities having a relatively small diffusion coefficient is formed at a deeper position under the bottom face of the trench. The p-type semiconductor region can thereby have a configuration in which it spreads, at the shallower position under the bottom face of the trench, along a lateral direction, whereas it spreads, at the deeper position under the bottom face of the trench, along a depth direction with its spreading along the lateral direction being suppressed. The semiconductor device can have a feature of a high withstand voltage and a low on-resistance.

- [0012] A manufacturing method of a semiconductor device disclosed in the present specification comprises forming a mask, forming a trench, irradiating a first type of p-type impurities and irradiating a second type of p-type impurities. In the forming of the mask, the mask is formed on one of main surfaces of a semiconductor layer, wherein an opening is formed in the mask. In the forming of the trench, the trench is formed to extend along a depth direction from the one of main surfaces which is exposed at the opening of the mask. In the irradiating of the first type of p-type impurities, the first type of p-type impurities is irradiated through the opening and toward the trench. In the irradiating of the second type of p-type impurities, the second type of p-type impurities is irradiated through the opening and toward the trench. The second type of p-type impurities is introduced to a deeper position under a bottom face of the trench than the first type of p-type impurities. A diffusion coefficient of the second type of p-type impurities is smaller than a diffusion coefficient of the first type of p-type impurities.
- [0013] According to the above-described manufacturing method, the first type of p-type impurities and the second type of p-type impurities are introduced under the bottom face of the trench, with the use of a common mask. This makes it possible to form a p-type semiconductor region that has the configuration in which it spreads, at a shallower position under the bottom face of the trench, along a lateral direction, whereas it spreads, at a deeper position under the bottom face of the trench, along a depth direction with its spreading along the lateral direction being suppressed. According to the above-described manufacturing method, it is therefore possible to manufacture a semiconductor device that comprises a p-type semiconductor region having such configuration.

### **Brief Description of Drawings**

- [0014] [fig.1]FIG. 1 schematically shows a cross section of a main part of a semiconductor device;
- [fig.2]FIG. 2 schematically shows an enlarged view of vicinity of an edge of a bottom face of a trench gate;
- [fig.3]FIG. 3 shows a relation between spreading of a p-type semiconductor region along a lateral direction and a withstand voltage of the semiconductor device, and a relation between spreading of the p-type semiconductor region along the lateral direction and an on-resistance of the semiconductor device;
- [fig.4]FIG. 4 shows a process of a manufacturing of a p-type semiconductor region in a manufacturing method of a semiconductor device;
- [fig.5]FIG. 5 shows a process of the manufacturing of the p-type semiconductor region in the manufacturing method of the semiconductor device;
- [fig.6]FIG. 6 shows a process of the manufacturing of the p-type semiconductor region

in the manufacturing method of the semiconductor device;

[fig.7]FIG. 7 shows a process of the manufacturing of the p-type semiconductor region in the manufacturing method of the semiconductor device;

[fig.8]FIG. 8 shows a process of the manufacturing of the p-type semiconductor region in the manufacturing method of the semiconductor device; and

[fig.9]FIG. 9 shows a process of the manufacturing of the p-type semiconductor region in the manufacturing method of the semiconductor device.

### **Description of Embodiments**

[0015] As shown in FIG. 1, a semiconductor device 1 comprises a semiconductor layer 10 made of silicon carbide, a drain electrode 22 that covers a rear surface of the semiconductor layer 10, a source electrode 24 that covers a front surface of the semiconductor layer 10, and a trench gate 30 provided at a front layer part of the semiconductor layer 10. The trench gate 30 extends from the front surface of the semiconductor layer 10 along a depth direction (a direction orthogonal to the front surface of the semiconductor layer 10, i.e., a direction from a top to a bottom on the paper). Although FIG. 1 shows only one trench gate 30, the semiconductor layer 10 is provided with a plurality of trench gates 30. In a view along the depth direction of the semiconductor layer 10 (in a planar view of the semiconductor layer 10), the plurality of trench gates 30 may be arranged in a stripe-shaped manner, or may be interspersed like islands. Each trench gate 30 includes a gate electrode 32 and a gate insulating film 34. The gate insulating film 34 covers the gate electrode 32.

[0016] The semiconductor layer 10 includes an n<sup>+</sup>-type drain region 12, an n-type drift region 14, a p-type semiconductor region 15, a p-type body region 16, and an n<sup>+</sup>-type source region 18. The drain region 12 is provided at a rear layer part of the semiconductor layer 10, and is in ohmic contact with the drain electrode 22. The drift region 14 is provided between the drain region 12 and the body region 16, and is in contact with a side face 30a of the trench gate 30. The drift region 14 is a remaining part that is obtained after other semiconductor regions are formed in the semiconductor layer 10. The p-type semiconductor region 15 is in contact with a bottom face 30b of the trench gate 30. The p-type semiconductor region 15 in this example is separated from the body region 16 by the drift region 14, and has a floating potential. As an alternative to this example, a p-type semiconductor region 15 may be configured to be in contact with a body region 16. The body region 16 is provided at the front layer part of the semiconductor layer 10, is provided between the drift region 14 and the source region 18, and is in contact with the side face 30a of the trench gate 30. The body region 16 is electrically connected to the source electrode 24 via a p<sup>+</sup>-type body contact region provided at a part of the cross section not shown. The source region 18 is

provided at the front layer part of the semiconductor layer 10, is in contact with the side face 30a of the trench gate 30, and is in ohmic contact with the source electrode 24. As such, a semiconductor structure that configures a MOSFET is provided in the semiconductor layer 10.

[0017] The p-type semiconductor region 15 includes a first p-type semiconductor region 15a and a second p-type semiconductor region 15b. The first p-type semiconductor region 15a is in contact with the bottom face 30b of the trench gate 30, and is provided at a shallower position under the bottom face 30b of the trench gate 30. The first p-type semiconductor region 15a has a width larger than a width of the second p-type semiconductor region 15b, along a width direction of the trench gate 30 (a direction connecting portions of side face 30a that face each other, hereinafter also referred to as a lateral direction). The second p-type semiconductor region 15b is in contact with the first p-type semiconductor region 15a, and is provided at a deeper position under the bottom face 30b of the trench gate 30. The first p-type semiconductor region 15a has boron introduced thereto as p-type impurities, and the second p-type semiconductor region 15b has aluminum introduced thereto as p-type impurities. In silicon carbide, boron has a diffusion coefficient larger than a diffusion coefficient of aluminum. Note that the first p-type semiconductor region 15a preferably contains boron at a concentration of at least equal to or more than  $1 \times 10^{16} \text{ cm}^{-3}$ , and in an example, the first p-type semiconductor region 15a is defined as containing boron at a concentration ranging from  $1 \times 10^{16}$  to  $1 \times 10^{18} \text{ cm}^{-3}$ . Similarly, the second p-type semiconductor region 15b preferably contains aluminum at a concentration of at least equal to or more than  $1 \times 10^{16} \text{ cm}^{-3}$ , and in an example, the second p-type semiconductor region 15b is defined as containing aluminum at a concentration ranging from  $1 \times 10^{16}$  to  $1 \times 10^{18} \text{ cm}^{-3}$ .

[0018] The first p-type semiconductor region 15a is also located under an edge 30c of the bottom face 30b of the trench gate 30, and projects out in a lateral direction from the edge 30c of the bottom face 30b of the trench gate 30. The second p-type semiconductor region 15b is located within a part of the first p-type semiconductor region 15a, in a view along the depth direction of the semiconductor layer 10. Moreover, the second p-type semiconductor region 15b is located within a part of the bottom face 30b of the trench gate 30, in the view along the depth direction of the semiconductor layer 10. As such, the p-type semiconductor region 15 has a configuration in which it spreads, at the shallower position under the bottom face 30b of the trench gate 30, along the lateral direction so as to be located under the edge 30c of the bottom face 30b of the trench gate 30, whereas it spreads, at the deeper position under the bottom face 30b of the trench gate 30, along the depth direction with its spreading along the lateral direction being suppressed, in other words, a T-shape configuration in cross section as

a whole.

[0019] FIGS. 2 and 3 show how the spreading of the first p-type semiconductor region 15a along the lateral direction affects a withstand voltage and an on-resistance of the semiconductor device 1. When the edge 30c of the bottom face 30b of the trench gate 30 is set as a reference A, a distance along the width direction of the trench gate 30 is set as X, and an orientation in which the first p-type semiconductor region 15a projects out along the lateral direction from the edge 30c of the bottom face 30b of the trench gate 30 is set positive, and a reverse orientation thereof is set negative. As shown in FIG. 3, in a range from -0.15 mm to +0.20 mm with respect to the reference A, the withstand voltage of the semiconductor device 1 is maintained high, and the on-resistance of the semiconductor device 1 is maintained low. In particular, in a case where the orientation is positive with respect to the reference A and the distance is equal to or smaller than 0.20 mm, in other words, in a case where the first p-type semiconductor region 15a projects out along the lateral direction from the edge 30c of the bottom face 30b of the trench gate 30 and a length by which the first p-type semiconductor region 15a projects out is equal to or smaller than 0.20 mm, the semiconductor device 1 can have superior characteristics in both the withstand voltage and the on-resistance.

[0020] In addition, the first p-type semiconductor region 15a is not in contact with the side face 30a of the trench gate 30. The side face 30a of the trench gate 30 is a part where a channel is formed when the semiconductor device 1 is on. Although the semiconductor device 1 includes the p-type semiconductor region 15, the p-type semiconductor region 15 does not exist at this part where the channel is formed, resulting in that an increase in on-resistance is suppressed.

[0021] The second p-type semiconductor region 15b has a width, along the lateral direction, smaller than the width of the first p-type semiconductor region 15a. For example, the p-type semiconductor region in the conventional techniques is formed by isotropic thermal diffusion, and hence has a configuration of being spread widely along the lateral direction at a depth corresponding to a depth of the second p-type semiconductor region 15b. Thus in the conventional semiconductor device, a current path of a current flowing in the drift region becomes narrow, resulting in an increase in on-resistance. On the other hand, in the semiconductor device 1, the spreading of the second p-type semiconductor region 15b along the lateral direction has been suppressed, and hence a wide current path of the current flowing in the drift region 14 is ensured, resulting in a low on-resistance. Moreover, the second p-type semiconductor region 15b has a configuration of being spread along the depth direction, resulting in that the withstand voltage of the semiconductor device 1 is maintained high.

[0022] A manufacturing process of forming a p-type semiconductor region 15 in a manu-

facturing method of a semiconductor device 1 will now be described. As for manufacturing processes other than the process of forming the p-type semiconductor region 15, known manufacturing steps can be utilized to manufacture the semiconductor device 1.

- [0023] Initially, as shown in FIG. 4, a semiconductor layer 10 made of silicon carbide is prepared. A body region 16 and a source region 18 have been formed at a front layer part of the semiconductor layer 10.
- [0024] Next, as shown in FIG. 5, a TEOS film 42 is deposited on a front surface of the semiconductor layer 10 with the use of a CVD. The TEOS film 42 has a thickness of approximately 1.5  $\mu\text{m}$ . Note that the TEOS film 42 is an example of a mask according to the appended claims. Next, an opening 42a is formed in the TEOS film 42 to expose the front surface of the semiconductor layer 10. Next, a trench 31 that extends along a depth direction from the front surface of the semiconductor layer 10, the front surface being exposed at the opening 42a of the TEOS film 42, is formed with the use of a dry-etching technique. The trench 31 has a side face inclined relative to the depth direction, and has a tapered shape in cross section. The trench 31 penetrates the source region 18 and the body region 16 to reach the drift region 14.
- [0025] Next, as shown in FIG. 6, boron ions 5a are irradiated toward the trench 31 through the opening 42a of the TEOS film 42 with the use of an ion implantation technique. The boron ions 5a have a low implantation energy of 60 to 240 keV, and are irradiated in a dose of  $2.0$  to  $2.5 \times 10^{15} \text{ cm}^{-2}$ . The boron ions 5a are irradiated in a multistage manner under the bottom face of the trench 31, so as to have a depth of equal to or smaller than 0.4  $\mu\text{m}$ . At this time, the boron ions 5a are also introduced to the side face of the trench 31.
- [0026] Next, as shown in FIG. 7, a part of the side and bottom faces of the trench 31 is cut with the use of a chemical dry-etching. A thickness to be cut is approximately 60 nm. Most or all of a part of the side face of the trench 31 where the boron ions have been introduced is thereby removed by cutting. As for the bottom face of the trench 31, most of a part where the boron ions have been introduced remains as it is. A concentration of the p-type impurities in the side face of the trench 31 is lowered to a concentration ( $5.0 \times 10^{15} \text{ cm}^{-3}$ ) that provides a desired threshold voltage when compared to the concentration before the etching.
- [0027] Next, as shown in FIG. 8, aluminum ions 5b are irradiated toward the trench 31 through the opening 42a of the TEOS film 42 with the use of an ion implantation. The aluminum ions 5b have a high implantation energy of 240 to 900 keV, and are irradiated in a dose of  $2.0$  to  $2.5 \times 10^{13} \text{ cm}^{-2}$ . The aluminum ions 5b are irradiated in a multistage manner, so as to have a depth ranging from 0.3 to 0.8  $\mu\text{m}$  under the bottom face of the trench 31. Due to the cutting, the side face of the trench 31 is located at a

position retracted from a plane that defines the opening 42a of the TEOS film 42. The side face of the trench 31 is therefore shielded by the TEOS film 42, in a view along a direction along which the aluminum ions 5b are irradiated. Accordingly, the aluminum ions 5b are not introduced to the side face of the trench 31, and selectively introduced to the bottom face of the trench 31.

[0028] Next, as shown in FIG. 9, activation annealing is performed after the TEOS film 42 is removed, so as to activate the boron ions 5a and the aluminum ions 5b having been introduced. A region where the boron ions 5a are activated serves as a first p-type semiconductor region 15a, whereas a region where the aluminum ions 5b are activated serves as a second p-type semiconductor region 15b, and a p-type semiconductor region 15 is thereby formed. At this time, the boron ions 5a have a large diffusion coefficient, and are thermally diffused by approximately 0.2 mm. On the other hand, the aluminum ions 5b have a small diffusion coefficient, and are hardly diffused. This allows the p-type semiconductor region 15 to have a T-shape configuration in cross section.

[0029] In the above-described manufacturing method, aluminum ions, which have a small diffusion coefficient, are introduced at a deeper position under the bottom face of the trench 31. This makes it possible to form the second p-type semiconductor region 15b at the deeper position under the bottom face of the trench 31, and hence it is not necessary to cause boron ions of which diffusion coefficient is large, to be thermally diffused widely along the depth direction. For example, in the conventional manufacturing method, it is necessary to cause boron ions of which diffusion coefficient is large, to be thermally diffused widely along the depth direction, resulting in that the boron ions are thermally diffused widely along the lateral direction unnecessarily. On the other hand, in the above-described manufacturing method, boron ions of which diffusion coefficient is large, only need to be introduced to a shallower position under the bottom face of the trench 31. In the above-described manufacturing method, it is possible to cause the boron ions, which have been introduced to the shallower position under the bottom face of the trench 31, to be thermally diffused at a desired position under the edge of the bottom face of the trench 31, without causing them to be thermally diffused widely along the depth direction. In addition, in the above-described manufacturing method, it is not necessary to cause the boron ions to be thermally diffused unnecessarily, and hence the activation annealing can be controlled such that the boron ions do not come into contact with the side face 30a of the trench gate 30. The above-described manufacturing method can thereby provide a semiconductor device in which an increase in on-resistance is suppressed.

[0030] Some advantages of the technique disclosed in the present specification are summarized below. Matters described below have independently technical usefulness.

- [0031] The technique disclosed in the present specification may be applied to various kinds of semiconductor devices comprising a trench gate. For example, the technique disclosed in the present specification may be applied to a MOSFET or an IGBT. One embodiment of a semiconductor device disclosed in the present specification may comprise a trench gate and a p-type semiconductor region. The trench gate may extend from one of main surfaces of a semiconductor layer along a depth direction. A configuration of the trench gate may not be especially limited, and a layout of the trench gate may not be especially limited. The p-type semiconductor region may be in contact with a bottom face of the trench gate. The p-type semiconductor region may include a first p-type semiconductor region containing a first type of p-type impurities and a second p-type semiconductor region containing a second type of p-type impurities. The first p-type semiconductor region may be located between the trench gate and the second p-type semiconductor region. An additional semiconductor region may be provided between the first p-type semiconductor region and the bottom face of the trench gate and/or between the first p-type semiconductor region and the second p-type semiconductor region. In a view along the depth direction, the second p-type semiconductor region may be located within a part of the first p-type semiconductor region. A diffusion coefficient of the second type of p-type impurities may be smaller than a diffusion coefficient of the first type of p-type impurities.
- [0032] The first p-type semiconductor region may be in contact with the bottom face of the trench gate, and may project out along a lateral direction from an edge of the bottom face of the trench gate. In this embodiment, an electric field at the edge of the bottom face of the trench gate is relaxed, and a withstand voltage of the semiconductor device is accordingly improved. Further, in this embodiment, it is preferable that a length by which the first p-type semiconductor region projects out along the lateral direction from the edge of the bottom face of the trench gate is equal to or smaller than 0.2 mm. In this embodiment, even if a p-type semiconductor region is provided, an increase in on-resistance of the semiconductor device is suppressed. Further, in this embodiment, it is preferable that the first p-type semiconductor region is not in contact with a side face of the trench gate. In this embodiment also, even if a p-type semiconductor region is provided, an increase in on-resistance of the semiconductor device is suppressed.
- [0033] In a view along the depth direction, the second p-type semiconductor region may be located within a part of the trench gate. In this embodiment, at a deeper position under the bottom face of the trench gate, spreading of the second p-type semiconductor region along the lateral direction is suppressed. Therefore, even if a p-type semiconductor region is provided, a wide current path is ensured and an increase in on-resistance of the semiconductor device is suppressed.
- [0034] A manufacturing method of a semiconductor device disclosed in the present speci-

fication may comprise forming a mask, forming a trench, irradiating a first type of p-type impurities, and irradiating a second type of p-type impurities. In the forming of the mask, the mask is formed on one of main surfaces of a semiconductor layer, wherein an opening is formed in the mask. In the forming of the trench, the trench is formed to extend along a depth direction from the one of main surfaces which is exposed at the opening of the mask. In the irradiating of the first type of p-type impurities, the first type of p-type impurities is irradiated through the opening and toward the trench. In the irradiating of the second type of p-type impurities, the second type of p-type impurities is irradiated through the opening and toward the trench. A performing order in which the irradiating of the first type of p-type impurities and the irradiating of the second type of p-type impurities are performed earlier or later, may not be especially limited. The second type of p-type impurities is introduced to a deeper position under a bottom face of the trench than the first type of p-type impurities. A diffusion coefficient of the second type of p-type impurities is smaller than a diffusion coefficient of the first type of p-type impurities.

[0035] The irradiating of the first type of p-type impurities may be performed prior to the irradiating of the second type of p-type impurities. In this case, the manufacturing method of the semiconductor device may further comprise removing side and bottom faces of the trench, in a state where the mask is maintained, so as to maintain the first type of p-type impurities having been introduced under the bottom face of the trench, wherein the removing is performed between the irradiating of the first type of p-type impurities and the irradiating of the second type of p-type impurities. According to this manufacturing method, in the irradiating of the second type of p-type impurities, the side face of the trench is shield by the mask so that the second type of p-type impurities is prevented from being irradiated to the side face of the trench.

[0036] While specific examples of the present invention have been described above in detail, these examples are merely illustrative and place no limitation on the scope of the patent claims. The technology described in the patent claims also encompasses various changes and modifications to the specific examples described above. The technical elements explained in the present description or drawings provide technical utility either independently or through various combinations. The present invention is not limited to the combinations described at the time the claims are filed. Further, the purpose of the examples illustrated by the present description or drawings is to satisfy multiple objectives simultaneously, and satisfying any one of those objectives gives technical utility to the present invention.

## Claims

- [Claim 1] A semiconductor device comprising:  
a trench gate extending from one of main surfaces of a semiconductor layer along a depth direction; and  
a p-type semiconductor region in contact with a bottom face of the trench gate,  
wherein  
the p-type semiconductor region includes a first p-type semiconductor region containing a first type of p-type impurities, and a second p-type semiconductor region containing a second type of p-type impurities,  
the first p-type semiconductor region is located between the trench gate and the second p-type semiconductor region,  
in a view along the depth direction, the second p-type semiconductor region is located within a part of the first p-type semiconductor region, and  
a diffusion coefficient of the second type of p-type impurities is smaller than a diffusion coefficient of the first type of p-type impurities.
- [Claim 2] The semiconductor device according to claim 1, wherein  
the first p-type semiconductor region is in contact with the bottom face of the trench gate, and projects out along a lateral direction from an edge of the bottom face of the trench gate.
- [Claim 3] The semiconductor device according to claim 2, wherein  
a length by which the first p-type semiconductor region projects out in the lateral direction from the edge of the bottom face of the trench gate is equal to or smaller than 0.2 mm.
- [Claim 4] The semiconductor device according to claim 2 or 3, wherein  
the first p-type semiconductor region is not in contact with a side face of the trench gate.
- [Claim 5] The semiconductor device according to any one of claims 1 to 4, wherein  
in a view along the depth direction, the second p-type semiconductor region is located within a part of the trench gate.
- [Claim 6] A manufacturing method of a semiconductor device, the method comprising:  
forming a mask on one of main surfaces of a semiconductor layer,  
wherein an opening is formed in the mask;  
forming a trench extending along a depth direction from the one of

main surfaces which is exposed at the opening of the mask;  
irradiating a first type of p-type impurities through the opening and  
toward the trench, and  
irradiating a second type of p-type impurities through the opening and  
toward the trench, wherein  
the second type of p-type impurities is introduced to a deeper position  
under a bottom face of the trench than the first type of p-type im-  
purities, and  
a diffusion coefficient of the second type of p-type impurities is smaller  
than a diffusion coefficient of the first type of p-type impurities.

[Claim 7]

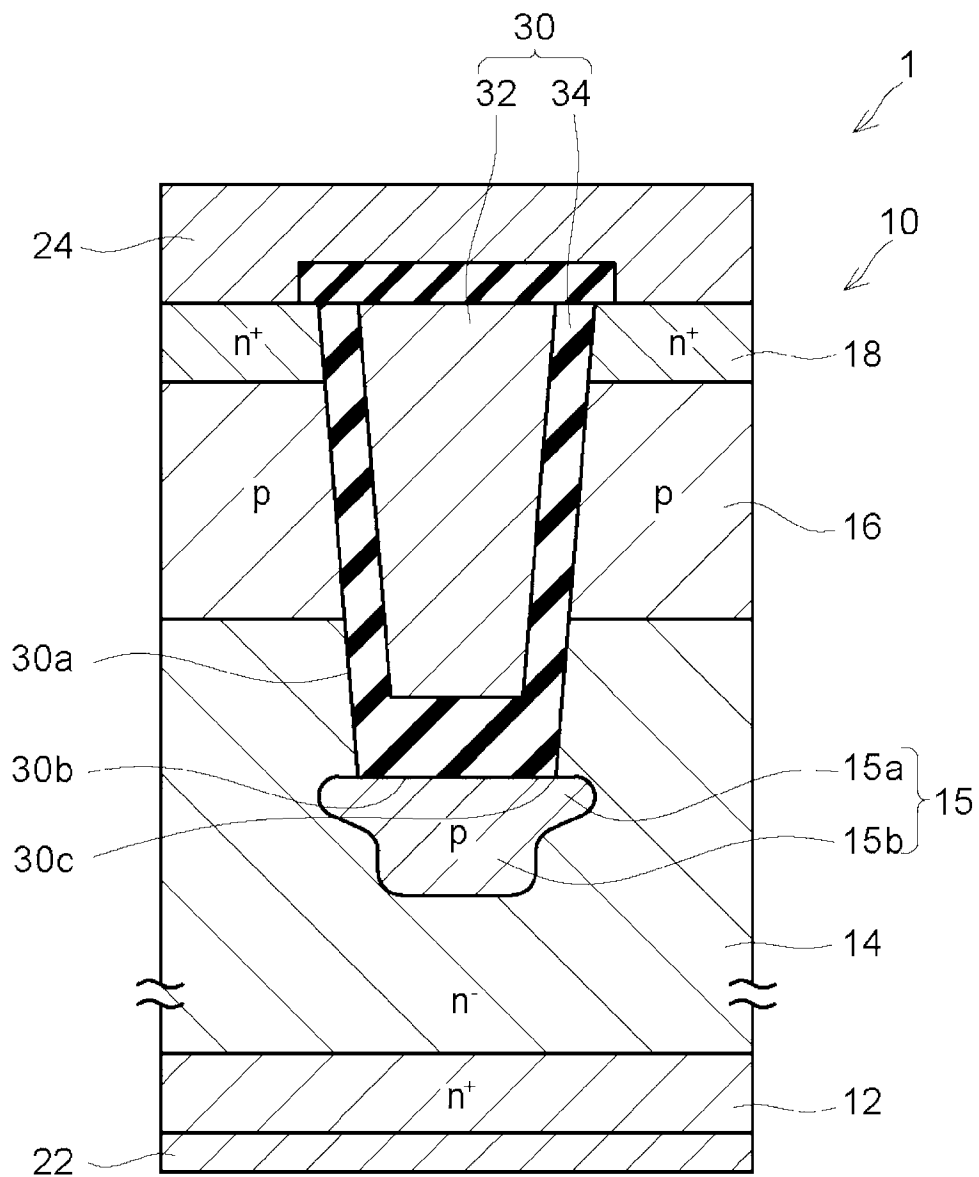
The manufacturing method of the semiconductor device according to  
claim 6, wherein  
the irradiating of the first type of p-type impurities is performed prior to  
the irradiating of the second type of p-type impurities.

[Claim 8]

The manufacturing method of the semiconductor device according to  
claim 7, the method further comprising:  
removing side and bottom faces of the trench, in a state where the mask  
is maintained, so as to maintain the first type of p-type impurities  
having been introduced under the bottom face of the trench, wherein  
the removing is performed between the irradiating of the first type of p-  
type impurities and the irradiating of the second type of p-type im-  
purities.

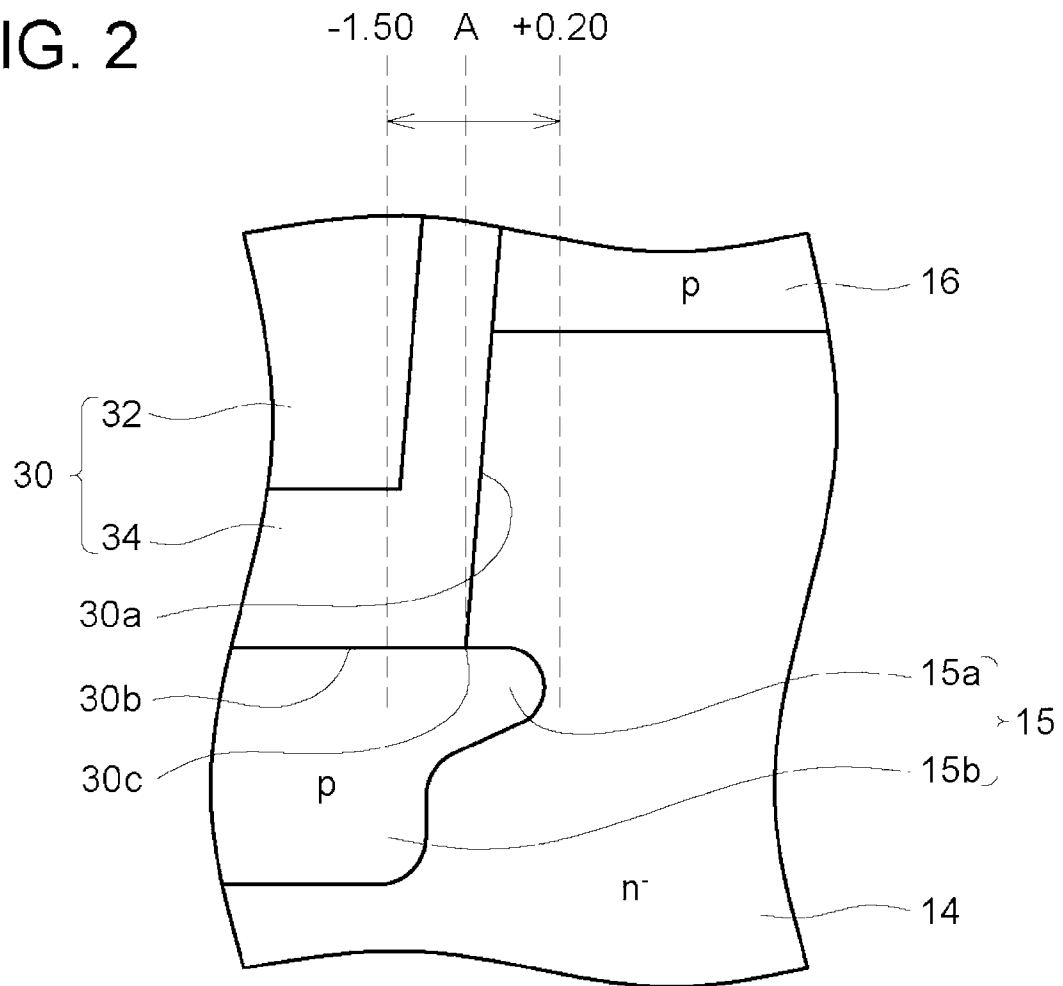
[Fig. 1]

FIG. 1

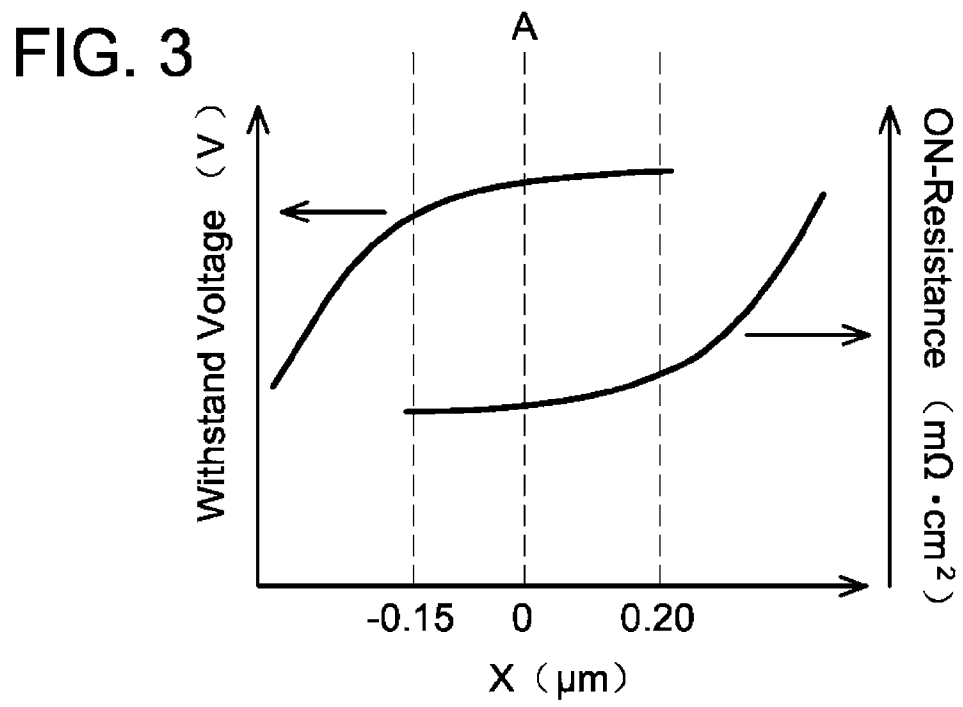


[Fig. 2]

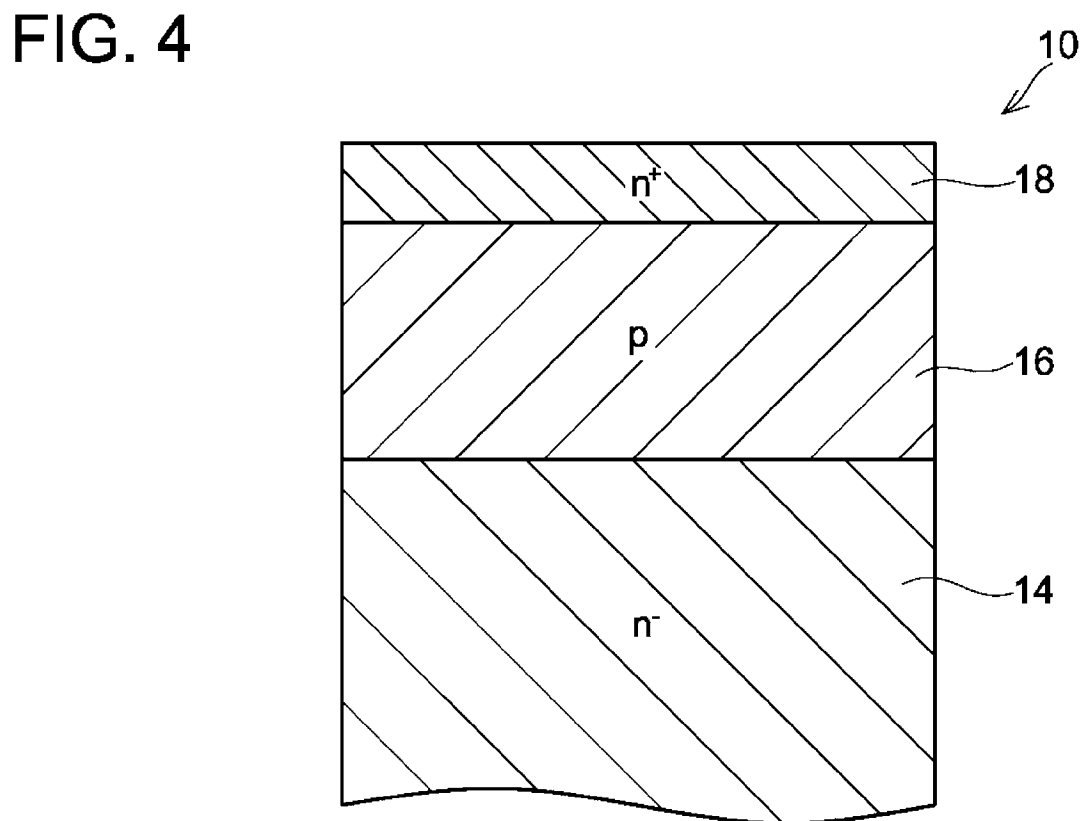
FIG. 2



[Fig. 3]

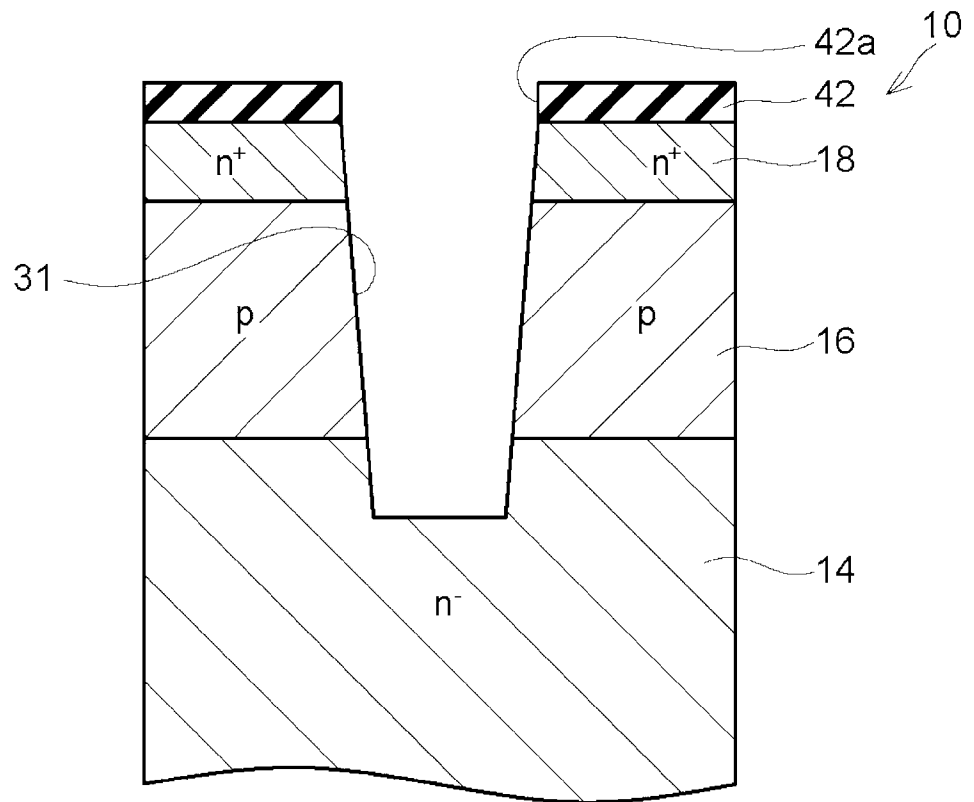


[Fig. 4]



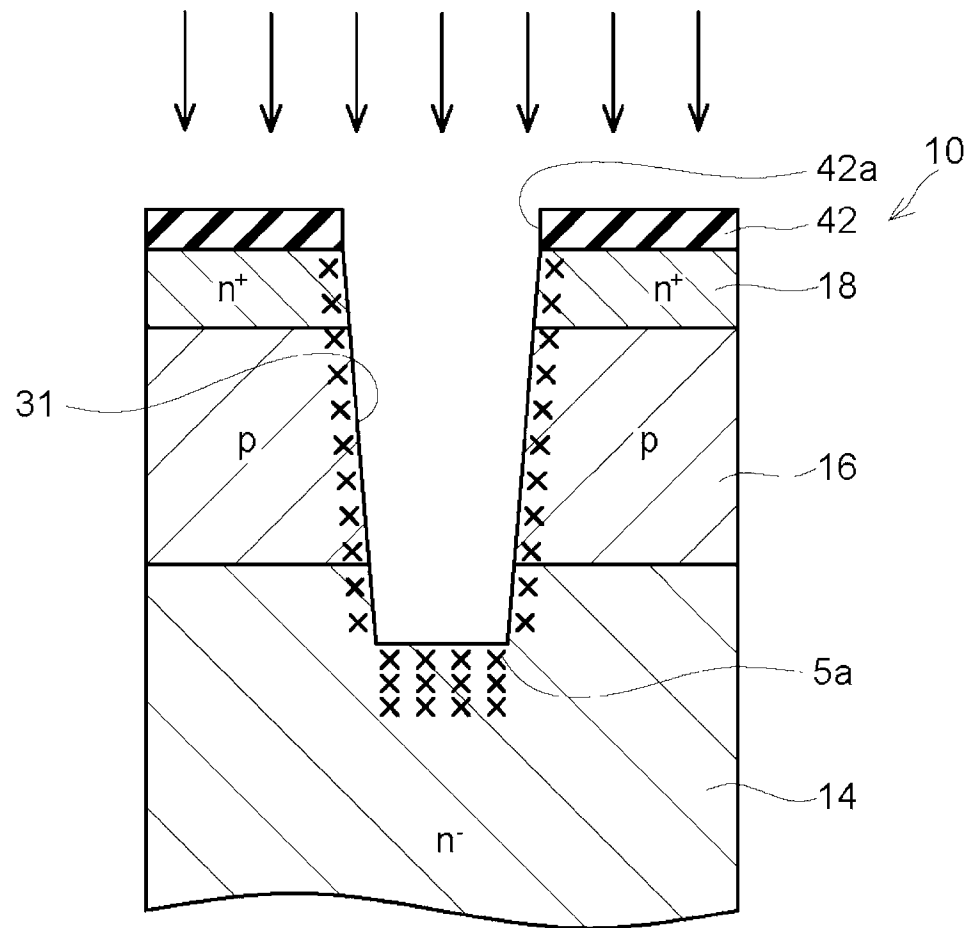
[Fig. 5]

FIG. 5



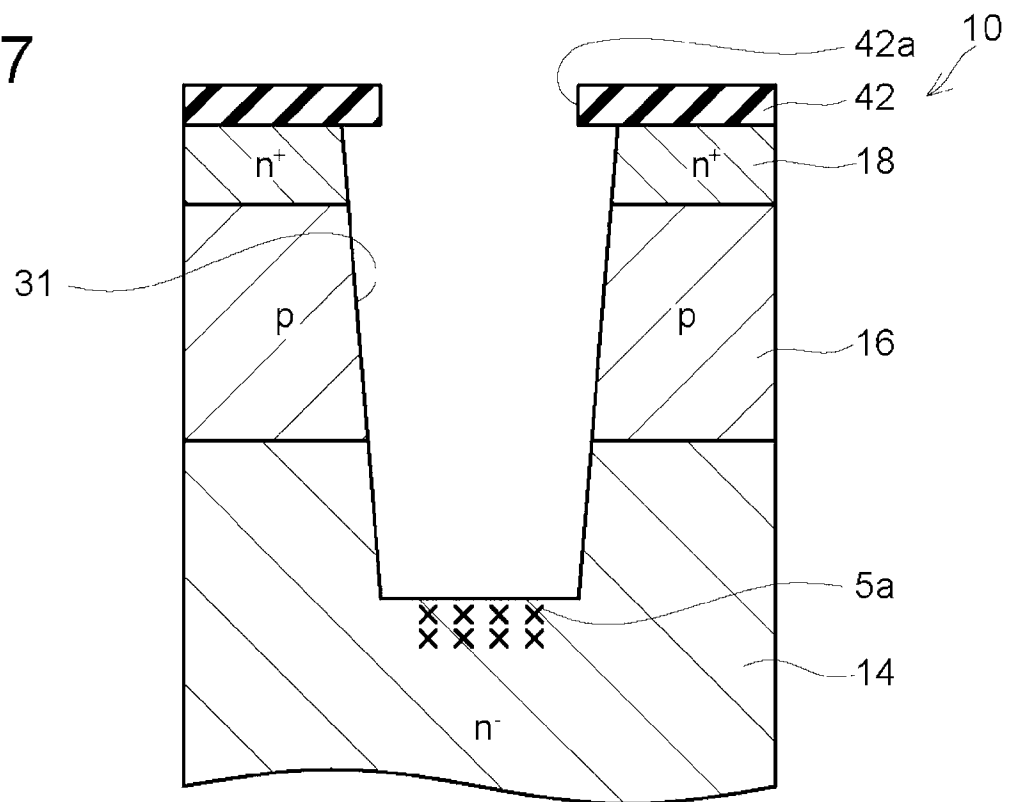
[Fig. 6]

FIG. 6



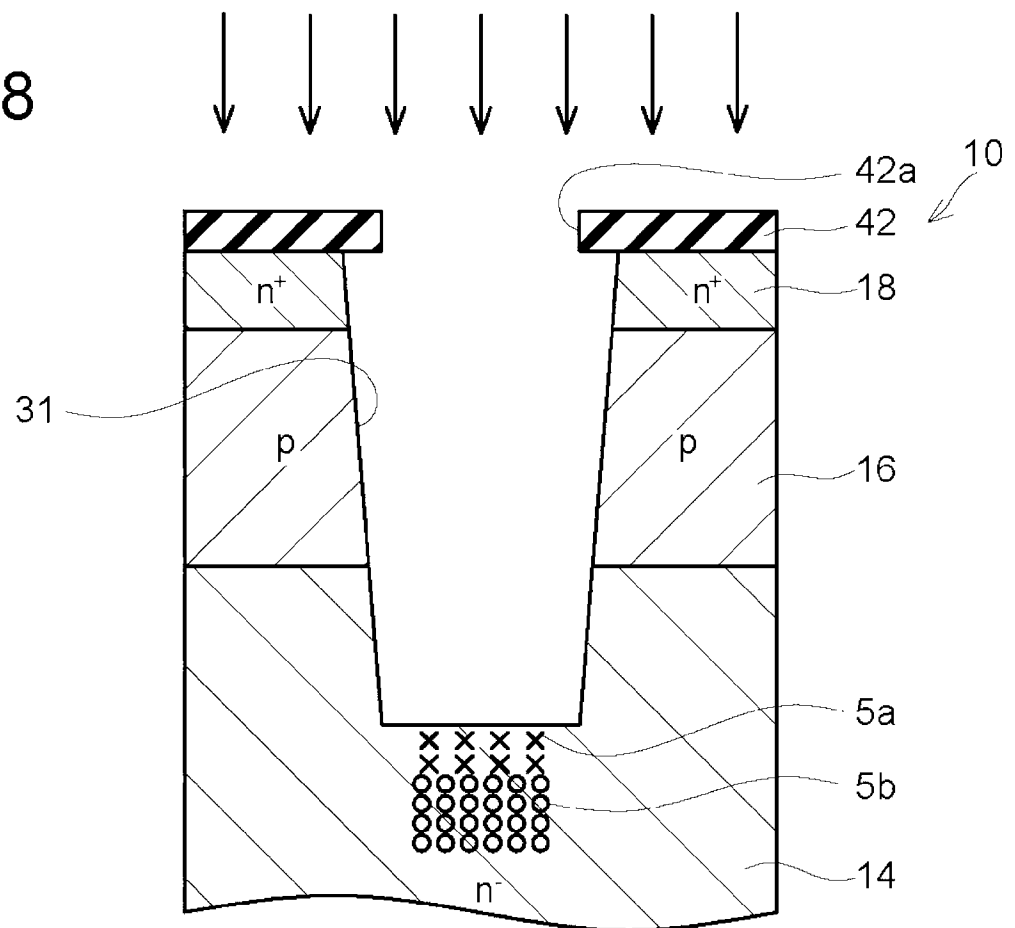
[Fig. 7]

FIG. 7



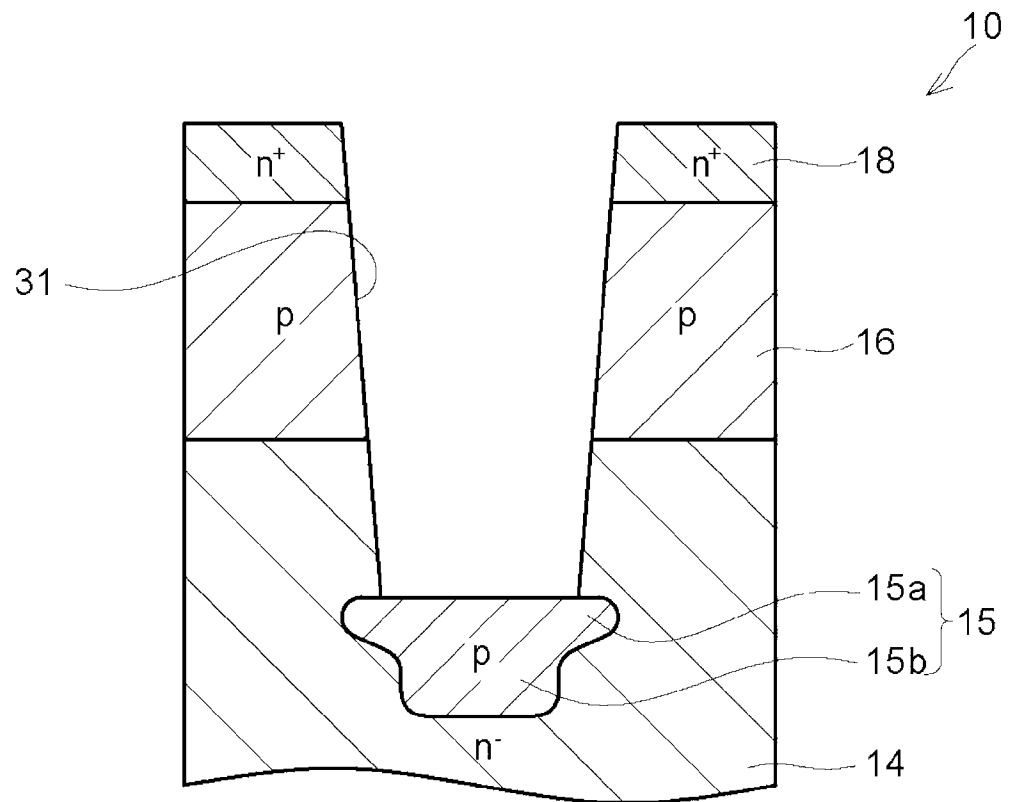
[Fig. 8]

FIG. 8



[Fig. 9]

FIG. 9



## INTERNATIONAL SEARCH REPORT

International application No

PCT/JP2015/006178

## A. CLASSIFICATION OF SUBJECT MATTER

INV. H01L29/78 H01L29/66 H01L29/06 H01L29/739  
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

## B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category* | Citation of document, with indication, where appropriate, of the relevant passages                                                                                                                                                                            | Relevant to claim No. |
|-----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------|
| X         | WO 2014/115280 A1 (TOYOTA MOTOR CO LTD [JP]; TOYOTA CHUO KENKYUSHO KK [JP]; DENSO CORP [J] 31 July 2014 (2014-07-31) abstract; figures 1,2,3,8-11                                                                                                             | 1-5                   |
| Y         | & US 2016/005861 A1 (NISHIMURA SHINYA [JP] ET AL) 7 January 2016 (2016-01-07) paragraph [0008]                                                                                                                                                                | 6                     |
| E         | paragraph [0023] - paragraph [0024]<br>paragraph [0027] - paragraph [0035];<br>figure 1<br>paragraph [0036]; figures 2, 3<br>paragraph [0046] - paragraph [0048];<br>figure 8.9<br>paragraph [0050]; figure 10<br>paragraph [0052]; figure 11<br>-----<br>-/- | 1-5                   |



Further documents are listed in the continuation of Box C.



See patent family annex.

\* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&amp;" document member of the same patent family

Date of the actual completion of the international search

18 March 2016

Date of mailing of the international search report

30/03/2016

Name and mailing address of the ISA/

European Patent Office, P.B. 5818 Patentlaan 2  
NL - 2280 HV Rijswijk  
Tel. (+31-70) 340-2040,  
Fax: (+31-70) 340-3016

Authorized officer

Lantier, Roberta

## INTERNATIONAL SEARCH REPORT

International application No  
PCT/JP2015/006178

| C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT |                                                                                                                                                                                             |                       |
|------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------|
| Category*                                            | Citation of document, with indication, where appropriate, of the relevant passages                                                                                                          | Relevant to claim No. |
| Y                                                    | US 2010/258815 A1 (TARUI YOICHIRO [JP])<br>14 October 2010 (2010-10-14)<br>paragraph [0036] - paragraph [0043];<br>figures 1-5                                                              | 6                     |
| A                                                    | -----<br>US 2009/166730 A1 (OKUNO EIICHI [JP] ET<br>AL) 2 July 2009 (2009-07-02)<br>paragraph [0013] - paragraph [0014]<br>paragraph [0079]; figure 10                                      | 1-8                   |
| A                                                    | -----<br>US 2014/264564 A1 (CHENG LIN [US] ET AL)<br>18 September 2014 (2014-09-18)<br>paragraph [0043] - paragraph [0058];<br>figure 2                                                     | 1-8                   |
| A                                                    | -----<br>WO 99/67825 A2 (CREE RESEARCH INC [US];<br>SUVOROV ALEXANDER V [US]; PALMOUR JOHN W<br>[US];) 29 December 1999 (1999-12-29)<br>page 6, line 29 - page 19, line 23;<br>figures 1A-F | 1-8                   |
| A                                                    | -----<br>US 2011/147766 A1 (TARUI YOICHIRO [JP])<br>23 June 2011 (2011-06-23)<br>the whole document                                                                                         | 1-8                   |
| A                                                    | -----<br>US 2011/272710 A1 (QUICK NATHANIEL R [US]<br>ET AL) 10 November 2011 (2011-11-10)<br>paragraph [0086]; figure 5                                                                    | 1-8                   |
|                                                      | -----                                                                                                                                                                                       |                       |

# INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/JP2015/006178

| Patent document<br>cited in search report | Publication<br>date | Patent family<br>member(s)                                                                                                                                                   | Publication<br>date                                                                                                                      |
|-------------------------------------------|---------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------|
| WO 2014115280 A1                          | 31-07-2014          | CN 105164812 A<br>DE 112013006497 T5<br>JP 5864784 B2<br>TW 201431090 A<br>US 2016005861 A1<br>WO 2014115280 A1                                                              | 16-12-2015<br>05-11-2015<br>17-02-2016<br>01-08-2014<br>07-01-2016<br>31-07-2014                                                         |
| US 2010258815 A1                          | 14-10-2010          | CN 101859706 A<br>DE 102009056453 A1<br>JP 5452062 B2<br>JP 2010245389 A<br>KR 20100112069 A<br>US 2010258815 A1<br>US 2011244643 A1                                         | 13-10-2010<br>11-11-2010<br>26-03-2014<br>28-10-2010<br>18-10-2010<br>14-10-2010<br>06-10-2011                                           |
| US 2009166730 A1                          | 02-07-2009          | DE 102008063128 A1<br>JP 4577355 B2<br>JP 2009158681 A<br>US 2009166730 A1                                                                                                   | 02-07-2009<br>10-11-2010<br>16-07-2009<br>02-07-2009                                                                                     |
| US 2014264564 A1                          | 18-09-2014          | US 2014264564 A1<br>US 2016005837 A1                                                                                                                                         | 18-09-2014<br>07-01-2016                                                                                                                 |
| WO 9967825 A2                             | 29-12-1999          | AU 6238399 A<br>CA 2334339 A1<br>CN 1304546 A<br>EP 1086487 A2<br>JP 2002519851 A<br>JP 2011103482 A<br>KR 100393399 B1<br>US 6100169 A<br>US 6303475 B1<br>WO 9967825 A2    | 10-01-2000<br>29-12-1999<br>18-07-2001<br>28-03-2001<br>02-07-2002<br>26-05-2011<br>31-07-2003<br>08-08-2000<br>16-10-2001<br>29-12-1999 |
| US 2011147766 A1                          | 23-06-2011          | CN 101887854 A<br>DE 102010005625 A1<br>JP 5223773 B2<br>JP 2010267783 A<br>KR 20100123592 A<br>KR 20120126057 A<br>KR 20130026469 A<br>US 2010291762 A1<br>US 2011147766 A1 | 17-11-2010<br>18-11-2010<br>26-06-2013<br>25-11-2010<br>24-11-2010<br>20-11-2012<br>13-03-2013<br>18-11-2010<br>23-06-2011               |
| US 2011272710 A1                          | 10-11-2011          | US 8067303 B1<br>US 2011272710 A1<br>US 2011275174 A1                                                                                                                        | 29-11-2011<br>10-11-2011<br>10-11-2011                                                                                                   |