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(54) Title: METHOD FOR PROVIDING A TARGET LAYER SURROUNDING A VERTICAL NANOSTRUCTURE

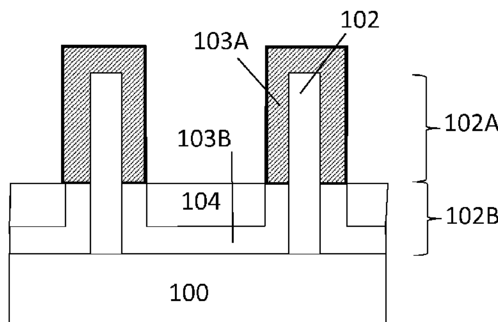

FIG.5

(57) Abstract: A method for providing a target layer surrounding a vertical nanostructure on a substrate surface is disclosed, the method comprising providing a vertical nanostructure extending outwardly from a substrate surface, the vertical nanostructure having a sidewall surface; the sidewall surface having an upper portion and a lower portion; providing a target layer at least along the sidewall surface of the vertical nanostructure and on the substrate surface; providing a protection layer covering the target layer; removing an upper portion of the protection layer, thereby exposing the target layer along the upper portion of the sidewall surface of the vertical nanostructure; thereafter removing the exposed target layer along the upper portion of the sidewall surface of the vertical nanostructure selective towards the protection layer; thereafter removing the remaining protection layer.

METHOD FOR PROVIDING A TARGET LAYER SURROUNDING A VERTICAL NANOSTRUCTURE

Field of the disclosure

[001] The present disclosure relates to a method for providing a target layer surrounding a vertical nanostructure.

State of the art

[002] Over the past decades, aggressive and continuous transistor scaling according to Moore's law has provided ever increasing device performance and density. For advanced (sub-)5nm nodes, to keep the growth pace, several options can be considered in terms of material choices, device architectures and circuits design. The gate-all-around (GAA) nanowire (NW) FET architecture, with the gate fully wrapped around the thin body of the device, is possible in a lateral or vertical configuration and it should allow superior short-channel electrostatics (SCE) control. It can be thought of as the ultimate scaling limit of conventional finFETs and one of the most promising candidates to further support the CMOS roadmap. At the same time, further cells scaling using conventional 2-dimensional (2D) layouts is also becoming more and more challenged by key factors such as the physical limits on gate and contact placement and interconnect routing congestion.

[003] Vertical nanowire (VNW) devices appear particularly well placed to overcome some of these limitations while exhibiting excellent SCE characteristics, but require early process-design cross-disciplinary interactions to address the technological and design challenges/opportunities of moving from a 2D to a 3D layout configuration for CMOS.

[004] In vertical nanowire (VNW) devices, since the gate length (L_{gate}) is defined vertically, it can be relaxed without area penalty, which in turn also allows some relaxation in the nanowire diameter, while keeping optimum short-channel-effects control. Moreover, L_{gate} relaxation can also be an important knob for variability optimization and leakage control, especially critical for instance in scaled SRAMs.

[005] However a vertical device flow, control of the thicknesses of the different layers surrounding the VNWs is key as that will determine L_{gate}, junction profiles (for conventional inversion-mode type of devices) and source/drain areas.

[006] However the current state of the art vertical device flows encounter different problems. One problem is related to the etch-layout dependency of the vertical devices for both wet and dry-etch processes. Another problem which is observed is the non-uniform thickness of the

layers surrounding the vertical nanostructures, which is crucial for defining gate length, junction profiles and source/drain regions.

[007] There is thus a need for new vertical device process flows which solve these disadvantages.

Summary of the disclosure

[008] It is an object of the invention to provide a method for forming a target layer surrounding a vertical nanostructure which is independent of layout dependency and wherein the formed target layer has a uniform thickness which is the target thickness of the final target layer.

[009] The above objectives are accomplished by the method according to embodiments of the present invention.

[0010] Particular and preferred aspects of the invention are set out in the accompanying independent and dependent claims. Features from the dependent claims may be combined with features of the independent claims and with features of other independent claims as appropriate and not merely as explicitly set out in the claims.

[0011] A first aspect relates to a method for providing a target layer surrounding a vertical nanostructure on a substrate surface, the method comprising: providing a vertical nanostructure extending outwardly from a substrate surface, the vertical nanostructure having a sidewall surface; the sidewall surface having an upper portion and a lower portion; providing a target layer along the sidewall surface of the vertical nanostructure and on the substrate surface; the target layer having a target thickness T on the substrate surface; providing a protection layer covering the target layer; the protection layer having an etch rate which is lower than the etch rate of the target layer; removing an upper portion of the protection layer, thereby exposing the target layer along the upper portion of the sidewall surface of the vertical nanostructure and leaving the target layer on the lower portion of the sidewall surface and on the substrate surface covered by the protection layer; thereafter etching the exposed target layer at most until the target thickness T is reached; thereafter removing the remaining protection layer.

[0012] According to embodiments of the present invention etching the exposed target layer comprises etching only the exposed target layer which is present along the upper portion of the sidewall surface of the vertical nanostructure.

[0013] According to embodiments of the present invention etching the exposed target layer comprises etching the exposed target layer which is present along the upper portion and along the lower portion of the sidewalls surface of the vertical nanostructure.

[0014] According to embodiments of the present invention removing an upper portion of the protection layer or removing the remaining protection layer comprises etching back the protection layer isotropically.

[0015] According to embodiments of the present invention etching back isotropically comprises etching with an O_2-based chemistry.

[0016] According to embodiments of the present invention the target layer comprises any of a nitride, amorphous silicon or polysilicon, a dielectric material, a low-k material, a spacer material, a gate stack material.

[0017] According to embodiments of the present invention etching back the exposed target layer comprises a F-based etch chemistry.

[0018] According to embodiments of the present invention the vertical semiconductor nanostructure comprises a conformal liner.

[0019] According to embodiments of the present invention the vertical semiconductor nanostructure forms part of a vertical semiconductor device.

[0020] According to embodiments of the present invention the target layer forms part of a gate stack of the vertical semiconductor device.

Brief description of the drawings

[0021] Figure 1 to 9 schematically illustrates different process steps of the method for providing a target layer surrounding a vertical nanostructure according to different embodiments of the present invention.

[0022] Figure 10 schematically illustrates the flow of different process steps of the method for providing a target layer surrounding a vertical nanostructure according to different embodiments of the present invention.

[0023] Figure 11A-11C show scanning electron microscopy (SEM) images which show the disadvantages and artifacts of target layers deposited in between two vertical nanostructures by using prior-art methods.

[0024] Figure 12-14 show scanning electron microscopy (SEM) images of different process steps of the method for providing a target layer surrounding a vertical nanostructure according to different embodiments of the present invention.

[0025] Any reference signs in the claims shall not be construed as limiting the scope.

[0026] In the different drawings, the same reference signs refer to the same or analogous elements.

Detailed description of the disclosure

[0027] The disclosure will be further elucidated by means of the following detailed description of several embodiments of the disclosure and the appended figures.

[0028] In the following detailed description, numerous specific details are set forth in order to provide a thorough understanding of the disclosure and how it may be practiced in particular embodiments. However, it will be understood that the present disclosure may be practiced without these specific details. In other instances, well-known methods, procedures and techniques have not been described in detail, so as not to obscure the present disclosure. While the present disclosure will be described with respect to particular embodiments and with reference to certain drawings, the disclosure is not limited hereto. The drawings included and described herein are schematic and are not limiting the scope of the disclosure. It is also noted that in the drawings, the size of some elements may be exaggerated and, therefore, not drawn to scale for illustrative purposes.

[0029] The term “comprising”, used in the claims, should not be interpreted as being restricted to the means listed thereafter; it does not exclude other elements or steps. It needs to be interpreted as specifying the presence of the stated features, integers, steps or components as referred to, but does not preclude the presence or addition of one or more other features, integers, steps or components, or groups thereof. Thus, the scope of the expression “a device comprising means A and B” should not be limited to devices consisting only of components A and B.

[0030] “Horizontal” refers to a general direction along or parallel to a primary surface of a substrate, and “vertical” is a direction generally orthogonal thereto. “Horizontal” and “vertical” are used as generally perpendicular directions relative to each other independent of the orientation of the substrate in the three-dimensional space.

[0031] In the following, certain embodiments will be described with reference to a silicon (Si) substrate, but it should be understood that they apply equally well to other semiconductor substrates. In embodiments, the “substrate” may include a semiconductor substrate such as e.g. a silicon, a germanium (Ge), or a silicon germanium (SiGe) substrate, a gallium arsenide (GaAs), a gallium arsenide phosphide (GaAsP), an indium phosphide (InP),. The “substrate” may include for example, an insulating layer such as a SiO_2 or a Si_3N_4 layer in addition to a semiconductor substrate portion. Thus, the term substrate also includes silicon-on-glass, silicon-on-sapphire substrates. The term “substrate” is thus used to define generally the elements for layers that underlie a layer or portions of interest. Also, the “substrate” may be any other base on which a layer is formed, for example a glass or metal layer. Accordingly a substrate may be a wafer such

as a blanket wafer or may be a layer applied to another base material, e.g. an epitaxial layer grown onto a lower layer.

[0032] Whenever there is referred to a nanostructure this may be regarded as a structure which is defined by a height H, a width or diameter W and a length L for which at least a cross-sectional dimension (for example a height or/and a width or/and a diameter) is less than 20nm, more preferably less than 10nm. The aspect ratio (length versus width of the nanostructure) is preferably greater than 10, more preferably greater than 100, or even more preferably greater than 1000. Exemplary embodiments of a nanostructure may be an elongated nanostructure such as a nanosheet or a nanowire. Other terms which are often used as examples for a nanostructure are nanopillar, nanorod, nanocolumn, nanocone. Further exemplary embodiments of a nanostructure may be fin-type structures, which are analogue to a nanosheet however with greater cross-sectional dimensions.

[0033] Figure 1 to 9 show the process according to certain embodiments of the invention. The process or manufacturing method comprises providing a substrate 100 comprising a vertical nanostructure extending outwardly from the substrate surface 101. The substrate 100 has a substrate surface 101 as shown in FIG 1, from which a vertical nanostructure 102 is extending. The substrate comprises at least one vertical nanostructure. The substrate may thus comprise more than one vertical nanostructure, for example two vertical nanostructures as shown as an example in FIG. 1. In FIG. 2 a top view of FIG. 1 is shown for a nanostructure having a circular sidewall surface (such as for example a nanowire or nanotube) (FIG. 2A) and for a nanostructure having a rectangular sidewall surface (such as for example a nanosheet or a fin-like structure) (FIG. 2B).

[0034] According to embodiments the vertical nanostructure may comprise a vertical nanowire. Vertical nanowires may be formed by different techniques known for a person skilled in the art depending also which is the targeted application. For example for the application of vertical nanowire devices such as vertical field-effect transistors VFETs, the device integration involves a channel-first or channel-last process flow. For the first case for example a down-top approach may be used wherein the vertical nanowire is defined with the use of 193nm immersion lithography followed by a dry-etch process, strip and clean. An alternative way for forming vertical nanowires is a bottom-up approach wherein the nanowire is selectively grown on an oxide template defined by advanced patterning. In the channel-last route, a hole with vertical sidewalls is etched through a sandwich stack after which selective epitaxial growth (SEG) followed by chemical mechanical polishing (CMP) is used to fill the hole. This approach is quite attractive in terms of the simplicity and process control as it allows for the definition of the gate

stack with a replacement metal gate (RMG) scheme, a module which enables further options for device fabrication such as decoupling the gate module from the doping/series resistance optimization for the top part of the NW.

[0035] Still another method for forming vertical nanowires involves vapour-liquid-solid (VLS) method which comprises a formation of metal catalyst nanodots and thereafter vertical nanowire growth by vapour-liquid-solid (VLS) from the metal catalyst and thereafter removing the metal catalyst.

[0036] The at least one vertical nanostructure has a sidewall surface. The sidewall surface shape may be circular for example for a vertical nanowire or a vertical nanotube or may be rectangular for example for a nanosheet or a fin-like structure. An upper portion 102A and a lower portion 102B of the vertical nanostructure and respectively an upper portion and a lower portion of the sidewall surface of the vertical nanostructure are defined.

[0037] The distance or spacing between different nanostructures is often referred to as the pitch P. Depending on the application the pitch may differ and different layouts are possible for the vertical nanostructures. For example for FET applications small pitch (for example below 100nm depending of the targeted technology node) is required, whereas for example for single-photon source applications a larger pitch (larger than 1 micrometer) may be used.

[0038] It is an advantage of the method for providing a target layer surrounding a vertical nanostructure on a substrate according to embodiments of the present invention that independent of the layout, otherwise said independent of the pitch in between different vertical nanostrucures a uniform target layer may be provided, which means having a uniform thickness along the substrate surface. With uniform thickness is meant that the thickness variation of the target layer is low, which means having a uniformity defined by the specifications of the deposition technique used for depositing the target layer. For example layers deposited using atomic layer deposition (ALD) are known to have excellent uniformity and conformality.

[0039] It is an advantage of the method for providing a target layer surrounding a vertical nanostructure on a substrate according to embodiments of the present invention wherein an initial target layer is first formed and after providing the method according the embodiments of the present invention a final target layer is formed wherein the thickness of the final target layer present in between the vertical nanostructure along the substrate surface is equal to the initial thickness of the initial target layer.

[0040] According to embodiments the vertical nanostructure is a vertical semiconductor nanostructure. The vertical semiconductor nanostructure may comprise a semiconductor

material such as for example Si, SiGe, III-V material or other semiconductors well-known for a person skilled in the art.

[0041] The vertical semiconductor nanostructure may comprise one or more regions such as for example a channel region, a source/drain region which may be doped or undoped.

[0042] The at least one vertical nanostructure is extending outwardly or protruding from the substrate surface. This means that the vertical nanostructure is surrounded by the substrate surface.

[0043] As shown in FIG. 3 a target layer 103, also referred to the as-formed target layer, is provided on the vertical nanostructure 102 and on the substrate surface 101, more specifically along the sidewall surface of the vertical nanostructure 102 and on the substrate surface 101. More precisely the target layer 103 is provided in a manner such that the as-formed thickness T of the target layer on the substrate surface (i.e. aside of the vertical nanostructure) is uniform along the substrate surface. The thickness of the as-formed target layer on the substrate surface is defining the final thickness T of the final target layer after providing all the steps for the method according to embodiments of the invention. The final thickness is thus the same as the initial thickness T of the as-formed target layer Along the sidewall surface some non-uniformity is accepted as the final target layer 103B, 103C will be that part of the as-formed target layer 103 which is present aside of the vertical nanostructure 102 on the substrate surface and not the part of the as-formed target layer 103 which is present along the sidewall of the nanostructure. However preferably the target layer is provided with a uniform thickness and conformal along the vertical nanostructure and the substrate surface. For example for a dense pitch in between the vertical nanostructures a good control of the thickness of the target layer 103 is needed in between the vertical nanostructures. Therefore conformal deposition techniques such as atomic layer deposition (ALD) are preferred. For more relaxed pitch the target layer is not necessary conformal along the patterned structure, but at least that part of the target layer along the substrate surface in between the vertical nanostructures should have uniform thickness.

[0044] After providing the target layer (the as-formed target layer) 103 a protection layer 104 is provided covering the as-formed target layer 103. Depending on the material of the vertical nanostructure 102 a different protection layer 104 may be chosen. According to embodiments the protection layer may comprise a resist material. This is for example advantageous for Si-comprising vertical nanostructures (which may further comprise an oxide liner) as the process parameters such as etch chemistries, deposition parameters for resist are well-known. According to alternative embodiments the protection layer may comprise an oxide. This may be

advantageous for III-V-comprising vertical nanostructures as an oxide liner is not needed in this case. According to alternative embodiments the protection layer may comprise a spin-coating material such as spin-on-glass (SOG) or spin-on-carbon (SOC).

[0045] According to embodiments the etch rate of the protection layer 104 is preferably lower than the etch rate of the target layer.

[0046] After providing the protection layer 104, upper portion of the protection layer 104 is removed, thereby exposing the target layer 103 along the upper portion 102A of the sidewall surface of the vertical nanostructure 102 (also referred to as the exposed target layer 103A) and leaving the target layer 103 along the lower portion 102B of the sidewall surface of the vertical nanostructure 102 unexposed (and thus covered by the protection layer 104) and leaving the target layer 103 on the surrounding substrate surface 101 unexposed (and thus covered by the protection layer 104). The unexposed part of the target layer 103 may be referred to as the unexposed target layer 103B, 103C as shown in FIG. 6,7.

[0047] According to embodiments of the present invention removal of upper portion of the protection layer 104 may comprise etching upper portion of the protection layer 104. For example an O_2-based etch chemistry may be used to isotropically etch-back a protection layer 104 comprising a resist material.

[0048] According to embodiments the removing of an upper portion of the protection layer 104 comprises removing an upper portion having a predetermined thickness of the protection layer. The thickness is determined based on the possible selectivity to the protection layer in the folllowing removal step (i.e. removal of an upper portion of the target layer).

[0049] After removing an upper portion of the protection layer 104, the exposed target layer 103B is etched. The exposed target layer 103 may be etched until the thickness T as this is the final thickness of the target layer to be achieved. The target layer is thus etched towards the protection layer 104. As a result only a bottom portion of the target layer 103B, 103C remains present. Depending on the material comprised in the target layer and in the protection layer a specific etch chemistry may be used as known for a person skilled in the art.

[0050] As an example wherein a target layer comprising SiN is formed and wherein the protection layer comprises a resist material, upper portion of the SiN layer may be removed selective to the resist using an F-based chemistry such as SF6 or NF3-based chemistry.

[0051] Etching the exposed target layer 103B has the effect that the final thickness or height of the final target layer is set in the area uncovered with the protection layer. FIG. 6 shows a possible embodiment wherein an upper portion of the target layer 103A is removed thereby defining the final target layer which comprises part of the target layer which is uniform along

the substrate surface and an lower portion of the target layer still present along the lower portion of the sidewall surface of the vertical nanostructure 102B. FIG. 7 shows another possible embodiment wherein a further portion of the unexposed target layer 103B is removed, more specifically the portion of the target layer still present along the lower portion of the sidewall surface of the vertical nanostructure, which is portion of the unexposed target layer which is present in between the protection layer and the vertical nanostructure. This results in a final target layer 103C which only comprises that part of the as-formed target layer which is uniformly present along the substrate surface.

[0052] After etching the exposed target layer, the remaining protection layer 104 is removed thereby resulting in the final target layer 103B, 103C having a uniform thickness in between the vertical nanostructures as shown in FIG. 8 and FIG. 9 for different alternative embodiments of the present invention.

[0053] Experimental results

[0054] In a vertical device flow, control of the thicknesses of the different layers surrounding the nanowire (NW) pillars is key as that will determine L_{gate}, junction profiles (for conventional inversion-mode type of devices) and S/D areas. FIG. 11A-11C illustrate some of the challenges faced when etching-back layers in-between NW pillars on the wafer, such as oxide or nitride (FIG. 11A), after their deposition and planarisation by chemical mechanial polishing (CMP): considerable etch-layout dependences for both wet (FIG. 11B) and dry-etch (FIG. 11C) processes are observed, preventing realization of pillars with layers of well-defined thickness surrounding them. This can be observed in the irregularities of the thickness profile in between the NW pillars as shown in FIG. 11B as well as thickness variation at the sidewall of the NW pillars as shown in FIG. 11C. To overcome these issues, the alternative approach according to embodiments of the present invention providing a target layer, otherwise said for (partially) etching-back (target) layers which is schematically illustrated in FIG. 10. It ensures that the thickness of the target layer obtained around the pillars is essentially its as-deposited thickness, everywhere on the wafer, independently of the maskset layout used. This scheme comprises according to an example according to embodiments of the present invention of the following steps (FIG. 10):

[0055] 1) starting from vertical NW pillars (with or without a hard-mask on top), a thin-oxide liner and a nitride layer are deposited on the wafer;

[0056] 2) a 248nm litho resist is coated on the wafer;

[0057] 3) the resist is etched-back isotropically using an O_2-based plasma, stopping at a targeted resist thickness ($t_{target,resist}$) in the areas in-between pillars, and with $t_{target,resist}$ determined by the etch selectivity towards resist during the next etch step;

[0058] 4) an isotropic etch is performed to etch-back the nitride layer (30,31) in areas not covered by resist (using a F-based chemistry) and set its final height or thickness there;

[0059] 5) the resist is removed by a O_2/N_2-based strip; and finally 6) the exposed part of the oxide liner can be removed with a short diluted HF (dHF) or a siconi/dHF process.

[0060] Examples of scanning electron microscopy (SEM) images at different stages of this process scheme are shown in FIGS 12-14. FIG. 12 shows a SEM image after resist coating. FIG. 14 shows a SEM image after nitride etch (removal of upper portion of the target layer) and FIG. 15 shows a SEM image of a zoom of 2 NW pillars after strip of the resist (i.e. removal of the remaining protection layer) thereby having formed a SiN layer in between the NW pillars with uniform thickness and without any irregularities or thickness variations.

CLAIMS

1. A method for providing a target layer surrounding a vertical nanostructure on a substrate surface, the method comprising:
   - providing a vertical nanostructure extending outwardly from a substrate surface, the vertical nanostructure having a sidewall surface; the sidewall surface having an upper portion and a lower portion;
   - providing a target layer along the sidewall surface of the vertical nanostructure and on the substrate surface; the target layer having a target thickness T on the substrate surface;
   - providing a protection layer covering the target layer; the protection layer having an etch rate which is lower than the etch rate of the target layer;
   - removing an upper portion of the protection layer, thereby exposing the target layer along the upper portion of the sidewall surface of the vertical nanostructure; thereafter
   - etching the exposed target layer at most until the target thickness T is reached; thereafter
   - removing the remaining protection layer.

2. A method according to claim 1, wherein etching the exposed target layer comprises etching only the exposed target layer which is present along the upper portion of the sidewall surface of the vertical nanostructure.

3. A method according to claim 1, wherein etching the exposed target layer comprises etching the exposed target layer which is present along the upper portion and along the lower portion of the sidewalls surface of the vertical nanostructure.

4. A method according to any of the preceding claims wherein removing an upper portion of the protection layer or removing the remaining protection layer comprises etching back the protection layer isotropically.

5. A method according to claim 4 wherein etching back isotropically comprises etching with an O_2-based chemistry.

6. A method according to any of the preceding claims wherein the target layer comprises any of a nitride, amorphous silicon or polysilicon, a dielectric material, a low-k material, a spacer material, a gate stack material.

7. A method according to any of the preceding claims etching back the exposed target layer comprises a F-based etch chemistry.

8. A method according to any of the preceding claims wherein the vertical semiconductor nanostructure comprises a conformal liner.

9. A method according to any of the preceding claims wherein the vertical semiconductor nanostructure forms part of a vertical semiconductor device.

10. A method according to claim 9 wherein the target layer forms part of a gate stack of the vertical semiconductor device.

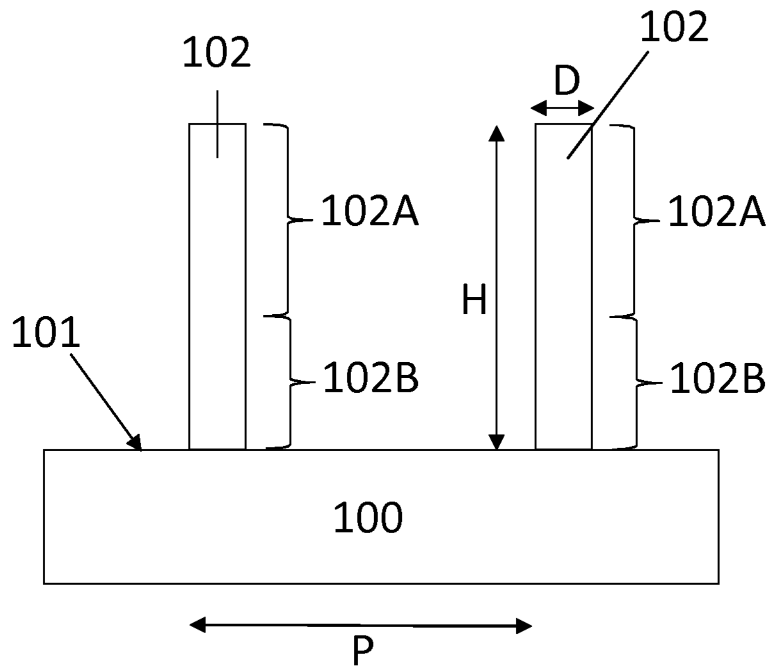

FIG.1

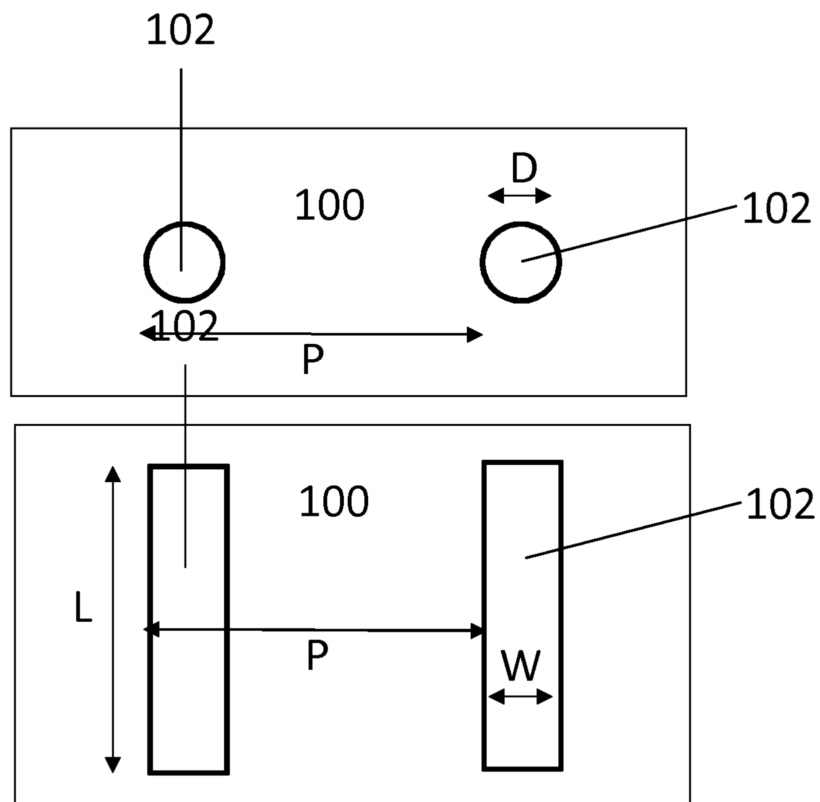

FIG.2

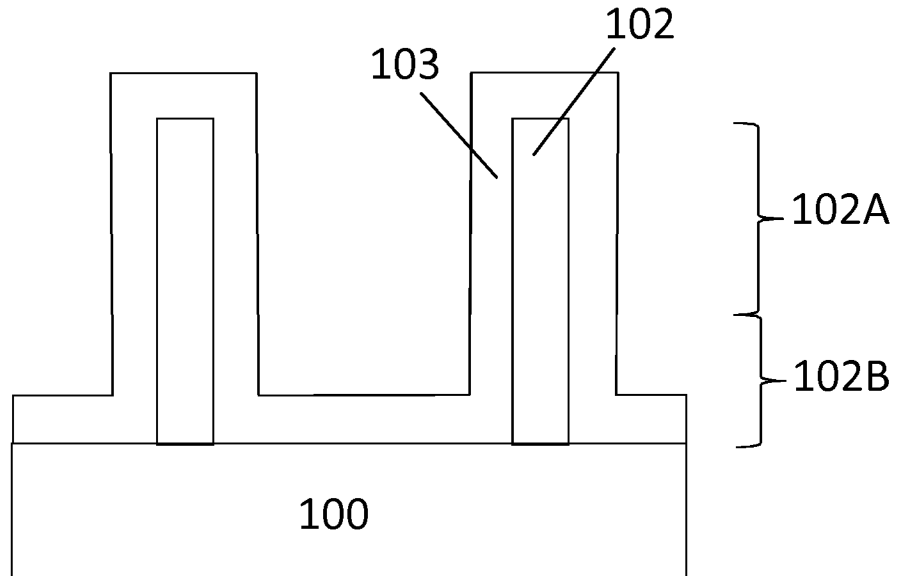

FIG.3

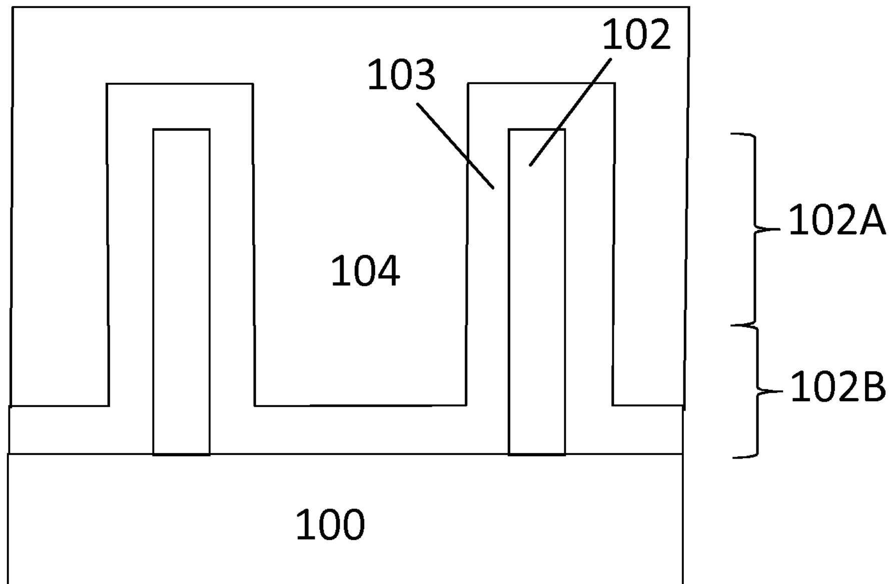

FIG.4

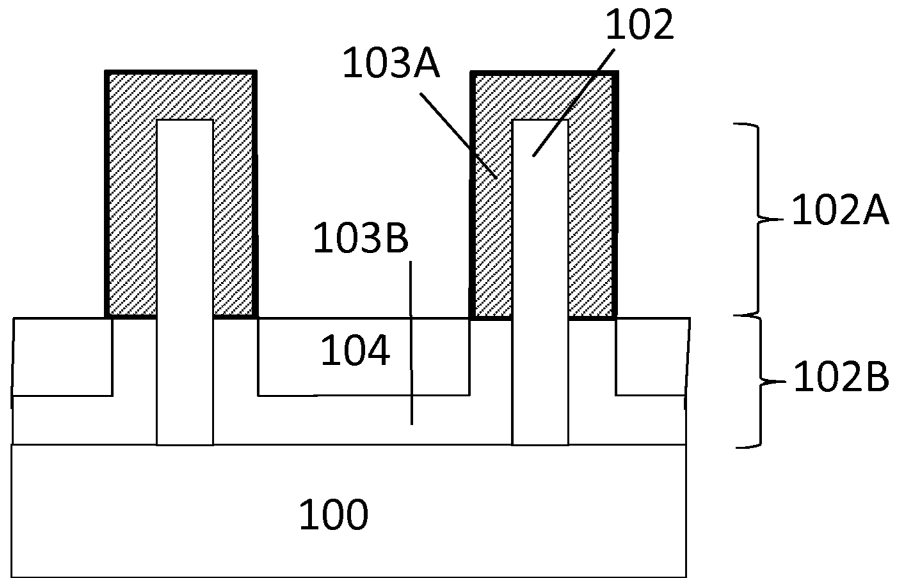

FIG.5

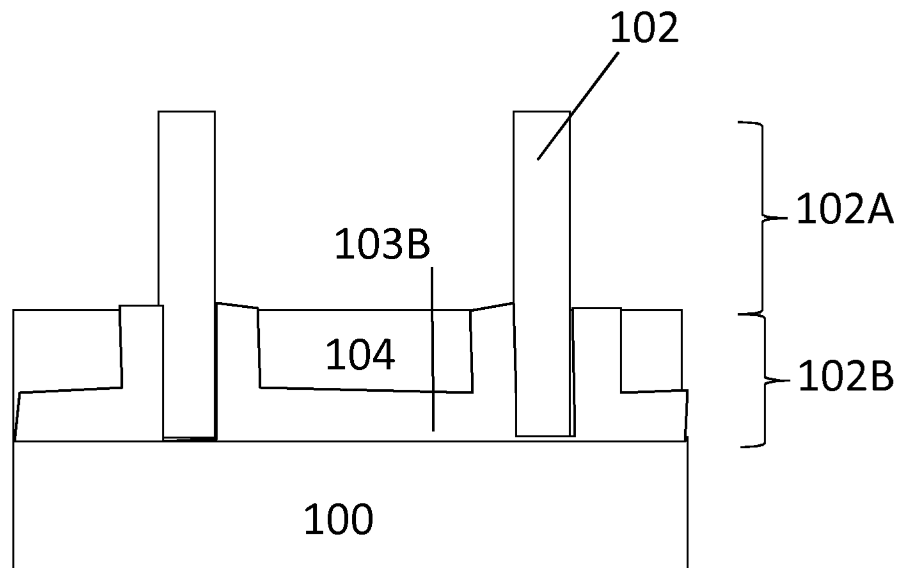

FIG.6

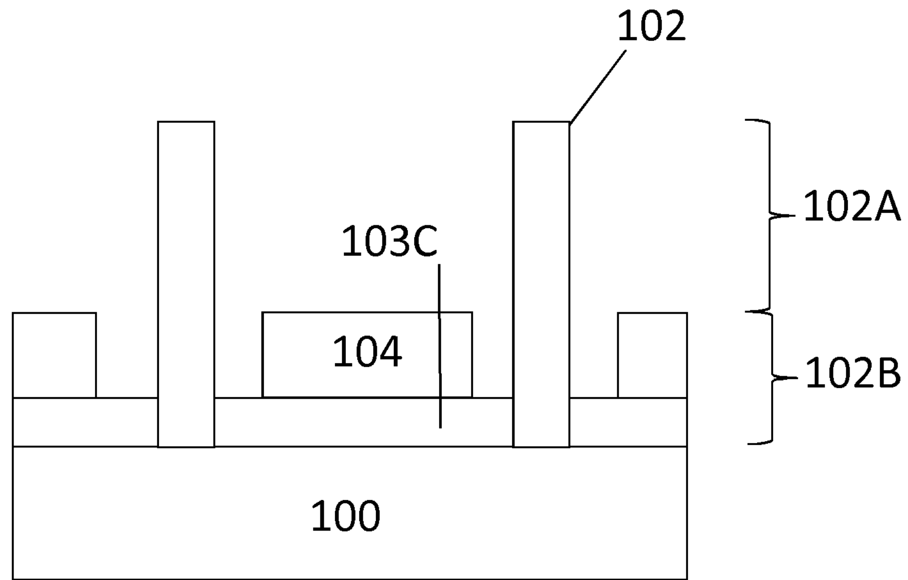

FIG. 7

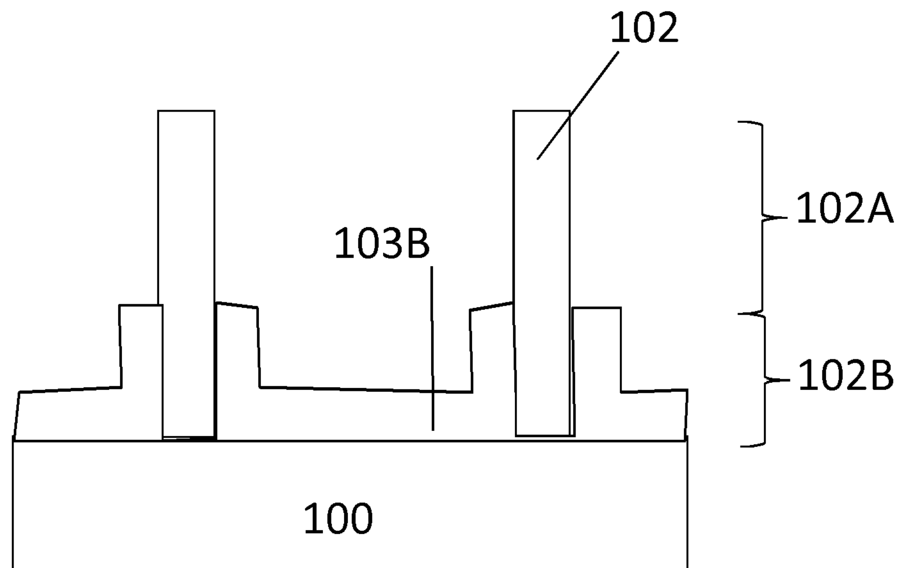

FIG.8

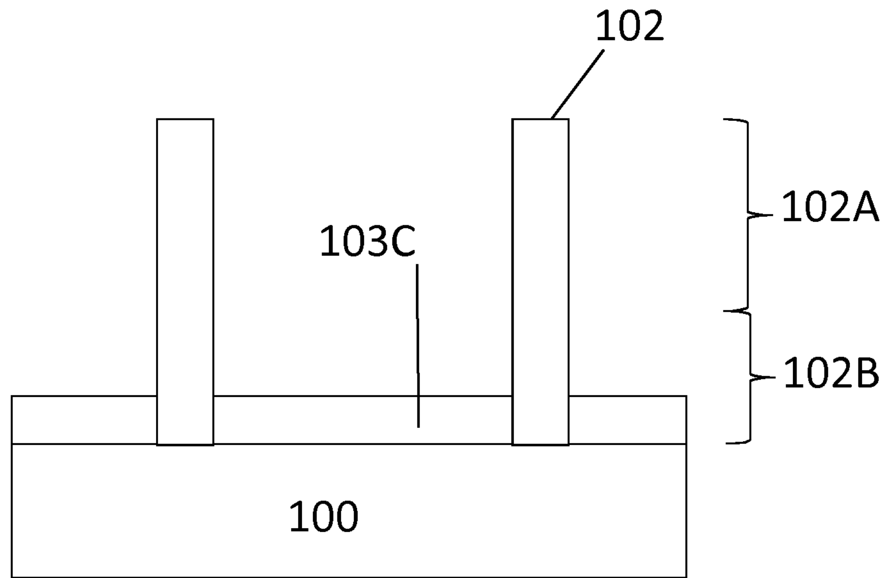

FIG. 9

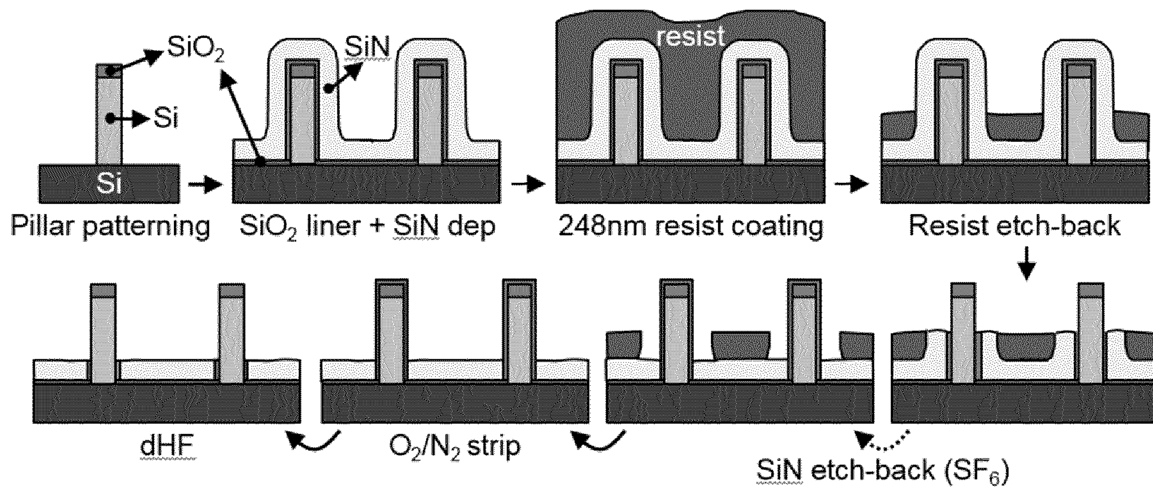

FIG. 10

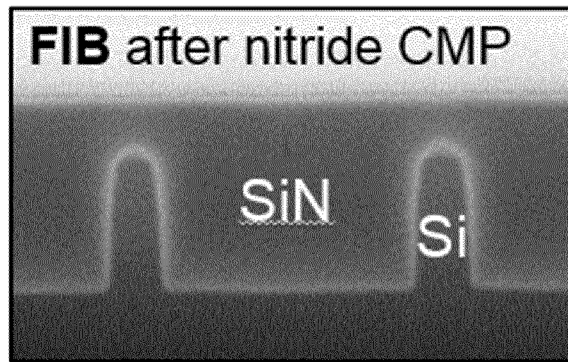

FIG. 11A

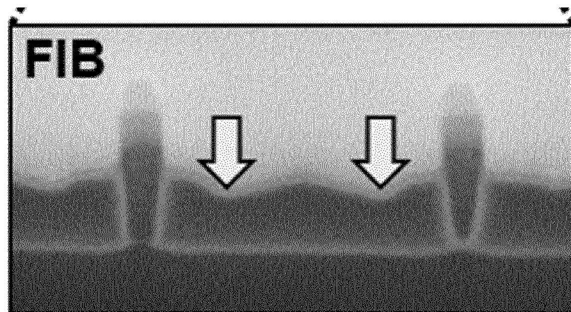

FIG. 11B

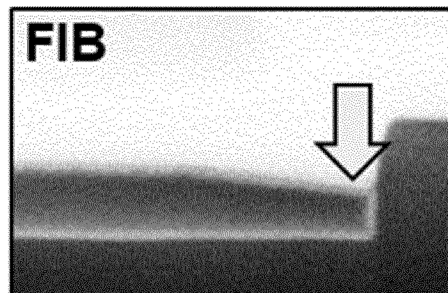

FIG. 11C

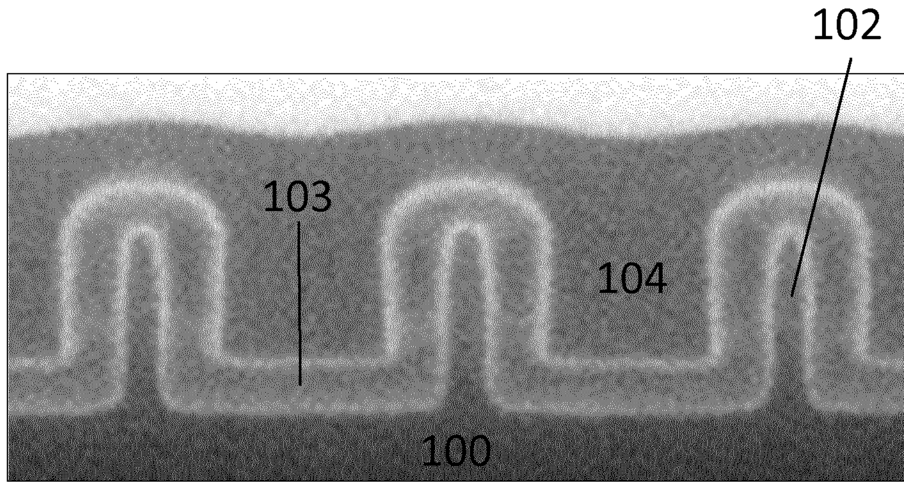

FIG. 12

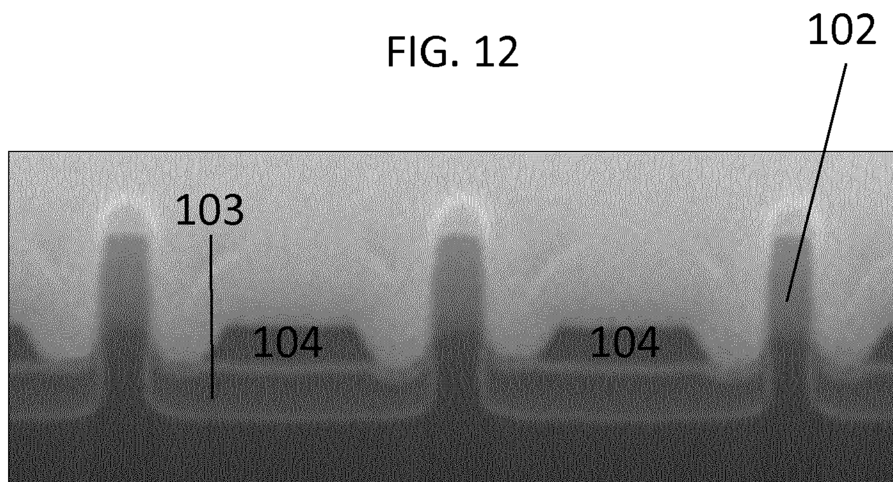

FIG. 13

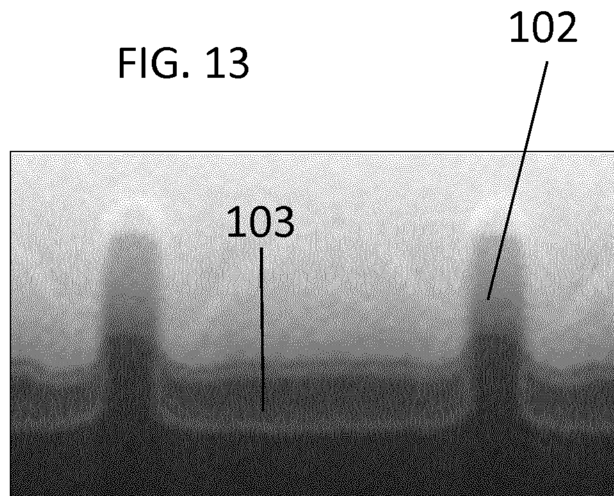

FIG. 14

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2017/054465

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L21/311 H01L29/06
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, INSPEC, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	B YANG ET AL: "CMOS compatible Gate-All-Around Vertical silicon-nanowire MOSFETs", 2014 44TH EUROPEAN SOLID STATE DEVICE RESEARCH CONFERENCE (ESSDERC), 18 November 2008 (2008-11-18), pages 318-321, XP055370707, ISSN: 1930-8876, DOI: 10.1109/ESSDERC.2008.4681762 ISBN: 978-1-4799-4378-4 II.NANOWIRE FORMATION AND DEVICE FABRICATION; figures 1,2,3 -----	1,2,4-10
X	US 2015/372140 A1 (LIU QING [US] ET AL) 24 December 2015 (2015-12-24) paragraphs [0076] - [0108]; figures 4,5A-10A -----	1-9
	-/--	

[X] Further documents are listed in the continuation of Box C. [X] See patent family annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
10 May 2017	19/05/2017

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Szarowski, Anne

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C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 2 180 314 A1 (STICHTING IMEC NEDERLAND [NL]) 28 April 2010 (2010-04-28) paragraphs [0027] - [0037] paragraphs [0038] - [0041], [0053]; figures 4a-4i; example I -----	1,2,4-10
X	US 2014/225184 A1 (COLINGE JEAN-PIERRE [TW] ET AL) 14 August 2014 (2014-08-14) paragraphs [0014] - [0018], [0025]; figures 1A-1H, 1Q -----	1,3-10

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/EP2017/054465

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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		US 2010176822 A1	15-07-2010
US 2014225184 A1	14-08-2014	KR 101423429 B1	24-07-2014
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		US 2016268427 A1	15-09-2016