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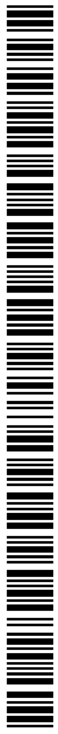

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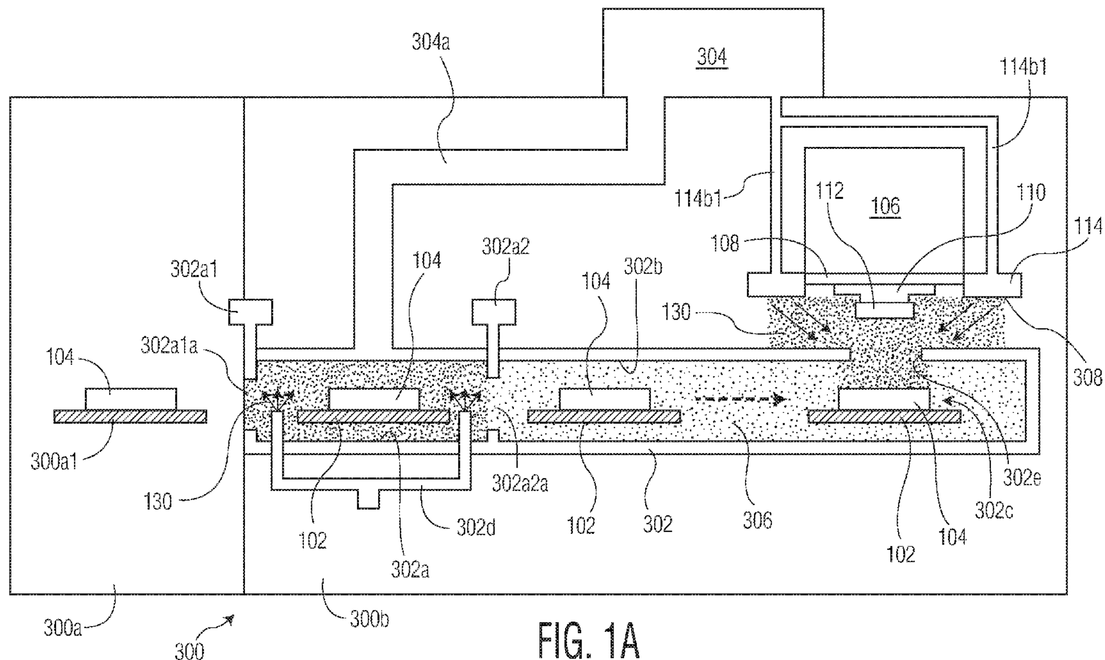

FIG. 1A

(57) Abstract: A bonding system for bonding a semiconductor element to a substrate is provided. The bonding system includes a substrate oxide reduction chamber configured to receive a substrate. The substrate includes a plurality of first electrically conductive structures. The substrate oxide reduction chamber is configured to receive a reducing gas to contact each of the plurality of first electrically conductive structures. The bonding system also includes a substrate oxide prevention chamber for receiving the substrate after the reducing gas contacts the plurality of first electrically conductive structures. The substrate oxide prevention chamber has an inert environment when receiving the substrate. The bonding system also includes a reducing gas delivery system for providing a reducing gas environment during bonding of a semiconductor element to the substrate.

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METHODS OF BONDING OF SEMICONDUCTOR ELEMENTS TO SUBSTRATES, AND RELATED BONDING SYSTEMS

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the benefit of U.S. Provisional Application No. 62/790,259, filed January 9, 2019, and of U.S. Provisional Application No. 62/907,562, filed September 28, 2019, the contents of both of which are incorporated herein by reference.

FIELD

[0002] The invention relates to bonding systems and processes (such as flip chip, thermocompression, and thermosonic bonding systems and processes), and more particularly, to improved systems and methods for bonding a semiconductor element to a substrate.

BACKGROUND

[0003] Traditional semiconductor packaging typically involves die attach processes and wire bonding processes. Advanced semiconductor packaging technologies (e.g., flip chip bonding, thermocompression bonding, etc.) continue to gain traction in the industry. For example, in thermocompression bonding (i.e., TCB), heat and/or pressure (and sometimes ultrasonic energy) are used to form a plurality of interconnections between (i) electrically conductive structures on a semiconductor element and (ii) electrically conductive structures on a substrate.

[0004] In certain flip chip bonding or thermocompression bonding applications, the electrically conductive structures of the semiconductor element and/or the substrate may include copper structures (e.g., copper pillars) or other material(s) that is subject to oxidation and/or other contamination. In such applications, it is desirable to provide an environment suitable for bonding. Conventionally, such an environment may be provided by using a reducing gas at the bonding area to reduce potential oxidation and/or contamination of the electrically conductive structures of the semiconductor element or the substrate to which it will be bonded.

[0005] Thus, it would be desirable to provide improved methods of bonding semiconductor elements to a substrate with the use of a reducing gas.

SUMMARY

[0006] According to an exemplary embodiment of the invention, a bonding system for bonding a semiconductor element to a substrate is provided. The bonding system includes a substrate oxide reduction chamber configured to receive a substrate. The substrate includes a plurality of first electrically conductive structures. The substrate oxide reduction chamber is configured to receive a reducing gas to contact each of the plurality of first electrically conductive structures. The bonding system also includes a substrate oxide prevention chamber for receiving the substrate after the reducing gas contacts the plurality of first electrically conductive structures. The substrate oxide prevention chamber has an inert environment when receiving the substrate. The bonding system also includes a reducing gas delivery system for providing a reducing gas environment during bonding of a semiconductor element to the substrate. The semiconductor element includes a plurality of second electrically conductive structures. The plurality of first electrically conductive structures are configured to be bonded with corresponding ones of the plurality of second electrically conductive structures.

[0007] According to another exemplary embodiment of the invention, a method of bonding a semiconductor element to a substrate is provided. The method includes the steps of: moving a substrate into a substrate oxide reduction chamber, the substrate including a plurality of first electrically conductive structures, the substrate oxide reduction chamber configured to receive a reducing gas to contact each of the plurality of first electrically conductive structures; moving the substrate into a substrate oxide prevention chamber after the reducing gas contacts the plurality of first electrically conductive structures, the substrate oxide prevention chamber having an inert environment when receiving the substrate; and providing a reducing gas environment during bonding of a semiconductor element to the substrate, the semiconductor element including a plurality of second electrically conductive structures, the plurality of first electrically conductive structures being configured to be bonded with corresponding ones of the plurality of second electrically conductive structures.

[0008] According to yet another exemplary embodiment of the invention, a method of bonding a semiconductor element to a substrate is provided. The method includes the

steps of: (a) carrying a semiconductor element with a bonding tool of a bonding machine, the semiconductor element including a plurality of first electrically conductive structures; (b) supporting a substrate with a support structure of the bonding machine, the substrate including a plurality of second electrically conductive structures; (c) providing a reducing gas in contact with each of the plurality of first electrically conductive structures and the plurality of second electrically conductive structures; and (d) bonding the corresponding ones of the plurality of first electrically conductive structures to the respective ones of the plurality of second electrically conductive structures after step (c). At least one of the plurality of first electrically conductive structures and the plurality of second electrically conductive structures includes a solder material.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] The invention is best understood from the following detailed description when read in connection with the accompanying drawings. It is emphasized that, according to common practice, the various features of the drawings are not to scale. On the contrary, the dimensions of the various features are arbitrarily expanded or reduced for clarity.

[0010] FIG. 1A is a block diagram illustration of a bonding system for bonding a semiconductor element to a substrate in accordance with an exemplary embodiment of the invention;

[0011] FIG. 1B is a block diagram illustration of a bonding system for bonding a semiconductor element to a substrate in accordance with an exemplary embodiment of the invention;

[0012] FIGS. 2A-2G are a series of block diagram illustrations of the bonding system of FIG. 1A, illustrating a method of bonding a semiconductor element to a substrate in accordance with an exemplary embodiment of the invention;

[0013] FIGS. 3A-3B are a series of block diagram illustrations of the bonding system of FIG. 1A, illustrating a method of bonding a semiconductor element to a substrate in accordance with an exemplary embodiment of the invention, while preparing another substrate for bonding;

[0014] FIG. 4 is a block diagram illustration of a bonding system for bonding a semiconductor element, having conductive structures including a solder material, to a substrate in accordance with an exemplary embodiment of the invention;

[0015] FIG. 5 is a block diagram illustration of a bonding system for bonding a semiconductor element to a substrate, having conductive structures including a solder material, in accordance with an exemplary embodiment of the invention;

[0016] FIG. 6 is a block diagram illustration of a bonding system for bonding a semiconductor element, having conductive structures including a solder material, to a substrate, having conductive structures including a solder material, in accordance with an exemplary embodiment of the invention;

[0017] FIG. 7 is a block diagram illustration of a bonding system for bonding a semiconductor element, having conductive structures formed of a solder material, to a substrate in accordance with an exemplary embodiment of the invention;

[0018] FIG. 8 is a block diagram illustration of a bonding system for bonding a semiconductor element to a substrate, having conductive structures formed of a solder material, in accordance with an exemplary embodiment of the invention;

[0019] FIG. 9 is a block diagram illustration of a bonding system for bonding a semiconductor element, having conductive structures formed of a solder material, to a substrate, having conductive structures formed of a solder material, in accordance with an exemplary embodiment of the invention;

[0020] FIGS. 10A-10D are a series of block diagram illustrations of the bonding system of FIG. 4, illustrating a method of bonding a semiconductor element to a substrate in accordance with an exemplary embodiment of the invention; and

[0021] FIGS. 11A-11D are a series of block diagram illustrations of another bonding system, illustrating a method of bonding a semiconductor element to a substrate in accordance with an exemplary embodiment of the invention.

DETAILED DESCRIPTION

[0022] As used herein, the term "semiconductor element" is intended to refer to any structure including (or configured to include at a later step) a semiconductor chip or die. Exemplary semiconductor elements include a bare semiconductor die, a semiconductor die on a substrate (e.g., a leadframe, a PCB, a carrier, a semiconductor chip, a semiconductor wafer, a BGA substrate, a semiconductor element, etc.), a packaged semiconductor device, a flip chip semiconductor device, a die embedded in a substrate, a stack of semiconductor die, amongst others. Further, the semiconductor element may include an element configured to be bonded or otherwise included in a semiconductor package (e.g., a spacer to be bonded in a stacked die configuration, a substrate, etc.).

[0023] As used herein, the term "substrate" is intended to refer to any structure to which a semiconductor element may be bonded. Exemplary substrates include, for example, a leadframe, a PCB, a carrier, a module, a semiconductor chip, a semiconductor wafer, a BGA substrate, another semiconductor element, etc.

[0024] In accordance with certain exemplary embodiments of the invention, a fluxless bonding system is provided using reducing gas/gases. The bonding system may be, for example, a flip chip bonding system, a thermocompression bonding system, a thermosonic bonding system, etc.

[0025] Aspects of the invention relate to a novel fluxless chip-to-substrate or chip-to-wafer system that avoids oxidation of metal and solder pads during bonding (e.g., during thermocompression bonding).

[0026] Exemplary systems include a "substrate oxide reduction chamber" (also referred to as a substrate cleaning compartment), a "substrate oxide prevention chamber" (also referred to as a substrate protection compartment), and a "reducing gas delivery system" (e.g., a localized chip and substrate oxide reduction bond head shroud, or other reducing gas delivery system) to eliminate the use of a fluxing process.

[0027] FIG. 1A illustrates exemplary bonding system 300. Bonding system 300 includes: a substrate source 300a (e.g., a wafer handler or other source) for providing a substrate(s) 104 (such as a wafer, a printed circuit board, etc.) on a support structure 300a1; and a processing system 300b. Substrate 104 is configured to be transferred to processing system 300b (e.g., including a tunnel 302, but may be a different type of structure). Tunnel 302 (or other structure, as desired) includes a substrate oxide

reduction chamber 302a, a substrate oxide prevention chamber 302b, and a bonding location 302c (which is part of substrate oxide prevention chamber 302b). A reducing gas delivery system 308 is also included in processing system 300b.

[0028] In the example shown in FIG. 1A, because tunnel 302 includes both substrate oxide reduction chamber 302a and a substrate oxide prevention chamber 302b, at least a portion of substrate oxide reduction chamber 302a has a common boundary with substrate oxide prevention chamber 302b. Substrate oxide reduction chamber 302a is closed using entry door 302a1 (which closes opening 302a1a) and exit door 302a2 (which closes opening 302a2a). Another reducing gas delivery system 302d (which may be interconnected with reducing gas delivery system 308 to use a common source of reducing gas) is provided to provide a reducing gas (e.g., formic acid vapor) in substrate oxide reduction chamber 302a. After processing (e.g., removal of oxides from conductive structures of substrate 104) in substrate oxide reduction chamber 302a, a substrate transfer system (which may be part of a material handling system including support structure 102) is used to transfer substrate 104 through exit door 302a2 to substrate oxide prevention chamber 302b. Substrate oxide prevention chamber 302b includes an inert environment 306 (e.g., through a nitrogen supply, not shown for simplicity). A material handling system (e.g., including support structure 102) is used to move substrate 104 within substrate oxide prevention chamber 302b to a bonding location 302c. While at bonding location 302c, a reducing gas 130 is provided by reducing gas delivery system 308.

[0029] FIG. 1A also illustrates bond head assembly 106, including heater 108, and bonding tool 110. FIG. 1A also illustrates main exhaust 304 which pulls exhaust gases (e.g., gases such as reducing gas vapors) through piping 304a and 114b1 (where piping 114b1 is coupled, directly or indirectly, to center channel 114b described below). Bond head assembly 106 carries a bond head manifold 114 for receiving and distributing fluids (e.g., gases, vapors, etc.) as desired in the given application. Details of an exemplary bond head assembly 106, including exemplary bond head manifold 114, are described below in connection with FIGS. 4-9, and FIGS. 10A-10D.

[0030] In connection with a bonding operation, semiconductor element 112 is bonded to substrate 104 using bonding tool 110. During the bonding operation, corresponding ones of electrically conductive structures of semiconductor element 112 are

bonded (e.g., using heat, force, ultrasonic energy, etc.) to respective ones of electrically conductive structures of substrate 104. Bond head manifold 114 provides a reducing gas 130 (e.g., where the reducing gas is a saturated vapor gas) in the area of semiconductor element 112 and substrate 104 in connection with a bonding operation. After reducing gas 130 is distributed in the area of semiconductor element 112 and substrate 104, reducing gas 130 contacts surfaces of each of electrically conductive structures of semiconductor element 112 and substrate 104.

[0031] FIG. 1B illustrates exemplary bonding system 400, which is similar in many respect to bonding system 300 of FIG. 1A (where like elements have the same reference numerals, or a numberal beginning with a "4" instead of a "3"). Bonding system 400 includes a substrate source 400a (e.g., a wafer handler or other source) for providing a substrate(s) 104 (such as a wafer, a printed circuit board, etc.) on a support structure 400a1. Substrate 104 is configured to be transferred to processing system 400b (e.g., including a tunnel 402, but may be a different type of structure). Tunnel 402 (or other structure, as desired) includes a substrate oxide reduction chamber 402a, a substrate oxide prevention chamber 402b, and a bonding location 402c (which is part of substrate oxide prevention chamber 402b).

[0032] In the example shown in FIG. 1B, because tunnel 402 includes both substrate oxide reduction chamber 402a and a substrate oxide prevention chamber402b, at least a portion of substrate oxide reduction chamber 402a has a common boundary with substrate oxide prevention chamber 402b. A reducing gas delivery system 408 is also included in processing system 400b. Substrate oxide reduction chamber 402a is closed using entry door 402a1 (which closes opening 402a1a) and exit door 402a2 (which closes opening 402a2a). Another reducing gas delivery system 402d (which may be interconnected with reducing gas delivery system 408 to use a common source of reducing gas) is provided to provide a reducing gas (e.g., formic acid vapor) in substrate oxide reduction chamber 402a. After processing (e.g., removal of oxides from conductive structures of substrate 104) in substrate oxide reduction chamber 402a, a substrate transfer system (which may be part of a material handling system including support structure 102) is used to transfer substrate 104 through opening 402a2a to substrate oxide prevention chamber 402b. Substrate oxide prevention chamber 402b includes an inert environment 406 (e.g., through a nitrogen supply, not shown for simplicity). A material handling system (e.g., including support structure 102) is used to move substrate

104 within substrate oxide prevention chamber 402b to a bonding location 402c. While at bonding location 402c, a reducing gas 130 is provided by reducing gas delivery system 408.

[0033] FIG. 1B also illustrates bond head assembly 106, including heater 108, and bonding tool 110. FIG. 1B also illustrates main exhaust 404 which pulls exhaust gases (e.g., gases such as reducing gas vapors) through piping 404a and 404b. A manifold 214 is provided for receiving and distributing fluids (e.g., gases, vapors, etc.) as desired in the given application. Details of an exemplary bond head assembly 106, and an exemplary manifold 214, are described below in connection with FIGS. 11A-11D).

[0034] In connection with a bonding operation, semiconductor element 112 is bonded to substrate 104 using bonding tool 110. During the bonding operation, corresponding ones of electrically conductive structures of semiconductor element 112 are bonded (e.g., using heat, force, ultrasonic energy, etc.) to respective ones of electrically conductive structures of substrate 104. Manifold 214 provides a reducing gas 130 (e.g., where the reducing gas is a saturated vapor gas) in the area of semiconductor element 112 and substrate 104 in connection with a bonding operation. After reducing gas 130 is distributed in the area of semiconductor element 112 and substrate 104, reducing gas 130 contacts surfaces of each of electrically conductive structures of semiconductor element 112 and substrate 104.

[0035] FIG. 2A-2G illustrate a method of bonding a semiconductor element 112 to a substrate 104 in connection with an exemplary embodiment of the invention, using bonding system 300 shown in FIG. 1A. FIG. 2A illustrates a substrate 104 in substrate source 300a, with entry door 302a1 in an open position. Substrate oxide reduction chamber 302a and substrate oxide prevention chamber 302b have an inert environment 306 (e.g., a nitrogen enviroment). At FIG. 2B, substrate 104 has been moved into substrate oxide reduction chamber 302a through opening 302a1a using a substrate handling system (e.g., a material handling system including support structure 102). At FIG. 2C, entry door 302a1 is closed, and a reducing gas 130 (e.g., formic acid vapor) is provided in substrate oxide reduction chamber 302a via reducing gas delivery system 302d. Reducing gas 130 removes residual oxide from the metal and solder pads (i.e., conductive structures) on substrate 104. At FIG. 2D, exit door 302a2 is opened, and substrate 104 is transferred from substrate oxide reduction chamber 302a to substrate

oxide prevention chamber 302b as shown in FIG. 2E. Substrate oxide prevention chamber 302b includes an inert environment 306 (e.g., a nitrogen environment). In FIG. 2F, substrate 104 has been moved (e.g., using a material handling system including support structure 102) to bonding location 302c. At bonding location 302c, a reducing gas 130 is directed from bond head manifold 114 toward semiconductor element 112 and substrate 104. This reducing gas 130 is provided during bonding of semiconductor element 112 to substrate 104 to reduce/remove oxides on semiconductor element 112 as well as any remaining residual oxides on substrate 104. At FIG. 2G, semiconductor element 112 has been bonded to substrate 104 using bond head assembly 106.

[0036] Although FIGS. 2A-2G illustrate bonding system 300, it is contemplated that a substantially similar process could be applied to bonding system 400 shown in FIG. 1B, or other bonding systems within the scope of the invention.

[0037] While the exemplary process of FIGS. 2A-2G illustrates a single substrate 104, it is contemplated that a plurality of substrates 104 may be involved in system 300 (or bonding system 400 of FIG. 1B) (or another bonding system within the scope of the invention). Thus, FIGS. 3A-3B illustrate multiple substrates 104. In FIG. 3A, a first substrate 104 (already having been processed using substrate oxide reduction chamber 302a) is being moved to bonding location 302c of substrate oxide prevention chamber 302b. In FIG. 3B, while that substrate 104 is at bonding location 302c, another substrate 104 is in substrate oxide reduction chamber 302a (e.g., for cleaning of conductive structures on the another substrate 104).

[0038] Exemplary aspects of the invention provides an opportunity to rework a substrate 104 (e.g., to transfer the substrate back to substrate oxide reduction chamber 302a). For example, such an approach might be useful in situations where prolonged substrate exposures to heating is unavoidable, for example, bonding of small dies (e.g. 0.1-1mm edge size) to a large area (e.g. 200-300 mm diameter substrate).

[0039] The invention may provide a number of benefits such as, for example: fluxless bonding (e.g., no fluxing of the semiconductor element or the substrate is required prior to or during bonding); reduction of oxides (e.g., metal oxides such as Cu and Sn oxides formed on pads/bumps) on both the semiconductor element and the substrate, as well as prevention of oxide formation during long heat exposures; a low consumption of nitrogen gas (or other gas providing the inert enviroment in the substrate oxide prevention

chamber); and a pre-cleaning chamber, an inert gas chamber, and an in-situ oxide cleaning bond head are all provided in the same bonding system.

[0040] While it is not explicitly shown in FIG. 1, FIGS. 2A-2G, and FIGS. 3A-3B, it is understood that a bonding operation may include bonding a semiconductor element 112 (or a plurality of elements) to a portion of the bond sites (bonding areas) of substrate 104 in the tunnel (e.g., tunnel 302). For example, that portion of the bond sites of substrate 104 may be exposed by an opening in the tunnel 302, where the bonding tool may be lowered through opening 302e to complete the bonding operation. By only exposing a portion of substrate 104 at a time, the environment within tunnel 302 is better maintained.

[0041] In connection with bonding (e.g., thermocompression bonding) of a semiconductor element 112 (including electrically conductive structures) to a substrate 104 (including electrically conductive structures), heat may be provided through bonding tool 110 (e.g., from a heater of bond head assembly 106). A reducing gas may also be provided for cleaning oxides and/or other contaminants on the surface of the electrically conductive structures (of semiconductor element 112 and/or substrate 104).

[0042] In specific examples of such methods, a semiconductor element 112 (e.g., a semiconductor chip) is transferred from a source (e.g., a semiconductor wafer) to bonding tool 110 of a thermocompression bonding machine or a flip chip bonding machine. With semiconductor element 112 carried by bonding tool 110 (e.g., using vaccum), bond head assembly 106 (carrying bonding tool 110) is moved to a desired bonding position. The semiconductor element 112 is bonded to the bonding position of substrate 104 (e.g., while heating the semiconductor element 112 and/or the substrate 104) (e.g., where the bonding occurs in the presence of a reducing gas). The respective conductive structures of the semiconductor element 112, and/or the substrate 104 may include a solder material (e.g., the conductive structures may include a solder material at a contact surface, the conductive structures may be formed of a solder material, etc.), or the conductive structures may be formed of another conductive material (e.g., copper).

[0043] Throughout the various drawings (including FIGS. 4-9, FIGS. 10A-10D, and FIGS. 11A-11D), like reference numerals refer to the like elements, except where explained herein.

[0044] Referring now to FIG. 4, a bonding machine 100 (e.g., a flip chip bonding machine, a thermocompression bonding machine, etc.) is provided. Bonding machine 100 includes a support structure 102 for supporting a substrate 104 during a bonding operation (where substrate 104 includes a plurality of electrically conductive structures 104a). Support structure 102 may include any appropriate structure for the specific application. In FIGS. 4-9 and FIGS. 10A-10D, support structure 102 includes top plate 102a (configured to directly support substrate 104), chuck 102c, and heater 102b disposed therebetween. In applications where heat for heating substrate 104 is desirable in connection with the bonding operation, a heater such as heater 102b may be utilized.

[0045] FIG. 4 also illustrates bond head assembly 106, which may be configured to move along (and about) a plurality of axes of bonding machine 100 such as, for example, the x-axis, y-axis, z-axis, theta (rotative) axis, etc. Bond head assembly 106 includes heater 108 and bonding tool 110. That is, in certain bonding machines (e.g., thermocompression bonding machines) it may be desirable to heat the bonding tool. Thus, while FIG. 4 illustrates a separate heater 108 for heating bonding tool 110 (for heating semiconductor element 112 including a plurality of electrically conductive structures 112a), it will be appreciated that heater 108 and bonding tool 110 may be integrated into a single element (e.g., a heated bonding tool).

[0046] In connection with a bonding operation, semiconductor element 112 is bonded to substrate 104 using bonding tool 110. During the bonding operation, corresponding ones of electrically conductive structures 112a are bonded (e.g., using heat, force, ultrasonic energy, etc.) to respective ones of electrically conductive structures 104a. In FIG. 4, electrically conductive structures 112a include a solder material 112a1 at a contact portion of each electrically conductive structure 112a (e.g., a portion configured to contact the electrically conductive structures 104a of substrate 104).

[0047] In certain bonding applications (e.g., flip chip and/or thermocompression bonding with copper conductive structures), it is desirable to provide an environment suitable for bonding. Conventionally, such an environment may be provided by using a reducing gas at the bonding area to reduce potential contamination of the electrically conductive structures of the semiconductor element or the substrate to which it will be bonded.

[0048] In FIG. 4, bond head assembly 106 carries a bond head manifold 114 for receiving and distributing fluids (e.g., gases, vapors, etc.) as desired in the given application. In FIG. 4, while bond head manifold 114 is illustrated in a cross sectional view, the actual bond head manifold 114 surrounds bonding tool 110 (e.g., bond head manifold 114 surrounds bonding tool 110 in a coaxial configuration). Of course, bond head manifold 114 may have different configurations from that shown in FIG. 4. Further, it is understood that certain details of bond head manifold 114 (e.g., interconnection with piping 120, structural details for distributing a reducing gas within bond head manifold 114, structural details for distributing a shielding gas within bond head manifold 114, structural details for drawing a vacuum through a center channel of bond head manifold 114, etc.) are omitted for simplicity.

[0049] Bond head manifold 114 includes three channels 114a, 114b, 114c having different functions. Outer channel 114a receives a shielding gas (e.g., nitrogen gas) from shielding gas supply 118. That is, a shielding gas is provided from shielding gas supply 118 (e.g., a nitrogen supply), through piping 120 (where piping 120 may include hard piping, flexible tubing, a combination of both, or any other structure adapted to carry the fluids described herein), to outer channel 114a of bond head manifold 114. From outer channel 114a of bond head manifold 114, the shielding gas 128 is provided as a shield from the outside environment (e.g., see FIGS. 10B-10C).

[0050] Inner channel 114c receives a reducing gas 130 (e.g., see FIGS. 10B-10C) (e.g., where the reducing gas is a saturated vapor gas) via piping 120, and provides reducing gas 130 in the area of semiconductor element 112 and substrate 104 in connection with a bonding operation. Reducing gas 130 is provided by a vapor generation system 122, but initiates as reducing gas 126. In the example shown in FIG. 4, vapor generation system 122 is a bubbler type system including an acid fluid 124 (e.g., formic acid, acetic acid, etc.) in vessel 122a of the bubbler type system. A carrier gas (e.g., nitrogen) is provided (via piping 120) into acid fluid 124 in vessel 122a, where the carrier gas acts as a carrier for the acid fluid 124. Collectively, the carrier gas (e.g., nitrogen) and acid fluid 124 are transported as reducing gas 126. Within piping 120, additional carrier gas (e.g., nitrogen) may be added to reducing gas 126 (e.g., to vary the concentration of the reducing gas, as desired) via piping section 120a, thereby providing reducing gas 130 in the area of semiconductor element 112 and substrate 104 in connection with the bonding operation. After reducing gas 130 is distributed in the area of semiconductor

element 112 and substrate 104, reducing gas 130 contacts surfaces of each of electrically conductive structures 104a and electrically conductive structures 112a (e.g., see FIG. 10B). The surfaces of electrically conductive structures 104a/112a may then include a reaction product (e.g., where the reaction product is provided as a result of (i) a surface oxide on electrically conductive structures 104a/112a, and (ii) reducing gas from reducing gas 130 (and possibly heat provided by heater 108 and transferred to electrically conductive structures 104a via contact with electrically conductive structures 112a, if desired). This reaction product is desirably removed from the bonding area (i.e., the area where electrically conductive structures 112a of semiconductor element 112 are bonded to corresponding electrically conductive structures 104a of substrate 104) using vaccum provided through center channel 114b of bond head manifold 114 via exit piping 116.

[0051] Thus, FIG. 4 illustrates: (i) various elements of bonding machine 100; (ii) a path of carrier gas from carrier gas supply 118 to outer channel 114a of bond head manifold 114; (iii) a path of reducing gas 126 (which may receive additional carrier gas from piping 120) from vapor generation system 122 to inner channel 114c of bond head manifold 114, where it is released to the bonding area as reducing gas 130; and (iv) a path of gas (which may carry away a reaction product from surfaces of electrically conductive structures 104a/112a) drawn by vacuum through center channel 114b of bond head manifold 114. The aforementioned paths are illustrated in FIG. 4 through various arrows even though gas is not flowing in FIG. 4 (see FIGS. 10A-10D for an exemplary operation).

[0052] FIG. 5 again illustrates bonding machine 100 as shown in FIG. 4; however, in FIG. 5 electrically conductive structures 112a do not include a solder material 112a1 as shown in FIG. 4. Rather, in FIG. 5, electrically conductive structures 104a include a solder material 104a1 at a contact portion of each electrically conductive structure 104a (e.g., a portion configured to contact the electrically conductive structures 112a of semiconductor element 112).

[0053] FIG. 6 again illustrates bonding machine 100 as shown in FIGS. 4-5; however, in FIG. 6 electrically conductive structures 112a include a solder material 112a1 as shown in FIG. 4, and electrically conductive structures 104a include a solder material 104a1 as shown in FIG. 5.

[0054] FIG. 7 again illustrates bonding machine 100 as shown in FIG. 4; however, in FIG. 7 electrically conductive structures 112a (shown in FIG. 4) are replaced by electrically conductive structures 112a2 which are formed of a solder material. That is, unlike FIG. 4, where electrically conductive structures 112a includes a solder material 112a1 at a contact portion, in FIG. 7, electrically conductive structures 112a2 are fully formed of a solder material.

[0055] FIG. 8 again illustrates bonding machine 100 as shown in FIG. 5; however, in FIG. 8 electrically conductive structures 104a (shown in FIG. 5) are replaced by electrically conductive structures 104a2 which are formed of a solder material. That is, unlike FIG. 5, where electrically conductive structures 104a includes a solder material 104a1 at a contact portion, in FIG. 8, electrically conductive structures 104a2 are fully formed of a solder material.

[0056] FIG. 9 again illustrates bonding machine 100 as shown in FIGS. 4-8; however, in FIG. 9 electrically conductive structures 112a (shown in FIGS. 4 and 6, including a solder material 112a1) are replaced by electrically conductive structures 112a2 (fully formed of a solder material) as shown in FIG. 7. Further, in FIG. 9, electrically conductive structures 104a (shown in FIG. 5, including a solder material 104a1) are replaced by electrically conductive structures 104a2 (fully formed of a solder material) as shown in FIG. 8.

[0057] Thus, according to certain aspects of the invention the electrically conductive structures of the semiconductor element being bonded, or the substrate configured to receive the semiconductor element during bonded, may include a solder material. The solder material may be included in a number of different configurations. For example, the solder material may be included at a contact portion of the electrically conductive structures (e.g., see FIGS. 4-6). In another non-limiting example, the entire electrically conductive structures may be formed of the solder material (e.g., see FIGS. 7-9).

[0058] FIGS. 10A-10D and FIGS. 11A-11D are block diagrams illustrating methods of bonding a semiconductor element to a substrate. In each of FIGS. 10A-10D and FIGS. 11A-11D: (i) the semiconductor element 112 (with electrically conductive structures 112a including solder material 112a1 at a contact portion) is shown as in FIG. 4; and (ii) the substrate 104 (with electrically conductive structures 104a not including a solder material) is shown as in FIG. 4. However, it is understood that the methods shown and described

with respect to FIGS. 10A-10D and FIGS. 11A-11D are equally applicable to the semiconductor elements and substrates of each of FIGS. 4-9, and are applicable to the semiconductor elements and substrates of any other embodiment within the scope of the invention.

[0059] Prior to the processes shown and described in connection with FIGS. 10A-10D and FIGS. 11A-11D, semiconductor element 112 and/or substrate 104 may be "cleaned". For example, the electrically conductive structures 112a, 104a of one or both of semiconductor element 112 and substrate 104 may be cleaned using a solution such as hydrochloric acid or acetic acid. Such a cleaning step may be performed, for example, by dipping at least a portion of semiconductor element 112 and/or substrate 104 into such a solution.

[0060] Referring now to FIG. 10A, semiconductor element 112 (carried by bond head 106) is positioned above substrate 104. As shown in FIG. 10B, vapor generation system 122 has been activated to produce reducing gas 130 at the bonding area. More specifically, FIG. 10B illustrates reducing gas 130 being provided at the bonding area, as well as shielding gas 128 being provided, and vacuum being drawn through center channel 114b of bond head manifold 114 via exit piping 116. Thus, the flow of reducing gas 130 reach desired portions of semiconductor element 112 and substrate 104 (e.g., electrically conductive structures 104a and electrically conductive structures 112a) for: removing contaminants from the electrically conductive structures 104a and electrically conductive structures 112a; and/or shielding electrically conductive structures 104a and electrically conductive structures 112a from further potential contamination.

[0061] Also shown in FIG. 10B, respective ones of electrically conductive structures 112a (of semiconductor element 112) are aligned with ones of electrically condutive structures 104a (of substrate 104). At FIG. 10C, the process proceeds to a bonding step (e.g., a thermocompression bonding step), for example, through the lowering of bond head 106. That is, electrically conductive structures 112a are bonded to corresponding electrically conductive structures 104a. This may be through a thermocompression bonding process (e.g., including heat and/or bond force, where the bond force may be a higher bond force such as 50-300 N), and may also include ultrasonic energy transfer (e.g., from an ultrasonic transducer included in bond head assembly 106). At FIG. 10D, the bonding process has been completed. That is, semiconductor element 112 has been

bonded to substrate 104, such that corresponding electrically conductive structures 112a, 104a are now bonded to one another with deformed solder materual 112a1 provided therebetween.

[0062] Although FIGS. 10A-10D (and FIGS. 4-9) illustrate manifold 114, integrated with the bond head, for: delivering the reducing gas; delivering the shielding gas; and providing vaccum – the invention is not limited thereto. For example, instead of such functions being provided through integration of a manifold with the bond head assembly, such functions may be provided through integration with a support structure for supporting the substrate. Further, such functions may be split between the bond head assembly and the support structure (and possibly other structures of the bonding machine). FIGS. 11A-11D are a series of block diagrams of a bonding machine 100″, with certain similar elements and functions to that illustrated and described with respect to FIG. 4 and FIGS. 10A-10D, except that the manifold functions (delivering the reducing gas; delivering the shielding gas; and providing vaccum) are integrated into a support structure 202.

[0063] FIG. 11A illustrates bonding machine 100″ (e.g., a flip chip bonding machine, a thermocompression bonding machine, etc.). Bonding machine 100″ includes a support structure 202 for supporting a substrate 104 during a bonding operation (where substrate 104 includes a plurality of electrically conductive structures 104a). Support structure 202 may include any appropriate structure for the specific application. In FIGS. 11A-11D, support structure 202 includes top plate 202a (configured to directly support substrate 104), chuck 202c, and heater 202b disposed therebetween. In applications where heat for heating substrate 104 is desirable in connection with the bonding operation, a heater such as heater 202b may be utilized.

[0064] FIG. 11A also illustrates bond head assembly 106 (including heater 108 and bonding tool 110), which may be configured to move along (and about) a plurality of axes of bonding machine 100″ such as, for example, the x-axis, y-axis, z-axis, theta (rotative) axis, etc. In FIG. 11A, bond head assembly 106 carries a plate 107 for partially containing at least one of shielding gas 128 and reducing gas 130 (see description below).

[0065] As opposed to a bond head manifold 114 carried by bond head assembly 106 (as in FIGS. 10A-10D), FIGS. 11A-11I illustrate a manifold 214 carried by, and/or intergrated with, support structure 202. Manifold 214 is configured for receiving and distributing fluids (e.g., gases, vapors, etc.) as desired in the given application. In FIG.

11A, while manifold 214 is illustrated in a cross sectional view, the actual manifold 214 at least partially surrounds substrate 104. Of course, manifold 214 may have different configurations from that shown in FIG. 11A. Further, it is understood that certain details of manifold 214 (e.g., interconnection with piping 120, structural details for distributing reducing gas 130 within manifold 214, structural details for distributing shielding gas 128 within manifold 214, structural details for drawing a vacuum through a center channel of manifold 214, etc.) are omitted for simplicity.

[0066] Manifold 214 includes three channels 214a, 214b, 214c having different functions. Outer channel 214a receives shielding gas 128 (e.g., nitrogen gas) from shielding gas supply 118 via piping 120. From outer channel 214a of manifold 214, shielding gas 128 is provided as a shield from the outside environment (e.g., see FIGS. 11B-11C). Inner channel 214c receives a reducing gas 130 (e.g., see FIGS. 11B-11C) (e.g., where the reducing gas is a saturated vapor gas) via piping 120, and provides reducing gas 130 in the area of semiconductor element 112 and substrate 104 in connection with a bonding operation. Reducing gas 130 is provided by a vapor generation system 122, but initiates as reducing gas 126 (e.g., see description above with respect to FIG. 4). After reducing gas 130 is distributed in the area of semiconductor element 112 and substrate 104, reducing gas 130 contacts surfaces of each of electrically conductive structures 104a and electrically conductive structures 112a. The surfaces of electrically conductive structures 104a/112a may then include a reaction product (e.g., where the reaction product is provided as a result of: (i) a surface oxide on electrically conductive structures 104a/112a, and (ii) reducing gas from reducing gas 130 (and possibly heat provided by heater 108, if desired). This reaction product is desirably removed from the bonding area (i.e., the area where electrically conductive structures 112a of semiconductor element 112 are bonded to corresponding electrically conductive structures 104a of substrate 104) using vaccum provided through center channel 214b of manifold 214 via exit piping 216.

[0067] Thus, FIG. 11A illustrates: (i) various elements of bonding machine 100''; (ii) a path of carrier gas from carrier gas supply 118 to outer channel 214a of manifold 214; (iii) a path of reducing gas 126 (which may receive additional carrier gas from piping 120a) from vapor generation system 122 to inner channel 214c of manifold 214, where it is released to the bonding area as reducing gas 130; and (iv) a path of gas (which may carry away a reaction product from surfaces of electrically conductive structures

104a/112a) drawn by vacuum through center channel 214b of manifold 214. The aforementioned paths are illustrated in FIG. 11A through various arrows even though gas is not flowing in FIG. 11A.

[0068] Referring now to FIG. 11A, semiconductor element 112 (carried by bond head 106) is positioned above substrate 104. As shown in FIG. 11B, vapor generation system 122 has been activated to produce reducing gas 130 at the bonding area. More specifically, FIG. 11B illustrates reducing gas 130 being provided at the bonding area, as well as shielding gas 128 being provided, and vacuum being drawn through center channel 114b of bond head manifold 114 via exit piping 116. Thus, the flow of reducing gas 130 reach desired portions of semiconductor element 112 and substrate 104 (e.g., electrically conductive structures 104a and electrically conductive structures 112a) for: removing contaminants from the electrically conductive structures 104a and electrically conductive structures 112a; and/or shielding electrically conductive structures 104a and electrically conductive structures 112a from further potential contamination.

[0069] Also shown in FIG. 11B, respective ones of electrically conductive structures 112a (of semiconductor element 112) are aligned with ones of electrically condutive structures 104a (of substrate 104). At FIG. 11C, the process proceeds to a bonding step (e.g., a thermocompression bonding step), for example, through the lowering of bond head 106. That is, electrically conductive structures 112a are bonded to corresponding electrically conductive structures 104a. This may be through a thermocompression bonding process (e.g., including heat and/or bond force, where the bond force may be a higher bond force such as 50-300 N), and may also include ultrasonic energy transfer (e.g., from an ultrasonic transducer included in bond head assembly 106). At FIG. 11D, the bonding process has been completed. That is, semiconductor element 112 has been bonded to substrate 104, such that corresponding electrically conductive structures 112a, 104a are now bonded to one another with deformed solder materual 112a2 provided therebetween.

[0070] Although the invention has been illustrated primarily with respect to one of manifolds 114, 214 for directing (i) the flow of reducing gas 130, (ii) the flow of shielding gas 128, and (iii) the pull of the vacuum, it is understood that the structure used to direct the flow patterns may be different from that illustrated. That is, the configuration of the

structure used to provide and direct fluids 130, 128 (and to draw vacuum) may vary considerably from that shown.

[0071] The invention described herein in connection with FIGS. 4-9, FIGS. 10A-10D, and FIGS. 11A-11D may provide a number of benefits such as, for example: fluxless bonding (e.g., no fluxing of the semiconductor element or the substrate is required prior to or during bonding); reduction of oxides on both the semiconductor element and the substrate; among others.

[0072] It will be appreciated by those skilled in the art that certain elements of bonding machine 100 (see FIGS. 4-9 and FIGS. 10A-10D), and/or bonding machine 100'' (see FIGS. 11A-11D) may be integrated into the systems of FIG. 1, FIGS. 2A-2G, and FIGS. 3A-3B, to replace at least a portion of the elements of the bondhead compartments (e.g., the bond head, the shroud, certaing piping, etc.).

[0073] Although the invention has been described and illustrated with respect to the exemplary embodiments thereof, it should be understood by those skilled in the art that the foregoing and various other changes, omissions and additions may be made therein and thereto, without parting from the spirit and scope of the present invention. Rather, various modifications may be made in the details within the scope and range of equivalents of the claims and without departing from the invention.

What is Claimed:

1. A bonding system for bonding a semiconductor element to a substrate, the bonding system comprising:

a substrate oxide reduction chamber configured to receive a substrate, the substrate including a plurality of first electrically conductive structures, the substrate oxide reduction chamber configured to receive a reducing gas to contact each of the plurality of first electrically conductive structures;

a substrate oxide prevention chamber for receiving the substrate after the reducing gas contacts the plurality of first electrically conductive structures, the substrate oxide prevention chamber having an inert environment when receiving the substrate; and

a reducing gas delivery system for providing a reducing gas environment during bonding of a semiconductor element to the substrate, the semiconductor element including a plurality of second electrically conductive structures, the plurality of first electrically conductive structures being configured to be bonded with corresponding ones of the plurality of second electrically conductive structures.

2. The bonding system of claim 1 further comprising a substrate transfer system for transferring the substrate from substrate oxide reduction chamber to the substrate oxide prevention chamber.

3. The bonding system of claim 1 wherein the substrate oxide prevention chamber is provided with nitrogen to create the inert environment.

4. The bonding system of claim 1 further comprising a material handling system for moving the substrate within the substrate oxide prevention chamber.

5. The bonding system of claim 1 wherein the substrate oxide prevention chamber includes a bonding location for receiving the substrate during bonding of the semiconductor element to the substrate.

6. The bonding system of claim 1 further comprising a bond head including a bonding tool for bonding the semiconductor element to the substrate, wherein the reducing gas delivery system is integrated with the bond head.

7. The bonding system of claim 1 further comprising a substrate support structure, the substrate support structure supporting the substrate during bonding of the semiconductor element to the substrate, wherein the reducing gas delivery system is integrated with the substrate support structure.

8. The bonding system of claim 1 wherein the semiconductor element is a semiconductor die.

9. The bonding system of claim 8 wherein the substrate is a semiconductor wafer.

10. The bonding system of claim 1 wherein the substrate may be returned to the substrate oxide reduction chamber after being received by the substrate oxide prevention chamber.

11. The bonding system of claim 1 wherein at least a portion of the substrate oxide reduction chamber has a common boundary with the substrate oxide prevention chamber.

12. The bonding system of claim 1 wherein the substrate oxide reduction chamber is configured to receive another substrate after the substrate is moved to the substrate oxide prevention chamber.

13. A method of bonding a semiconductor element to a substrate, the method comprising the steps of:

moving a substrate into a substrate oxide reduction chamber, the substrate including a plurality of first electrically conductive structures, the substrate oxide reduction chamber configured to receive a reducing gas to contact each of the plurality of first electrically conductive structures;

moving the substrate into a substrate oxide prevention chamber after the reducing gas contacts the plurality of first electrically conductive structures, the substrate oxide prevention chamber having an inert environment when receiving the substrate; and

providing a reducing gas environment during bonding of a semiconductor element to the substrate, the semiconductor element including a plurality of second electrically conductive structures, the plurality of first electrically conductive structures

being configured to be bonded with corresponding ones of the plurality of second electrically conductive structures.

14. A method of bonding a semiconductor element to a substrate, the method comprising the steps of:

(a) carrying a semiconductor element with a bonding tool of a bonding machine, the semiconductor element including a plurality of first electrically conductive structures;

(b) supporting a substrate with a support structure of the bonding machine, the substrate including a plurality of second electrically conductive structures;

(c) providing a reducing gas in contact with each of the plurality of first electrically conductive structures and the plurality of second electrically conductive structures; and

(d) bonding the corresponding ones of the plurality of first electrically conductive structures to the respective ones of the plurality of second electrically conductive structures after step (c),

wherein at least one of the plurality of first electrically conductive structures and the plurality of second electrically conductive structures includes a solder material.

15. The method of claim 14 wherein each of the plurality of first electrically conductive structures and the plurality of second electrically conductive structures includes solder material.

16. The method of claim 14 wherein at least one of the plurality of first electrically conductive structures and the plurality of second electrically conductive structures includes solder material at a contact portion thereof.

17. The method of claim 14 wherein the plurality of first electrically conductive structures includes solder material at a contact portion thereof.

18. The method of claim 14 wherein the plurality of second electrically conductive structures includes solder material at a contact portion thereof.

19. The method of claim 14 wherein both of the plurality of first electrically conductive structures and the plurality of second electrically conductive structures includes solder material at a contact portion thereof.

20. The method of claim 14 wherein at least one of the plurality of first electrically conductive structures and the plurality of second electrically conductive structures is formed of solder material.

21. The method of claim 14 wherein the plurality of first electrically conductive structures are formed of solder material.

22. The method of claim 14 wherein the plurality of second electrically conductive structures are formed of solder material.

23. The method of claim 14 wherein both of the plurality of first electrically conductive structures and the plurality of second electrically conductive structures are formed of solder material.

24. The method of claim 14 wherein the reducing gas includes a carrier gas and an acid.

25. The method of claim 24 wherein the acid includes one of formic acid and acetic acid.

26. The method of claim 14 wherein the reducing gas is a saturated vapor gas provided via a vapor generation system included on the bonding machine.

27. The method of claim 14 wherein step (d) includes applying ultrasonic energy between the semiconductor element and the substrate.

28. The method of claim 14 wherein step (d) includes bonding the corresponding ones of the plurality of first electrically conductive structures to the respective ones of the plurality of second electrically conductive structures through a thermocompression bonding process.

29. The method of claim 14 wherein the bonding tool is carried by a bond head of the bonding machine, and wherein step (c) includes providing the reducing gas in contact with each of the plurality of first electrically conductive structures and the plurality of second electrically conductive structures via a manifold integrated with the bond head.

30. The method of claim 14 wherein step (c) includes providing the reducing gas in contact with each of the plurality of first electrically conductive structures and the plurality of second electrically conductive structures via a manifold integrated with the support structure.

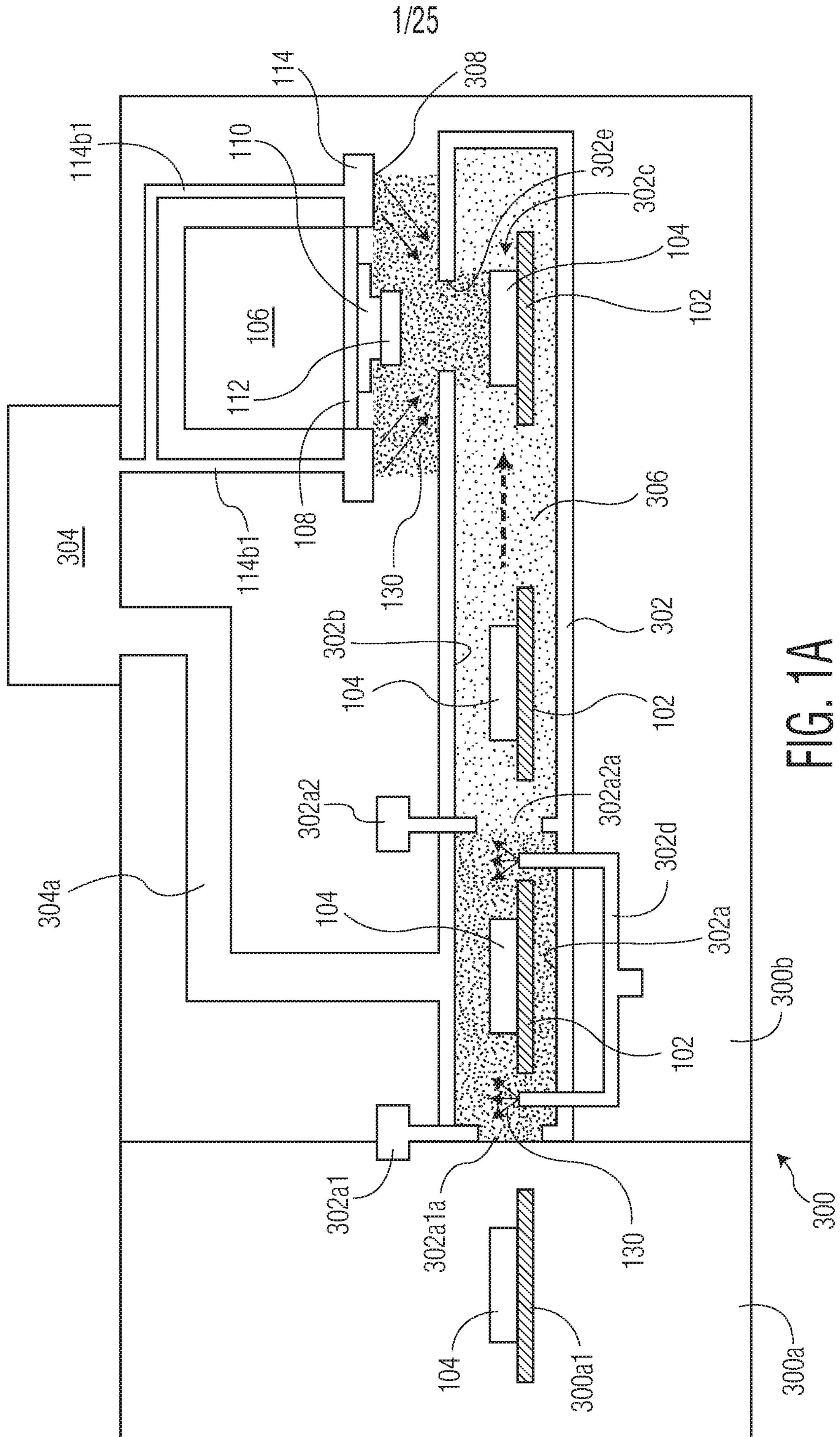

FIG. 1A

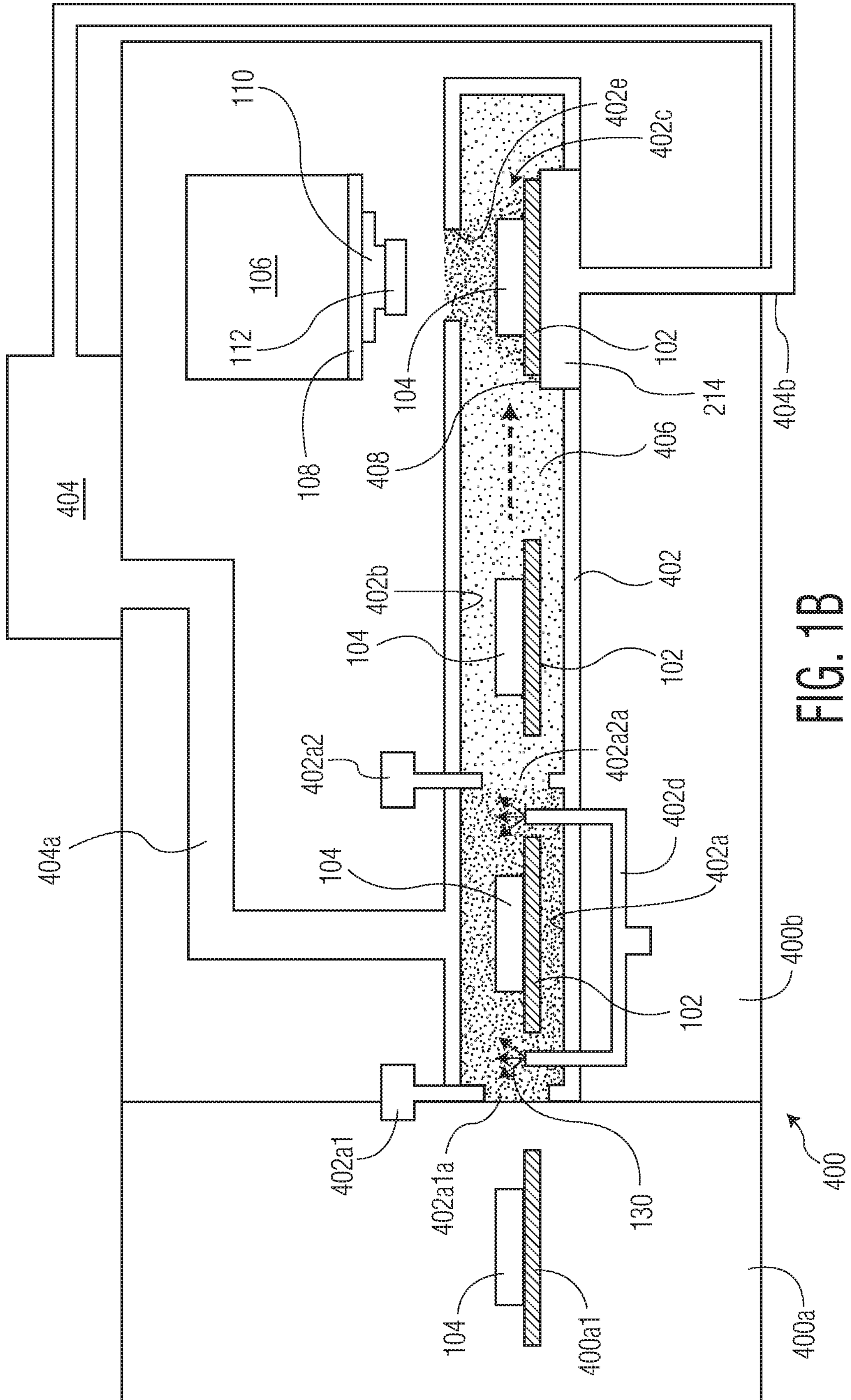

FIG. 1B

114b1 110 114 308 302e 302c 106 112 108 114b1 304 306 302b 302 302a2 304a 302d 302a 300b 102 302a1 302a1a 300 104 300a1 300a

FIG. 2A

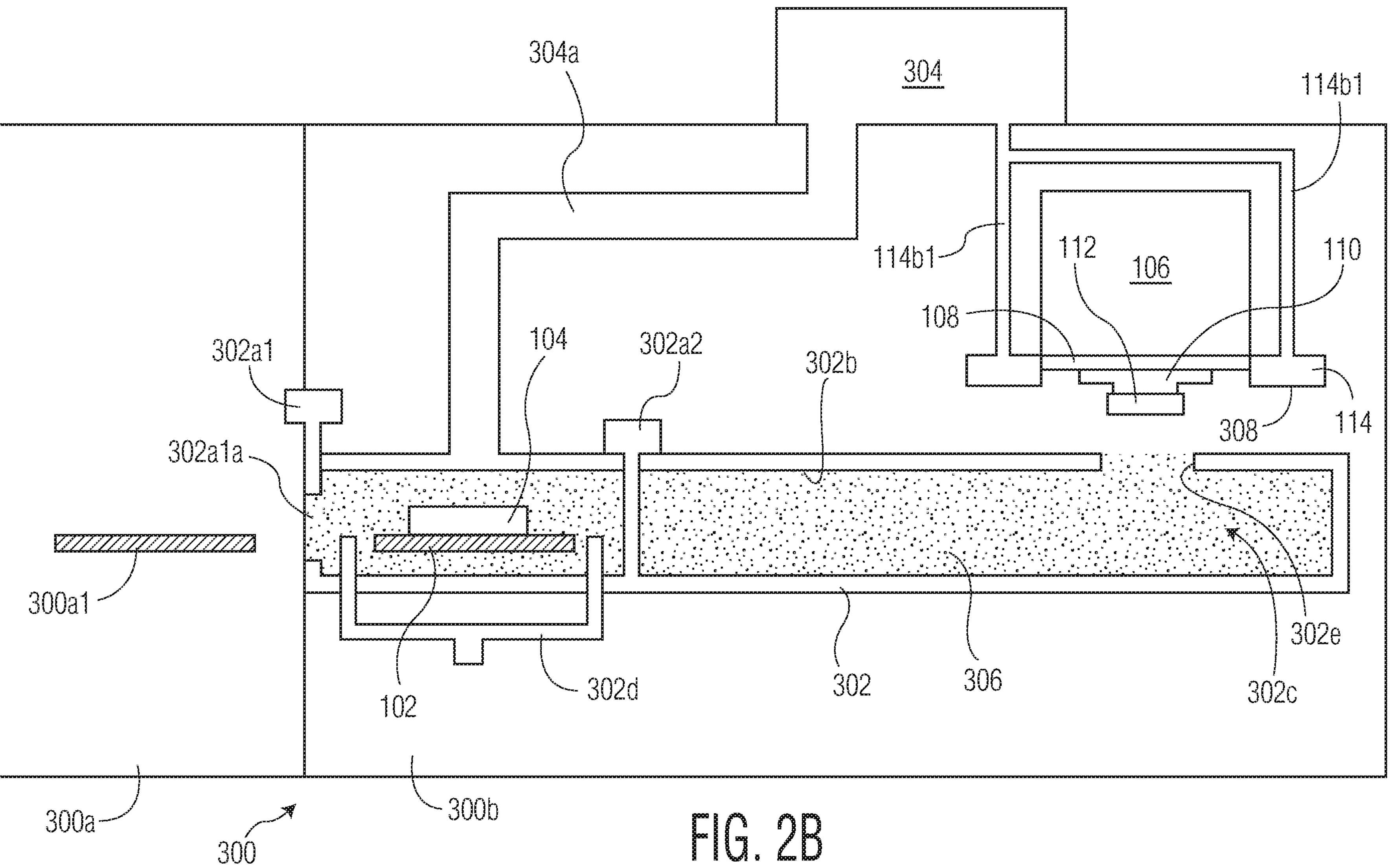

FIG. 2B

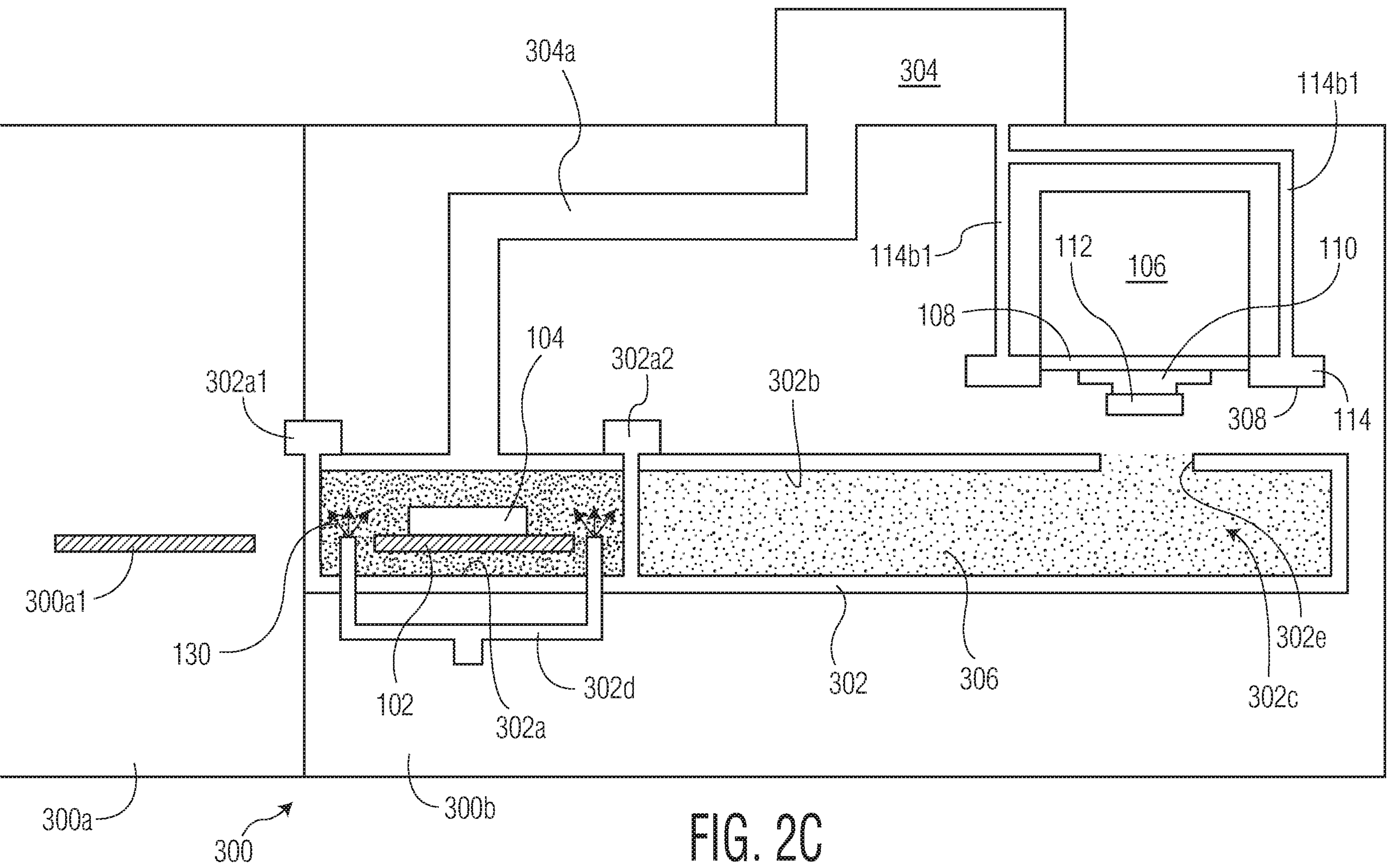

FIG. 2C

FIG. 2D

FIG. 2E

FIG. 2F

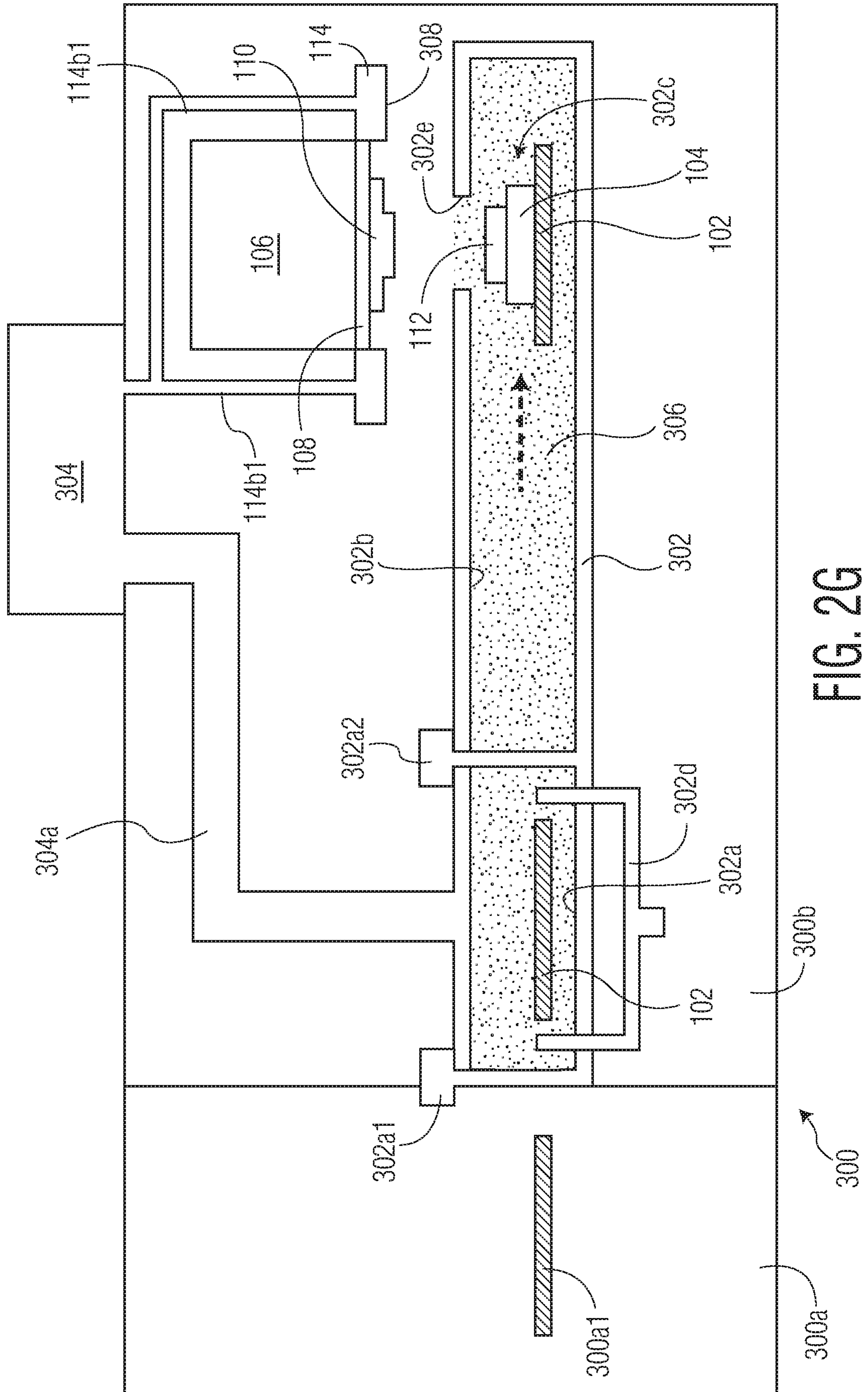

FIG. 2G

FIG. 3A

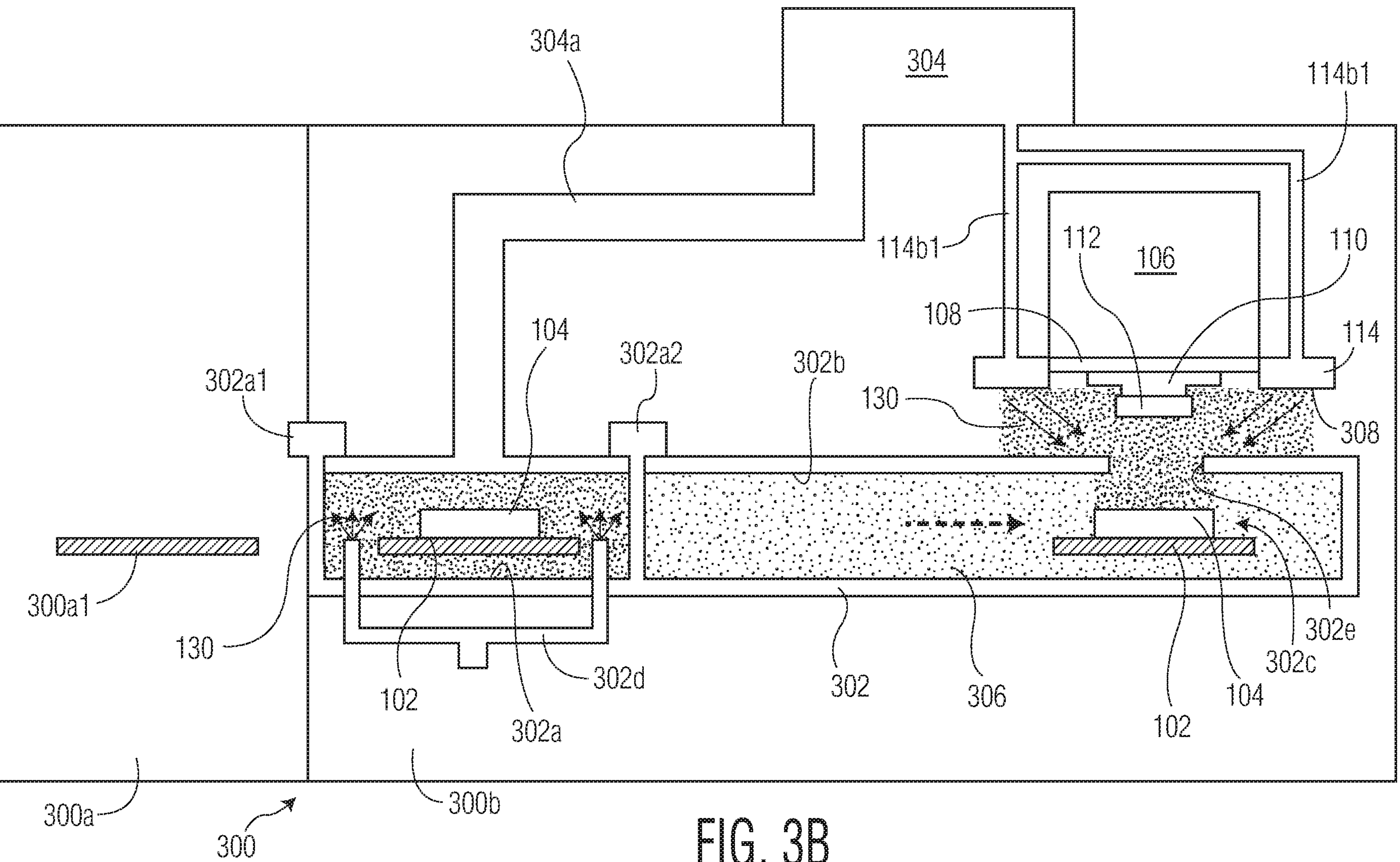

FIG. 3B

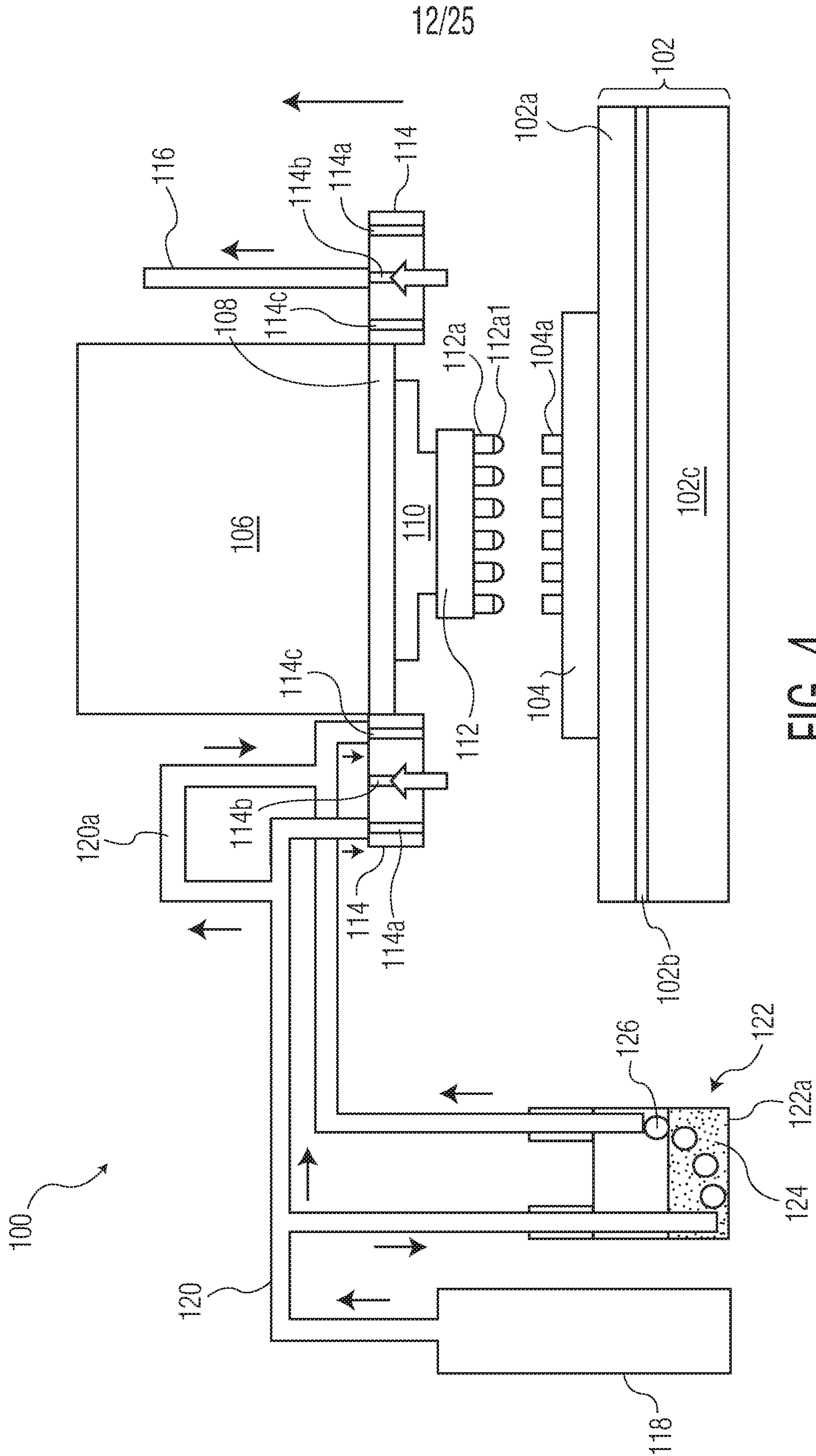

FIG. 4

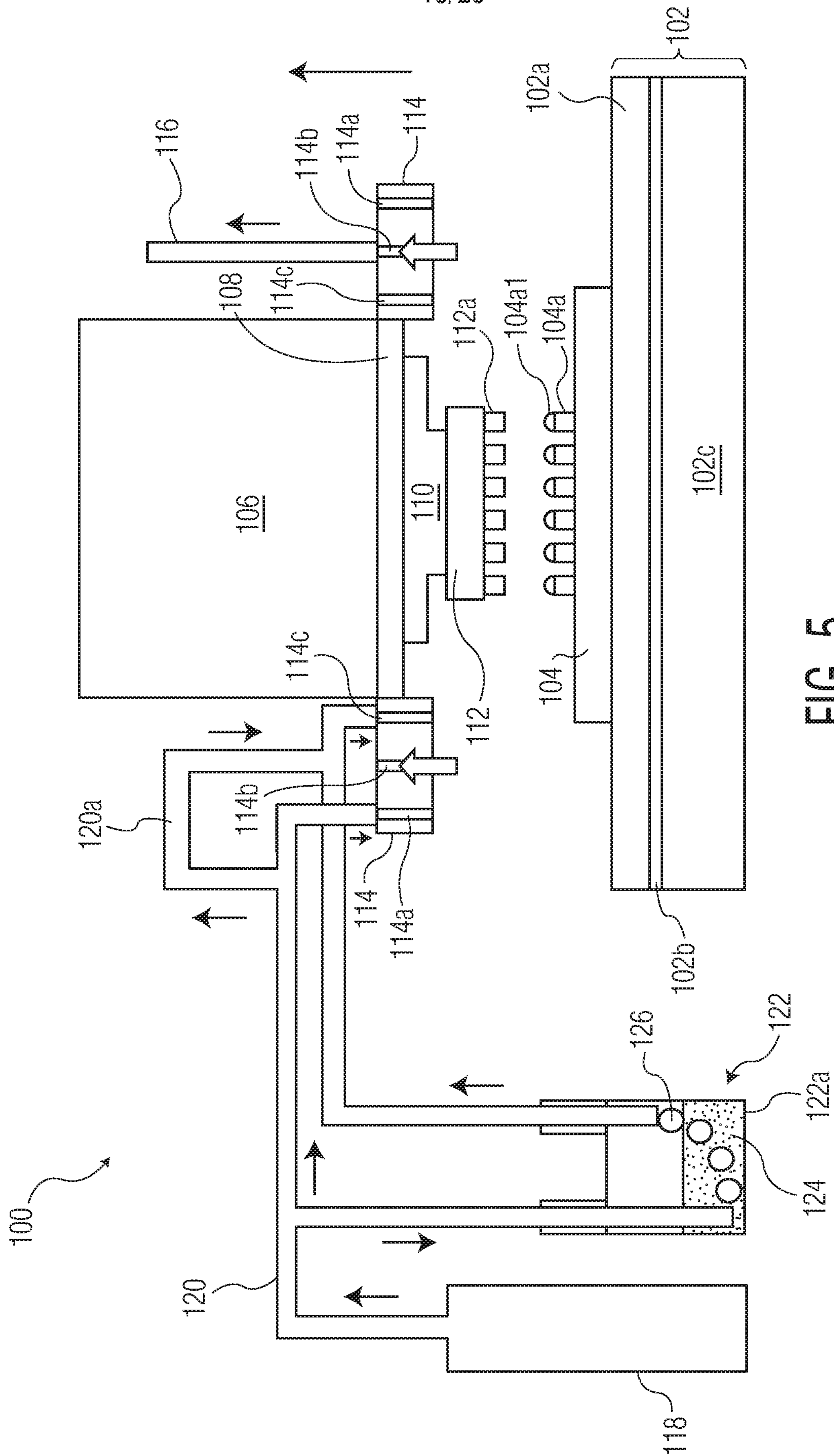

FIG. 5

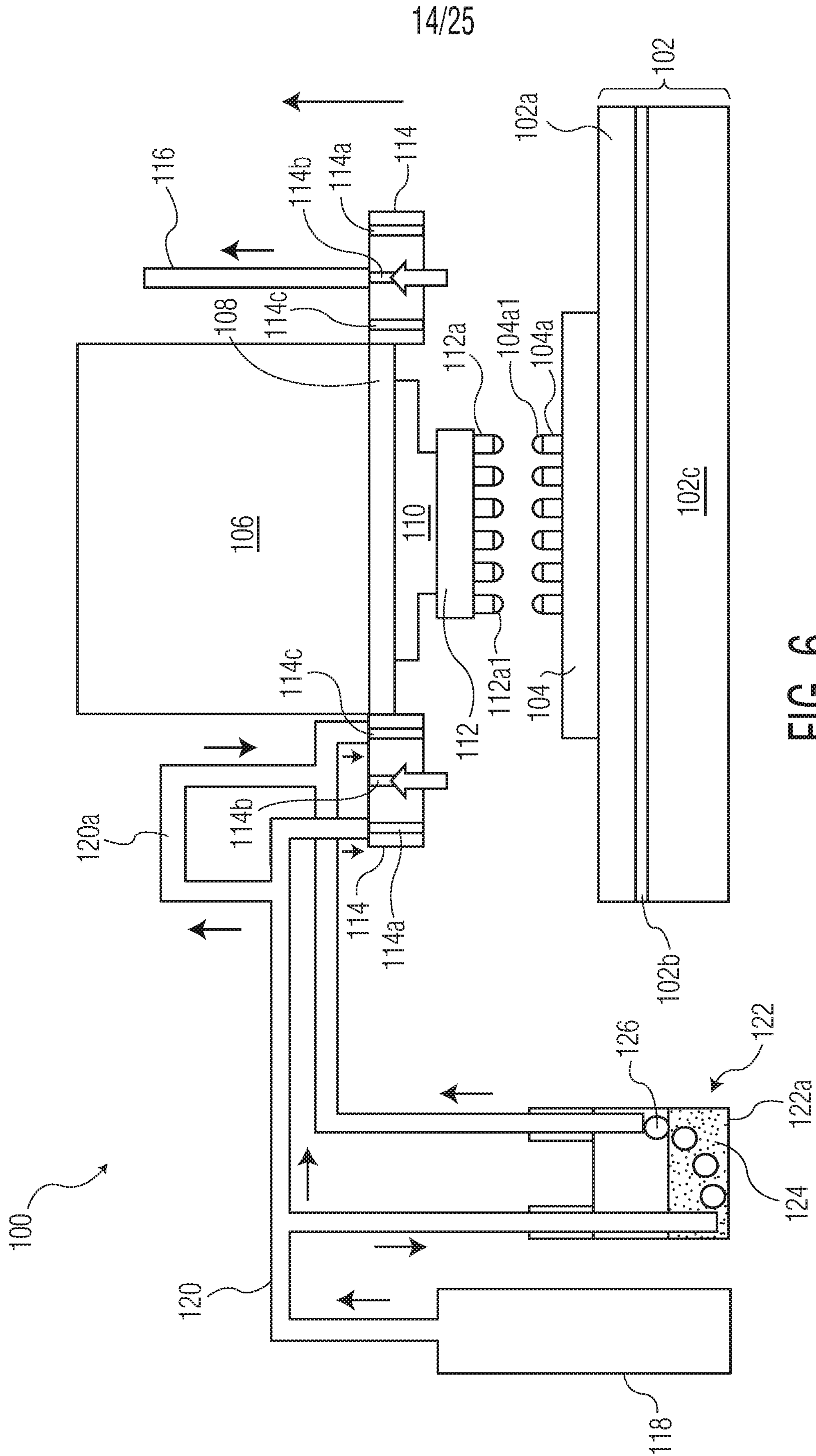

FIG. 6

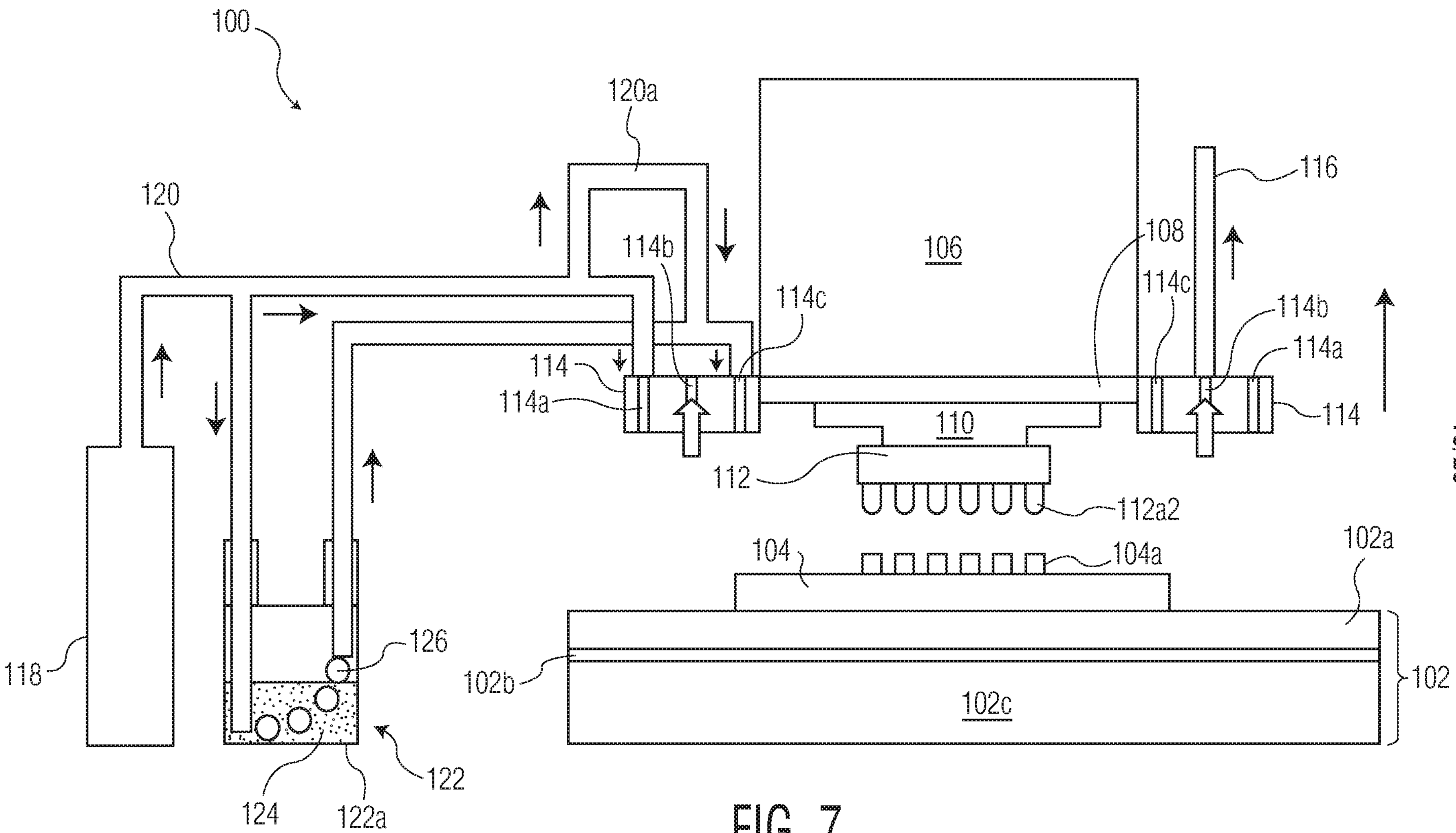

FIG. 7

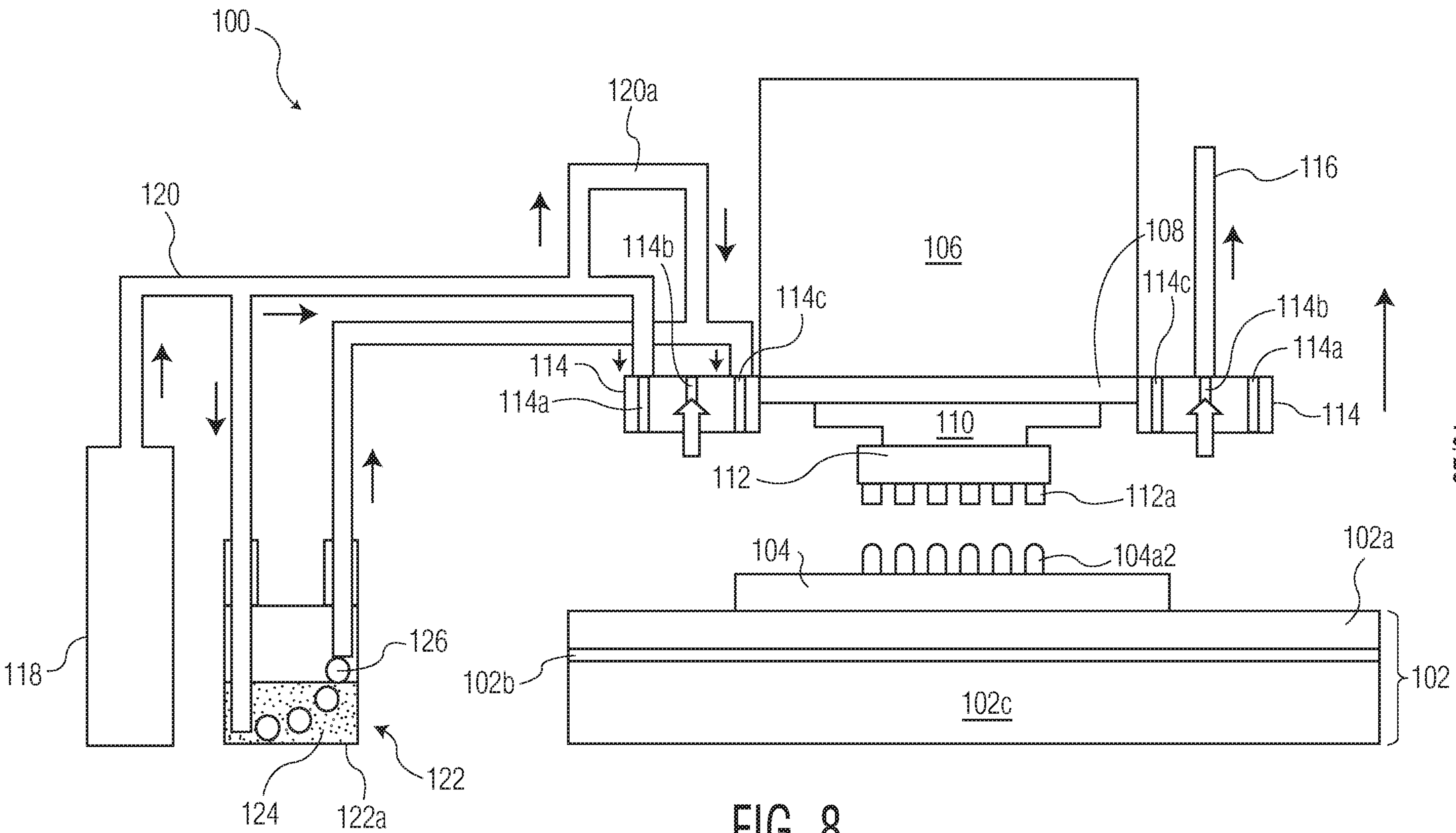

FIG. 8

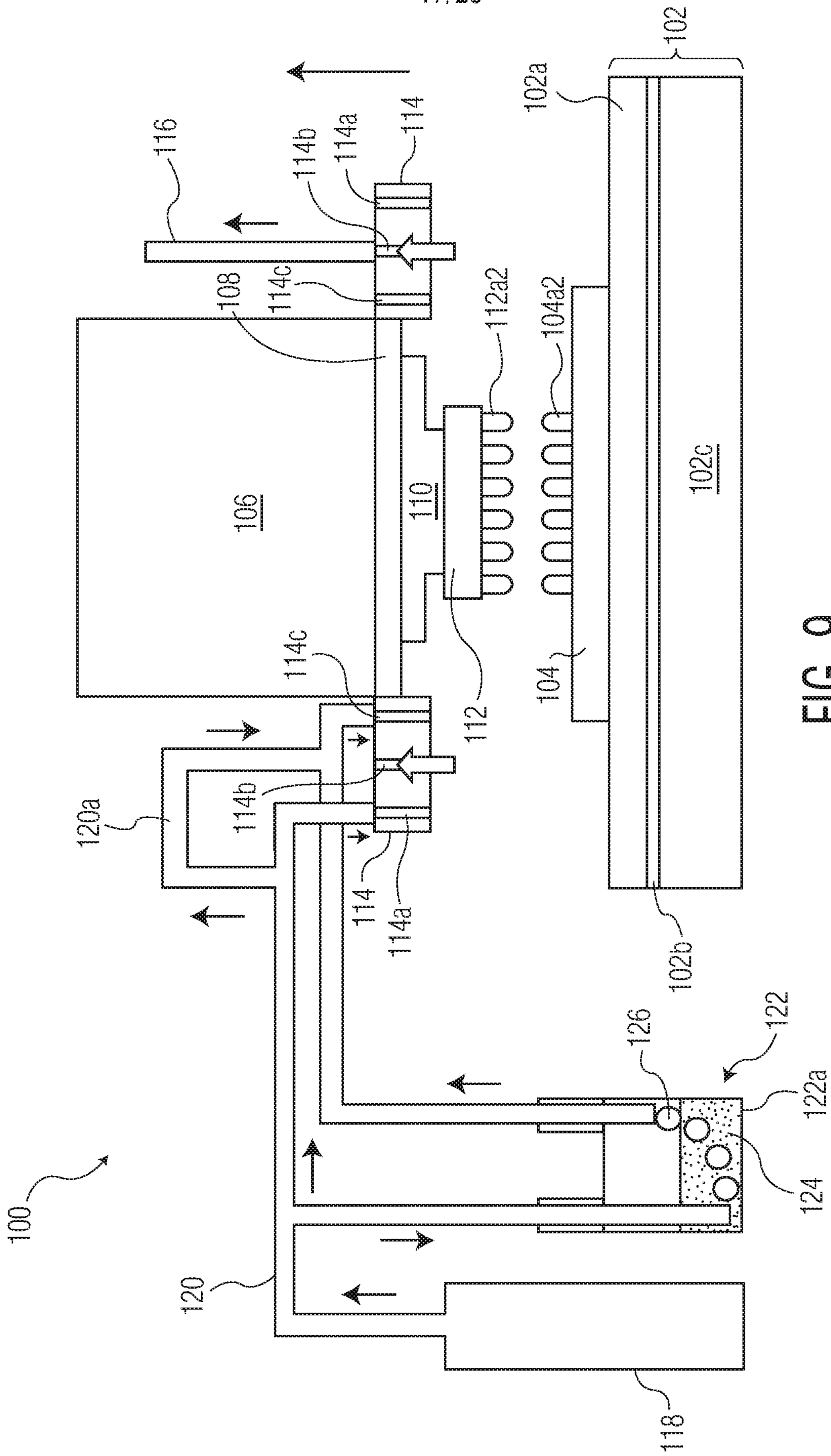

FIG. 9

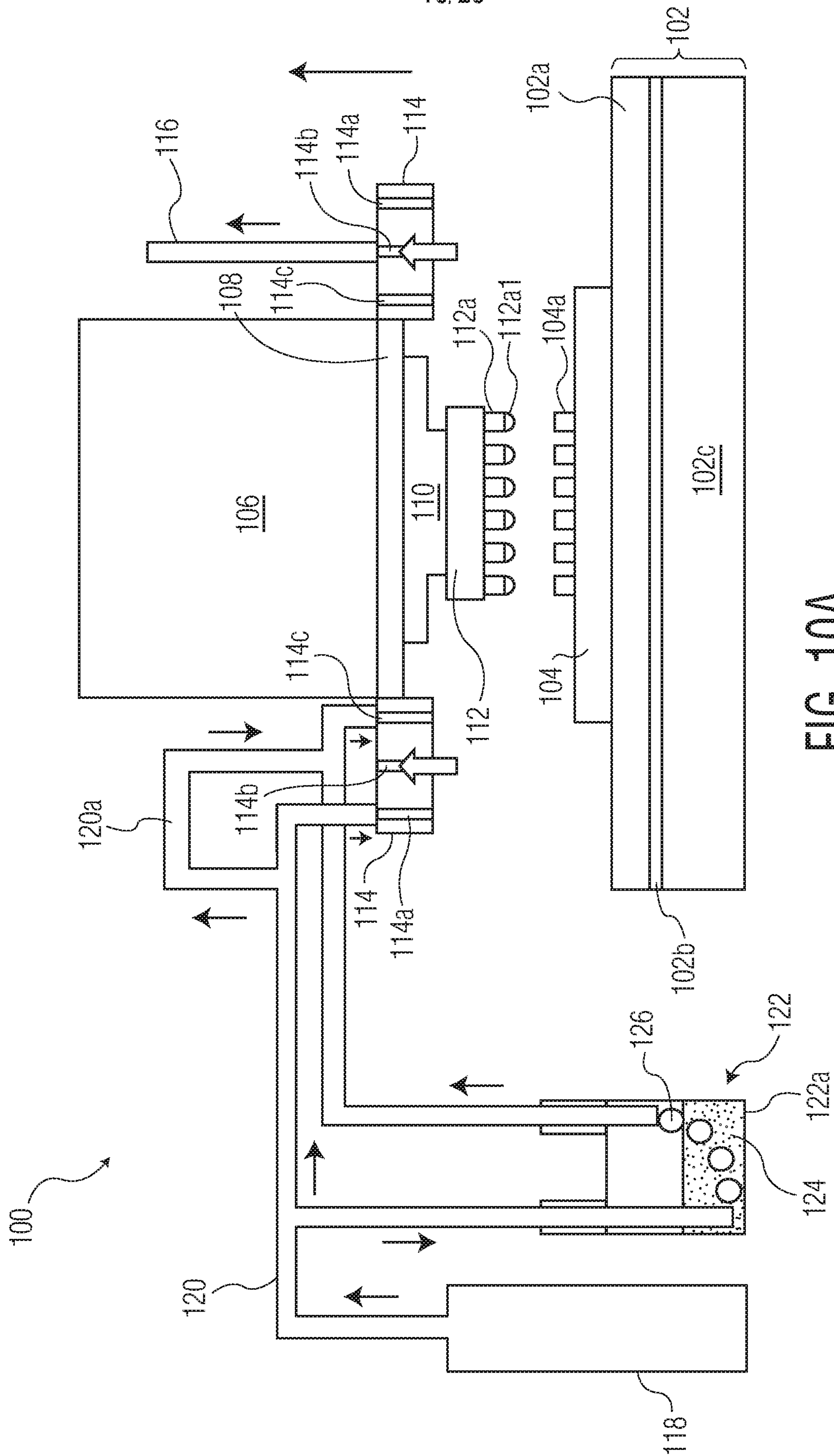

FIG. 10A

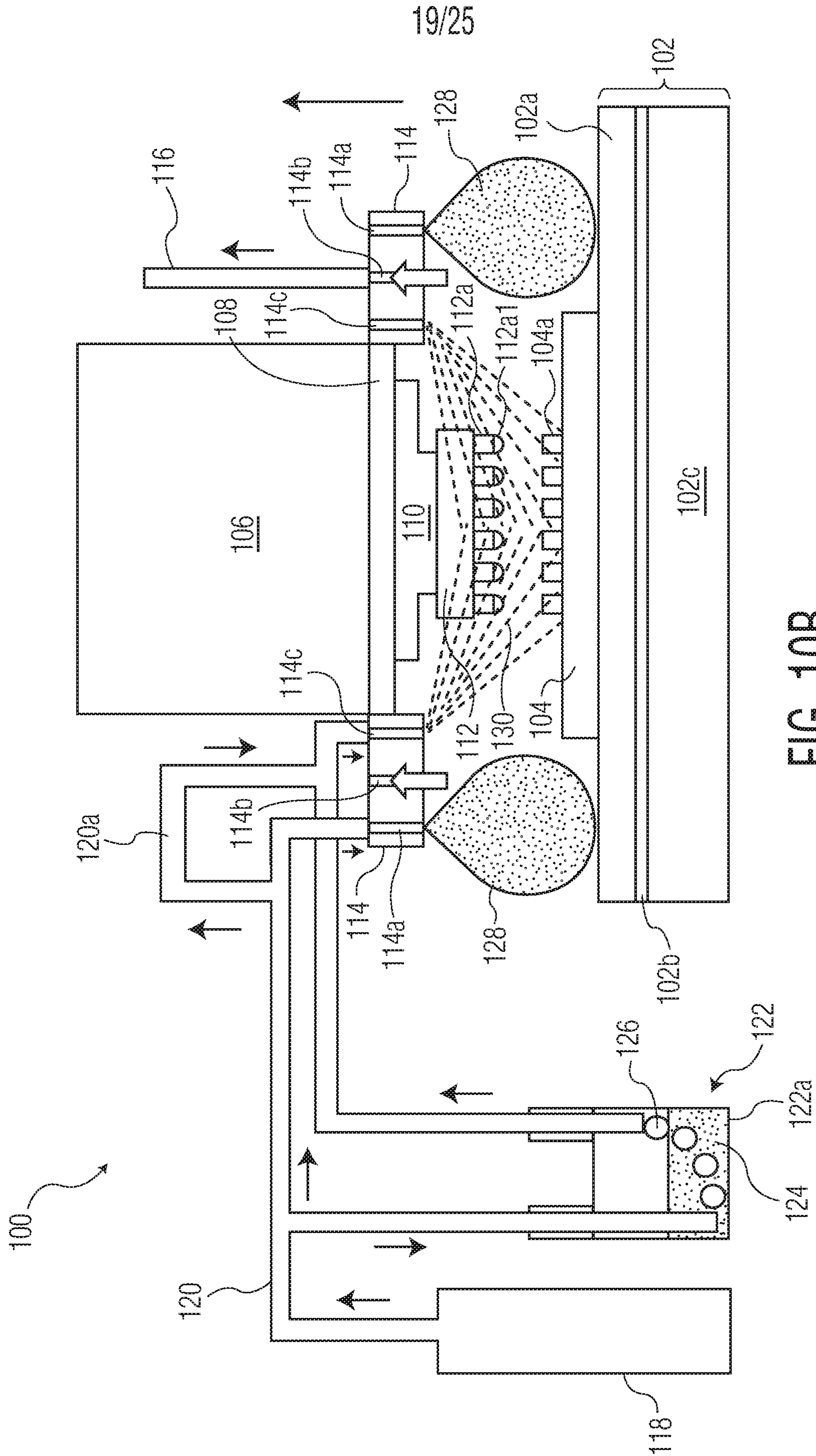

FIG. 10B

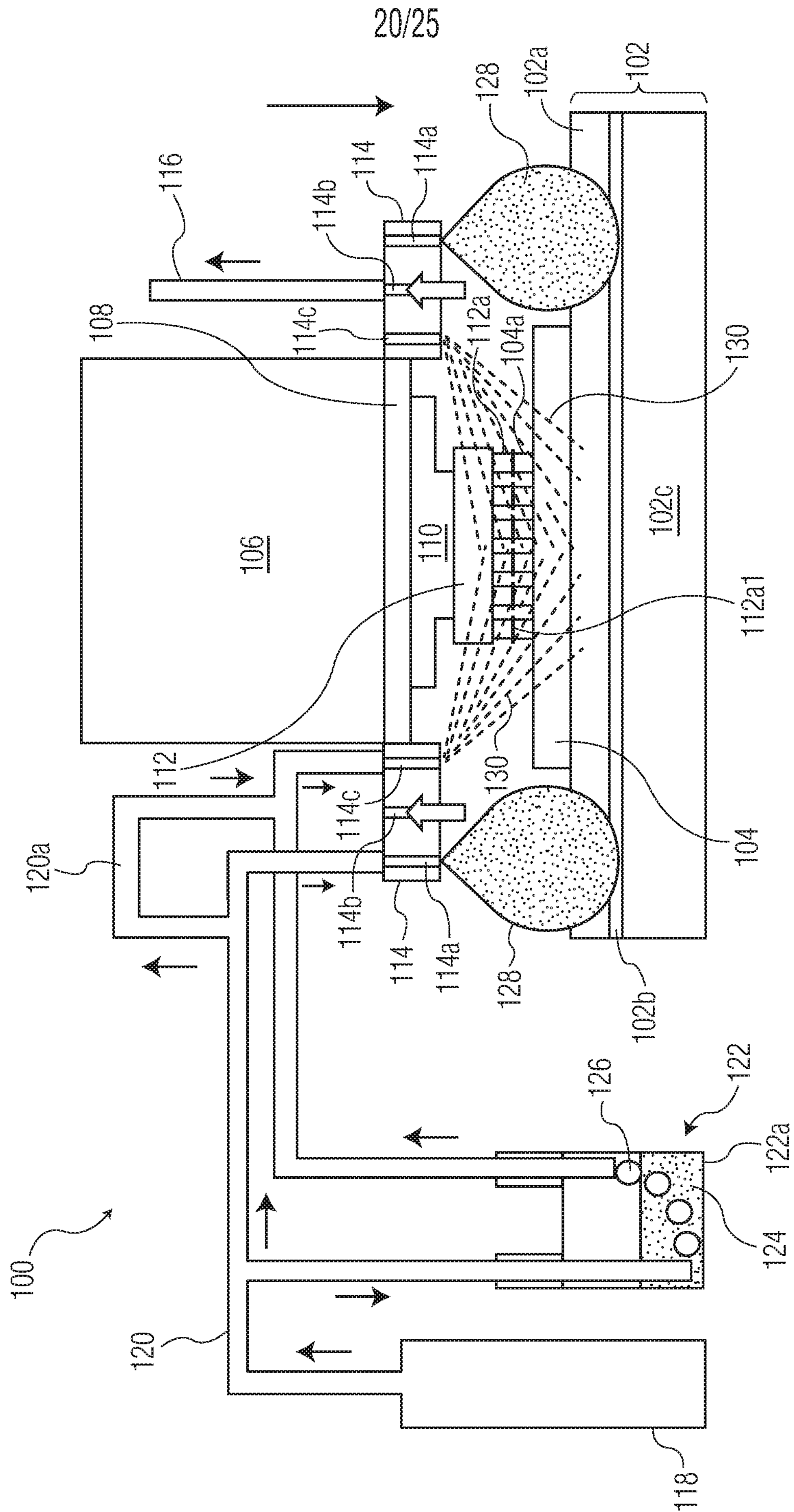

FIG. 10C

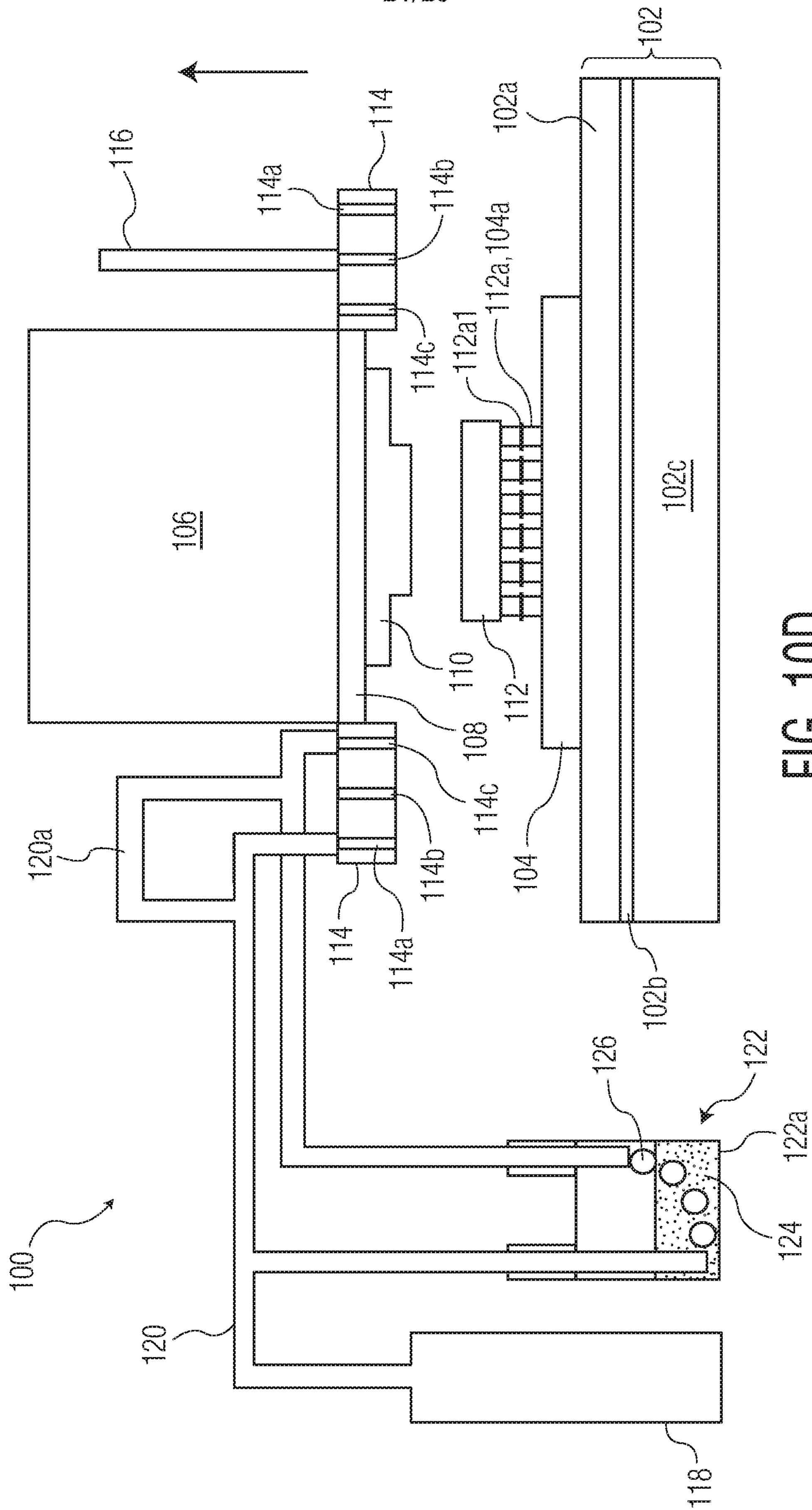

FIG. 10D

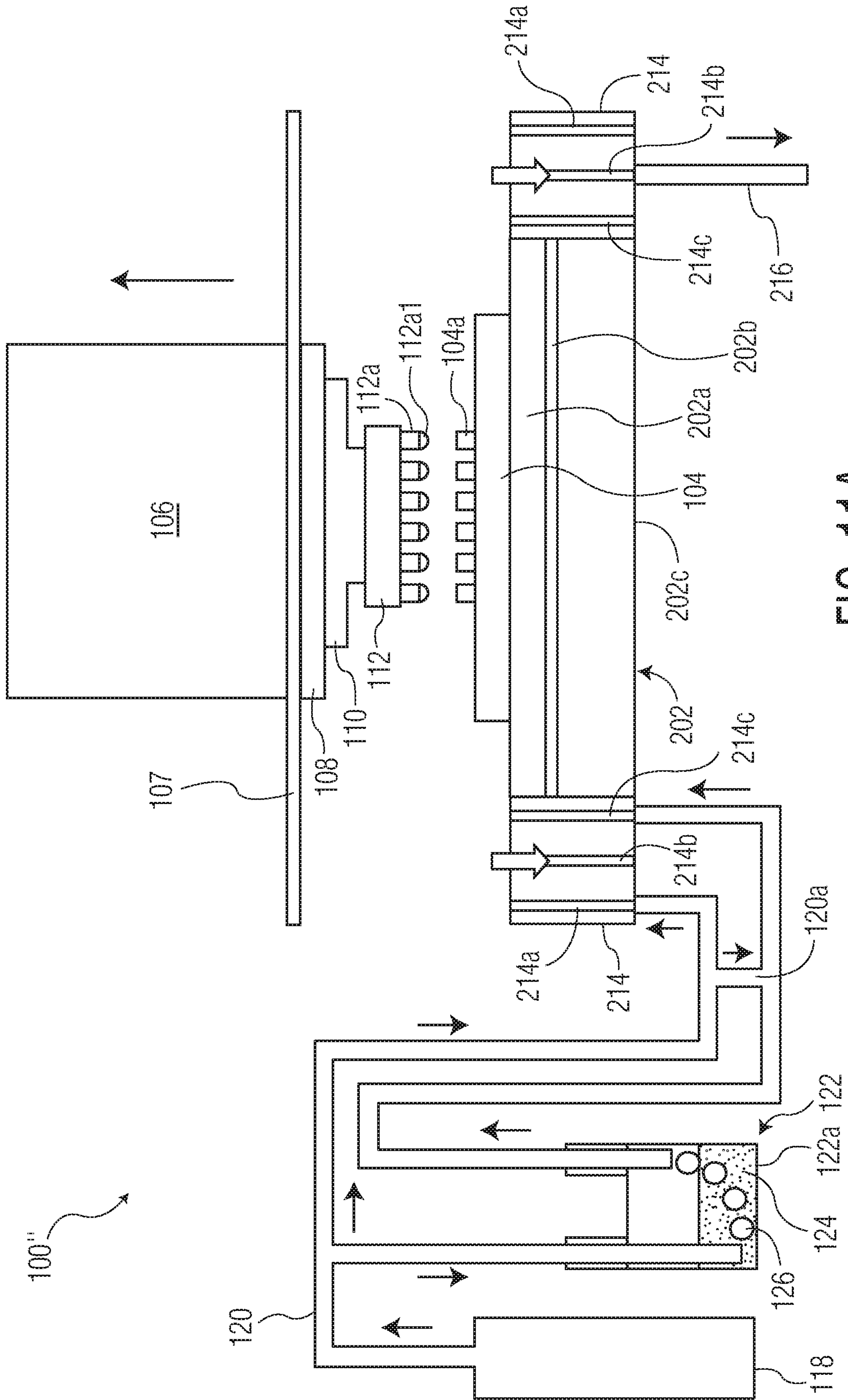

FIG. 11A

FIG. 11B

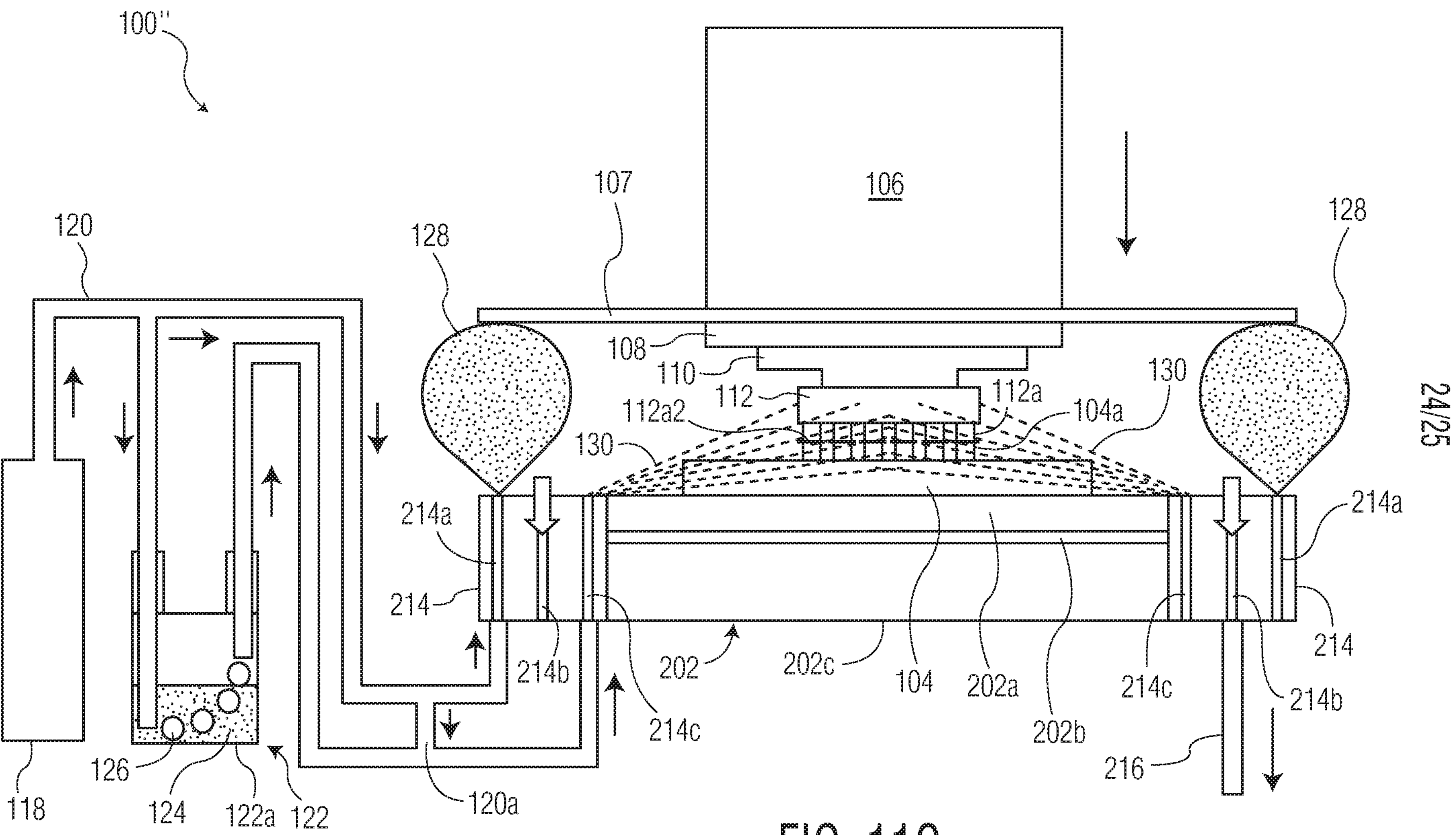

FIG. 11C

FIG. 11D

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2020/012690

A. CLASSIFICATION OF SUBJECT MATTER

H01L 23/00(2006.01)i, H01L 23/525(2006.01)i, H01L 23/528(2006.01)i, H01L 21/67(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 23/00; B23K 001/08; B23K 020/08; B23K 31/02; C23C 8/16; H01L 21/02; H01L 21/46; H01L 21/60; H01L 25/065; H01L 23/525; H01L 23/528; H01L 21/67

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: solder, bonding, oxide-reduction, acid, chamber

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2002-0130164 A1 (HIROHISA MATSUKI et al.) 19 September 2002 Paragraphs 64-337; claims 1, 13, 40, 54; and figures 3-9B, 37A, 40A-41D.	1-30
Y	US 2015-0048523 A1 (TADATOMO SUGA et al.) 19 February 2015 Paragraphs 1, 211-310; and figures 31, 34.	1-30
A	JP 2013-251404 A (TADATOMO SUGA et al.) 12 December 2013 Paragraphs 24, 42-68; and figure 2.	1-30
A	KR 10-2013-0083400 A (TOKYO ELECTRON LIMITED) 22 July 2013 The entire document.	1-30
A	US 2011-0045653 A1 (YASUHIDE OHNO et al.) 24 February 2011 The entire document.	1-30

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
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"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
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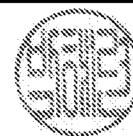
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
29 April 2020 (29.04.2020)	**29 April 2020 (29.04.2020)**

Name and mailing address of the ISA/KR	Authorized officer
International Application Division Korean Intellectual Property Office 189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea	PARK, Hye Lyun 
Facsimile No. +82-42-481-8578	Telephone No. +82-42-481-3463

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