A semiconductor device comprising a semiconductor substrate and a composite capacitor structure on the semiconductor substrate, wherein the composite capacitor structure comprises a capacitor stack comprising a lower and an upper capacitor, respectively comprising first and second dielectric materials, wherein the first and second dielectric materials are different materials and/or have different thicknesses from each other. This can minimize the voltage dependence of the capacitance of the composite capacitor structure. It is also possible to provide a composite capacitor structure on the semiconductor substrate, wherein the composite capacitor structure comprises at least a first and a second capacitor stack, each comprising a lower and an upper capacitor. The capacitors can be MIM capacitors.
CAPACITOR STRUCTURES FOR SEMICONDUCTOR DEVICE

The present invention relates to capacitor structures, in particular on a semi-conductor substrate. The invention finds particular application in MIM (Metal-Insulator-Metal) capacitors, although it is not limited thereto.

US Patent No. 6680521 B1 entitled "High Density Composite MIM Capacitor with reduced voltage dependence in semiconductor dies" discloses the layout of a stack MIM. The stack MIM is formed with an upper and a lower capacitor, and these are connected to each other in a way which results in good voltage linearity.

The present inventors have devised a technique for improving the voltage linearity further. Accordingly, some embodiments aim to provide a capacitor structure having an improved voltage linearity. Other embodiments do not necessarily improve the voltage linearity but aim to provide a capacitor structure with good capacitance density. Other embodiments aim to provide a capacitor structure which enables the voltage coefficients of capacitance (VCC) of the structure to be manipulated in order to achieve a desired effect.

In one aspect, the present invention provides a semiconductor device comprising: a semiconductor substrate; a composite capacitor structure on the semiconductor substrate, wherein the composite capacitor structure comprises a capacitor stack comprising a lower and an upper capacitor, respectively comprising first and second dielectric materials, wherein the first and second dielectric materials are different materials and/or have different thicknesses from each other.

In another aspect, the present invention provides a semiconductor device comprising: a semiconductor substrate; a composite capacitor structure on the semiconductor substrate, wherein the composite capacitor structure comprises at least a first and a second capacitor stack, each comprising a lower and an upper capacitor.
Some preferred embodiments of the invention will now be described by way of example only and with reference to the accompanying drawings, in which:

Figures 1A and 1B show normalized C-V (capacitance vs. bias voltage) curves for various dielectrics.

Figure 2 shows a graph indicating the quadratic coefficient (a) of the voltage linearity of capacitance for different dielectrics in a single layer MIM.

Figure 3 shows a graph indicating the linear coefficient (β) of the voltage linearity of capacitance for different dielectrics in a single layer MIM.

Figure 4 is a schematic section through a capacitor structure according to an embodiment of the present invention.

Figure 5 is a circuit diagram equivalent to the capacitor structure of Figure 4.

Figure 6A is a graph illustrating the linearity performance (quadratic and linear voltage coefficients of capacitance) in dependence on the dielectrics thickness for nitride.

Figure 6B is a graph illustrating the linearity performance (quadratic and linear voltage coefficients of capacitance) in dependence on the dielectrics thickness for oxide.

Figure 7A is a graph illustrating the capacitance density for nitride and oxide in a MIM capacitor.

Figure 7B is a graph illustrating the breakdown voltage for nitride and oxide in a MIM capacitor.

Figure 8 is a schematic section through a capacitor structure according to an embodiment of the present invention.

Figure 9 is a circuit diagram equivalent to the capacitor structure of Figure 8.
Figure 10 is a graph illustrating the resultant normalised capacitance density for particular embodiments of a capacitor structure constructed according to Figure 8.

In the area of mixed signal analog application devices, precise performance of passive devices is often required across different technologies. The quality of passive components such as filters, mixers, dividers, converters...etc, is often as important as the characteristics of active devices in amplifiers, oscillators...etc. MIM (metal-insulator-metal) capacitors are widely used, as compared to PIP (poly-insulator-poly) or MOS devices (varactors), as the latter two tend to exhibit depletion effects. The associated parasitic capacitance can cause undesirable capacitance variations with voltage bias fluctuations. The metal plates of MIM capacitors can provide depletion-free, high-conductance electrodes suitable for high speed applications at low cost. The quality of MIM capacitors depends on a combination of having a high capacitance (storing electrical energy in the form of electrical charges) without occupying too much area, i.e. unit capacitance density. The stability of the MIM can be regarded as the ability to maintain precise values independent of operating conditions. Shifts in capacitance with different operating frequencies, known as dispersion, can lead to high distortion in analog signals. Linearity determines the changes in capacitance with the bias voltage. As such, for high performance analog circuits, MIM desirable characteristics are low voltage and thermal linearity, non-dispersive characteristics, low leakage, high capacitance density as well as high breakdown field strength.

For a fuller understanding of the first embodiment shown in Figure 4, an explanation of a capacitance model is provided first.

In general, the normalized capacitance can be modelled as follows:

\[
\frac{dC}{C_o} = \frac{C(V) - C_o}{C_o} = \alpha V^2 + \beta V
\]  

where \( C_o \) is the capacitance at zero voltage and \( V \) is the voltage applied between the MIM electrodes, \( \alpha \) and \( \beta \) are the quadratic and linear coefficients of the MIM capacitor in ppm/V\(^2\) and ppm/V respectively. Figures 1A and 1B show normalised C-V (capacitance vs. bias voltage) curves for various dielectrics.
A trade off relationship is usually observed for the capacitance density and voltage coefficients. In other words, it is difficult to achieve both high capacitance density as well as low VCC, as shown in Figures 2 and 3.

The reader is referred to above-mentioned US patent No. 6,680,521, as regards a calculation of the overall capacitance of the capacitor stack disclosed in this patent. This document is incorporated herein by reference in its entirety for all purposes.

Figure 4 shows a section through a capacitor structure according to an embodiment of the present invention. The capacitor structure 100 appears similar to the structure disclosed in US 6,680,521, and one skilled in the art will understand, based on the disclosure of this patent and the teaching of the present specification (as well as general knowledge) how a capacitor structure shown in Figure 4 could be manufactured.

The capacitor structure 100 has lower and upper capacitors 104 and 105. The lower capacitor 104 is formed with a bottom plate 120 and a top plate 122 with a dielectric material 121 therebetween. Similarly, the upper capacitor 105 is formed with a bottom plate 124 and a top plate 126 with dielectric material 125 therebetween. In the example shown in Figure 4, the top and bottom plates are made from metal, and the capacitor structure is constructed on a semiconductor substrate.

The top plate 122 of the lower capacitor 104 is connected to the bottom plate 124 of the upper capacitor 105 by means of metallic material 131 located in vias. The capacitor structure 100 is provided with an additional plate 128 located above the upper capacitor 105. The additional plate 128 extends laterally beyond the upper capacitor 105. The additional plate 128 is connected to the top plate 126 of the upper capacitor 105 by means of metallic material 132 located in vias, generally above metallic material 131. Further, the additional plate 128 is connected to the bottom plate 120 of the lower capacitor 104 by means of metallic material 133 located in vias and metallic material 130.

Figure 5 shows a circuit diagram equivalent to the capacitor structure of Figure 4. Two contact points T1 and T2 are indicated in Figures 4 and 5, for external connection.
relation to the external connections T1 and T2, the upper and lower capacitors 105 and 104 are connected in parallel.

Given that the two terminals T1 and T2 of the stack capacitor 100 are placed such that the upper and lower capacitors 105 and 104 are connected in parallel, the total capacitance of the stack capacitor 100 is equal to the sum of the capacitances of the upper and lower capacitors respectively, i.e. $C_T = C_1 + C_2$, whereby the index T refers to the (total) capacitor structure 100, and the indexes “1” and “2” relate to the upper and lower capacitors 105 and 104.

Using the above equation (1), the capacitance of the upper and lower capacitors can be modelled as follows:

$$\frac{dC_i}{C_{i0}} = \frac{C_i(V) - C_{i0}}{C_{i0}} = \alpha_i V^2 + \beta_i V, \quad i = 1, 2 \quad \ldots (2)$$

Bearing in mind that the total capacitance of capacitor stack 100 is equal to the sum of the upper and lower capacitors 105 and 104, the voltage coefficients for the total (or composite) capacitor 100 become:

$$\alpha_T = \frac{C_{10} \alpha_1 + C_{20} \alpha_2}{C_{10} + C_{20}} ; \quad \beta_T = \frac{C_{10} \beta_1 + C_{20} \beta_2}{C_{10} + C_{20}} \quad \ldots (3),(4)$$

The present inventors have found that the resultant voltage coefficients of the composite capacitor structure 100 can be optimised (i.e. minimised) by appropriate choice of different materials as dielectric materials 121 and 125 respectively of the lower and upper capacitors. The inventors have in particular found that, if dielectric materials are chosen with opposite signs of voltage coefficients, the resultant voltage coefficients $\alpha_T$ and $\beta_T$ can have ultra low values.

The inventors have found that using oxide and nitride as dielectric materials is particularly advantageous.

The thickness of the dielectric materials 121 and 125 also influences the total capacitance and the voltage coefficients of the capacitor stack 100. In any event, the capacitance density of the stack capacitor 100 is increased when compared with a single (non-stacked) capacitor. If dielectrics 121 and 125 were made from the same material
and had the same thickness, then the total capacitance would be doubled when compared with a single capacitor.

The breakdown voltage $BV_T$ of the composite capacitor 100 is the smaller of the breakdown voltages of the upper and lower capacitors 105 and 104, i.e.:

$$BV_T = \min(BV_1, BV_2)$$ ...

Figures 6A and 6B show the characteristics curves for the linearity performance (vertical axis) in dependence on the dielectric thickness (horizontal axis), respectively for nitride and oxide. The electrical properties, capacitance density and breakdown voltage are respectively shown in Figures 7A and 7B for oxide and nitride.

The voltage coefficients $\alpha_x$ and $\beta_x$, as well as the capacitance density $C_T$ and the breakdown voltage $BV_T$ can be optimised using the above equations and choosing appropriate materials and thicknesses. The table below lists examples of combinations of the dielectrics thicknesses using oxide and nitride respectively for the upper and lower capacitors and indicating resultant values for the stack capacitor. The values are expressed in the following units: $C_x$ capacitance density in fF/$\mu\text{m}^2$; $\alpha_x$ quadratic voltage coefficients in ppm/V$^2$; $\beta_x$ linear voltage coefficients in ppm/V; $x$ refers to N: nitride; O: oxide; S: Stack.

<table>
<thead>
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<th>Dielectric THK(Å)</th>
<th>Nitride</th>
<th>Oxide</th>
<th>Stack MIM</th>
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<tr>
<td></td>
<td>$C_N$</td>
<td>$BV_N$</td>
<td>$\alpha_N$</td>
</tr>
<tr>
<td>Nitride</td>
<td>380</td>
<td>480</td>
<td>1.69</td>
</tr>
<tr>
<td>300</td>
<td>450</td>
<td>2.16</td>
<td>21.1</td>
</tr>
<tr>
<td>300</td>
<td>408</td>
<td>2.16</td>
<td>21.1</td>
</tr>
<tr>
<td>200</td>
<td>300</td>
<td>3.27</td>
<td>10.4</td>
</tr>
<tr>
<td>180</td>
<td>275</td>
<td>3.64</td>
<td>8.3</td>
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<tr>
<td>160</td>
<td>260</td>
<td>4.10</td>
<td>6.1</td>
</tr>
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</table>

From the above table it is apparent that a stack capacitor can be manufactured with a relatively high capacitance density of about 5fF/$\mu\text{m}^2$ and having a quadratic term in $VCC < 1\text{ppm/V}^2$.

It will be appreciated from the above description that certain embodiments enable the voltage dependence of the capacitance of the composite stack capacitor to be
minimized by choosing different dielectrics with different thicknesses respectively for
the upper and lower capacitor, in particular by choosing materials having VCCs of
opposite signs. However, in certain scenarios it may be unnecessary or not even
desirable to minimize the voltage dependence of the composite capacitor, and
accordingly embodiments are provided where the dielectrics of the upper and lower
capacitors 105 and 104 are made from different materials but have the same thickness,
or are made from the same material but have different thicknesses. These
embodiments are still expected to result in a composite capacitor having a higher
capacitance density than a single capacitor.

Figure 8 shows a further embodiment of a composite capacitor structure 1. This
comprises first and second capacitor stacks 2 and 3, each of which are similar in
construction to the capacitor stack shown in Figure 4. Like features carry like reference
signs and have a corresponding function. However, the external connections are
different from those shown in Figures 4 and 5. In the Figure 8 embodiment, the bottom
plate 24 of the upper capacitor 5 of the first capacitor stack 2 is electrically connected
(contact T1) to the bottom plate 60 of the lower capacitor 54 of the second capacitor
stack 3 (at contact T2'). This in turn is connected to the additional plate 68 of the
second capacitor stack 3 by means of metallic materials 73 and 70. Further, the
bottom plate 20 of the lower capacitor 4 of the first capacitor stack 2 is connected (T2)
to the additional plate 28 of the first capacitor stack 2 by means of metallic material 33
and 30. These plates are also connected to the bottom plate 64 of the upper capacitor
55 of the second capacitor stack 3 at contact T1'. An equivalent electrical circuit
diagram is shown in Figure 9. As can be seen from Figure 9, if for example, contact
points T1 and T2 are considered to be contacts of the composite capacitor 1 for
external connection, then all of the four individual capacitors are connected in parallel.
With the two capacitor stacks 2 and 3 connected to each other with their terminals
cross-wired (T1 to T2', T2 to T1') as shown in Figures 8 and 9, the linear coefficients
of the individual capacitors cancel each other out since respective pairs of the
individual transistors are biased in opposite directions. Accordingly, the resultant βT
can be further reduced.

Given the structure shown in Figures 8 and 9, inter alia the following variants are
possible:
1. All four individual capacitors use the same material with the same thickness for the dielectric materials 21, 25, 61 and 65.

2. The dielectric materials 25 and 65 are made from a first material, and the dielectric materials 21 and 61 are made from a second, different, material. All four dielectrics may or may not have the same thickness.

3. The dielectric materials 25 and 65 have a first thickness, and the dielectric materials 21 and 61 have a second, different, thickness from the first. The materials of the four individual capacitors may or may not be the same.

4. The dielectric materials 21 and 25 are made from a first material, and the dielectric materials 61 and 65 are made from a second, different, material. All four dielectrics may or may not have the same thickness.

5. The dielectric materials 21 and 25 have a first thickness, and the dielectric materials 61 and 65 have a second, different, thickness from the first. The materials of the four individual capacitors may or may not be the same.

Figure 10 illustrates capacitance density in dependence on applied voltage based on an example of a composite capacitor according to Figure 8, whereby the lower capacitors 4 and 54 use oxide as dielectric materials, and the upper capacitors 5 and 55 use nitride as dielectric material. The respective thicknesses of the dielectric materials were chosen to be 408 Angstrom (40.8nm) for oxide and 300 Angstrom (30nm) for nitride so that the quadratic and linear voltage coefficients and the capacitance density of the individual capacitors were as follows:

\[
a_{\text{oxide}} = -26.9 \text{ppm/V}^2; P_{\text{oxide}} = 57.1 \text{ ppm/V}; C_{\text{ox}} = 0.98 \text{fF/m}^2;
\]

\[
a_{\text{nitride}} = 17.4 \text{ppm/V}^2; P_{\text{nitride}} = -5.1 \text{ ppm/V}; C_{\text{nit}} = 2.16 \text{fF/m}^2;
\]

This corresponds to line 3 of the above table. The capacitance density in dependence on applied voltage for each individual capacitor 4, 5, 54, 55 is represented by circles (nitride) and squares (oxide) in Fig. 10.

For each capacitor stack 2 and 3, the resultant quadratic and linear voltage coefficients and capacitance density became:

\[
a_{\text{stack}} = 3.53 \text{ppm/V}^2; p_{\text{stack}} = 14.3 \text{ppm/V}; C_{\text{stack}} = 3.14 \text{fF/m}^2;
\]
This is represented by the curves "Stack N+0" (filled-in diamonds) and "Stack N+0_r" (triangles) in Fig. 10. The suffix ",r" indicates that the voltage of one of the stack capacitors is applied in reverse when compared with the other stack capacitor, as results from the "cross-coupling" of the two stacks 2, 3 by means of lines 10, 11 (see in particular Fig. 9).

By cross-coupling the stack capacitors 2 and 3 as per Figures 8 and 9, the linear term \( \beta \) of the voltage coefficient of the composite capacitor structure 1 was significantly reduced further, or virtually eliminated. The cross-coupled capacitor structure had a quadratic voltage coefficient \( a_{cs} \) of 3.5ppm/V\(^2\), with \( \beta_{cs} \) having been reduced to 0 for most practical purposes. The capacitance density \( C_{cs} \) of the cross-coupled capacitor structure was 3.04fF/m\(^2\). This is represented by the curve "CS" (empty diamonds) in Fig. 10.

It will be understood that other combinations of dielectric materials and/or thicknesses will reduce or virtually cancel the voltage coefficients of the composite capacitor, and one skilled in the art will not have any difficulties to identify such combinations, using the present specification as guidance.

Whilst complete capacitor structures and their wiring have been described above, it will be appreciated that he invention extends to "incomplete" capacitor structures and complete or incomplete capacitor structures without their wiring. For example, the invention extends to embodiments similar to the Figure 4 embodiment but with the additional plate 128 and possibly some or all of the metallic material 130, 132 and 133 omitted. Capacitor structures according to such embodiments may be useful when used in combination with other devices which complete the connections as per the Figure 4 embodiment. It is also conceivable that wiring and/or the additional plate 128 and metallic material 130, 132 and 133 is retro-fitted to such an "incomplete" capacitor structure. Similar considerations apply with respect to other embodiments disclosed herein.

Although the invention has been described in terms of preferred embodiments as set forth above, it should be understood that these embodiments are illustrative only and that the claims are not limited to those embodiments. Those skilled in the art will be able to make modifications and alternatives in view of the disclosure which are
contemplated as falling within the scope of the appended claims. Each feature disclosed or illustrated in the present specification may be incorporated in the invention, whether alone or in any appropriate combination with any other feature disclosed or illustrated herein.
CLAIMS:

1. A semiconductor device comprising:
   a semiconductor substrate;
   a composite capacitor structure on the semiconductor substrate, wherein the
   composite capacitor structure comprises a capacitor stack comprising a lower and an
   upper capacitor, respectively comprising first and second dielectric materials, wherein
   the first and second dielectric materials are different materials and/or have different
   thicknesses from each other.

2. A semiconductor device according to Claim 1, wherein the first and second
dielectric materials are different materials.

3. A semiconductor device according to Claim 1 or 2, wherein the linear voltage
coefficients of capacitance respectively of the first and second dielectric materials have
opposite signs.

4. A semiconductor device according to any one of Claims 1 to 3, wherein the
quadratic voltage coefficients of capacitance respectively of the first and second
dielectric materials have opposite signs.

5. A semiconductor device according to any one of Claims 1 to 4, wherein one of
the first and second dielectric materials comprises an oxide and the other comprises a
nitride.

6. A semiconductor device according to any one of Claims 1 to 5, wherein the
thickness of the first dielectric material is different from the thickness of the second
dielectric material.

7. A semiconductor device according to any one of Claims 1 to 6, wherein the
lower capacitor and the upper capacitor are connected, or are arranged to be
connected, in parallel.

8. A semiconductor device according to any one of Claims 1 to 7, wherein the
lower capacitor and the upper capacitor each have a lower plate and an upper plate,
wherein the lower plate of the upper capacitor defines a first terminal of the composite capacitor structure and is connected to the upper plate of the lower capacitor, and the device further comprises, or is arranged to receive, a second terminal of the composite capacitor structure connected, or arranged to be connected, to the upper plate of the upper capacitor and the lower plate of the lower capacitor.

9. A semiconductor device comprising:
   a semiconductor substrate;
   a composite capacitor structure on the semiconductor substrate, wherein the composite capacitor structure comprises at least a first and a second capacitor stack, each comprising a lower and an upper capacitor.

10. A semiconductor device according to Claim 9, wherein the dielectric material of the upper capacitor of the first and second stacks comprises a first dielectric material, and the dielectric material of the lower capacitor of the first and second stacks comprises a second dielectric material, wherein the first and second dielectric materials are different.

11. A semiconductor device according to Claim 9, wherein the dielectric material of the upper and lower capacitors of the first stack comprises a first dielectric material, and the dielectric material of the upper and lower capacitors of the second stack comprises a second dielectric material, wherein the first and second dielectric materials are different.

12. A semiconductor device according to Claim 10 or 11, wherein the linear voltage coefficients of capacitance of the first and second dielectric materials have opposite signs.

13. A semiconductor device according to any one of Claims 10 to 12, wherein the quadratic voltage coefficients of capacitance of the first and second dielectric materials have opposite signs.

14. A semiconductor device according to any one of Claims 10 to 13, wherein one of the first and second dielectric materials comprises an oxide, and the other comprises a nitride.
15. A semiconductor device according to any one of Claims 9 to 14, wherein the dielectric material of at least one of the capacitors of the device has a different thickness from the dielectric material of at least one further capacitor of the device.

16. A semiconductor device according to any one of Claims 9 to 15, wherein all of the capacitors are connected, or are arranged to be connected, in parallel.

17. A semiconductor device according to any one of Claims 9 to 16, wherein each lower and upper capacitor has a lower plate and an upper plate, wherein the lower plate of the upper capacitor of the first stack defines a first terminal of the composite capacitor structure and is connected to the upper plate of the lower capacitor of the first stack and is connected, or is arranged to be connected, to the upper plate of the upper capacitor of the second stack and to the lower plate of the lower capacitor of the second stack, and the device further comprises, or is arranged to receive, a second terminal of the composite capacitor structure connected, or arranged to be connected, to the upper plate of the upper capacitor of the first stack and to the lower plate of the lower capacitor of the first stack and to the lower plate of the upper capacitor of the second stack and to the upper plate of the lower capacitor of the second stack.

18. A semiconductor device according to any one of Claims 9 to 17, wherein the substrate is a common substrate for the two capacitor stacks.

19. A semiconductor device according to any one of Claims 1 to 18, wherein each capacitor is a MIM (Metal-Insulator-Metal) capacitor.

20. A semiconductor device according to any one of Claims 1 to 19, wherein the dielectric material of each individual capacitor is substantially uniform.
Fig. 10
### A. CLASSIFICATION OF SUBJECT MATTER

**INV.** H01G/7/06 H01L21/02

According to International Patent Classification (IPC) or to both national classification and IPC.

### B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

- H01G
- H01L
- H02H

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched.

Electronic database consulted during the international search (name of data base and, where practical, search terms used)

**EPO-Internal**

### C. DOCUMENTS CONSIDERED TO BE RELEVANT

<table>
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<th>Citation of document, with indication, where appropriate, of the relevant passages</th>
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<td>wo 2008/047000 A2 (COMMISSARIAT ENERGIE ATOMIQUES [FR] ; ST MICROELECTRONICS CROLLES 2 [FR]) 24 April 2008 (2008-04-24) abstract page 3, line 15 - line 20 page 4, line 9 - page 5, line 25 page 7, lines 10-31 - page 12, lines 1-5 page 14, lines 1-10 - page 15, lines 15-20 page 16, lines 20-31; claims 1,4; figure 1</td>
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* Further documents are listed in the continuation of Box C.  
* See patent family annex.

* Special categories of cited documents:

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**Date of the actual completion of the international search**

18 March 2011

**Date of mailing of the international search report**

24/03/2011

**Name and mailing address of the ISA/**

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**Authorized officer**

Dessaux, Christophe
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