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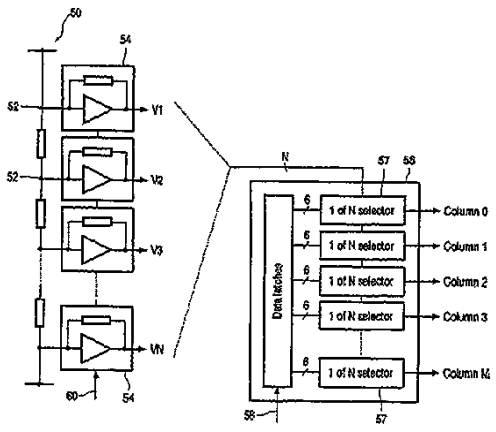
(54)【発明の名称】アクティブマトリックスディスプレイデバイス

(57)【要約】
ディスプレイは、別々の信号レベルラインに可能な全ての画素駆動信号レベルを発生する回路（５０）を有する。バッファ（５４）は各信号レベルラインと関連する。バッファの出力は列に選択的に切換えて供給しうる。各列に対する信号レベルはメモリ（７２）に記憶され、バッファは記憶された信号レベルに応じて制御される。バッファの応答は出力負荷に著しく依存し、バッファの出力負荷は、バッファ出力を与える必要のある列の個数の関数として極めて大きく変化する。バッファを、記憶した信号レベルに応じて制御し、いかなる出力負荷に対してもバッファを安定化させる。



【特許請求の範囲】
【請求項１】
行及び列に配置された液晶画素のアレイを有するディスプレイデバイスであって、画素駆動信号が与えられる列導体を画素の各列が共有し、画素駆動信号を発生する列アドレス回路が設けられており、この列アドレス回路は、別々の信号レベルラインに可能な全ての駆動信号レベルを発生する回路と、各信号レベルラインと関連するバッファとを有しており、バッファの出力は列に選択的に切換えて供給され、列アドレス回路が更に、各列に与える信号レベルを記憶するメモリを有し、バッファは記憶された信号レベルに応じて制御されるようになっているディスプレイデバイス。
【請求項２】
請求項１に記載のディスプレイデバイスにおいて、各バッファに対するバイアス電流が、バッファ出力を切換えて供給すべき列の個数に応じて制御されるようになっているディスプレイデバイス。
【請求項３】
請求項１に記載のディスプレイデバイスにおいて、各信号レベルラインが複数のバッファと関連しており、これら複数のバッファの各々は互いに異なる出力負荷に適しており、バッファ出力を切換えて供給すべき列の個数に応じて前記複数のバッファの１つを選択するようになっているディスプレイデバイス。
【請求項４】
請求項３に記載のディスプレイデバイスにおいて、各信号レベルラインに２つのバッファが関連しているディスプレイデバイス。
【請求項５】
請求項１に記載のディスプレイデバイスにおいて、各バッファが複数の出力段を有し、使用する出力段の個数が、バッファ出力を切換えて供給すべき列の個数に応じて制御されるようになっているディスプレイデバイス。
【請求項６】
請求項１に記載のディスプレイデバイスにおいて、このディスプレイデバイスが更に、追加のバッファを有し、この追加のバッファは、個々のバッファ出力を切換えて供給すべき列の個数が列の総数の半分を超えた場合に用いられるようになっているディスプレイデバイス。
【請求項７】
請求項６に記載のディスプレイデバイスにおいて、複数の追加のバッファが設けられ、これら追加のバッファは、個々のバッファ出力を切換えて供給すべき列の個数が列の総数の予め決定した一部を超えた場合に用いられるようになっているディスプレイデバイス。
【請求項８】
請求項１～７のいずれか一項に記載のディスプレイデバイスにおいて、各画素が薄膜トランジスタスイッチング装置と液晶セルとを有し、各列の画素が、当該列における画素の薄膜トランジスタのゲートに接続された行導体を共有しており、行駆動回路が行の画素のトランジスタをスイッチング制御する行アドレス信号を生じるようになっているディスプレイデバイス。
【請求項９】
行及び列に配置された液晶画素のアレイを有するディスプレイデバイスに画素駆動信号を供給する画素駆動信号供給方法であって、
可能な全ての画素駆動信号レベルを発生させる工程と、
各画素駆動信号レベルを関連のバッファに供給する工程と、
画素の行に対する必要な画素駆動信号をメモリ内に記憶する工程と、
各画素駆動信号によりアドレスすべき行の画素の必要数を計算する工程と、
この計算されて画素の必要数に応じてバッファを制御する工程と、
アドレスすべき行に対する行アドレス周期中、バッファの出力を列上に切換えて供給する工程と

を有する画素駆動信号供給方法。
【請求項１０】
請求項９に記載の画素駆動信号供給方法において、バッファを制御する前記工程が、バッファに適切なバイアス電流を供給する工程を有している画素駆動信号供給方法。
【請求項１１】
請求項９に記載の画素駆動信号供給方法において、バッファを制御する前記工程が、各画素駆動信号レベルに対し二者択一のバッファを選択する工程を有している画素駆動信号供給方法。
【請求項１２】
請求項９に記載の画素駆動信号供給方法において、バッファを制御する前記工程が、各バッファに接続すべき複数の出力段を選択する工程を有している画素駆動信号供給方法。
【請求項１３】
請求項９に記載の画素駆動信号供給方法において、バッファを制御する前記工程が、個々のバッファ出力を切換えて供給する必要のある列の個数が列の総数の半分を超える場合に個々のバッファの出力負荷を共有する追加のバッファを用いる工程を有している画素駆動信号供給方法。
【請求項１４】
請求項１３に記載の画素駆動信号供給方法において、バッファ出力を切換えて供給する必要のある列の個数が列の総数のうち予め決定した一部を超える場合に１つ以上のバッファの出力負荷を共有する複数の追加のバッファを用いる画素駆動信号供給方法。
【請求項１５】
別々の信号レベルライン上に可能なあらゆる駆動信号レベルを発生する回路と、各信号レベルラインと関連するバッファとを有し、液晶ディスプレイの列を駆動する列駆動回路であって、バッファの出力が列出力上に選択的に切換えて供給されるようになっており、列駆動回路が更に、各列に与えるべき信号レベルを記憶するメモリを有しており、バッファは記憶された信号レベルに応じて制御されるようになっている列駆動回路。
【発明の詳細な説明】
【技術分野】
【０００１】
本発明は、アクティブマトリックスディスプレイデバイス、特にディスプレイの画素に駆動信号を供給するのに用いる回路に関するものである。
【０００２】
アクティブマトリックスディスプレイデバイスは、代表的に、行及び列に配置した画素のアレイを有する。各行の画素は、この行における画素の薄膜トランジスタのゲートに接続された行導体を共有している。各列の画素は、画素駆動信号が与えられる列導体を共有している。行導体における信号は、トランジスタがターンオンしているかターンオフしているかを決定するものであり、この行導体における高電圧パルスによりトランジスタがターンオンすると、列導体からの信号が液晶材料の領域に流され、これにより液晶材料を光透過特性に変える。行電極パルスを除去した後にも液晶材料上に電圧が維持されているようにするために、画素構造の一部として追加の蓄積キャパシタを設けることができる。米国特許第 5130829号明細書には、アクティブマトリックスディスプレイデバイスの設計がより詳細に開示されている。
【０００３】
アクティブマトリックスディスプレイデバイスに対するフレーム（フィールド）周期では、画素の行を短時間でアドレスする必要があり、従って、液晶材料を所望の電圧レベルに充電又は放電させるためには、トランジスタの電流駆動能力に条件が課せられる。これらの電流条件を満足させるためには、薄膜トランジスタに印加されるゲート電圧が、約３０ボルトだけ離れた値間で変動する必要がある。例えば、（ソースに対して）約－１０ボルト又はそれよりも低いゲート電圧を印加することによりトランジスタをターンオフでき、一方、液晶材料を充分に急速に充電又は放電させるのに必要とするソース‐ドレイン電流

を生じるのに充分にトランジスタをバイアスするには、約２０ボルト又はそれよりも高い電圧が必要になる。

【０００４】

行導体でこのように大きな電圧変動を得るには、高電圧素子を用いて行駆動回路を構成する必要がある。

【０００５】

列導体に与えられる電圧は、代表的に約１０ボルトだけ変化し、この変化は、液晶材料を白及び黒状態間で駆動するのに要する駆動信号間の差を表わす。列導体における電圧変動を低減させうる種々の駆動方式が提案されている為、列駆動回路には低電圧素子を用いることができる。いわゆる“共通電極駆動方式”においては、液晶材料層の全体に接続された共通電極が発振電圧に駆動される。いわゆる“４レベル駆動方式”は、容量結合効果を用いて列導体における電圧変動を低減させるために、より複雑な行電極波形を用いる。

【０００６】

これらの駆動方式によれば、列駆動回路に対し低電圧素子を用いうるようになる。しかし、列駆動回路では、複雑性及び電力の非効率性が依然として大きい。各行が順番にアドレスされ、いずれの１行の行アドレス期間中にも、各列に画素信号が与えられる。従来では、行アドレス周期の全期間に亙り列中の画素を駆動信号レベルに保持するために、各列にバッファが設けられていた。この多数のバッファの為に電力消費量が高くなった。

【０００７】

群の列間でバッファを共有する多重方式を形成することが提案された。バッファの出力は群の列に順番に切換る。バッファが１つの列に信号を与えている際には、このバッファはスイッチにより他の列から分離されている。ディスプレイのライン周期は、列を所要電圧に充電するのに要する時間よりも著しく長い為、多重化は可能である。モバイル分野の小型のディスプレイでは、ライン周期を１５０μｓよりも長くでき、一方、１列を充電するのに要する時間は代表的に１０μｓよりも短い。

【０００８】

列が所要の電圧に充電され、且つこの列への所要の電圧の印加が終了された後に、充電された列のキャパシタンスと画素キャパシタンスとの間で電荷転送が行われる。列キャパシタンスは画素キャパシタンスの約３０倍にすることができる為、画素への電荷転送による電圧変化はほんの僅かとなる。しかし、この電荷転送によれば、（ＴＦＴの抵抗値が高い結果）画素の時定数が大きくなるにもかかわらず、短い列アドレスパルスを用いて画素を充電しうるようになる。

【０００９】

この多重方式に対する問題は、群内の列間にクロストークがあるということである。その理由は、特に、群のうちの１つの列を除く全ての列が如何なる時点においても有効に浮動状態にあり、従って、信号レベルの変動を受けやすい為である。行アドレス周期中、行中の全ての画素のＴＦＴがスイッチオンされる（実際にはこれにより列キャパシタンスと画素との間で電荷転送を可能にする）為、列導体におけるいかなる信号変動もクロストークの結果として画素に伝達される。

【００１０】

本発明は、列駆動回路にとって必要とされるバッファの個数を減少させる他の方法を提供することにある。

【００１１】

本発明の第１の観点によれば、行及び列に配置された液晶画素のアレイを有するディスプレイデバイスであって、画素駆動信号が与えられる列導体を画素の各列が共有し、画素駆動信号を発生する列アドレス回路が設けられており、この列アドレス回路は、別々の信号レベルラインに可能な全ての駆動信号レベルを発生する回路と、各信号レベルラインと関連するバッファとを有しており、バッファの出力は列に選択的に切換えて供給され、列アドレス回路が更に、各列に与える信号レベルを記憶するメモリを有し、バッファは記憶された信号レベルに応じて制御されるようになっているディスプレイデバイスを提供するも

のである。

【００１２】

本発明は、可能な各グレーレベル出力に対しバッファをグレーレベル発生回路に設けた他の解決策を提供する。バッファの応答は出力負荷に極めて依存し、これらのバッファは代表的に、特定の範囲の出力負荷に対し適しているように設計される。ディスプレイには多数の列がある為、バッファの出力負荷には、バッファ出力を与える必要のある列の個数の関数として極めて大きな変化が生じる。従って、記憶された信号レベルに応じてバッファを制御し、いかなる出力負荷に対しもバッファが確実に安定化されるようにする。

【００１３】

一例では、各バッファに対するバイアス電流が、バッファ出力を切換えて供給すべき列の個数に応じて制御されるようにする。

【００１４】

他の例では、各信号レベルラインが複数のバッファと関連しており、これら複数のバッファの各々は互いに異なる出力負荷に適しており、バッファ出力を切換えて供給すべき列の個数に応じて前記複数のバッファの１つを選択するようにする。各信号レベルラインは２つのバッファと関連させることができる。

【００１５】

更に他の例では、各バッファが複数の出力段を有し、使用する出力段の個数が、バッファ出力を切換えて供給すべき列の個数に応じて制御されるようにする。

【００１６】

更に他の例では、追加のバッファを設け、この追加のバッファは、個々のバッファ出力を切換えて供給すべき列の個数が列の総数の半分を超えた場合に用いられるようにする。

【００１７】

これらの各例は、バッファ構成を安定化するために、各バッファに必要とする出力負荷を用いてバッファ構成を制御しうるようにする配列を得るものである。グレーレベルの個数は代表的に列の個数よりも著しく少ない為、本発明の構成によれば、必要とするバッファの個数が低減される。

【００１８】

好ましくは、各画素が薄膜トランジスタスイッチング装置と液晶セルとを有し、各列の画素が、当該列における画素の薄膜トランジスタのゲートに接続された行導体を共有しており、行駆動回路が行の画素のトランジスタをスイッチング制御する行アドレス信号を生じるようにする。

【００１９】

本発明の第２の観点によれば、行及び列に配置された液晶画素のアレイを有するディスプレイデバイスに画素駆動信号を供給する画素駆動信号供給方法であって、
可能な全ての画素駆動信号レベルを発生させる工程と、
各画素駆動信号レベルを関連のバッファに供給する工程と、
画素の行に対する必要な画素駆動信号をメモリ内に記憶する工程と、
各画素駆動信号によりアドレスすべき行の画素の必要数を計算する工程と、
この計算されて画素の必要数に応じてバッファを制御する工程と、
アドレスすべき行に対する行アドレス周期中、バッファの出力を列上に切換えて供給する工程と
を有する画素駆動信号供給方法を提供する。

【００２０】

バッファを制御する前記工程は、バッファに適切なバイアス電流を供給する工程を有するか、又は各画素駆動信号レベルに対し二者択一のバッファを選択する工程を有するか、又は各バッファに接続すべき複数の出力段を選択する工程を有するようにしうる。

【００２１】

本発明は、別々の信号レベルライン上に可能なあらゆる駆動信号レベルを発生する回路と、各信号レベルラインと関連するバッファとを有し、液晶ディスプレイの列を駆動する列

駆動回路であって、バッファの出力が列出力上に選択的に切換えて供給するようになっており、列駆動回路が更に、各列に与えるべき信号レベルを記憶するメモリを有し、バッファは記憶された信号レベルに応じて制御されるようになっている列駆動回路をも提供する。

【００２２】

本発明の実施例を以下に添付図面を用いて詳細に説明する。

図１は、アクティブマトリックス液晶ディスプレイに対する通常の画素構造を示す。ディスプレイは行及び列の画素アレイとして構成されている。各行の画素は行導体１０を共用し、各列の画素は列導体１２を共用している。各画素は、共通の列導体１２と共通電位点１８との間に直列に配置された薄膜トランジスタ（ＴＦＴ）１４及び液晶セル１６を有する。トランジスタ１４は共通の行導体１０に与えられる信号によりスイッチオン及びスイッチオフされる。従って、行導体１０は関連する画素行の各トランジスタ１４のゲート１４ａに接続されている。各画素は更に、一端２２で次の行電極、又は前の行電極、又は別のキャパシタ電極に接続されている蓄積キャパシタ２０を有することができる。この蓄積キャパシタ２０は、トランジスタ１４がターンオフした後に駆動電圧を液晶セル１６の両端間に維持する手助けをする。キックバックのような種々の影響を低減せしめたり、画素キャパシタンスのグレーレベル依存性を低減せしめたりするには、総合の画素キャパシタンスを更に高くするのも望ましい。

【００２３】

必要なグレーレベルを得るための所望の電圧に液晶セル１６を駆動するには、行導体１０における行アドレスパルスと同期した適切な信号を列導体１２に与える。この行アドレスパルスは薄膜トランジスタ１４をターンオンさせ、これにより、列導体１２が液晶セル１６を所望の電圧に充電するとともに蓄積キャパシタ２０を同じ電圧に充電するようにする。

【００２４】

トランジスタ１４は行アドレスパルスの終了時にターンオフする。蓄積キャパシタ２０は、液晶漏洩効果を減少させるとともに、液晶セルキャパシタンスの電圧依存性により生ぜしめられる画素キャパシタンスの百分率変化を減少させる。行は、これらの全てが１フレーム周期内でアドレスされるように順次にアドレスされ、次のフレーム周期内でリフレッシュされる。

【００２５】

図２に示すように、行アドレス信号は行駆動回路３０により与えられ、画素駆動信号は列アドレス回路３２により表示画素のアレイ３４に与えられる。

【００２６】

アモルファスシリコン薄膜装置として構成した薄膜トランジスタ１４を介して充分な電流を取出しうるようにするには、高いゲート電圧を用いる必要がある。特に、トランジスタがターンオンしている期間は、ディスプレイをリフレッシュさせる必要のある期間を行数で分割した期間にほぼ等しい。オフ状態の漏洩電流を必要な程度小さくするにはオン状態のゲート電圧とオフ状態のゲート電圧とを約３０ボルト相違させ、液晶セル１６を使用可能時間内で充放電させるにはオン状態で充分な電流を流すことは周知である。その結果、行駆動回路３０は高電圧成分を用いる。

【００２７】

図１のディスプレイを駆動するには、種々の既知のアドレス様式があるが、これらの点はここで詳細に説明しない。既知の動作技術の幾つかは、例えば、米国特許第 5130829号明細書及び国際公開パンフレットＷＯ99/52012に詳細に説明されている。これらの文献は参考のためのものである。本発明はいかなる特定の駆動様式にも適合でき、この理由で、いずれの駆動様式の正確な動作の更なる説明も省略する。これは当業者にとって周知なことである。

【００２８】

図３は、通常の列駆動回路を示す。個数ｎの異なる画素駆動信号レベルはグレーレベル発

生器４０、例えば、抵抗アレイにより発生される。スイッチングマトリックス４２が各列（Column）への所要レベルの切換えを制御し、このスイッチングマトリックスはラッチ回路４４からのデジタル入力に基づくｎ個のグレーレベルのうちの１つを選択するコンバータ４３のアレイを有する。このデジタル入力は、必要とする画像データ４５を記憶しているＲＡＭから取出される。各列には、列中の画素を行アドレス周期の全期間の間所要の駆動信号レベルに保持するバッファ４６が設けられている。バッファ４６の個数がこのように多い為に、電力消費量が高くなる。

【００２９】

アクティブマトリックスＬＣＤを駆動する低電力チップセットにおける電力を低減させるためには、バッファの全個数を少なくする必要がある。これにより、占領される面積も小さくしうる。本発明によれば、グレーレベル電圧を発生させ、次に、図４に示すように関連のバッファを経て関連の列に切換えて供給する。

【００３０】

グレーレベル発生器５０は、最大電圧点及び最小電圧点間の抵抗アレイを有しており、各タップ５２が関連のバッファ５４に対し設けられている。合計でＮ個のバッファがあり、これらがＮ個のグレースケールレベルを生ぜしめる。スイッチングマトリックス５６にはＮ個の信号レベルが与えられ、このスイッチングマトリックスがＮ個のレベルうちの１つのレベルを、ＲＡＭから与えられる画像データ５８に基づいて各列に切換えて供給するようになっている。各列は、Ｎ個のうちの１つを選択する１オブＮ（１of Ｎ）セレクタ５７と関連する。図４の例では、必要とする画素データが６ビットワードにより規定されており、グレースケールレベルの総数Ｎを６４とする。

【００３１】

いずれの１つのバッファ５４が駆動している列の個数は、アドレスされた行において同じ画素データを有する画素の個数に依存する。このことは、５００個の列を有するディスプレイの場合、各バッファが有する可能な最大／最小負荷比は５００／１であることを意味する。この負荷範囲はあまりにも大きすぎ、バッファが不安定又は極めて大きくなってしまう。これを回避するために、本発明によれば、列の個数が分り、従って、各バッファが対処している負荷を決定しうる構成を提供する。

【００３２】

行に対する画素データのヒストグラムをＲＡＭ中に構成する。これにより、各バッファが駆動している列数を決定しうるようにし、従って、負荷を計算しうるようにする。次に、図４に矢印６０で線図的に示し、ＲＡＭヒストグラムデータを表わす記憶された画素データに応じてバッファを制御する。

【００３３】

図５は、ヒストグラムデータを記憶するＲＡＭの構成を示す。画像データは、通常のように、入力端７０においてホストから受ける。この画像データは、ラインストア７４を用いているメモリの画像データ記憶区分７２内に書込まれる。本発明は、画像中の各行に対するヒストグラムデータを記憶するのに準備したＲＡＭの追加の領域７６を用いて実行しうる。ヒストグラムデータはカウンタ７８を用いて得る。１行に対するメモリのヒストグラム部分７６の構成を図６に詳細に示す。Ｎ個の信号レベルＶ１、Ｖ２、…、ＶＮの各々を有する行における画素の個数を数N_{VN}として記憶する。

【００３４】

画像データはホストからＲＡＭの領域７２に書込まれ、次に、列駆動スイッチングマトリックス５６をリフレッシュする必要がある場合にはいつでも、領域７２からこの列駆動スイッチングマトリックス５６に画像データが送られる。データがラインストア７４を介してＲＡＭの領域７２に書込まれている間中、一連のカウンタ７８がヒストグラムデータを構築し、行データの全てが到来した際に、カウンタ７８によりヒストグラムをＲＡＭ中の適切な位置７６に記憶させる。従って、ヒストグラムは、データが到来した際に１度だけ計算する必要があるだけである。他の方法は、ディスプレイを更新している際で、ヒストグラムデータをＲＡＭから読出している際に、このヒストグラムデータを計算する方法で

ある。しかし、この後者の場合には、各行当りのヒストグラムの計算回数は１秒当りフレームレートに相当し、これに電力を要する。

【００３５】

このヒストグラムデータを用いてバッファの構成を制御し、バッファが所要の出力負荷で安定となるようにするには種々の方法がある。

【００３６】

図７は、ヒストグラムデータを用いて、簡単な２段増幅器の容量性駆動能力を変えるようにする第１の例を示す。通常の２段回路８０を、出力段８２を並列に追加することにより拡張する。これらの追加の出力段８２は、ヒストグラム情報（Ｈ０、Ｈ１、Ｈ２及びＨ３）からの制御の下で有効となる。従って、複数の出力段を、所要の出力負荷の関数として動作状態に切換えることができる。このようにすることにより、低出力の要求がある際に低電力消費を保つことができ、しかもバッファを流れる電流を高めることにより高出力要求を許容することもできる。このように、第２段を負荷容量に適合するように制御でき、これにより種々の負荷に対し同様な設定特性を与えることができる。例えば、選択出力段を切換えることにより、出力インピーダンス、スルーレート及び安定余裕を制御することができる。図示の回路では、出力段の切換えの“分解能”は４列である為、増幅器の各出力段は、最低値からこの最低値の４倍である最高値まで変化する容量性負荷を駆動しうるようにする必要がある。図示の例では、最初の出力段は１～４列に対するものであり、次の出力段は５～１６列に対するものであり、以下の出力段は同様な関係の出力段に対するものである。増幅器の出力段を調整するこの方法によれば、バッファの出力インピーダンスを有効に調整して所要の出力負荷に対する安定性を維持する。使用されないバッファ分の電力を下げることができる為、全体の電力が減少される。

【００３７】

所望の出力負荷に応じてバッファ構成を変えるのに他の方式があること勿論である。例えば、バッファにバイアス電流入力を与えることができる。この場合、バイアス電流を出力負荷の関数として変えて所望の整合をとるようにすることができる。或いはまた、バッファにバッファローディング用キャパシタを設けることができる。出力負荷が増大すると、バッファローディング用キャパシタを回路から切り離し、全体の負荷キャパシタンス（バッファローディング用キャパシタンス及び出力負荷キャパシタンス）がほぼ一定に維持されるようにする。

【００３８】

図８は、各信号レベルラインが２つのバッファ５４ａ及び５４ｂと関連している回路構成を示す。２つのバッファの各々は、互いに異なる出力負荷に適している。これら２つのバッファの１つは、バッファ出力を切換えて供給する必要のある列の個数に依存して選択される。従って、入力端６０におけるヒストグラムデータは、相補対に配置されたスイッチ６２を制御する。これにより、最大の出力負荷変化を半分にしうる。各信号レベルラインをより多くのバッファと関連させることができること勿論である。

【００３９】

図９の例では、追加のバッファ９２が設けられており、この追加のバッファ９２は、個々のバッファ出力を切換えて供給する必要のある列の個数が列の総数の半分を超えた場合に用いられる。従って、図９のバッファ５４０が、（ヒストグラムデータ６０から決定される）行の画素の半分よりも多い画素に給電する必要がある場合には、スイッチングマトリックス９４が対応する信号レベルＶ１をグレーレベル発生器５０から追加のバッファ９２に供給する。このバッファ９２の出力は幾つかの列を駆動するのに用いられ、バッファ５４０の出力がその他の列を駆動するのに用いられる。その後、スイッチングマトリックス５６がＮ＋１個の信号レベルを受け、ヒストグラムデータ６０がスイッチングマトリックス５６を制御するのに用いられる為、行の画素の半分よりも多い画素に対し１つの信号レベルが必要である場合には、この負荷がこの信号レベルに対するバッファと追加のバッファとで共有される。

【００４０】

追加のバッファを２つ以上として、個々のバッファに必要とする出力負荷範囲を更に減少させることができる。

【００４１】

言葉“行”及び“列”は、本明細書においては任意性があるものである。これらの言葉は、共通接続ラインを共有する素子の直交ラインを有する素子アレイが存在することを明瞭にするために用いたものである。通常、行はディスプレイの左右に延在し、列はディスプレイの上下に延在するものと考えられているが、これらの言葉の使用はこの点に制限されるものではない。

【００４２】

列駆動回路は集積回路として構成することができ、本発明は上述したディスプレイを構成する列駆動回路にも関するものである。

本発明の他の特徴は当業者にとって明らかである。

【図面の簡単な説明】

【００４３】

【図１】アクティブマトリックス液晶ディスプレイに対する既知の画素構成の一例を示す回路図である。

【図２】行及び列駆動回路を有するディスプレイデバイスを示す線図である。

【図３】通常の列駆動回路を示す構成図である。

【図４】本発明による列駆動回路を示す構成図である。

【図５】図４の回路のメモリを詳細に示すブロック線図である。

【図６】図５のメモリの一部を詳細に示す線図である。

【図７】本発明の列駆動回路に用いるバッファの１つの構成例を示す回路である。

【図８】本発明の列駆動回路に用いるバッファの他の構成例を示す回路図である。

【図９】本発明の列駆動回路に用いるバッファの更に他の構成例を示す回路図である。

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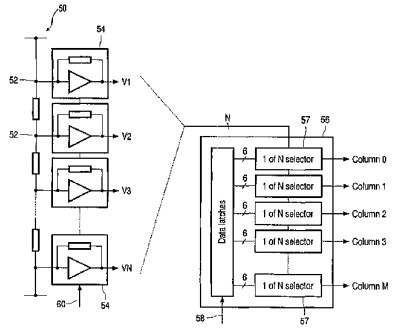
(54) Title: ACTIVE MATRIX DISPLAY DEVICE



(57) Abstract: A display has circuitry (50) which generates all possible pixel drive signal levels on separate signal level lines. A buffer (54) is associated with each signal level line. The outputs of the buffers are selectably switchable onto the columns. The signal levels for each column are stored in a memory (72) and the buffers are controlled in dependence on the stored signal levels. The response of the buffers is heavily dependent on the output load, and there is a very large variation in the output load of the buffers (54), as a function of the number of columns to which the buffer output is to be provided. The buffers are controlled in dependence on stored signal levels to ensure stability of the buffers for any output load.

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ACTIVE MATRIX DISPLAY DEVICE

This invention relates to active matrix display devices, and relates in particular to the circuitry used for providing drive signals to the pixels of the display.

Active matrix display devices typically comprise an array of pixels arranged in rows and columns. Each row of pixels shares a row conductor which connects to the gates of the thin film transistors of the pixels in the row. Each column of pixels shares a column conductor, to which pixel drive signals are provided. The signal on the row conductor determines whether the transistor is turned on or off, and when the transistor is turned on, by a high voltage pulse on the row conductor, a signal from the column conductor is allowed to pass on to an area of liquid crystal material, thereby altering the light transmission characteristics of the material. An additional storage capacitor may be provided as part of the pixel configuration to enable a voltage to be maintained on the liquid crystal material even after removal of the row electrode pulse. US-A-5 130 829 discloses in more detail the design of an active matrix display device.

The frame (field) period for active matrix display devices requires a row of pixels to be addressed in a short period of time, and this in turn imposes a requirement on the current driving capabilities of the transistor in order to charge or discharge the liquid crystal material to the desired voltage level. In order to meet these current requirements, the gate voltage supplied to the thin film transistor needs to fluctuate between values separated by approximately 30 volts. For example, the transistor may be turned off by applying a gate voltage of around -10 volts, or even lower, (with respect to the source) whereas a voltage of around 20 volts, or even higher, may be required to bias the transistor sufficiently to provide the required source-drain current to charge or discharge the liquid crystal material sufficiently rapidly.

The requirement for large voltage swings in the row conductors requires the row driver circuitry to be implemented using high voltage components.

The voltages provided on the column conductors typically vary by approximately 10 volts, which represents the difference between the drive signals required to drive the liquid crystal material between white and black states. Various drive schemes have been proposed enabling the voltage swing on the column conductors to be reduced, so that lower voltage components may be used in the column driver circuitry. In the so-called "common electrode drive scheme", the common electrode, connected to the full liquid crystal material layer, is driven to an oscillating voltage. The so-called "four-level drive scheme" uses more complicated row electrode waveforms in order to reduce the voltage swing on the column conductors, using capacitive coupling effects.

These drive schemes enable lower voltage components to be used for the column driver circuitry. However, there is still a significant amount of complexity and power inefficiency in the column driver circuits. Each row is addressed in turn, and during the row address period of any one row, pixel signals are provided to each column. In the past, each column would be provided with a buffer for holding a pixel in the column to a drive signal level for the full duration of the row address period. This large number of buffers results in high power consumption.

There have been proposals to provide a multiplexing scheme, in which a buffer is shared between a group of columns. The output of the buffer is switched in turn to the columns of the group. When the buffer is providing a signal to one column, it is isolated from the other columns by a switch. Multiplexing is possible because the line time of the display is significantly greater than the time required to charge a column to the required voltage. In small displays for mobile applications, the line time may be in excess of 150 μs whereas the time required to charge a column is typically less than 10 μs.

Once the column has been charged to the required voltage, and after the end of the application of the required voltage to the column, charge transfer takes place between the charged column capacitance and the pixel

capacitance. The column capacitance may be around 30 times larger than the column capacitance, so that the charge transfer to the pixel results in only a small voltage change. However, this charge transfer enables the pixel to be charged using a short column address pulse, despite the longer time constant of the pixel (resulting from the high TFT resistance).

A problem with this multiplexing approach is that there is cross talk between the columns within the group, particularly as all but one of the columns of the group are effectively floating at any point in time, and are therefore susceptible to signal level fluctuations. During the row address period, the TFTs of all pixels in the row are switched on (and indeed this enables the charge transfer to take place between the column capacitance and the pixel), so that any signal fluctuations on the column conductors as a result of cross talk are passed onto the pixels.

The invention provides an alternative approach for reducing the number of buffers required by the column driver circuitry.

According to a first aspect of the invention, there is provided a display device comprising an array of liquid crystal pixels arranged in rows and columns, wherein each column of pixels shares a column conductor to which pixel drive signals are provided, wherein column address circuitry is provided for generating the pixel drive signals, the column address circuitry comprising circuitry for generating all possible drive signal levels on separate signal level lines and a buffer associated with each signal level line, the outputs of the buffers being selectably switchable onto the columns, wherein the column address circuitry further comprises a memory for storing the signal levels to be provided to each column, and wherein the buffers are controlled in dependence on the stored signal levels.

The invention provides an alternative approach by which a grey level generation circuit is provided with a buffer for each possible grey level output. The response of the buffers is heavily dependent on the output load, and such buffers are typically designed to be suitable for specific ranges of output loads. As a result of the large number columns in a display, there is a very large

variation in the output load of the buffers, as a function of the number of columns to which the buffer output is to be provided. Therefore, the buffers are controlled in dependence on stored signal levels to ensure stability of the buffers for any output load.

In one example, a bias current to each buffer is controlled in dependence on the number of columns to which the buffer output is to be switched.

In another example, each signal level line is associated with a plurality of buffers, each of the plurality of buffers being suitable for different output loads, wherein one of the plurality of buffers is selected in dependence on the number of columns to which the buffer output is to be switched. Each signal level line may be associated with two buffers.

In another example, each buffer has a plurality of output stages, and wherein the number of output stages used is controlled in dependence on the number of columns to which the buffer output is to be switched.

In a further example, an additional buffer is provided and the additional buffer is used when the number of columns to which an individual buffer output is to be switched exceeds half the total number of columns.

These examples each provide arrangements which enable the output load required of each buffer to be used to provide control of the buffer configuration, in order to ensure stability of the buffer arrangements. The number of grey levels will typically be much smaller than the number of columns, so that the arrangement of the invention reduces the number of buffers required.

Preferably, each pixel comprises a thin film transistor switching device and a liquid crystal cell, wherein each row of pixels share a row conductor which connects to the gates of the thin film transistors of the pixels in the row, and wherein row driver circuitry provides row address signals for controlling the switching of the transistors of the pixels of the row.

According to a second aspect of the invention, there is provided a method of providing pixel drive signals to a display device comprising an array of liquid crystal pixels arranged in rows and columns, the method comprising:

generating all possible pixel drive signal levels;

providing each pixel drive signal level to an associated buffer;

storing the required pixel drive signals for a row of pixels in a memory;

calculating the required number of pixels of the row to be addressed by each drive signal;

controlling the buffers in dependence on the calculated number of pixels; and

switching the buffer outputs onto the columns during the row address period for the row to be addressed.

The step of controlling the buffers may comprise applying an appropriate bias current to the buffers, selecting between alternative buffers for each pixel drive signal level or selecting a number of output stages to be connected to each buffer.

The invention also provides column address circuitry for driving the columns of a liquid crystal display, comprising circuitry for generating all possible drive signal levels on separate signal level lines and a buffer associated with each signal level line, the outputs of the buffers being selectably switchable onto the column outputs, wherein the column address circuitry further comprises a memory for storing the signal levels to be provided to each column, and wherein the buffers are controlled in dependence on the stored signal levels.

Examples of the invention will now be described in detail with reference to the accompanying drawings, in which:

Figure 1 shows one example of a known pixel configuration for an active matrix liquid crystal display;

Figure 2 shows a display device including row and column driver circuitry;

Figure 3 shows a conventional column driver circuit;

Figure 4 shows a column driver circuit according to the invention;

Figure 5 shows in greater detail the memory in the circuit of Figure 4;

Figure 6 shows in greater detail part of the memory of Figure 5;

Figure 7 shows one buffer configuration for use in the column driver circuit of the invention;

Figure 8 shows another buffer configuration for use in the column driver circuit of the invention; and

Figure 9 shows a further buffer configuration for use in the column driver circuit of the invention.

Figure 1 shows a conventional pixel configuration for an active matrix liquid crystal display. The display is arranged as an array of pixels in rows and columns. Each row of pixels shares a common row conductor 10, and each column of pixels shares a common column conductor 12. Each pixel comprises a thin film transistor 14 and a liquid crystal cell 16 arranged in series between the column conductor 12 and a common potential 18. The transistor 14 is switched on and off by a signal provided on the row conductor 10. The row conductor 10 is thus connected to the gate 14a of each transistor 14 of the associated row of pixels. Each pixel may additionally comprise a storage capacitor 20 which is connected at one end 22 to the next row electrode, to the preceding row electrode, or to a separate capacitor electrode. This capacitor 20 helps to maintain the drive voltage across the liquid crystal cell 16 after the transistor 14 has been turned off. A higher total pixel capacitance is also desirable to reduce various effects, such as kickback, and to reduce the grey-level dependence of the pixel capacitance.

In order to drive the liquid crystal cell 16 to a desired voltage to obtain a required grey level, an appropriate signal is provided on the column conductor 12 in synchronism with a row address pulse on the row conductor 10. This row address pulse turns on the thin film transistor 14, thereby allowing the column conductor 12 to charge the liquid crystal cell 16 to the desired voltage, and also to charge the storage capacitor 20 to the same voltage.

At the end of the row address pulse, the transistor 14 is turned off. The storage capacitor 20 reduces the effect of liquid crystal leakage and reduces the percentage variation in the pixel capacitance caused by the voltage dependency of the liquid crystal cell capacitance. The rows are addressed

sequentially so that all rows are addressed in one frame period, and refreshed in subsequent frame periods.

As shown in Figure 2, the row address signals are provided by row driver circuitry 30, and the pixel drive signals are provided by column address circuitry 32, to the array 34 of display pixels.

In order to enable a sufficient current to be driven through the thin film transistor 14, which is implemented as an amorphous silicon thin film device, a high gate voltage must be used. In particular, the period during which the transistor is turned on is approximately equal to the total frame period within which the display must be refreshed, divided by the number of rows. It is well known that the gate voltage for the on-state and the off-state differ by approximately 30 volts in order to provide the required small leakage current in the off-state, and sufficient current flow in the on-state to charge or discharge the liquid crystal cell 16 within the available time. As a result, the row driver circuitry 30 uses high voltage components.

There are various known addressing schemes for driving the display of Figure 1, and these will not be described in detail in this text. Some of the known operational techniques are described in greater detail, for example in US-A-5 130 829 and WO 99/52012, and these documents are incorporated herein by way of reference material. The invention is applicable to any particular drive scheme, and for this reason, no further explanation will be given of the precise operation of any particular drive scheme. This will be well known to those skilled in the art.

Figure 3 shows a conventional column driver circuit. The number n of different pixel drive signal levels are generated by a grey level generator 40, for example a resistor array. A switching matrix 42 controls the switching of the required level to each column and comprises an array of converters 43 for selecting one of the n grey levels based on a digital input from a latch 44. The digital input is derived from a RAM storing the required image data 45. Each column is provided with a buffer 46 for holding a pixel in the column to the required drive signal level for the full duration of the row address period. This large number of buffers 46 results in high power consumption.

To reduce power in a low power chipset to drive the active matrix LCD, the total number of buffers needs to be reduced. This also enables less area to be occupied. In accordance with the invention, the grey level voltages are generated and then switched through an associated buffer to the relevant column, as shown in Figure 4.

The grey level generation circuit 50 comprises a resistor array between maximum and minimum voltages, with each tap 52 being provided to an associated buffer 54. There are N buffers in total, providing the N grey scale levels. The N signal levels are provided to a switching matrix 56 which enables one of the N levels to be switched to each column, based on the image data 58 provided from a RAM. Each column is associated with a 1 of N selector 57. In the example of Figure 4, the required pixel data is defined by a six bit word, giving a total number of grey scale levels, N, of 64.

The number of columns that any one buffer 54 is driving will depend on the number of pixels in the addressed row which have the same pixel data. This means that each buffer has a possible maximum to minimum load ratio of 500 to 1 for a display with 500 columns. This load range is too large and results in unstable or extremely large buffers. To overcome this, the invention provides an architecture by which the number of columns is known, and hence the load seen by each buffer can be determined.

A histogram is constructed in RAM of the pixel data for the row. This enables the number of columns each buffer will be driving to be determined, and therefore enables the load to be calculated. The buffers are then controlled in dependence on the stored pixel data, as represented schematically by arrow 60 in Figure 4, which represents the RAM histogram data.

Figure 5 shows the architecture of the RAM for storage of the histogram data. In conventional manner, image data is received from a host at the input 70. This is written into an image data storage section 72 of the memory using a line store 74. The invention can be implemented using an additional area of RAM 76, which is reserved for storing the histogram data for each row in the image. The histogram data is obtained using counters 78. The organisation of

the histogram part 76 of the memory for one row is shown in detail in Figure 6. The number of pixels in a row having each of the N signal levels V1, V2 ... VN, is stored, as number N_{VN}.

Image data is written from the host to the area 72 of the RAM and is then piped from the area 72 to the column driver switching matrix 56, whenever the latter needs to be refreshed. During the period when data is being written to the area 72 of RAM via the line store 74, the series of counters 78 build up the histogram data and, when all of the row data has arrived, stores the histogram at the appropriate location 76 in the RAM. In this way, the histogram only needs to be calculated once when the data arrives. The alternative is to calculate the histogram data when it is being read out from the RAM as the display is being updated. However, in this latter case the histograms will be calculated up to frame rate times per second for each row and this will cost power.

There are various ways to use this histogram data to control the configuration of the buffers, so that the buffers are stable at the required output load.

Figure 7 shows a first example in which the histogram data is used to vary the capacitive drive capability of simple 2-stage amplifier. A conventional 2-stage circuit 80 is extended by adding extra output stages 82 in parallel. These additional output stages 82 are enabled under control from the histogram information (Ho, H1, H2 and H3). Thus, a number of output stages can be switched into operation as a function of the required output load. This enables a low power consumption to be maintained when there is low output demand, but enables a high output demand to be tolerated by increasing the currents flowing through the buffer. In this way, the second stage can be controlled to match the load capacitance, thereby giving similar settling characteristics for the different loads. For example, the output impedance, slew rate and stability margin can be controlled by switching in selected output stages. In the illustrated circuit, the "resolution" of the output stage switching is four columns, so that each configuration of the amplifier needs to be capable of driving a capacitive load that varies from a lowest value to a highest value a

factor of 4 greater than the lowest value. In the example shown, one output configuration is for 1 to 4 columns, the next configuration is for 5 to 16 columns, and so on. This method of adjusting the output stages of the amplifier effectively adjusts the output impedance of the buffer to maintain stability for the required output load. Unused buffers can be powered down, again to reduce the total power.

There are of course other schemes for varying the buffer configuration in dependence on the desired output load. For example, the buffers may have a bias current input. The bias current may then be altered as a function of the output load, to provide the desired matching. Alternatively, the buffer may be provided with a buffer loading capacitor. As the output load is increased, the buffer loading capacitor can be switched out of circuit, so that the overall load capacitance (the buffer loading capacitance and the output load capacitance) remains fairly constant.

Figure 8 shows an arrangement in which each signal level line is associated with two buffers 54a and 54b. Each of the two of buffers is suitable for different output loads. One of the two buffers is selected in dependence on the number of columns to which the buffer output is to be switched. Thus, the histogram data at input 60 controls switches 62 arranged in complementary pairs. This enables the maximum output load variation to be halved. Each signal level line may of course be associated with a greater number of buffers.

In the example of Figure 9, an additional buffer 92 is provided and the additional buffer 92 is used when the number of columns to which an individual buffer output is to be switched exceeds half the total number of columns. Thus, if buffer 540 in Figure 9 is to supply more than half the pixels of a row (as determined from the histogram data 60), a switching matrix 94 routes the corresponding signal level V1 from the grey level generator 50 to the additional buffer 92. The output of buffer 92 is used to drive some columns whereas the output of buffer 540 is used to drive others. The switching matrix 56 then receives N+1 signal levels, and the histogram data 60 is used to control the switching matrix 56 so that when one signal level is required for more than half

of the pixels of the row, this load is shared between the buffer for that signal level and the additional buffer.

There may be two or more additional buffers, which enables the required output load range of the individual buffers to be reduced further.

The terms "row" and "column" are somewhat arbitrary in the description and claims. These terms are intended to clarify that there is an array of elements with orthogonal lines of elements sharing common connections. Although a row is normally considered to run from side to side of a display and a column to run from top to bottom, the use of these terms is not intended to be limiting in this respect.

The column circuit may be implemented as an integrated circuit, and the invention also relates to the column circuits for implementing the display architecture described above.

Other features of the invention will be apparent to those skilled in the art.

CLAIMS

1. A display device comprising an array of liquid crystal pixels arranged in rows and columns, wherein each column of pixels shares a column conductor to which pixel drive signals are provided, wherein column address circuitry is provided for generating the pixel drive signals, the column address circuitry comprising circuitry for generating all possible drive signal levels on separate signal level lines and a buffer associated with each signal level line, the outputs of the buffers being selectably switchable onto the columns, wherein the column address circuitry further comprises a memory for storing the signal levels to be provided to each column, and wherein the buffers are controlled in dependence on the stored signal levels.

2. A display device as claimed in claim 1, wherein a bias current to each buffer is controlled in dependence on the number of columns to which the buffer output is to be switched.

3. A display device as claimed in claim 1, wherein each signal level line is associated with a plurality of buffers, each of the plurality of buffers being suitable for different output loads, wherein one of the plurality of buffers is selected in dependence on the number of columns to which the buffer output is to be switched.

4. A display device as claimed in claim 3, wherein each signal level line is associated with two buffers.

5. A display device as claimed in claim 1, wherein each buffer has a plurality of output stages, and wherein the number of output stages used is controlled in dependence on the number of columns to which the buffer output is to be switched.

6. A display device as claimed in claim 1, further comprising an additional buffer, and the additional buffer is used when the number of columns to which an individual buffer output is to be switched exceeds half the total number of columns.

7. A display device as claimed in claim 6, in which a plurality of additional buffers are provided, and the additional buffers are used when the number of columns to which individual buffer outputs are to be switched exceed a predetermined fraction of the total number of columns.

8. A display device as claimed in any preceding claim, wherein each pixel comprises a thin film transistor switching device and a liquid crystal cell, wherein each row of pixels share a row conductor which connects to the gates of the thin film transistors of the pixels in the row, and wherein row driver circuitry provides row address signals for controlling the switching of the transistors of the pixels of the row.

9. A method of providing pixel drive signals to a display device comprising an array of liquid crystal pixels arranged in rows and columns, the method comprising:

generating all possible pixel drive signal levels;

providing each pixel drive signal level to an associated buffer;

storing the required pixel drive signals for a row of pixels in a memory;

calculating the required number of pixels of the row to be addressed by each drive signal;

controlling the buffers in dependence on the calculated number of pixels; and

switching the buffer outputs onto the columns during the row address period for the row to be addressed.

10. A method as claimed in claim 9, wherein the step of controlling the buffers comprises applying an appropriate bias current to the buffers.

11. A method as claimed in claim 9, wherein the step of controlling the buffers comprises selecting between alternative buffers for each pixel drive signal level.

12. A method as claimed in claim 9, wherein the step of controlling the buffers comprises selecting a number of output stages to be connected to each buffer.

13. A method as claimed in claim 9, wherein the step of controlling the buffers comprises using an additional buffer to share the output load of an individual buffer when the number of columns to which the individual buffer output is to be switched exceeds half the total number of columns.

14. A method as claimed in claim 13, wherein a plurality of additional buffers are used to share the output loads of one or more buffers when the number of columns to which those buffer outputs are to be switched exceed a predetermined fraction of the total number of columns.

15. Column address circuitry for driving the columns of a liquid crystal display, comprising circuitry for generating all possible drive signal levels on separate signal level lines and a buffer associated with each signal level line, the outputs of the buffers being selectably switchable onto the column outputs, wherein the column address circuitry further comprises a memory for storing the signal levels to be provided to each column, and wherein the buffers are controlled in dependence on the stored signal levels.

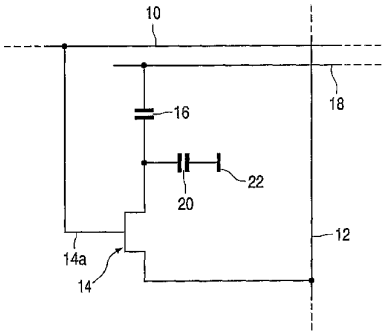

FIG. 1

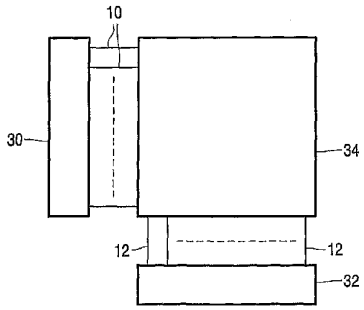

FIG. 2

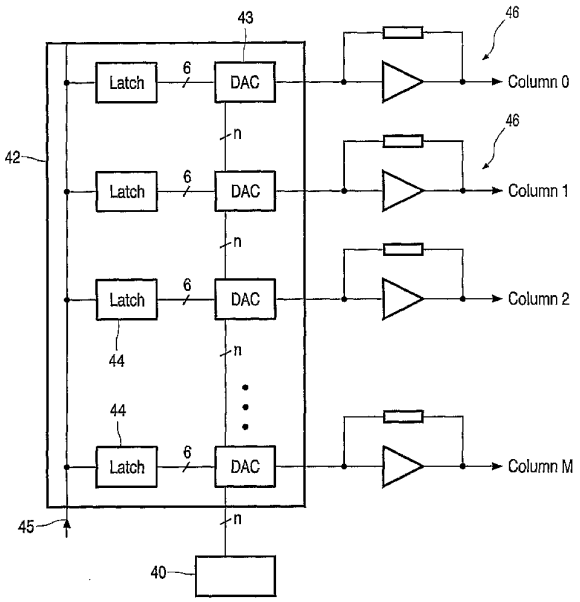
43
46
Latch
6
DAC
Column 0
n
42
46
Latch
6
DAC
Column 1
n
Latch
6
DAC
Column 2
44
n
44
Latch
6
DAC
Column M
45
n
40

FIG. 3

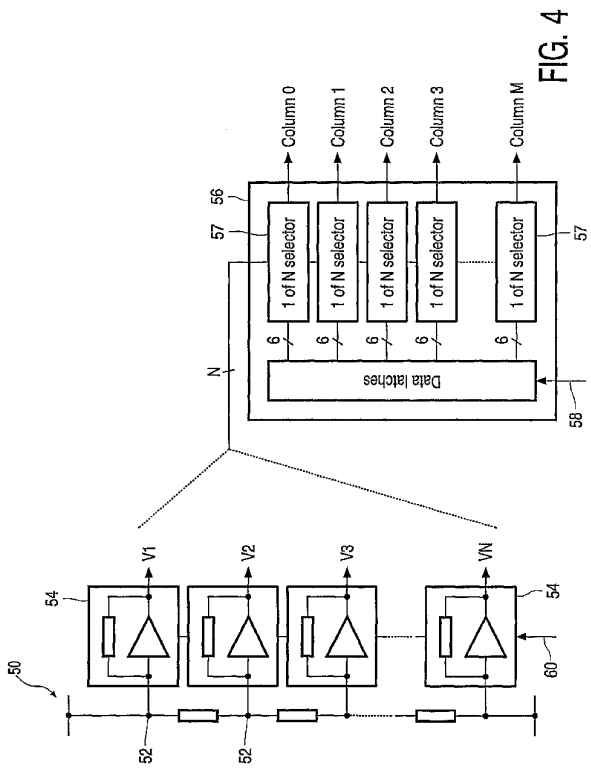
Column 0
Column 1
Column 2
Column 3
Column M
56
57
1 of N selector
6
N
Data latches
58
V1
V2
V3
VN
54
50
52
60

FIG. 4

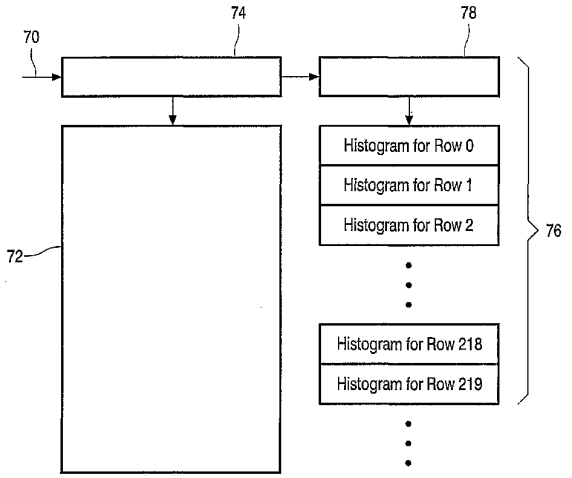
70
74
78
72
Histogram for Row 0
Histogram for Row 1
Histogram for Row 2
Histogram for Row 218
Histogram for Row 219
76

FIG. 5

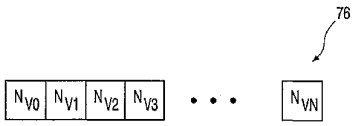
76
N_{V0}
N_{V1}
N_{V2}
N_{V3}
N_{VN}

FIG. 6

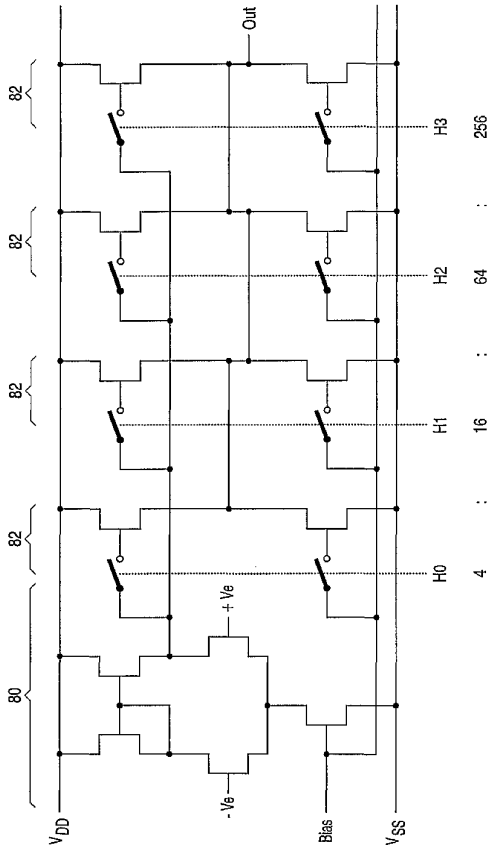

FIG. 7

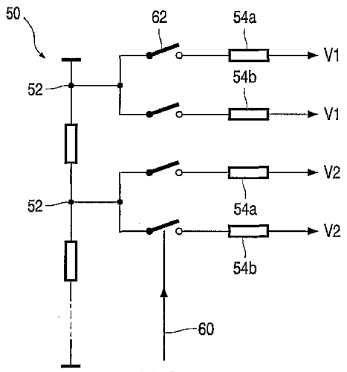
50
62
54a
V1
52
54b
V1
V2
52
54a
V2
54b
60

FIG. 8

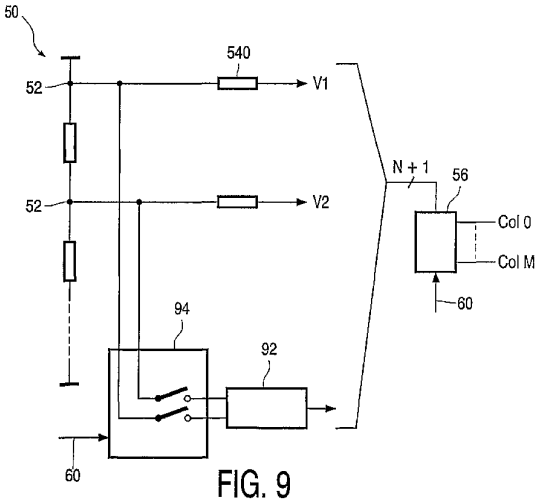
50
540
52
V1
N + 1
56
52
V2
Col 0
Col M
60
94
92
60

FIG. 9

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(74) Agent: WILLIAMSON, Paul, L.; Internationaal Octrooibureau B.V., Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL).

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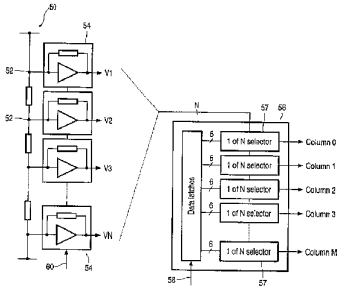
(54) Title: ACTIVE MATRIX DISPLAY DEVICE



(57) Abstract: A display has circuitry (50) which generates all possible pixel drive signal levels on separate signal level lines. A buffer (54) is associated with each signal level line. The outputs of the buffers are selectably switchable onto the columns. The signal levels for each column are stored in a memory (72) and the buffers are controlled in dependence on the stored signal levels. The response of the buffers is heavily dependent on the output load, and there is a very large variation in the output load of the buffers (54), as a function of the number of columns to which the buffer output is to be provided. The buffers are controlled in dependence on stored signal levels to ensure stability of the buffers for any output load.

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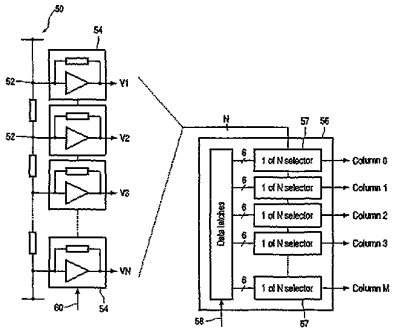

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ACTIVE MATRIX DISPLAY DEVICE

This invention relates to active matrix display devices, and relates in particular to the circuitry used for providing drive signals to the pixels of the display.

Active matrix display devices typically comprise an array of pixels arranged in rows and columns. Each row of pixels shares a row conductor which connects to the gates of the thin film transistors of the pixels in the row. Each column of pixels shares a column conductor, to which pixel drive signals are provided. The signal on the row conductor determines whether the transistor is turned on or off, and when the transistor is turned on, by a high voltage pulse on the row conductor, a signal from the column conductor is allowed to pass on to an area of liquid crystal material, thereby altering the light transmission characteristics of the material. An additional storage capacitor may be provided as part of the pixel configuration to enable a voltage to be maintained on the liquid crystal material even after removal of the row electrode pulse. US-A-5 130 829 discloses in more detail the design of an active matrix display device.

The frame (field) period for active matrix display devices requires a row of pixels to be addressed in a short period of time, and this in turn imposes a requirement on the current driving capabilities of the transistor in order to charge or discharge the liquid crystal material to the desired voltage level. In order to meet these current requirements, the gate voltage supplied to the thin film transistor needs to fluctuate between values separated by approximately 30 volts. For example, the transistor may be turned off by applying a gate voltage of around -10 volts, or even lower, (with respect to the source) whereas a voltage of around 20 volts, or even higher, may be required to bias the transistor sufficiently to provide the required source-drain current to charge or discharge the liquid crystal material sufficiently rapidly.

The requirement for large voltage swings in the row conductors requires the row driver circuitry to be implemented using high voltage components.

The voltages provided on the column conductors typically vary by approximately 10 volts, which represents the difference between the drive signals required to drive the liquid crystal material between white and black states. Various drive schemes have been proposed enabling the voltage swing on the column conductors to be reduced, so that lower voltage components may be used in the column driver circuitry. In the so-called "common electrode drive scheme", the common electrode, connected to the full liquid crystal material layer, is driven to an oscillating voltage. The so-called "four-level drive scheme" uses more complicated row electrode waveforms in order to reduce the voltage swing on the column conductors, using capacitive coupling effects.

These drive schemes enable lower voltage components to be used for the column driver circuitry. However, there is still a significant amount of complexity and power inefficiency in the column driver circuits. Each row is addressed in turn, and during the row address period of any one row, pixel signals are provided to each column. In the past, each column would be provided with a buffer for holding a pixel in the column to a drive signal level for the full duration of the row address period. This large number of buffers results in high power consumption.

There have been proposals to provide a multiplexing scheme, in which a buffer is shared between a group of columns. The output of the buffer is switched in turn to the columns of the group. When the buffer is providing a signal to one column, it is isolated from the other columns by a switch. Multiplexing is possible because the line time of the display is significantly greater than the time required to charge a column to the required voltage. In small displays for mobile applications, the line time may be in excess of 150 μs whereas the time required to charge a column is typically less than 10 μs.

Once the column has been charged to the required voltage, and after the end of the application of the required voltage to the column, charge transfer takes place between the charged column capacitance and the pixel

capacitance. The column capacitance may be around 30 times larger than the column capacitance, so that the charge transfer to the pixel results in only a small voltage change. However, this charge transfer enables the pixel to be charged using a short column address pulse, despite the longer time constant of the pixel (resulting from the high TFT resistance).

A problem with this multiplexing approach is that there is cross talk between the columns within the group, particularly as all but one of the columns of the group are effectively floating at any point in time, and are therefore susceptible to signal level fluctuations. During the row address period, the TFTs of all pixels in the row are switched on (and indeed this enables the charge transfer to take place between the column capacitance and the pixel), so that any signal fluctuations on the column conductors as a result of cross talk are passed onto the pixels.

The invention provides an alternative approach for reducing the number of buffers required by the column driver circuitry.

According to a first aspect of the invention, there is provided a display device comprising an array of liquid crystal pixels arranged in rows and columns, wherein each column of pixels shares a column conductor to which pixel drive signals are provided, wherein column address circuitry is provided for generating the pixel drive signals, the column address circuitry comprising circuitry for generating all possible drive signal levels on separate signal level lines and a buffer associated with each signal level line, the outputs of the buffers being selectably switchable onto the columns, wherein the column address circuitry further comprises a memory for storing the signal levels to be provided to each column, and wherein the buffers are controlled in dependence on the stored signal levels.

The invention provides an alternative approach by which a grey level generation circuit is provided with a buffer for each possible grey level output. The response of the buffers is heavily dependent on the output load, and such buffers are typically designed to be suitable for specific ranges of output loads. As a result of the large number columns in a display, there is a very large

variation in the output load of the buffers, as a function of the number of columns to which the buffer output is to be provided. Therefore, the buffers are controlled in dependence on stored signal levels to ensure stability of the buffers for any output load.

In one example, a bias current to each buffer is controlled in dependence on the number of columns to which the buffer output is to be switched.

In another example, each signal level line is associated with a plurality of buffers, each of the plurality of buffers being suitable for different output loads, wherein one of the plurality of buffers is selected in dependence on the number of columns to which the buffer output is to be switched. Each signal level line may be associated with two buffers.

In another example, each buffer has a plurality of output stages, and wherein the number of output stages used is controlled in dependence on the number of columns to which the buffer output is to be switched.

In a further example, an additional buffer is provided and the additional buffer is used when the number of columns to which an individual buffer output is to be switched exceeds half the total number of columns.

These examples each provide arrangements which enable the output load required of each buffer to be used to provide control of the buffer configuration, in order to ensure stability of the buffer arrangements. The number of grey levels will typically be much smaller than the number of columns, so that the arrangement of the invention reduces the number of buffers required.

Preferably, each pixel comprises a thin film transistor switching device and a liquid crystal cell, wherein each row of pixels share a row conductor which connects to the gates of the thin film transistors of the pixels in the row, and wherein row driver circuitry provides row address signals for controlling the switching of the transistors of the pixels of the row.

According to a second aspect of the invention, there is provided a method of providing pixel drive signals to a display device comprising an array of liquid crystal pixels arranged in rows and columns, the method comprising:

generating all possible pixel drive signal levels;

providing each pixel drive signal level to an associated buffer;

storing the required pixel drive signals for a row of pixels in a memory;

calculating the required number of pixels of the row to be addressed by each drive signal;

controlling the buffers in dependence on the calculated number of pixels; and

switching the buffer outputs onto the columns during the row address period for the row to be addressed.

The step of controlling the buffers may comprise applying an appropriate bias current to the buffers, selecting between alternative buffers for each pixel drive signal level or selecting a number of output stages to be connected to each buffer.

The invention also provides column address circuitry for driving the columns of a liquid crystal display, comprising circuitry for generating all possible drive signal levels on separate signal level lines and a buffer associated with each signal level line, the outputs of the buffers being selectably switchable onto the column outputs, wherein the column address circuitry further comprises a memory for storing the signal levels to be provided to each column, and wherein the buffers are controlled in dependence on the stored signal levels.

Examples of the invention will now be described in detail with reference to the accompanying drawings, in which:

Figure 1 shows one example of a known pixel configuration for an active matrix liquid crystal display;

Figure 2 shows a display device including row and column driver circuitry;

Figure 3 shows a conventional column driver circuit;

Figure 4 shows a column driver circuit according to the invention;

Figure 5 shows in greater detail the memory in the circuit of Figure 4;

Figure 6 shows in greater detail part of the memory of Figure 5;

Figure 7 shows one buffer configuration for use in the column driver circuit of the invention;

Figure 8 shows another buffer configuration for use in the column driver circuit of the invention; and

Figure 9 shows a further buffer configuration for use in the column driver circuit of the invention.

Figure 1 shows a conventional pixel configuration for an active matrix liquid crystal display. The display is arranged as an array of pixels in rows and columns. Each row of pixels shares a common row conductor 10, and each column of pixels shares a common column conductor 12. Each pixel comprises a thin film transistor 14 and a liquid crystal cell 16 arranged in series between the column conductor 12 and a common potential 18. The transistor 14 is switched on and off by a signal provided on the row conductor 10. The row conductor 10 is thus connected to the gate 14a of each transistor 14 of the associated row of pixels. Each pixel may additionally comprise a storage capacitor 20 which is connected at one end 22 to the next row electrode, to the preceding row electrode, or to a separate capacitor electrode. This capacitor 20 helps to maintain the drive voltage across the liquid crystal cell 16 after the transistor 14 has been turned off. A higher total pixel capacitance is also desirable to reduce various effects, such as kickback, and to reduce the grey-level dependence of the pixel capacitance.

In order to drive the liquid crystal cell 16 to a desired voltage to obtain a required grey level, an appropriate signal is provided on the column conductor 12 in synchronism with a row address pulse on the row conductor 10. This row address pulse turns on the thin film transistor 14, thereby allowing the column conductor 12 to charge the liquid crystal cell 16 to the desired voltage, and also to charge the storage capacitor 20 to the same voltage.

At the end of the row address pulse, the transistor 14 is turned off. The storage capacitor 20 reduces the effect of liquid crystal leakage and reduces the percentage variation in the pixel capacitance caused by the voltage dependency of the liquid crystal cell capacitance. The rows are addressed

sequentially so that all rows are addressed in one frame period, and refreshed in subsequent frame periods.

As shown in Figure 2, the row address signals are provided by row driver circuitry 30, and the pixel drive signals are provided by column address circuitry 32, to the array 34 of display pixels.

In order to enable a sufficient current to be driven through the thin film transistor 14, which is implemented as an amorphous silicon thin film device, a high gate voltage must be used. In particular, the period during which the transistor is turned on is approximately equal to the total frame period within which the display must be refreshed, divided by the number of rows. It is well known that the gate voltage for the on-state and the off-state differ by approximately 30 volts in order to provide the required small leakage current in the off-state, and sufficient current flow in the on-state to charge or discharge the liquid crystal cell 16 within the available time. As a result, the row driver circuitry 30 uses high voltage components.

There are various known addressing schemes for driving the display of Figure 1, and these will not be described in detail in this text. Some of the known operational techniques are described in greater detail, for example in US-A-5 130 829 and WO 99/52012, and these documents are incorporated herein by way of reference material. The invention is applicable to any particular drive scheme, and for this reason, no further explanation will be given of the precise operation of any particular drive scheme. This will be well known to those skilled in the art.

Figure 3 shows a conventional column driver circuit. The number n of different pixel drive signal levels are generated by a grey level generator 40, for example a resistor array. A switching matrix 42 controls the switching of the required level to each column and comprises an array of converters 43 for selecting one of the n grey levels based on a digital input from a latch 44. The digital input is derived from a RAM storing the required image data 45. Each column is provided with a buffer 46 for holding a pixel in the column to the required drive signal level for the full duration of the row address period. This large number of buffers 46 results in high power consumption.

To reduce power in a low power chipset to drive the active matrix LCD, the total number of buffers needs to be reduced. This also enables less area to be occupied. In accordance with the invention, the grey level voltages are generated and then switched through an associated buffer to the relevant column, as shown in Figure 4.

The grey level generation circuit 50 comprises a resistor array between maximum and minimum voltages, with each tap 52 being provided to an associated buffer 54. There are N buffers in total, providing the N grey scale levels. The N signal levels are provided to a switching matrix 56 which enables one of the N levels to be switched to each column, based on the image data 58 provided from a RAM. Each column is associated with a 1 of N selector 57. In the example of Figure 4, the required pixel data is defined by a six bit word, giving a total number of grey scale levels, N, of 64.

The number of columns that any one buffer 54 is driving will depend on the number of pixels in the addressed row which have the same pixel data. This means that each buffer has a possible maximum to minimum load ratio of 500 to 1 for a display with 500 columns. This load range is too large and results in unstable or extremely large buffers. To overcome this, the invention provides an architecture by which the number of columns is known, and hence the load seen by each buffer can be determined.

A histogram is constructed in RAM of the pixel data for the row. This enables the number of columns each buffer will be driving to be determined, and therefore enables the load to be calculated. The buffers are then controlled in dependence on the stored pixel data, as represented schematically by arrow 60 in Figure 4, which represents the RAM histogram data.

Figure 5 shows the architecture of the RAM for storage of the histogram data. In conventional manner, image data is received from a host at the input 70. This is written into an image data storage section 72 of the memory using a line store 74. The invention can be implemented using an additional area of RAM 76, which is reserved for storing the histogram data for each row in the image. The histogram data is obtained using counters 78. The organisation of

the histogram part 76 of the memory for one row is shown in detail in Figure 6. The number of pixels in a row having each of the N signal levels V1, V2 ... VN, is stored, as number N_{VN}.

Image data is written from the host to the area 72 of the RAM and is then piped from the area 72 to the column driver switching matrix 56, whenever the latter needs to be refreshed. During the period when data is being written to the area 72 of RAM via the line store 74, the series of counters 78 build up the histogram data and, when all of the row data has arrived, stores the histogram at the appropriate location 76 in the RAM. In this way, the histogram only needs to be calculated once when the data arrives. The alternative is to calculate the histogram data when it is being read out from the RAM as the display is being updated. However, in this latter case the histograms will be calculated up to frame rate times per second for each row and this will cost power.

There are various ways to use this histogram data to control the configuration of the buffers, so that the buffers are stable at the required output load.

Figure 7 shows a first example in which the histogram data is used to vary the capacitive drive capability of simple 2-stage amplifier. A conventional 2-stage circuit 80 is extended by adding extra output stages 82 in parallel. These additional output stages 82 are enabled under control from the histogram information (Ho, H1, H2 and H3). Thus, a number of output stages can be switched into operation as a function of the required output load. This enables a low power consumption to be maintained when there is low output demand, but enables a high output demand to be tolerated by increasing the currents flowing through the buffer. In this way, the second stage can be controlled to match the load capacitance, thereby giving similar settling characteristics for the different loads. For example, the output impedance, slew rate and stability margin can be controlled by switching in selected output stages. In the illustrated circuit, the "resolution" of the output stage switching is four columns, so that each configuration of the amplifier needs to be capable of driving a capacitive load that varies from a lowest value to a highest value a

factor of 4 greater than the lowest value. In the example shown, one output configuration is for 1 to 4 columns, the next configuration is for 5 to 16 columns, and so on. This method of adjusting the output stages of the amplifier effectively adjusts the output impedance of the buffer to maintain stability for the required output load. Unused buffers can be powered down, again to reduce the total power.

There are of course other schemes for varying the buffer configuration in dependence on the desired output load. For example, the buffers may have a bias current input. The bias current may then be altered as a function of the output load, to provide the desired matching. Alternatively, the buffer may be provided with a buffer loading capacitor. As the output load is increased, the buffer loading capacitor can be switched out of circuit, so that the overall load capacitance (the buffer loading capacitance and the output load capacitance) remains fairly constant.

Figure 8 shows an arrangement in which each signal level line is associated with two buffers 54a and 54b. Each of the two of buffers is suitable for different output loads. One of the two buffers is selected in dependence on the number of columns to which the buffer output is to be switched. Thus, the histogram data at input 60 controls switches 62 arranged in complementary pairs. This enables the maximum output load variation to be halved. Each signal level line may of course be associated with a greater number of buffers.

In the example of Figure 9, an additional buffer 92 is provided and the additional buffer 92 is used when the number of columns to which an individual buffer output is to be switched exceeds half the total number of columns. Thus, if buffer 540 in Figure 9 is to supply more than half the pixels of a row (as determined from the histogram data 60), a switching matrix 94 routes the corresponding signal level V1 from the grey level generator 50 to the additional buffer 92. The output of buffer 92 is used to drive some columns whereas the output of buffer 540 is used to drive others. The switching matrix 56 then receives N+1 signal levels, and the histogram data 60 is used to control the switching matrix 56 so that when one signal level is required for more than half

of the pixels of the row, this load is shared between the buffer for that signal level and the additional buffer.

There may be two or more additional buffers, which enables the required output load range of the individual buffers to be reduced further.

The terms "row" and "column" are somewhat arbitrary in the description and claims. These terms are intended to clarify that there is an array of elements with orthogonal lines of elements sharing common connections. Although a row is normally considered to run from side to side of a display and a column to run from top to bottom, the use of these terms is not intended to be limiting in this respect.

The column circuit may be implemented as an integrated circuit, and the invention also relates to the column circuits for implementing the display architecture described above.

Other features of the invention will be apparent to those skilled in the art.

CLAIMS

1. A display device comprising an array of liquid crystal pixels arranged in rows and columns, wherein each column of pixels shares a column conductor to which pixel drive signals are provided, wherein column address circuitry is provided for generating the pixel drive signals, the column address circuitry comprising circuitry for generating all possible drive signal levels on separate signal level lines and a buffer associated with each signal level line, the outputs of the buffers being selectably switchable onto the columns, wherein the column address circuitry further comprises a memory for storing the signal levels to be provided to each column, and wherein the buffers are controlled in dependence on the stored signal levels.

2. A display device as claimed in claim 1, wherein a bias current to each buffer is controlled in dependence on the number of columns to which the buffer output is to be switched.

3. A display device as claimed in claim 1, wherein each signal level line is associated with a plurality of buffers, each of the plurality of buffers being suitable for different output loads, wherein one of the plurality of buffers is selected in dependence on the number of columns to which the buffer output is to be switched.

4. A display device as claimed in claim 3, wherein each signal level line is associated with two buffers.

5. A display device as claimed in claim 1, wherein each buffer has a plurality of output stages, and wherein the number of output stages used is controlled in dependence on the number of columns to which the buffer output is to be switched.

6. A display device as claimed in claim 1, further comprising an additional buffer, and the additional buffer is used when the number of columns to which an individual buffer output is to be switched exceeds half the total number of columns.

7. A display device as claimed in claim 6, in which a plurality of additional buffers are provided, and the additional buffers are used when the number of columns to which individual buffer outputs are to be switched exceed a predetermined fraction of the total number of columns.

8. A display device as claimed in any preceding claim, wherein each pixel comprises a thin film transistor switching device and a liquid crystal cell, wherein each row of pixels share a row conductor which connects to the gates of the thin film transistors of the pixels in the row, and wherein row driver circuitry provides row address signals for controlling the switching of the transistors of the pixels of the row.

9. A method of providing pixel drive signals to a display device comprising an array of liquid crystal pixels arranged in rows and columns, the method comprising:

generating all possible pixel drive signal levels;

providing each pixel drive signal level to an associated buffer;

storing the required pixel drive signals for a row of pixels in a memory;

calculating the required number of pixels of the row to be addressed by each drive signal;

controlling the buffers in dependence on the calculated number of pixels; and

switching the buffer outputs onto the columns during the row address period for the row to be addressed.

10. A method as claimed in claim 9, wherein the step of controlling the buffers comprises applying an appropriate bias current to the buffers.

11. A method as claimed in claim 9, wherein the step of controlling the buffers comprises selecting between alternative buffers for each pixel drive signal level.

12. A method as claimed in claim 9, wherein the step of controlling the buffers comprises selecting a number of output stages to be connected to each buffer.

13. A method as claimed in claim 9, wherein the step of controlling the buffers comprises using an additional buffer to share the output load of an individual buffer when the number of columns to which the individual buffer output is to be switched exceeds half the total number of columns.

14. A method as claimed in claim 13, wherein a plurality of additional buffers are used to share the output loads of one or more buffers when the number of columns to which those buffer outputs are to be switched exceed a predetermined fraction of the total number of columns.

15. Column address circuitry for driving the columns of a liquid crystal display, comprising circuitry for generating all possible drive signal levels on separate signal level lines and a buffer associated with each signal level line, the outputs of the buffers being selectably switchable onto the column outputs, wherein the column address circuitry further comprises a memory for storing the signal levels to be provided to each column, and wherein the buffers are controlled in dependence on the stored signal levels.

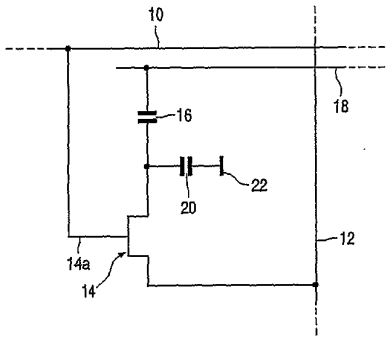


FIG. 1

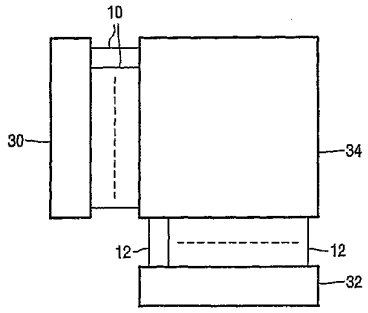
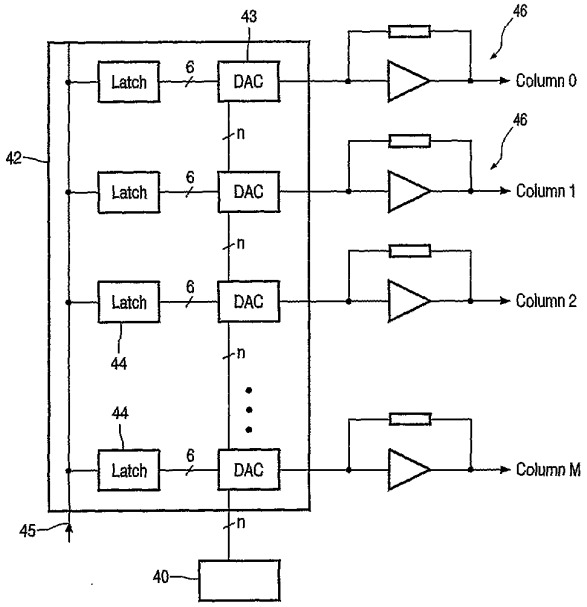


FIG. 2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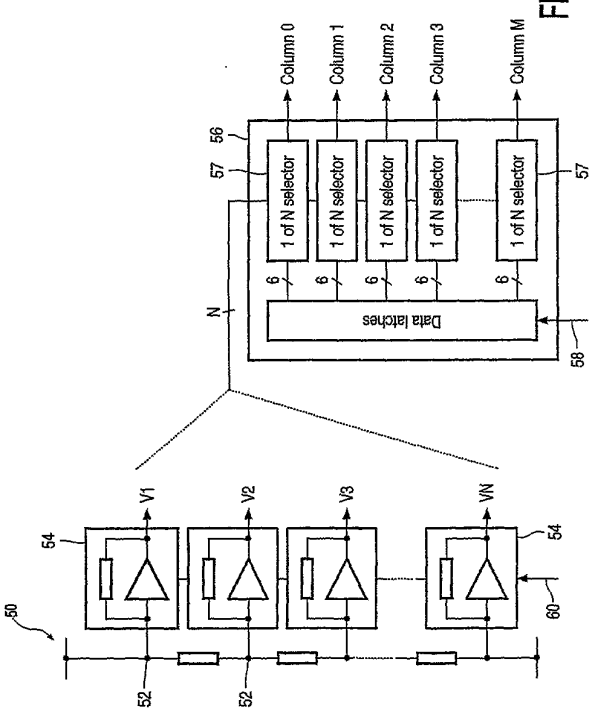
46
Latch
6
DAC
Column 0
n
42
46
Latch
6
DAC
Column 1
n
Latch
6
DAC
Column 2
44
n
44
Latch
6
DAC
Column M
45
n
40

FIG. 3

FIG. 4


Column 0
Column 1
Column 2
Column 3
Column M
56
57
1 of N selector
6
N
Data latches
58
V1
V2
V3
VN
54
60
50
52

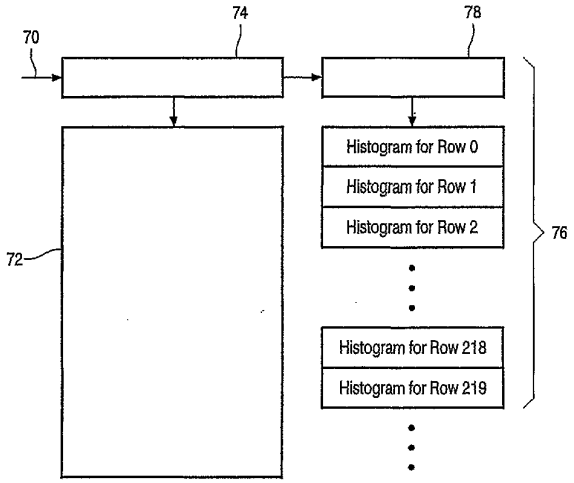

70
74
78
72
Histogram for Row 0
Histogram for Row 1
Histogram for Row 2
Histogram for Row 218
Histogram for Row 219
76

FIG. 5

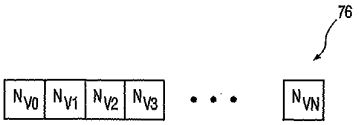

76
N_{V0}
N_{V1}
N_{V2}
N_{V3}
N_{VN}

FIG. 6

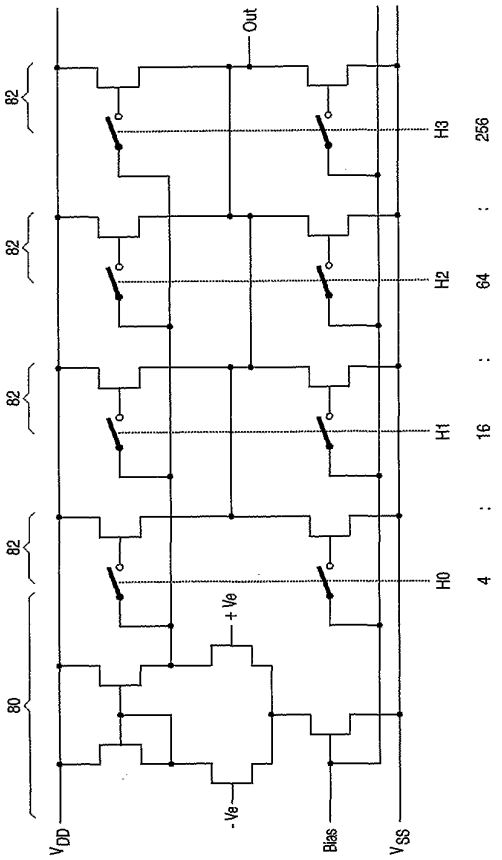


FIG. 7

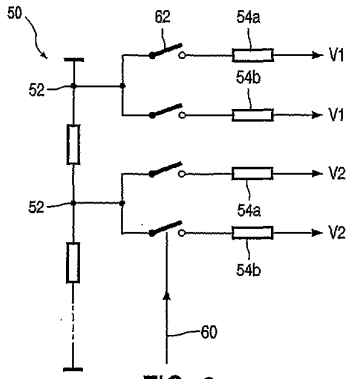

50
62
54a
V1
52
54b
V1
V2
52
54a
V2
54b
60

FIG. 8

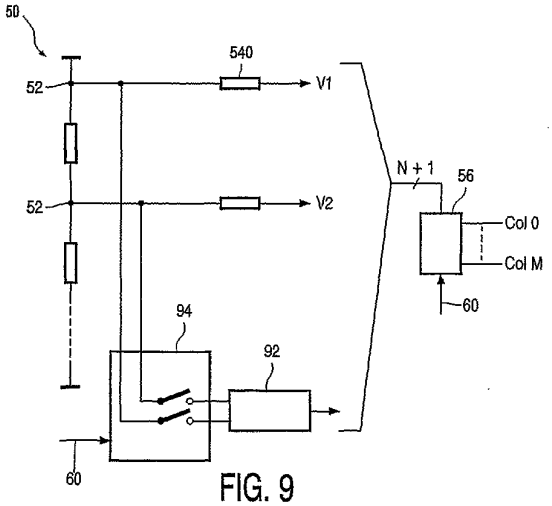

50
540
52
V1
52
V2
N + 1
56
Col 0
Col M
60
94
92
60

FIG. 9

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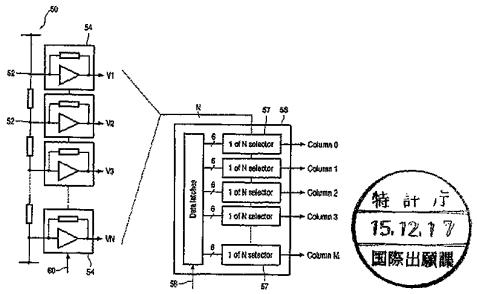
(54) Title: ACTIVE MATRIX DISPLAY DEVICE



(57) Abstract: A display has circuitry (50) which generates all possible pixel drive signal levels on separate signal level lines. A buffer (54) is associated with each signal level line. The outputs of the buffers are selectably switchable onto the columns. The signal levels for each column are stored in a memory (72) and the buffers are controlled in dependence on the stored signal levels. The response of the buffers is heavily dependent on the output load, and there is a very large variation in the output load of the buffers (54), as a function of the number of columns to which the buffer output is to be provided. The buffers are controlled in dependence on stored signal levels to ensure stability of the buffers for any output load.

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【国際調査報告】

INTERNATIONAL SEARCH REPORT

Int nal Application No
PCT/IB 02/00570

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According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G09G

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	WO 98 09269 A (SILICON IMAGE) 5 March 1998 (1998-03-05) page 14, line 30 -page 15, line 17; figure 7B	1,9,15
A	US 5 574 475 A (CALLAHAN ET AL.) 12 November 1996 (1996-11-12) column 8 -column 9; figure 3B	1,9,15
A	US 6 157 360 A (JEONG ET AL.) 5 December 2000 (2000-12-05) column 9, line 44 - line 67; figure 9	1,9,15
A	GB 2 300 773 A (SEIKO EPSON) 13 November 1996 (1996-11-13) page 25 -page 26, line 18; figures 1,4	1,9,15

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
29 August 2003	11/09/2003

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Lange, J

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/IB 02/00570

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