United States Patent

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[54] **AUTOMATIC ELECTRONIC COUNTER APPARATUS**
5 Claims, 3 Drawing Figs.

[52] **U.S. Cl.** **235/156,** 235/164
[51] **Int. Cl.** **G06f 7/38,** G06f 7/39
[50] **Field of Search** 235/152, 156, 159, 160, 164; 324/78, 79; 328/134

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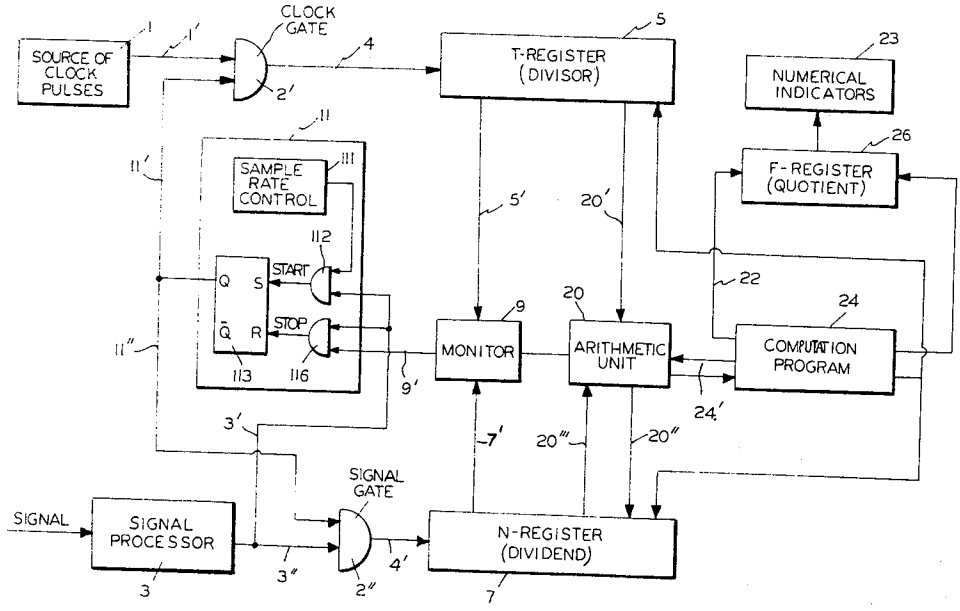
ABSTRACT: An improved automatic electronic digital counter is disclosed in which frequency-range switching is automatically effected and a quotient of the count of a clock pulse-fed counting register and a signal-period counting register is continually indicated.



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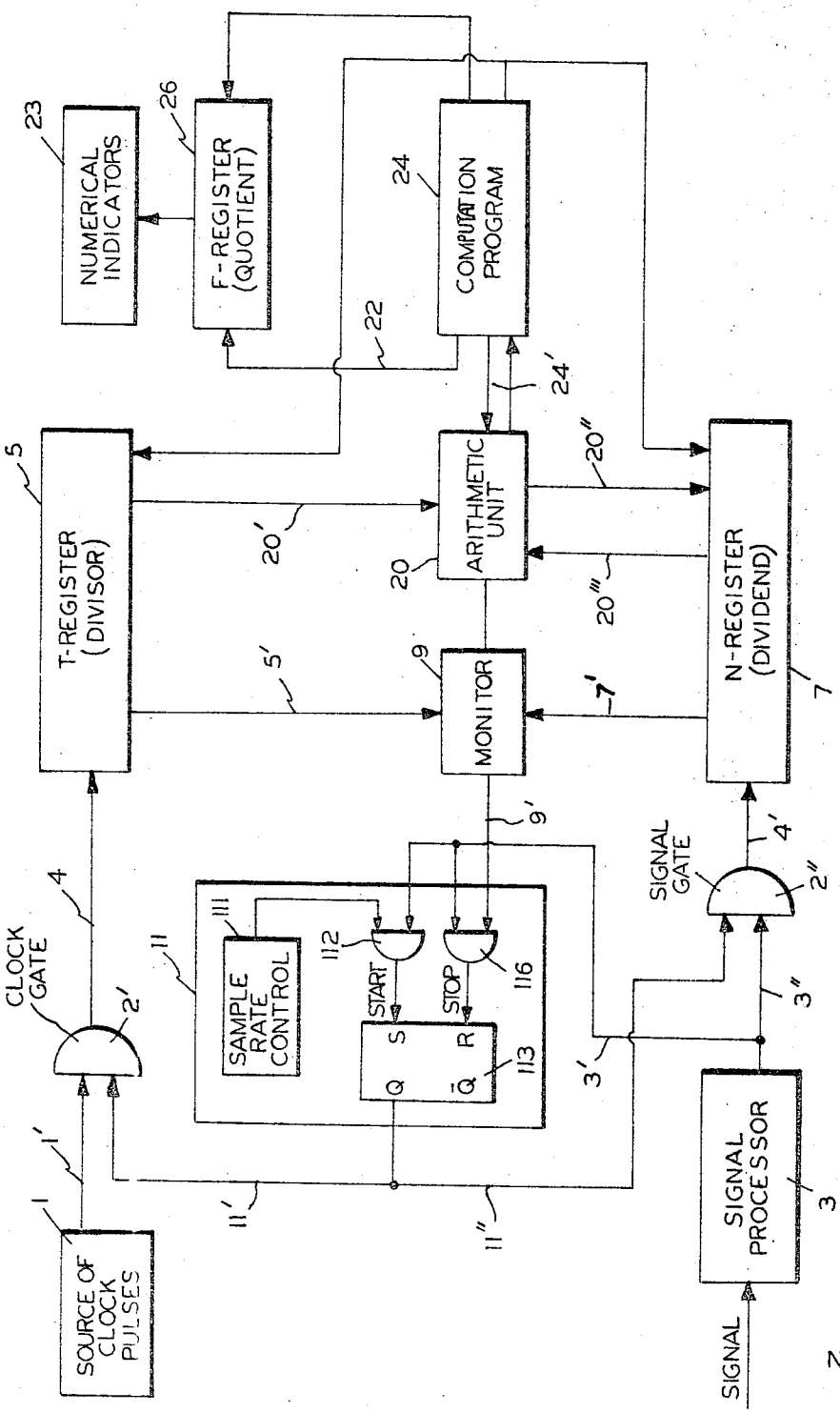

FIG. 1

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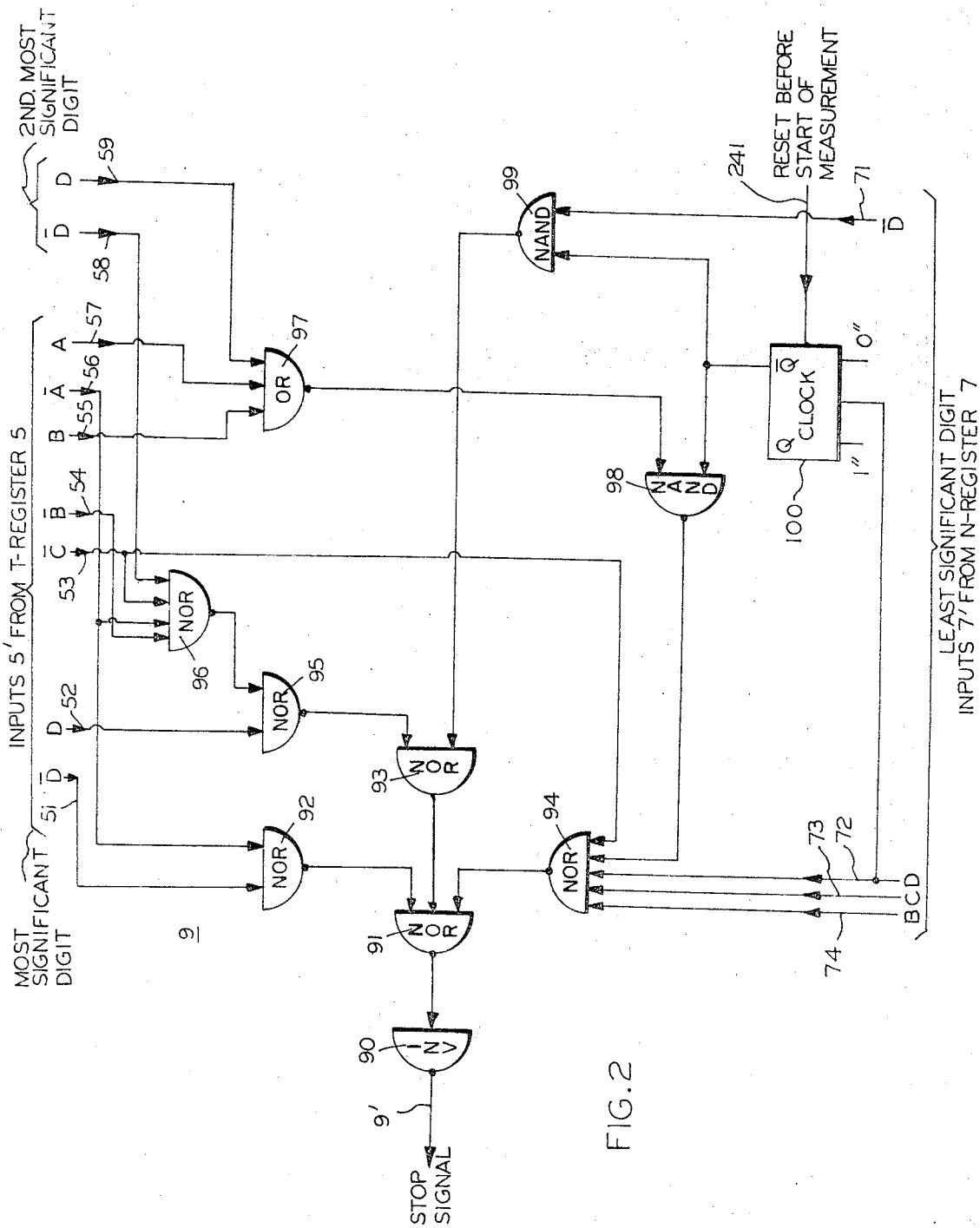

FIG. 2

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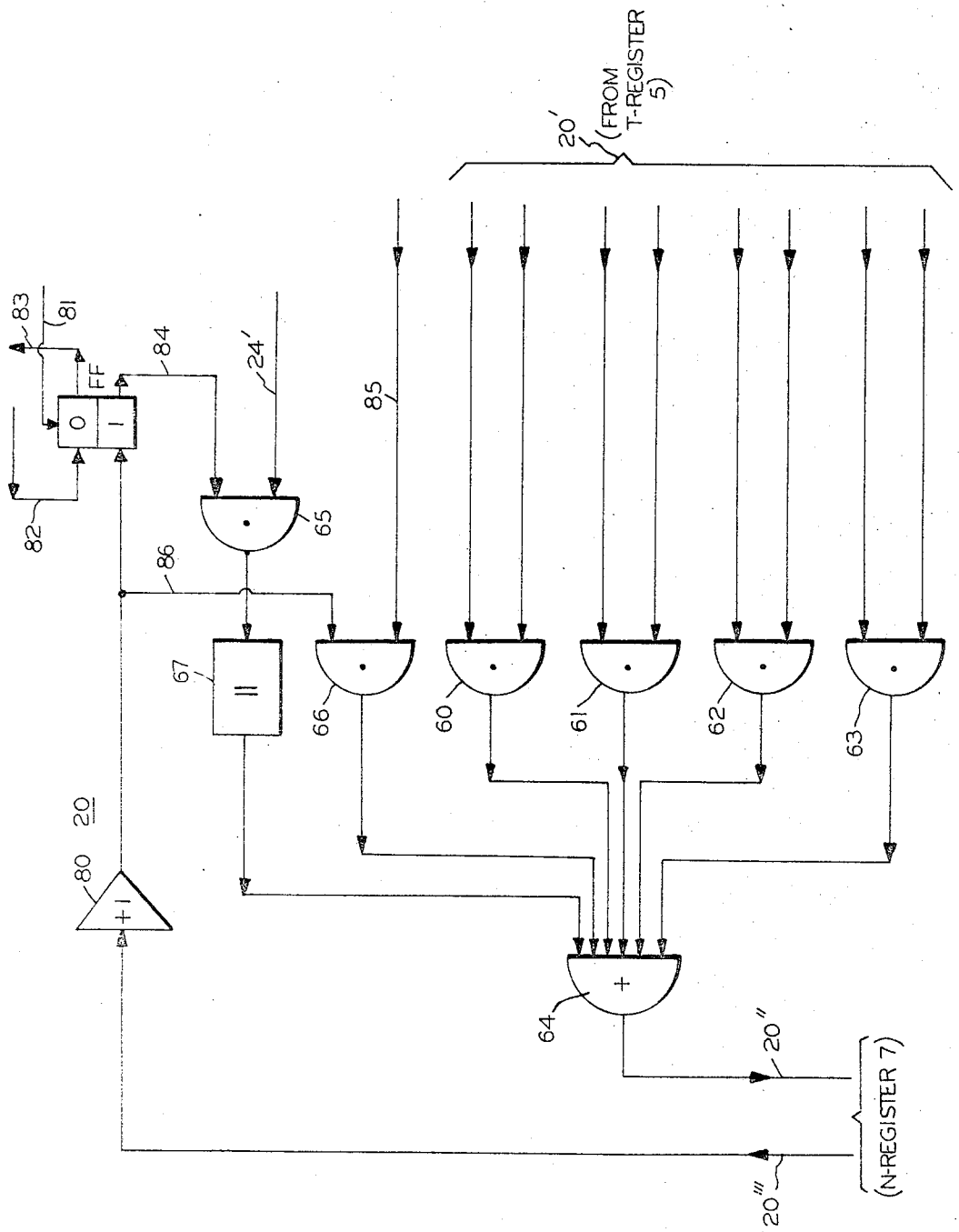

FIG. 3

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AUTOMATIC ELECTRONIC COUNTER APPARATUS

The present invention relates to automatic electronic counter apparatus in which frequency-range switching is automatically effected.

In copending application of Richard W. Frank, Robert G. Fulks and James K. Skilling, Ser. No. 730,430, filed May 20, 1968, for Automatically Adaptive Counter Apparatus, automatic counter apparatus of the character described is disclosed wherein a pair of counting registers is provided, one for accumulating clock pulse counts and the other for accumulating signal periods. Programming means controls the commencement and duration of the period measurement in accordance with an indication from monitoring means as to the degree of filling of the registers. While the systems therein disclosed are quite useful, they have certain limitations that in some applications are not desired. Such limitations may include either relatively slow computation of the reciprocal of the period measurement, or nonoverlapping switching ranges and loss of resolution at the low decade frequency range.

An object of the present invention, accordingly, is to provide novel automatic counter apparatus of the type described in said copending application, but void of the above-mentioned limitations. In summary, these ends are attained by a combined measurement computation system in which counting registers for accumulating the number of signal periods and the number of clock pulses are provided (the ratio being the frequency); and divisor, dividend and quotient registers are employed, with the counts in the divisor registers being subtracted iteratively from those in the dividend register to compute the quotient, the quotient register counting the number of subtractions to indicate the calculated frequency.

Other and further objects are hereinafter pointed out and delineated in the appended claims.

The invention will now be described with reference to the accompanying drawings, FIG. **1** of which is a block diagram of a preferred apparatus embodying the invention;

FIG. **2** is a similar diagram of a suitable monitor circuit for use in the system of FIG. **1**; and

FIG. **3** is a logic and block diagram of a suitable arithmetic unit for performing the functions required of such a unit in the embodiment of FIG. **1**.

Referring to FIG. **1**, a source of clock pulses **1** is shown applying the same at **1'** to a gate **2'**, enabled by an appropriate input at **11'** from a programmer **11** comprising a flip-flop **113**, start and stop controlling gates **112**, **116**, and a sample rate control **111**. A signal processor **3** similarly applies pulses corresponding to signal periods or cycles at **3''** to a similar gate **2''**, enabled by an input at **11''** from the programmer **11**. The gates **2'** and **2''** feed respective counting registers **5** (T-register-divisor) and **7** (N-register-dividend) by conductor lines **4** and **4'**, respectively. The registers **5** and **7** have their accumulated counts fed at **5'** and **7'** to a monitor circuit **9**, assuming the form of a switching gate control logic circuit, later described, that, via conductor **9'** controls the programmer gate **116**. Programmer gate **112** is controlled by the sample rate control **111**. Gates **112** and **116** are further connected at **3'** to the signal processor **3** which preferably produces one pulse for each cycle of the signal, with such pulses having a substantially uniform time relation to the zero crossings of the signal.

An arithmetic means **20** is shown connected at **20'** to register **5** and at **20''** to register **7**. Under the control of a conventional computer programmer **24**, the arithmetic means **20** subtracts the contents of register **5** from register **7** (N-T), adds **5** to **7** (N+T) or multiplies the contents of **7** by **10** (ION) and returns the result to register **7** via **20''**, replacing the original contents, with carries from a lower order being fed from the N-register **7** via conductor **20'''**, as later explained. Whenever a subtraction (N−T) results in a positive remainder, an output is produced at **22** and applied to a frequency (or quotient) F-register **26** that, in turn, enables frequency display or other utilization in any desired manner, such as the numerical indicators **23**.

The problem underlying the invention resides in the determination of the preferred realization of an automatic-ranging digital frequency meter which operates on the principal of measuring the time of a multiple of the period of the input signal and calculating the frequency from the measured data. The objectives include the minimum amount of apparatus and the best realization of the potentials of the system to provide the greatest accuracy in the shortest measurement time. Although the problem may be subdivided into a measurement problem and a computation problem, the objective of minimum apparatus requires that some of the circuits be used for both measurement and computation.

In the measurement part of the program, the two counting registers **5** and **7** are used; one counting the number of cycles of the signal (N), and the other counting the number of time units (T), with frequency F determined by the relation F=N/T.

In the computation portion, three registers are required: first, the divisor register **5** in which the divisor is stored; second, the dividend register **7** in which the dividend is placed at the start of computation and from which the divisor is subtracted iteratively to compute the quotient; and thirdly, the quotient register **26** which counts the number of subtractions. The number in the quotient register **26** at the end of the computation is, of course, the calculated frequency. In accordance with a preferred form of the invention, the divisor register is made the same as the time-unit T-register **5** and the dividend register is the same as the N register **7**, as shown in FIG. **1**.

These two registers **5** and **7** are designed to function as counting registers during the measurement part of the program. During the computation portion, one or both registers are required to function as shift registers in accordance with the design of the arithmetic means **20**. These registers may be either binary or decimal in accordance with the design of the arithmetic means **20** and the monitor circuit **9**.

The arithmetic means **20** may be designed to receive all of the digits or bits from both registers simultaneously, which is the parallel form, or it may be designed to receive a single digit or bit at a time from each register beginning with the least significant pair, which is the serial form. In general, the serial system usually results in fewer components, while the parallel system gives higher speed of computation. Since adequate speed can presently be achieved in a serial system built with economical components, the serial system is to be preferred except where application requires the ultimate in computational speed. When the serial form is used in the arithmetic means **20**, then the registers **5** and **7** are required to shift toward the least significant digit or bit.

In making period measurements, the gating logic is arranged so that N is measured exactly and T is measured to within plus or minus one time unit. The resolution, therefore, depends upon the number of time units measured. The measurement program is preferably arranged to constrain N to be any value which makes T lie in a predetermined range; with optimum resolutions attained under conditions: (100 percent of register capacity)$>T\geq$(100 percent$-1/F$).

The required resolution is equal to that of the result which is to be calculated. Thus, if a six digit result is desired, then about 10^6 time units should be accumulated. If decade counting is used in registers **5** and **7**, then the T-register **5** will have the same number of decades as the F-register **26**. When **5** and **7** are binary registers, the number of bits should be such as to give the same equivalent capacity. A six-digit result, for example, requires a 20 bit T-register **5**.

Requiring the lower bound of T to be continuously variable, makes the monitor circuit **9** unnecessarily complicated. A preferred compromise for decade registers is to monitor only the least significant digit of the N-register **7** and the two most significant digits of the T-register **5** setting. 100 percent $>T>$90 percent for $N>8$, and to program wider ranges of T for N=1 to 8. This provides overlapping ranges and without unduly complicated logic. Preferred numbers together with

frequency ranges for a T-register capacity of 100 ms. are shown in the table below:

N	T, msec.	F range, Hz.
1	100–48	10–20. 8333
2	48	20–41. 6666
3	78	30–38. 4615
4	78	40–51. 2820
5	78	50–64. 1025
6	78	60–76. 9230
7	78	70–89. 7435
8	78	80–102. 564
9	90	90–100. 000
10	90	100–111. 111
11, etc	90	110–122. 222

Since overlapping ranges are provided, the gating logic need not be fast. Frequency shifts smaller than the range overlap will not cause erroneous readings. Since the T-register **7** is always at 90 percent capacity (except at low frequencies), the full resolution capability of the system is very nearly achieved.

For binary registers, the monitor **9** can be further optimized by taking advantage of the fact that the capacities of the registers are not precisely powers of ten; that is to say, the minimum number of bits gives a capacity larger than that required for resolution. A six-digit result requires a T-register **5** of 20 bits or a capacity of 1,048,575. The nature of the computation, however, requires that the N-register **7** be 10 times as large, which requires 24 bits or 16,777,215. By adding one extra bit to the T-register **5**, we can, therefore, increase its useful capacity to 1,677,721, or binary 110,011,001,100,110,011,001. A preferred monitor circuit **9** for binary registers will monitor the six most significant bits of the T-register **5** and the two least significant bits of the N-register **7**. Preferred numbers together with frequency ranges for a 21 bit T-register **5** are shown in the table below:

N	T (binary) 2^{15}	T, msec.	F range, Hz.
1	110, 011–011, 000	167. 1168–78. 6432	5. 98384–12. 7156
2	011, 100	91. 7504	11. 9677–21. 7982
3	011, 110	98. 3040	17. 9516–30. 5175
4	011, 111	101. 5808	23. 9354–39. 3775
5	011, 111	------	29. 9192–49. 2218
6	011, 111	------	35. 9031–59. 0662
7	011, 111	------	41. 8869–68. 9106
8	011, 111	------	47. 8708–78. 7550
9	011, 111	------	53. 8546–88. 5994
10	011, 111	------	59. 8384–98. 4437
11, etc	------	------	65. 8223–108. 288

In this realization, the resolution will be in excess of that required for all frequencies requiring more than the three periods for measurement.

The principle of the division program is to subtract the divisor from the dividend iteratively until the remainder is smaller than the divisor, $N-FT<T$. (Systems which perform the operation $N+F\overline{T}<T$ or $\overline{N}+FT>T$ are equivalent and need not be considered separately). Subtracting is begun at the highest possible order (as is done in hand calculations). When the remainder is less than the divisor, it is multiplied by **10** together with shifting the order of the decade in which the quotient is accumulated.

At the start of computation, the divisor or clock pulse count is stored in the T-register **5** and the dividend or number of periods in the N-register **7**. The steps in computation may, for example, be as follows. The F-register decades **26** are reset to zero. The arithmetic means **20** subtracts T from N. If the remainder is positive, this is repeated until a negative remainder results. The number of subtractions which result in a positive remainder is counted by the first decade of the F-register **26** and is the most significant digit of the quotient. When a negative remainder occurs, the computer programmer **24** switches to addition, and the arithmetic means **20**, via **24'**, adds T to N once. The arithmetic means **20** then multiplies the remainder to the N-register **7** by 10 (in a decade register this is done by shifting once to the left), and shifts the order of the F-register decade in which the quotient is accumulated. If the first digit is zero, the shifting of the F-register **26** will be inhibited until a nonzero digit has been computed. The said subtraction, addition and multiplication steps are then repeated until the desired number of digits has been calculated. If roundoff is desired, one more digit is calculated, but this time the subtractions are counted by a scale of five and any carry allowed to propagate through the register.

Thus, to summarize, when the monitor **9** indicates that the count in the clock pulse or T-register (divisor) **5** has reached a predetermined number less than the complete full count thereof, the programmer **11** effects termination of the measurement at a next appropriate output from the signal processor **3**. The gate control logic circuit of the monitor **9**, moreover, having received the most significant digits or bits of the T-register **5** and the least significant digits or bits of the N-register **7** and having determined when the former count has reached the said predetermined number required by the value of the latter count, applies a stop signal at **9'** to the programmer **11** which is caused to terminate the outputs **11'–11''** to the gates **2'–2''**, respectively, upon the feeding of the next signal via **3'** from the signal processor. The division of the count of register **5** into that of register **7**, as indicated by quotient register **26**, provides a measure of the frequencies corresponding to the signal periods.

It now remains to describe the types of circuits that may be employed in the system of FIG. **1**.

The gate control logic monitor **9** for switching control of the programmer **11** may assume the form, for example, of FIG. **2**. FIG. **2**, appropriate to decimal counting in registers **5** and **7**. The circuit illustrated is a configuration for decimal registers (**1-2-4-2** decade) and consists basically of an inverter **90**, NOR gates **91** through **96**, an OR gate **97**, NAND gates **98** and **99** and flip-flop **100**. Inputs **71—74** are from the N-register **7** representing the least significant digit thereof, such as B, C, D (at **74**, **73** and **72**) from three flip-flops of a register decade, and $\overline{D}$ (at **71**), the inverted output of the third flip-flop.

Inputs **51—59** are from the T-register **5** with the most significant digit represented by $\overline{D}$, D, $\overline{C}$, $\overline{B}$, B, $\overline{A}$ and A at **51—57**, respectively, and the second most significant digit $\overline{D}$, D, applied at **58** and **59**. Initially the B C D inputs are at **0** level and the inputs $\overline{D}$ are at **1** level, as later discussed.

Input **241** is a reset signal from the computer programmer **24** which sets the output of flip-flop **100** to the **1** level before the start of a new measurement, and is simultaneously applied to registers **5** and **7**, setting their respective outputs at conductors **52, 55, 57, 59, 72, 73** and **74** to the **1** level, and their outputs at **51, 53, 56, 58** and **71**, to the **0** level. **1** level inputs at **51** and **56** cause the output of gate **92** to be at the **0** level; while **1** level inputs at **53, 54, 56** and **58** cause the output of gate **96** to be at **0** level, which, together with a **0** level input at **52**, produces a **1** level output from the gate **95**. The **1** level output from gate **95**, in turn, produces a **0** level from gate **93**. **0** level inputs at conductors **55, 57**, and **59**, on the other hand, result in a **0** level output from gate **97**; which, applied to gate **98**, produces a **1** level output. This **1** level output from gate **98** and the **1** level input at **53** cause a **0** level output from gate **94**. **0** levels from gates **92, 93** and **94**, however, cause a **1** level output from gate **91**, which thereupon causes a **0** output from the inverter **90**, serving as the stop signal at **9'**. Thus, the stop signal at **9'** is initially at the **0** level. In order to change to the **1** level, one of the inputs to gate **91** must change to the **1** level.

Upon commencement of the measurement, the inputs at **51—59** and **71—74** will change in accordance with the number of counts accumulated in registers **5** and **7**, respectively. If less than two counts have been accumulated in the N-register **7**, as for a one or two period measurement, the stop signal at **9'** will change from **0** to **1** level when the two most significant digits of the T-register **5** are four and eight. At this count, inputs at **53** and **58** will have changed from the **1** level to the **0** level, and the input at **59** will have changed from the **0** to the **1** level. The **1** level at input **59** causes a **1** level output from gate **97**, which, together with the **1** level output from flip-flop **100**, produces a **0** level output from gate **98**. Since the inputs of

gate **94** are now all at the **0** level, a **1** level output will be produced and will be applied to gate **91**, causing the stop signal at **9'** to change to the **1** level.

If two to seven counts have been accumulated in the N-register **7**, as for a three to eight period measurement, the stop signal at **9'** will change from the **0** to the **1** level when the two most significant digits of the T-register **5** are seven and eight. A two to seven count in the N-register **7**, moreover, will cause one or both of the inputs **73** and **74** to have changed from the **0** to the **1** level, producing a **0** level at the output of gate **94** for any T-register count. At a T-register count of **78**, inputs at **53**, **54**, **56** and **58** will have changed from the **1** level to the **0** level, and inputs at **55**, **57** and **59** will have changed from the **0** to the **1** level. **0** inputs at **53**, **54**, **56** and **58** cause a **1** level output from gate **96** which, in turn, produces a **0** level output from gate **95**. The **1** level input at **71** and the **1** level output from flip-flop **100** produces a **0** level from gate **99**. Together with the **0** level from gate **95**, this causes a **1** level output from gate **93** causing the stop signal **9'** to change to the **1** level.

If eight or more counts have been accumulated in the N-register **7**, as for a nine or more periods measurement, the stop signal at **9'** will change from the **0** to the **1** level when the most significant digit of the T-register **5** is nine. When eight or nine counts have been accumulated in the N-register **7**, however, input **71** will have changed from the **1** level to the **0** level, producing a **1** level output from gate **99**, which produces a **0** level output from gate **93**. Input **72** will have changed from the **0** to the **1** level, which produces a **0** level from the output of gate **94**. When the 10th count is recorded by the N-register **7**, the input at **72** will return to the **0** level, which correspondingly sets the output of flip-flop **100** to the **0** level. This produces **1** level outputs from gates **98** and **99** which cause **0** level outputs from gates **94** and **93**, respectively, for this and all higher counts in the N-register **7**. When the most significant digit of the T-register **5** reaches nine, inputs **51** and **56** will have changed from the **1** to the **0** level and inputs **52** and **57** will have changed from the **0** to the **1** level. **0** level inputs at **51** and **56** cause a **1** level output from gate **92** to be applied to gate **91**, causing the stop signal at **9'** to change to the **1** level.

The arithmetic matrix unit **20** may, as an example, be of the type shown in FIG. **3** to perform the required before-mentioned functions. Conductors **20'** apply to the unit **20** pulse train inputs from the divisor or T-register **5** (which may be termed ADD1, $\bar{1}$, ADD2, $\bar{2}$, ADD4, $\bar{4}$, ADD2' and $\bar{2}'$ Apulses). These are applied through respective gates **60** through **63** to the addition gate **64**; whence, for each cycle, they are added into the corresponding decade in the N-register **7** along conductor **20''**.

A carry from a lower order, as before discussed, is fed from the N-register **7** via conductor **20'''** and inverter **80** to flip-flop FF, to which the **0** level set is applied at **81** and the carry reset, at **82**; the carry complement being available at conductor **83**. The output from the **1** section of the flip-flop FF is shown applied at **84** to a carry gate **65** to which a carry gate pulse is applied along a conductor **24'** from the programmer **24** (FIG. **1**). A further gate **66** is energized by an AC level controlling count gate pulse fed via conductor **85** and the output of **80**, applied at **86**, and also feeds the adder **64**. Also applied to adder gate **64** is the output of gate **65**, as differentiated at **67**. When the carry gate **65** is turned on, therefore, the output thereof is differentiated at **67** and produces a pulse to add one more at the adder **64** to the next higher decade. If, during the time the carry gate **65** is open because, for example, of a carry from further down the line, a lower order carry at **20'''** (from the N-register **7**) will complement the flip-flop FF and send a pulse through the adder gate **64** in the same manner above-described. The basic system of addition herein involved is further described, for example, in Arithmetic Operations In Digital Computers, by R. K. Richards, Van Nostrand, 1955, commencing with page 234.

The counters **5**, **7** and **26** may, as further illustrations, be of the bidirectional decade type, and the programmer **24** may be any conventional type. As before explained, moreover, the invention is applicable to binary as well as decade apparatus.

As an illustration, a successful counter having the above described features has been constructed with a frequency range of from 0.6 Hz to 20 MHz., six-digit resolution, and an average measurement time of 100 milliseconds above 6 Hz., 1 second down to 0.6 Hz. All six digits are always used; a measurement at the counter's low frequency limit is actually presented with microhertz resolution. A 10 MHz. clock was employed. A register capacity of 167 ms. was provided, which corresponds to a frequency of 5.99 Hz. The lower limits of measurement time were programmed to produce the following results:

Number of Periods:	Minimum measurement time, msec.
1	78. 6
2	91. 8
3	98. 3
4 and higher	101. 6

It should be borne in mind that the steps referred to in the above program do not represent range changes in the usual sense; that is, there is no interruption of the measurement, but only a decision as to when to terminate. The range (i.e., decimal-point position and measured units) is determined entirely in the subsequent computation.

In order to measure lower frequencies, the measurement time must be increased, as by the lowering of the clock frequency.

In summary of the previously described operation, the registers **5** and **7** function either as counting registers or as shift registers by application of proper programming signals. They count signal pulses and clock pulses during the measurement; and during computation, they become, respectively, the dividend and divisor registers in a serial computer. The method of computation thus involves subtracting the divisor from the dividend and testing for a positive remainder. If the remainder is positive, a pulse is applied to the first decade of the quotient register **26** and another subtraction is performed. When the remainder is negative, the divisor is added to restore a positive remainder, completing the calculation of the first digit. The remainder is then multiplied by 10 and the process repeated to calculate the second digit. Usually the dividend is initially smaller than the divisor (except where the signal frequency exceeds the clock frequency), so that the first digit is usually zero. The quotient register **26** is designed to ignore such nonsignificant zeros, however, and will wait until a non-zero digit is recorded in the first decade before transferring its input to the second decade. The steps required to perform this normalization are counted to determine decimal point position and units. Computation is continued until seven digits have been computed, the last of which is not displayed but is used to generate a roundoff in the quotient register **26**. The time required for computation depends upon the frequency, varying from about 150 μs. for 10.0000 + MHz. to about 675 μs. for 9.99999 Hz. in the above-mentioned instrument. Because of this short computation time, the result is displayed at **23** directly from the quotient register **26** without the need for buffer storage.

Further modifications will, also, of course, suggest themselves to those skilled in this art; and all such are considered to fall within the spirit and scope of the invention as defined in the appended claims.

I claim:

1. Counter apparatus having, in combination, a signal processor for producing impulses the signal periods of which are to be measured, a source of clock pulses, gating means connected with said source and said signal processor, respectively, and each having output circuit means, a pair of counting registers connected with said output circuit means, respectively, one to accumulate counts of said clock pulses and a

second to count signal periods during a measurement time, programming means connected with the gating means for controlling the commencement and duration of the measurement time, monitoring means connected with both counting registers for determining when the count in the said one register has reached any one of several predetermined numbers less than the complete full count thereof and dependent upon the concurrent count in said second register, means for connecting the monitoring means with the programming means to cause the programming means to effect the termination of the said measurement time in response to the said determining, and means connected to said registers for dividing the count of the said one register into that of the said second register to provide a measure of the frequency corresponding to the said signal periods.

2. Apparatus as claim in claim 1 and in which the said counting registers are decimal and the said monitoring means comprises gate control logic circuit means having means for receiving the most significant digit count of the said one register and the least significant digit count of the said second register and in which the programming means has means to produce a stop signal for application to the gating means upon the advent of the next pulse from the said signal processor after the said determining.

3. Counter apparatus having, in combination, a signal processor which produces one pulse for each cycle of the signal, the periods of which are to be measured, said pulses having a uniform time relation to the zero crossing of said signal, a source of clock pulses, gating means connected with said source and said signal processor, respectively, and each having output circuit means, a pair of counting registers connected with said output circuit means, respectively, one to accumulate counts of said clock pulses and a second to count signal periods during a measurement time, programming means connected with the gating means for controlling the commencement and duration of the measurement time, monitoring means connected with both counting registers for determining when the count in said one register has reached any one of several predetermined numbers less than the complete full count thereof, and dependent upon the concurrent count in said second register, means for connecting the monitoring means with the programming means to cause the programming means to effect the termination of the said measurement time in response to the said determining, and means connected to said registers for dividing the count of the said one register into that of the said second register to provide a measure of the frequency corresponding to the said signal periods.

4. Apparatus as claim in claim 3 and in which the said counting registers are decimal and the said monitoring means comprises gate control logic circuit means having means for receiving the two most significant digits of the said one register and the last significant digit of the said second register and in which the said programming means has means to produce a stop signal for application to the gating means upon the advent of the next pulse from the said signal processor after the said determining.

5. Apparatus as claimed in claim 3 and in which the said counting registers are binary and the said monitoring means comprises gate control logic circuit means having means for receiving the second through the sixth most significant bits of the said one register and the two least significant bits of the said second register and in which the said programming means has means to produce a stop signal for application to the gating means upon the advent of the next pulse from a said signal processor after the said determining.