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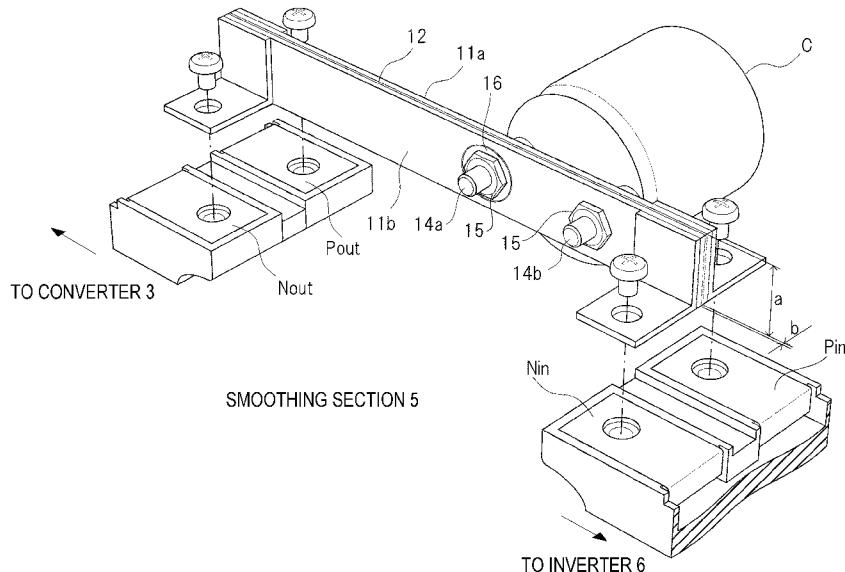
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(54) Title: INDUCTION HEATING POWER SUPPLY APPARATUS



(57) Abstract: An induction heating power supply apparatus includes a smoothing section to smooth pulsating current of DC power output from a DC power supply section, and an inverter to convert the DC power smoothed by the smoothing section to AC power. The smoothing section includes a pair of bus bars connected to the inverter and a capacitor connected to the pair of bus bars. Each of the bus bars has an external surface extending in a current flow direction, the external surface including a flat face having a larger surface dimension than another face of the external surface in a direction perpendicular to the current flow direction. The bus bars are arranged in a layered manner such that the flat faces of the bus bars are opposed to each other and such that an insulator is sandwiched between the flat faces of the bus bars.

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Description

Title of Invention: INDUCTION HEATING POWER SUPPLY APPARATUS

Technical Field

[0001] The present invention relates to an induction heating power supply apparatus.

Background Art

[0002] Induction heating is used as a heating method in a treat treatment of steel workpieces. In the induction heating, AC power is applied to a heating coil to cause the heating coil to generate a magnetic field, and a workpiece placed in the magnetic field is heated by electric current induced in the workpiece.

[0003] A related art power supply apparatus for supplying AC power to such a heating coil has a converter to convert AC power of a commercial power supply to DC power, a capacitor to smooth pulsating current of the DC power, and an inverter to convert the smoothed DC power back to AC power to generate high frequency AC power to be supplied to the heating coil (see, e.g., JP 2009-277577A).

[0004] The inverter typically has a bridge circuit including a plurality of power semiconductor devices capable of performing a high speed switching operation to produce high frequency AC power

Summary

[0005] The high speed switching operation of a power semiconductor device causes a rapid change in electric current flowing in the power semiconductor device. The current change di/dt produces surge voltage $Lxdi/dt$ between terminals of the power semiconductor device due to a parasitic inductance L of a conductive path between the power semiconductor device and the capacitor serving as a voltage source.

[0006] Excessive surge voltage may cause a damage to the power semiconductor device. The current change di/dt is primarily determined by the characteristics of the power semiconductor device. Therefore, reducing the parasitic inductance L is a way to suppress the surge voltage.

[0007] Illustrative aspects of the present invention provide an induction heating power supply apparatus in which surge voltage is suppressed to improve a protection of an inverter.

[0008] According to an illustrative aspect of the present invention, an induction heating power supply apparatus includes a smoothing section configured to smooth pulsating current of DC power output from a DC power supply section, and an inverter configured to convert the DC power smoothed by the smoothing section to AC power. The smoothing section includes a pair of bus bars connected to the inverter and at least

one capacitor connected to the pair of bus bars. Each of the bus bars has an external surface extending in a current flow direction. The external surface includes at least one flat face having a larger surface dimension than another face of the external surface in a direction perpendicular to the current flow direction. The pair of bus bars are arranged in a layered manner such that the flat faces of the pair of bus bars are opposed to each other and such that an insulator is sandwiched between the flat faces of the pair of bus bars.

Brief Description of Drawings

- [0009] [fig.1]Fig. 1 is a circuit diagram of an induction heating power supply apparatus according to an embodiment of the present invention.
- [fig.2]Fig. 2 is a perspective view illustrating an example of a configuration of a smoothing section of the induction heating power supply apparatus of Fig. 1.
- [fig.3]Fig. 3 is an exploded perspective view of the smoothing section of Fig. 2.
- [fig.4]Fig. 4 is a sectional view of the smoothing section of Fig. 2.
- [fig.5]Fig. 5 is a perspective view of a reference example of the smoothing section.
- [fig.6]Fig. 6 is a perspective view of another reference example of the smoothing section.
- [fig.7]Fig. 7 is a circuit diagram of an induction heating power supply apparatus according to another embodiment of the present invention.
- [fig.8]Fig. 8 is a circuit diagram of an induction heating power supply apparatus according to another embodiment of the present invention.
- [fig.9]Fig. 9 is a perspective view illustrating an example of a configuration of a smoothing section of the induction heating power supply apparatus of Fig. 8.
- [fig.10]Fig. 10 is a sectional view of the smoothing section of Fig. 9.
- [fig.11]Fig. 11 is a circuit diagram of an induction heating power supply apparatus according to another embodiment of the present invention..

Description of Embodiments

- [0010] Fig. 1 illustrates an induction heating power supply apparatus 1 according to an embodiment of the present invention.
- [0011] The induction heating power supply apparatus 1 has a DC power supply section 4, a smoothing section 5 and an inverter 6. The DC power supply section 4 includes a converter 3 configured to convert AC power supplied from a commercial AC power supply 2 to DC power. The smoothing section 5 is configured to smooth pulsating current of the DC power output from the DC power supply section 4. The inverter 6 is configured to convert the DC power smoothed by the smoothing section 5 to high frequency AC power.
- [0012] The inverter 6 has an arm including power semiconductor devices Q1, Q2 connected

in series, and another arm including power semiconductor devices Q3, Q4 also connected in series. The invert 6 is configured as a full bridge circuit so that a series connection point between the power semiconductor devices in each of the arms serves as an output terminal. Freewheel diodes D are connected in parallel with the power semiconductor devices Q1, Q2, Q3, Q4 respectively.

- [0013] For example, various power semiconductor devices which can perform switching operation, such as an insulated gate bipolar transistor (IGBT) and a metal-oxide-semiconductor field-effect transistor (MOSFET) may be used as each power semiconductor device. In addition, examples of the material of the power semiconductor device may include silicon (Si) and silicon carbide (SiC).
- [0014] A heating coil 7 is connected between the series connection point of the power semiconductor devices Q1, Q2 and the series connection point of the power semiconductor devices Q3, Q4 so that high frequency power is supplied to the heating coil 7 by the switching operations of the power semiconductor devices Q1, Q2, Q3, Q4.
- [0015] Figs. 2 to 4 illustrate an example of a configuration of the smoothing section 5.
- [0016] The smoothing section 5 includes a pair of bus bars 11a, 11b, and at least one capacitor C connected to the pair of bus bars 11a, 11b.
- [0017] Each of the bus bars 11a, 11b is a flat plate conductor having a pair of flat plate faces and a pair of flat side faces, the pair of flat plate faces and the pair of flat side faces forming the external surface of the conductor extending in a current flow direction (the longitudinal direction). The bus bars 11a, 11b are arranged in a layered manner such that the flat plate faces of the bus bars 11a, 11b or the flat side faces of the bus bars 11a, 11b, those having relatively large surface dimension in a direction (width direction) perpendicular to the current flow direction are opposed to each other and such that an insulator sheet 12 is sandwiched between the bus bars 11a, 11b.
- [0018] One end portion of the bus bar 11a is connected to a positive electrode Pout of an output terminal of the converter 3 while the other end portion of the bus bar 11a is connected to a positive electrode Pin of an input terminal of the inverter 6. One end portion of the bus bar 11b is connected to a negative electrode Nout of an output terminal of the converter 3 while the other end portion of the bus bar 11b is connected to a negative electrode Nin of an input terminal of the inverter 6.
- [0019] A pair of terminals 14a, 14b of the capacitor C connected to the bus bars 11a, 11b are formed as screw terminals and arranged side by side on one side of the capacitor C. The terminals 14a, 14b are arranged to extend through the bus bars 11a, 11b and the insulator 12 in a direction in which the bus bars 11a, 11b and the insulator 12 are layered in the order of the bus bar 11a, the insulator 12 and the bus bar 11b. Nuts 15 are screwed onto distal end portions of the terminals 14a, 14b respectively so that the capacitor C is fixed to the bus bars 11a, 11b.

[0020] As shown in Figs. 3 and 4, the terminal 14a and the nut 15 screwed to the terminal 14a are electrically insulated from the bus bar 11b by an insulating washer 16. On the other hand, a large-diameter flange portion 17a formed in a base end portion of the terminal 14a makes contact with the bus bar 11a so that the terminal 14a and the bus bar 11a are electrically coupled to each other. Thus, the terminal 14a is connected only to the bus bar 11a.

[0021] The terminal 14b and a large-diameter flange portion 17b formed in a base end portion of the terminal 14b are electrically insulated from the bus bar 11a by an insulating washer 16. On the other hand, the nut 15 screwed to the terminal 14b makes contact with the bus bar 11b so that the terminal 14b and the bus bar 11b are electrically coupled to each other through the nut 15. Thus, the terminal 14b is connected only to the bus bar 11b.

[0022] Figs. 5 and 6 illustrate reference examples of the smoothing section 5 respectively.

[0023] In the example shown in Fig. 5, the pair of bus bars 11a, 11b are arranged such that side faces of the bus bars 11a, 11b are opposed to each other. In the example shown in Fig. 6, the pair of bus bars 11a, 11b are arranged such that plate faces of the bus bars 11a, 11b are opposed to each other with a capacitor being interposed between the bus bars 11a, 11b. In the example shown in Fig. 6, one of the pair of the terminals is provided on one side of the capacitor and the other terminal is provided on the opposite side of the capacitor.

[0024] The inductance of a pair of parallel flat plate conductors is associated with b/a , wherein “a” is the width of opposed faces of the pair of parallel flat plate conductors, i.e. a dimension in a direction perpendicular to an extension direction of the conductors (flowing direction of a current), and “b” is the distance between the opposed faces of the conductors. More specifically, the inductance becomes smaller as b/a becomes smaller. With the width “a” of the opposed faces being constant, the inductance becomes smaller as the distance “b” between the opposed faces becomes smaller. With the distance “b” between the opposed faces being constant, the inductance becomes smaller as the width “a” of the opposed faces becomes larger.

[0025] As shown in Figs. 2 to 4, the bus bars 11a, 11b are arranged in a layered manner such that the plate faces of the bus bars 11a, 11b are opposed to each other and such that the insulator sheet 12 is sandwiched between the bus bars 11a, 11b. In this case, as compared with the reference example shown in Fig. 5 in which the side faces of the pair of bus bars 11a, 11b are opposed to each other, the width “a” of the opposed faces of the pair of bus bars 11a, 11b is larger so that an inductance of the pair of bus bars 11a, 11b is reduced.

[0026] Moreover, as compared with the reference example shown in Fig. 6 in which the plate faces of the pair of bus bars 11a, 11b are opposed to each other and the capacitor

is interposed between the bus bars 11a, 11b, the distance “b” between the opposed faces of the pair of bus bars 11a, 11b is shorter so that an inductance of the pair of bus bars 11a, 11b is further reduced.

- [0027] Thus, by arranging the bus bars 11a, 11b in a layered manner such that the plate faces of the pair of bus bars 11a, 11b are opposed to each other and such that the insulator sheet 12 is sandwiched between the bus bars 11a, 11b, a parasitic inductance of a conductive path between the capacitor C and the power semiconductor devices Q1, Q2, Q3, Q4 to which DC power is supplied from the capacitor C can be reduced. Accordingly, surge voltage occurring between opposite terminals of the power semiconductor devices Q1, Q2, Q3, Q4 due to the parasitic inductance is suppressed so that the protection of the inverter 6 improved.
- [0028] A film capacitor, a ceramic capacitor, or the like, which is smaller in internal inductance than an electrolytic capacitor is preferably used as the capacitor C.
- [0029] Although one capacitor C is connected to the pair of bus bars 11a, 11b in the examples described above, a plurality of capacitors C may be connected to the pair of bus bars 11a, 11b in parallel.
- [0030] In an example shown in Fig. 7, the arm including the power semiconductor devices Q1, Q2 and the arm including the power semiconductor devices Q3, Q4 are each configured as a module. The first module M1 including the power semiconductor devices Q1, Q2 is connected to a pair of bus bars 11a-1, 11b-1, and a second module M2 including the power semiconductor devices Q3, Q4 is connected to a pair of bus bars 11a-2, 11b-2. In this case, the pair of bus bars 11a-1, 11b-1 and the pair of bus bars 11a-2, 11b-2 may be provided in the smoothing section 5, and each of the pair of bus bars 11a-1, 11b-1 and the pair of bus bars 11a-2, 11b-2 may be configured such that, like the pair of bus bars 11a, 11b described above, the pair of bus bars are arranged in a layered manner with the insulator sheet 12 being sandwiched between the plate faces of the pair of bus bars. At least one capacitor C is connected to the pair of bus bars 11a-1, 11b-1, and at least one capacitor C is connected to the pair of bus bars 11a-2, 11b-2.
- [0031] Fig. 8 illustrates an induction heating power supply apparatus 101 according to another embodiment of the present invention. The elements of the induction heating power supply apparatus 101 that are the same as those of the induction heating power supply apparatus 1 described above will be denoted by the same reference signs and description thereof will be omitted or simplified.
- [0032] The induction heating power supply apparatus 101 includes a DC power supply section 4, a smoothing section 105, and an inverter 106. The DC power supply section 4 includes an AC power supply 2 and a converter 3. The smoothing section 105 is configured to smooth pulsating current of DC power output from the DC power supply

section 4. The inverter 106 is configured to convert the DC power smoothed by the smoothing section 105 to high frequency AC power.

- [0033] A plurality of bridge circuits each formed by a set of power semiconductor devices Q1, Q2, Q3, Q4 are provided in the inverter 106. In the illustrated example, two bridge circuits, i.e. a first bridge B1 and a second bridge B2, are provided in the inverter 106. The first bridge B1 and the second bridge B2 are connected to a heating coil 7 in parallel so that power to be supplied to the heating coil 7 can be distributed into the first bridge B1 and the second bridge B2.
- [0034] Figs. 9 and 10 show a configuration example of the smoothing section 105.
- [0035] The smoothing section 105 includes a pair of bus bars 111a, 111b, capacitors C1, C2 and connection portions 118, 119. The capacitors C1, C2 are connected to the pair of bus bars 111a, 111b. The pair of bus bars 111a, 111b are connected to the inverter 106 through the connection portions 118, 119.
- [0036] Each of the pair of bus bars 111a, 111b is a flat plate conductor having a pair of flat plate faces and a pair of flat side faces, the pair of flat plate faces and the pair of flat side faces forming the external surface of the conductor extending in a current flow direction (the longitudinal direction). The bus bars 111a, 111b are arranged in a layered manner such that the flat plate faces of the bus bars 111a, 111b or the flat side faces of the bus bars 111a, 111b, those having a relatively large surface dimension in a direction (width direction) perpendicular to the current flow direction are opposed to each other and such that an insulator sheet 112 is sandwiched between bus bars 111a, 111b. In this manner, an inductance of the bus bars 111a, 111b can be reduced, like the pair of bus bars 111a, 111b of the smoothing section 5 described above.
- [0037] The connection portions 118, 119 are provided respectively for the bridge circuits of the inverter 106. The connection portion 118 is connected to the first bridge B1. The connection portion 119 is connected to the second bridge B2.
- [0038] The connection portion 118 includes a pair of flat plate conductors 120a, 120b, and an insulator sheet 121. Each of the pair of conductors 120a, 120b has a pair of flat plate faces and a pair of flat side faces, the pair of flat plate faces and the pair of flat side faces forming the external surface of the conductor extending in a current flow direction thereof. The pair of conductors 120a, 120b are arranged in a layered manner such that the flat plate faces of the conductors 120a, 120b or the flat side faces of the conductors 120a, 120b, those having a relatively large surface dimension in a direction perpendicular to the current flow direction are opposed to each other and such that the insulator 121 is sandwiched between the conductors 120a, 120b. A base end portion of the conductor 120a is arranged on the bus bar 111b such that the insulator 121 is sandwiched between bus bar 111b and the base end portion of the conductor 120a. Thus, the conductor 120a and the bus bar 111b are electrically insulated from each

other. A base end portion of the conductor 120b is arranged directly on the bus bar 111b. Thus, the conductor 120b and the bus bar 111b are electrically coupled to each other.

[0039] The connection portion 119 also includes a pair of flat plate conductors 120a, 120b, and an insulator sheet 121. The pair of conductors 120a, 120b are arranged in a layered manner such that the plate faces of the conductors 120a, 120b are opposed to each other and such that the insulator 121 is sandwiched between the conductors 120a, 120b. A base end portion of the conductor 120a is placed on the bus bar 111b such that the insulator 121 is sandwiched between the bus bar 111b and the base end portion of the conductor 120a. Thus, the conductor 120a and the bus bar 111b are electrically insulated from each other. A base end portion of the conductor 120b is arranged directly on the bus bar 111b. Thus, the conductor 120b and the bus bar 111b are electrically coupled to each other.

[0040] A pair of terminals 114a, 114b of the capacitor C1 are formed as screw terminals and arranged side by side on one side of the capacitor. The terminals 114a, 114b are arranged to extend through the bus bars 111a, 111b and the insulator 112 in a direction in which the bus bars 111a, 111b and the insulator 112 are layered in the order of the bus bar 111a, the insulator 112 and the bus bar 111b. A distal end portion of the terminal 114a extends further through the insulator 121 and the conductor 120a of the connection portion 118 placed on the bus bar 111b. A distal end portion of the terminal 114b extends further through the conductor 120b of the connection portion 118 superimposed on the bus bar 111b. Nuts 115 are screwed onto the distal end portions of the terminals 114a, 114b so that the capacitor C1 is fixed to the bus bars 111a, 111b and the connection portion 118.

[0041] The terminal 114a and the bus bar 111b are electrically insulated from each other by an insulating washer 116. A large-diameter flange portion 117a formed in a base end portion of the terminal 114a makes contact with the bus bar 111a so that the terminal 114a and the bus bar 111a are electrically coupled to each other. In addition, the nut 115 screwed to the terminal 114a makes contact with the conductor 120a of the connection portion 118 so that the terminal 114a and the conductor 120a can be electrically coupled to each other through the nut 115. Thus, the terminal 114a is connected to the bus bar 111a and the conductor 120a.

[0042] The terminal 114b and a large-diameter flange portion 117b formed in a base end portion of the terminal 114b are electrically insulated from the bus bar 111a by an insulating washer 16. On the other hand, the nut 115 screwed to the terminal 114b makes contact with the conductor 120b of the connection portion 118 so that the terminal 114b can be electrically coupled to the conductor 120b and the bus bar 111b through the nut 115. Thus, the terminal 114b is connected to the bus bar 111b and the

conductor 120b.

- [0043] A distal end portion of the conductor 120a of the connection portion 118 is connected to a positive electrode Pin of an input terminal of the first bridge B1. A distal end portion of the conductor 120b of the connection portion 118 is connected to a negative electrode Nin of an input terminal of the first bridge B1. DC power is supplied from the capacitor C1 to the first bridge B1.
- [0044] A pair of terminals 114a, 114b of the capacitor C2 are fixed to the bus bars 111a, 111b and the connection portion 119, similarly to the terminals 114a, 114b of the capacitor C1. The terminal 114a is connected to the bus bar 111a and the conductor 120a. The terminal 114b is connected to the bus bar 111b and the conductor 120b.
- [0045] A distal end portion of the conductor 120a of the connection portion 119 is connected to a positive electrode Pin of an input terminal of the second bridge B2. A distal end portion of the conductor 120b of the connection portion 119 is connected to a negative electrode Nin of an input terminal of the second bridge B2. DC power is supplied from the capacitor C2 to the second bridge B2.
- [0046] A plurality of connection portions through which the pair of bus bars 111a, 111b are connected to the inverter 106 are provided respectively for the bridges of the inverter 106. The capacitors are connected to the connection portions 118, 119 respectively. In this manner, both the length of a conductive path between the first bridge B1 and the capacitor C1 which is a voltage source of the first bridge B1, and the length of a conductive path between the second bridge B2 and the capacitor C2 which is a voltage source of the second bridge B2 can be shortened so that a parasitic inductance of each of the two conductive paths can be reduced. Thus, surge voltage occurring between opposite terminals of the power semiconductor devices Q1, Q2, Q3, Q4 due to the parasitic inductance can be suppressed so that protection of the inverter 106 can be enhanced.
- [0047] Further, by arranging the pair of conductors 120a, 120b of each of the connection portions 118, 119 in a layered manner such that the plate faces of the conductors 120a, 120b are opposed to each other and such that the insulator sheet 121 is sandwiched between conductors 120a, 120b, an inductance of each of the connection portions 118, 119 can be reduced, like the pair of bus bars 111a, 111b. Thus, surge voltage occurring at the opposite terminals of the power semiconductor devices Q1, Q2, Q3, Q4 due to the parasitic inductance is further suppressed to improve the protection of the inverter 106.
- [0048] Although one capacitor is connected to each of the connection portions 118, 119 in the example described above, a plurality of capacitors may be connected to each of the connection portions 118, 119 in parallel.
- [0049] In an example shown in Fig. 11, each arm including the power semiconductor

devices Q1, Q2 and each arm including the power semiconductor devices Q3, Q4 are each configured as a module. The first modules M1 each including the power semiconductor devices Q1, Q2 and belonging to a first bridge B1 and a second bridge B2 respectively are connected to a pair of bus bars 111a-1, 111b-1. The second modules M2 each including the power semiconductor devices Q3, Q4 and belonging to the first bridge B1 and the second bridge B2 respectively are connected to a pair of bus bars 111a-2, 111b-2. In this case, the pair of bus bars 111a-1, 111b-1 and the pair of bus bars 111a-2, 111b-2 may be provided in the smoothing section 105, and each of the pair of bus bars 111a-1, 111b-1 and the pair of bus bars 111a-2, 111b-2 may be configured such that, like the pair of bus bars 111a, 111b described above, the pair of bus bars are arranged in a layered manner with an insulator being sandwiched between plate faces of the pair of bus bars. Connection portions to the first modules M1 may be provided in the pair of bus bars 111a-1, 111b-1 on an individual module basis, and connection portions to the second modules M2 may be provided in the pair of bus bars 111a-2, 111b-2 on an individual module basis. At least one capacitor C is connected to each of the connection portions 118-1, 119-1 in the pair of bus bars 111a-1, 111b-1. At least one capacitor is connected to each of the connection portions 118-2 and 119-2 in the pair of bus bars 111a-2, 111b-2.

[0050] In the above description, the pair of bus bars 111a, 111b, the pair of bus bars 111a, 111b and the conductors 120a, 120b are all flat plates, i.e. have a rectangular cross section taken along a plane perpendicular to the current flow direction. However, those bus bars may not be flat plates. For example, they may have a semi-circular cross section in a plane perpendicular to the current flow direction. In this case, the external surface of each of bus bars extending in the current flow direction has a flat face forming the diameter portion of the semi-circular cross section and a semi-cylindrical face forming an arc portion of the semi-circular cross section, and the bus bars are arranged in a layered manner such that the flat faces of the bus bars are opposed to each other with an insulator being sandwiched between the flat faces of the bus bars.

[0051] This application is based on Japanese Patent Application No. 2015-177757 filed on September 9, 2015, the entire content of which is incorporated herein by reference.

Claims

[Claim 1] An induction heating power supply apparatus comprising:
a smoothing section configured to smooth pulsating current of DC power output from a DC power supply section; and
an inverter configured to convert the DC power smoothed by the smoothing section to AC power,
wherein the smoothing section comprises a pair of bus bars connected to the inverter and at least one capacitor connected to the pair of bus bars,
wherein each of the bus bars comprises an external surface extending in a current flow direction, the external surface including at least one flat face having a larger surface dimension than another face of the external surface in a direction perpendicular to the current flow direction, and
wherein the pair of bus bars are arranged in a layered manner such that the flat faces of the pair of bus bars are opposed to each other and such that an insulator is sandwiched between the flat faces the pair of bus bars.

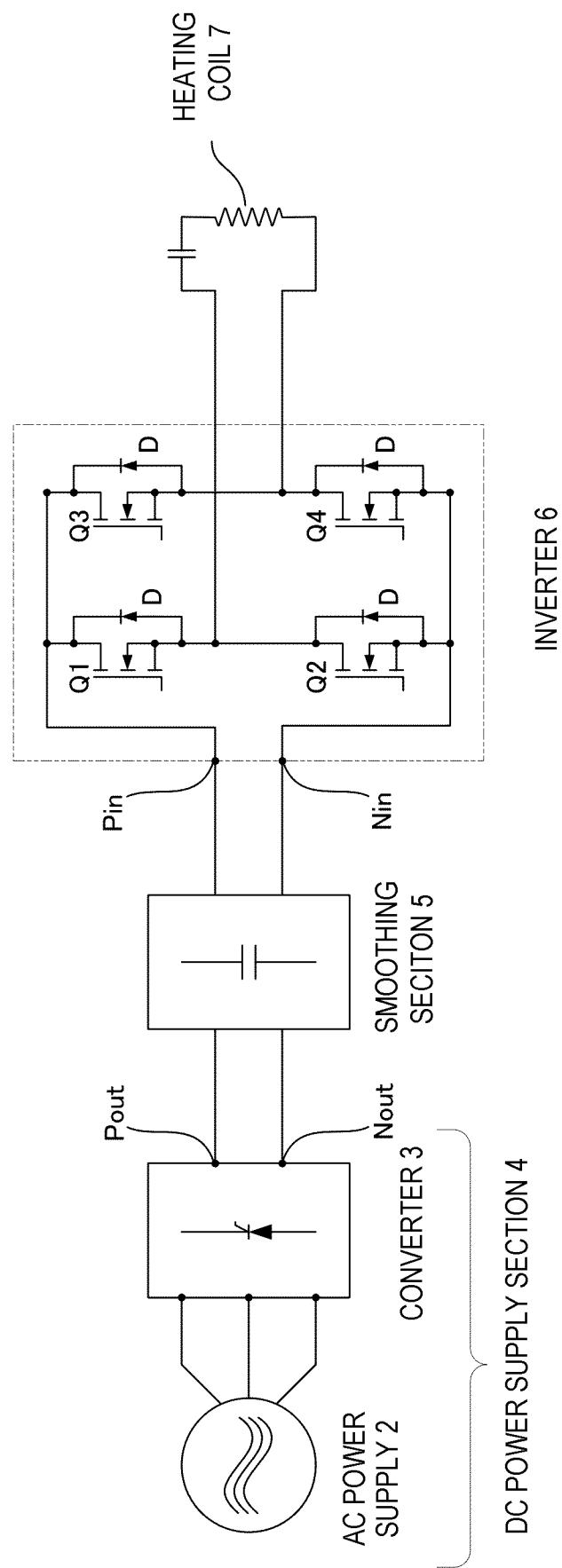
[Claim 2] The induction heating power supply apparatus according to claim 1, wherein the capacitor comprises a pair of terminals arranged side by side on one side of the capacitor, and
wherein the pair of terminals are connected to the pair of bus bars such that the pair of terminals extends through the pair of bus bars and the insulator in a direction in which the bus bars and the insulator are layered.

[Claim 3] The induction heating power supply apparatus according to claim 2, further comprising a plurality of connection portions, each of the connection portions connecting the pair of bus bars to the inverter, wherein the at least one capacitor is provided for each of the connection portions and is connected to the connection portions.

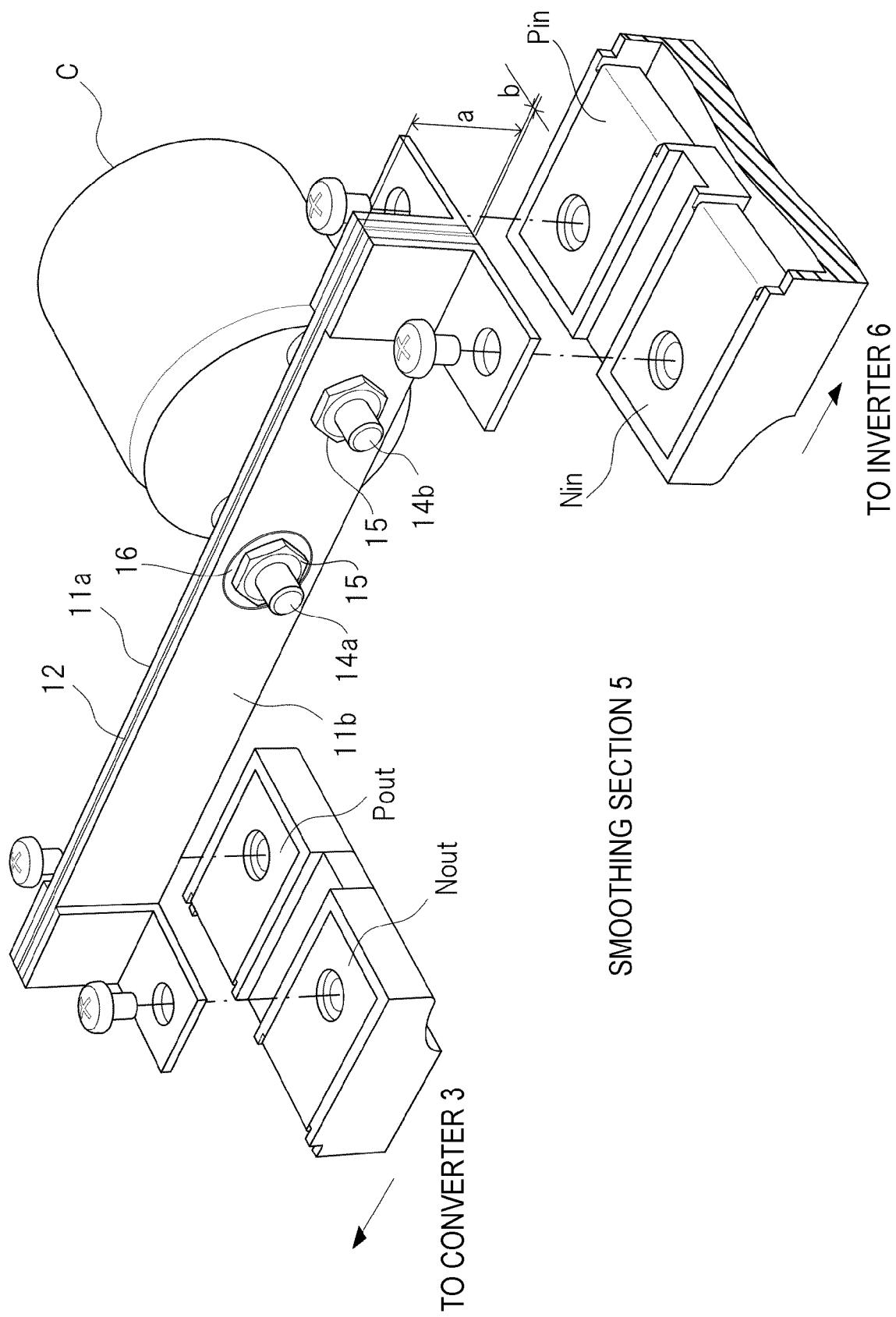
[Claim 4] The induction heating power supply apparatus according to claim 3, wherein each of the connection portions comprises a pair of conductors and an insulator;
wherein each of the conductors comprises an external surface extending in a current flow direction of each of the conductors, the external surface including at least one flat face having a larger surface dimension than another face of the external surface in a direction perpendicular to the current flow direction of each of the conductors, and

wherein the pair of conductors are arranged in a layered manner such that the flat faces of the pair of conductors are opposed to each other and such that the insulator is sandwiched between the flat faces of the pair of conductors.

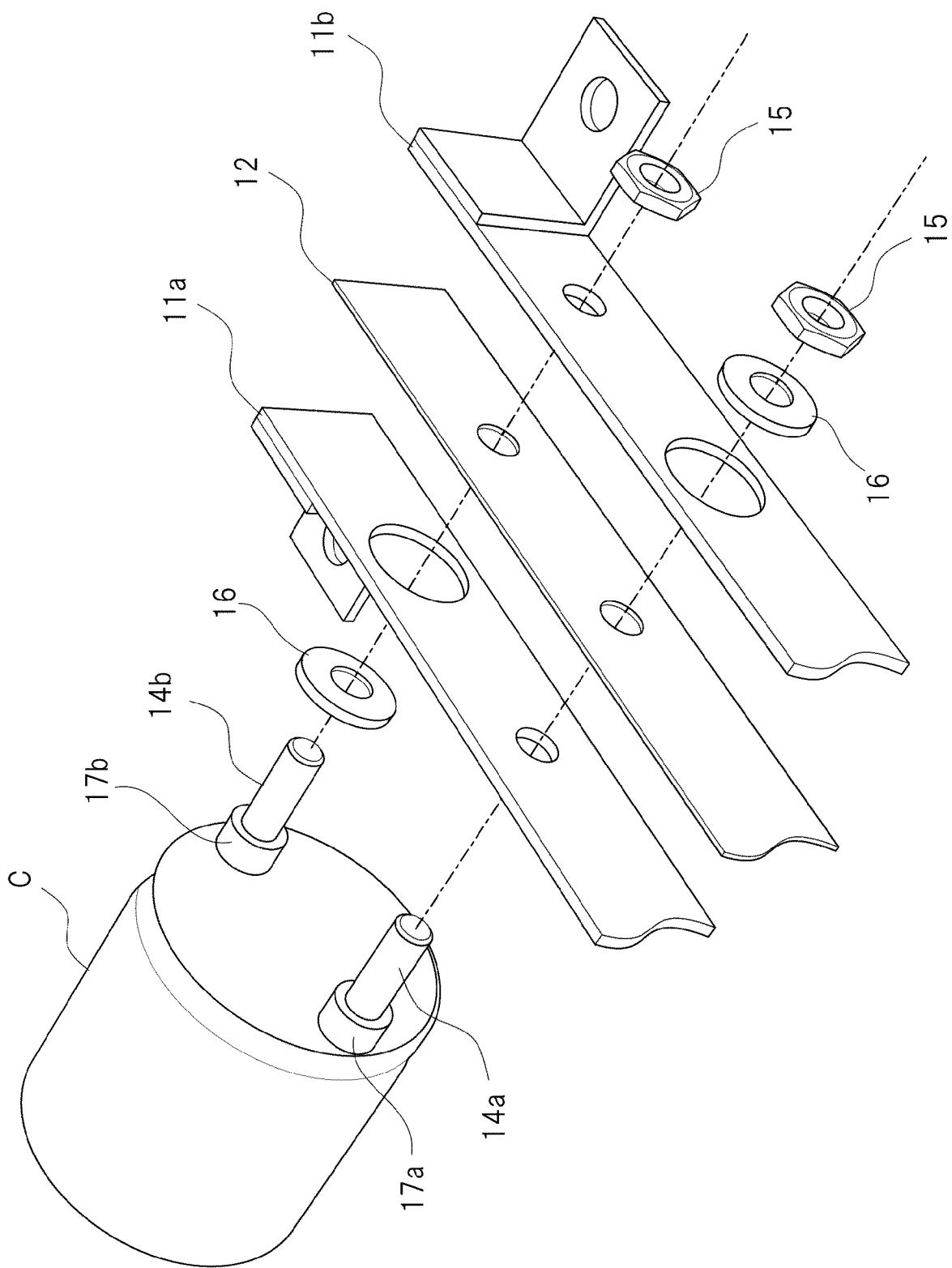
[Fig. 1]



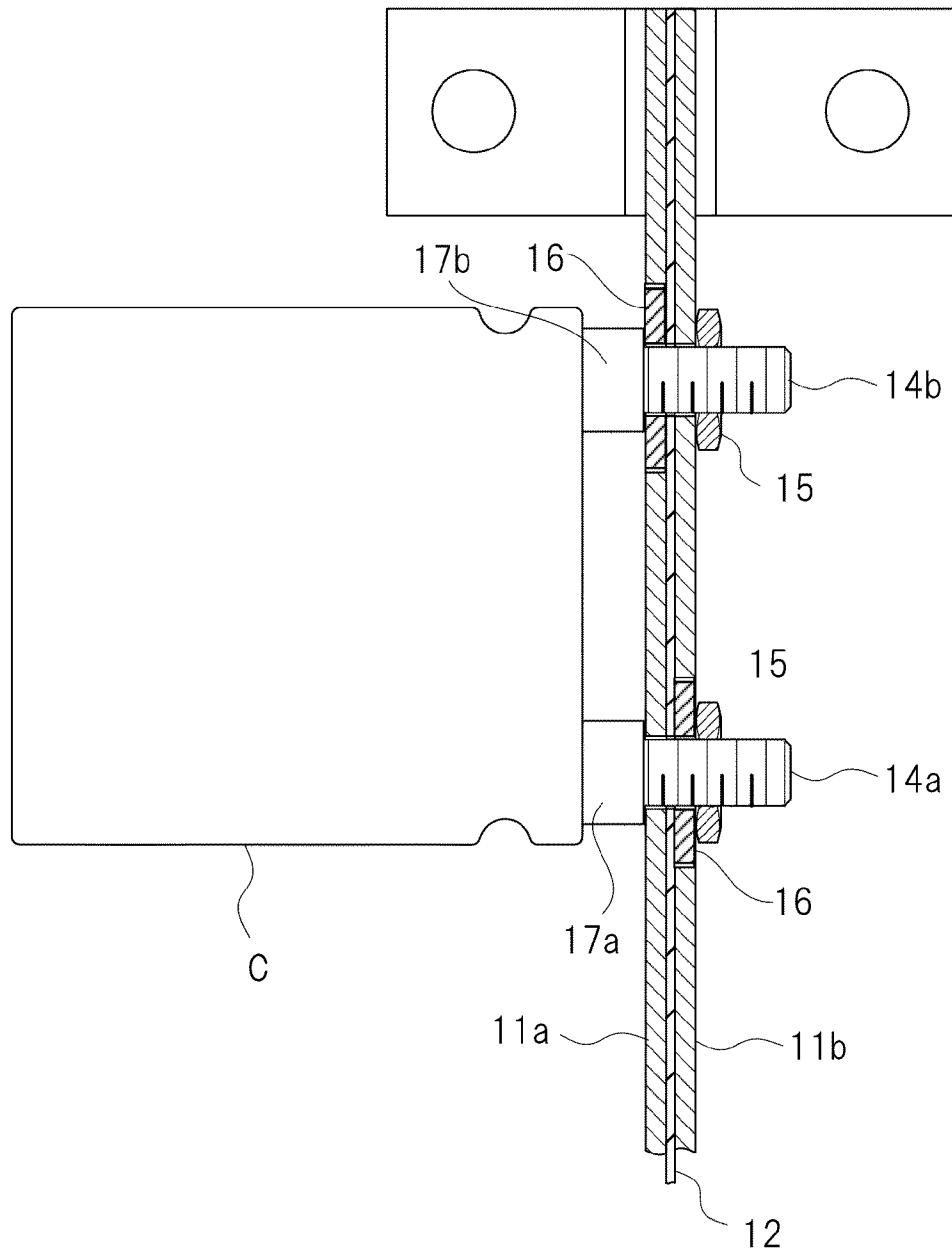
[Fig. 2]



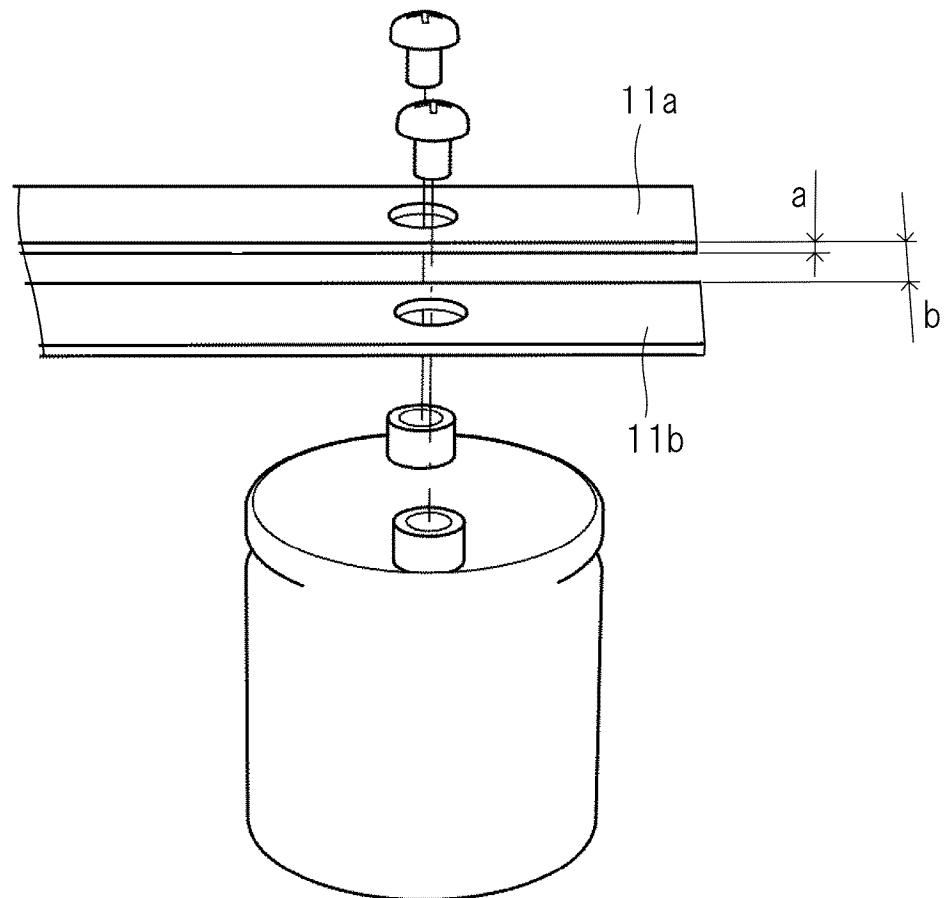
[Fig. 3]



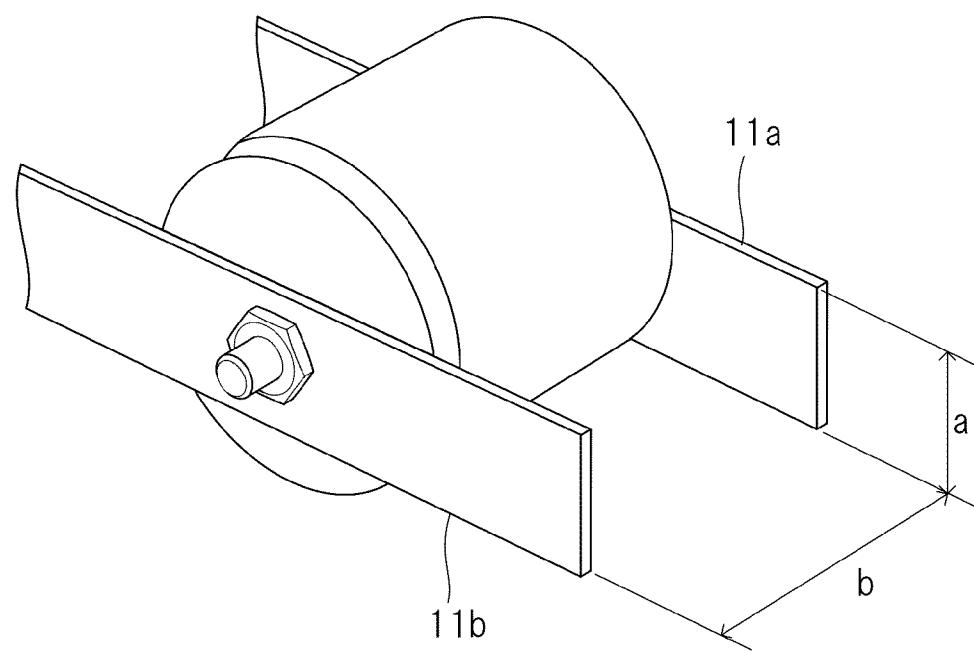
[Fig. 4]



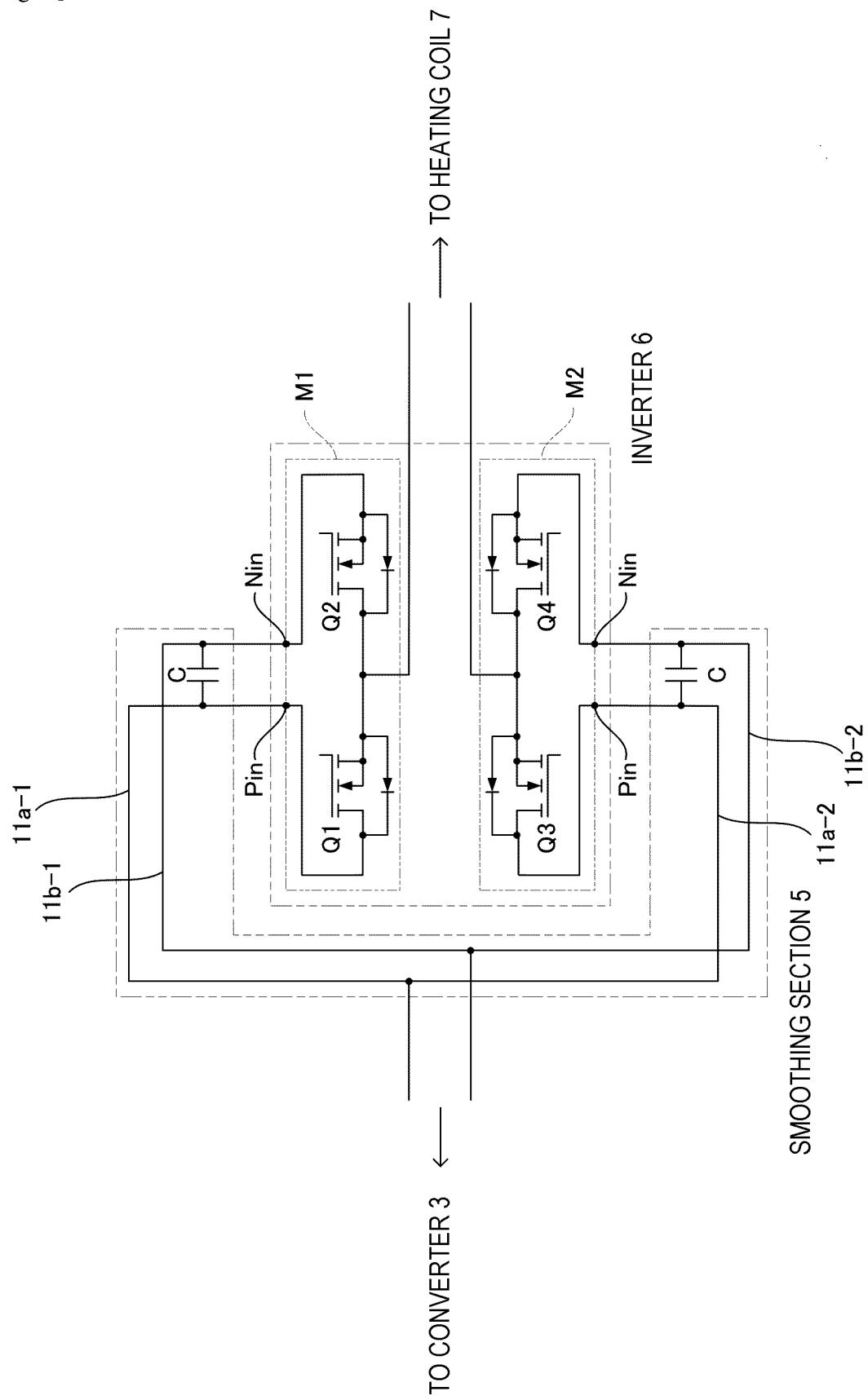
[Fig. 5]



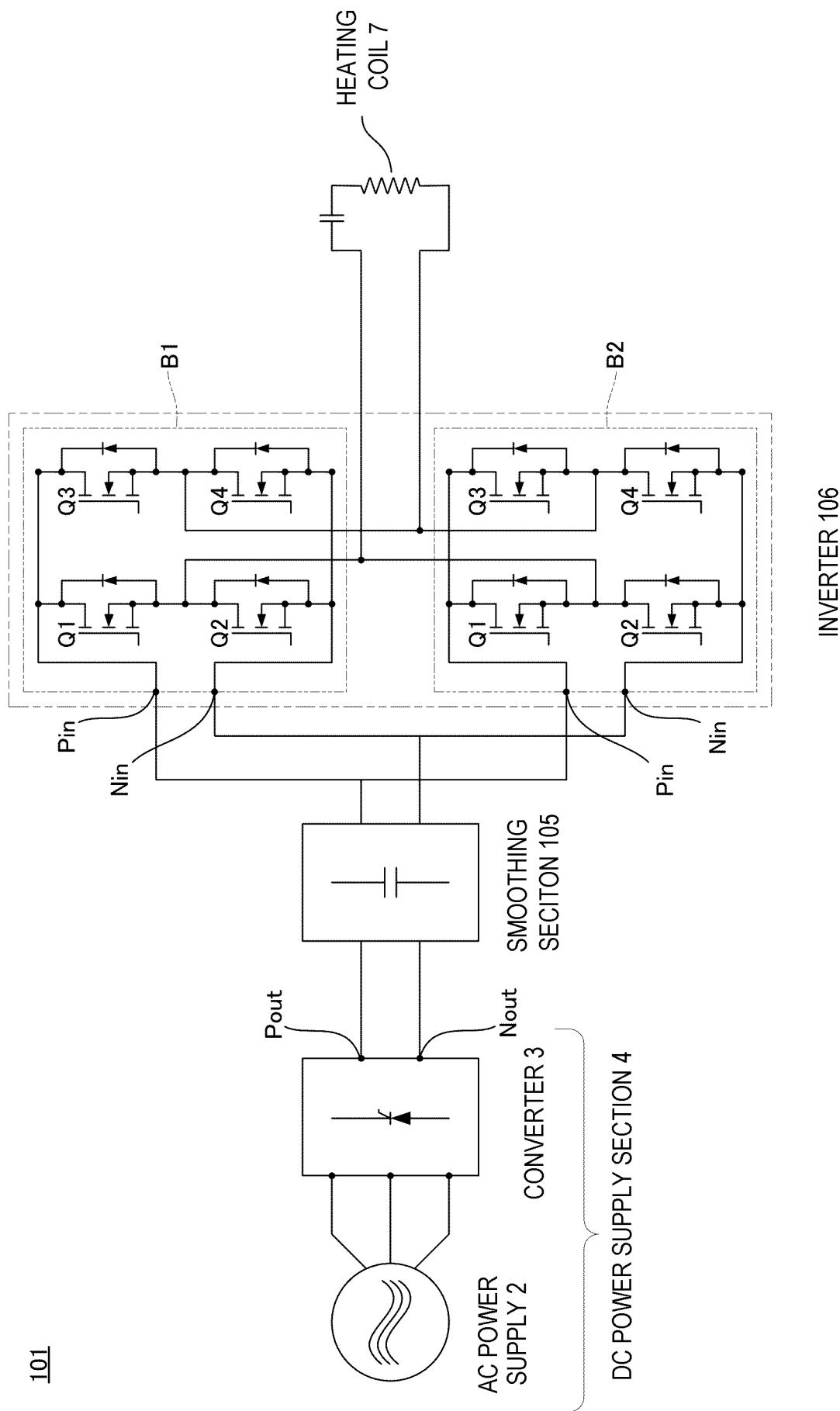
[Fig. 6]



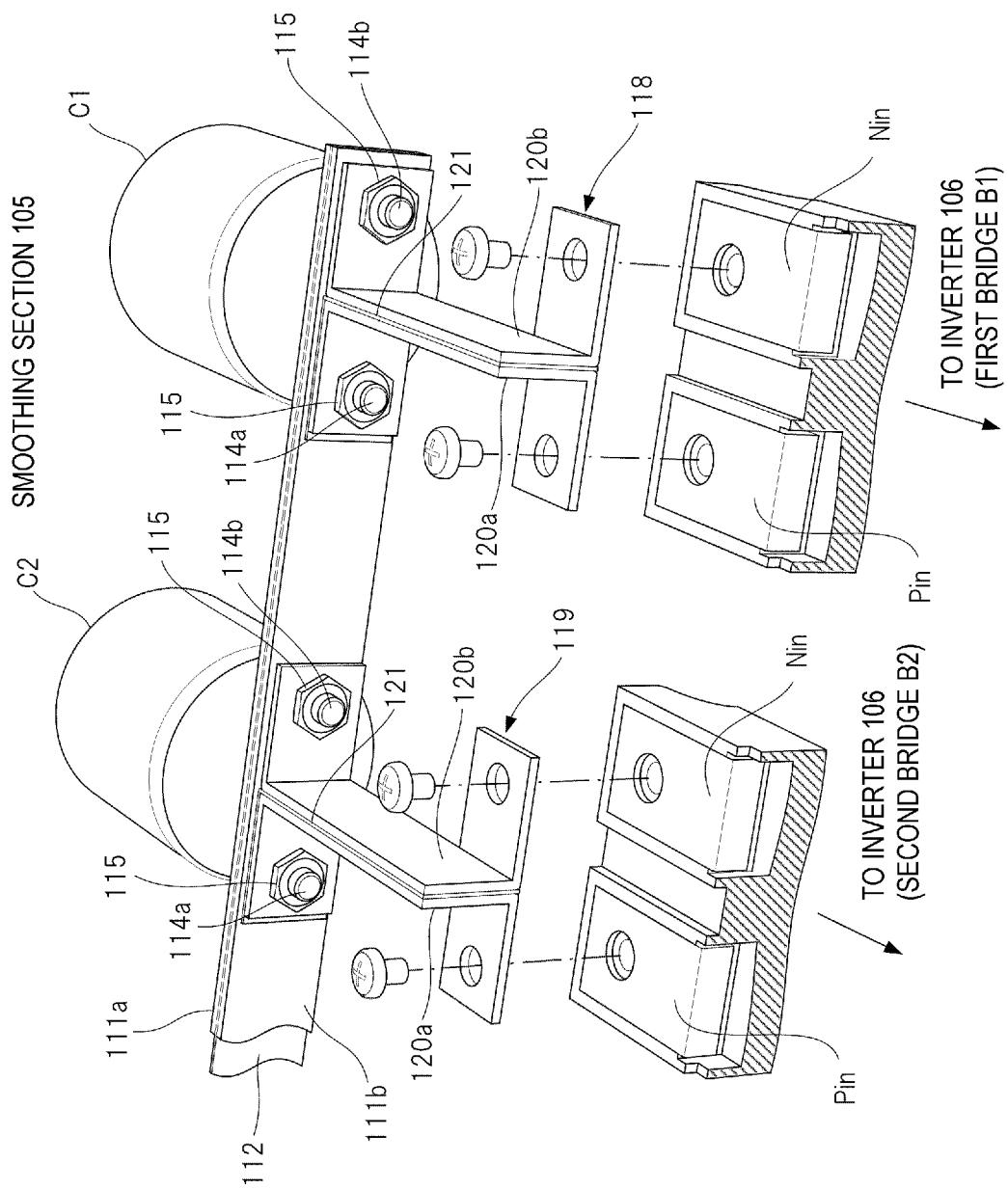
[Fig. 7]



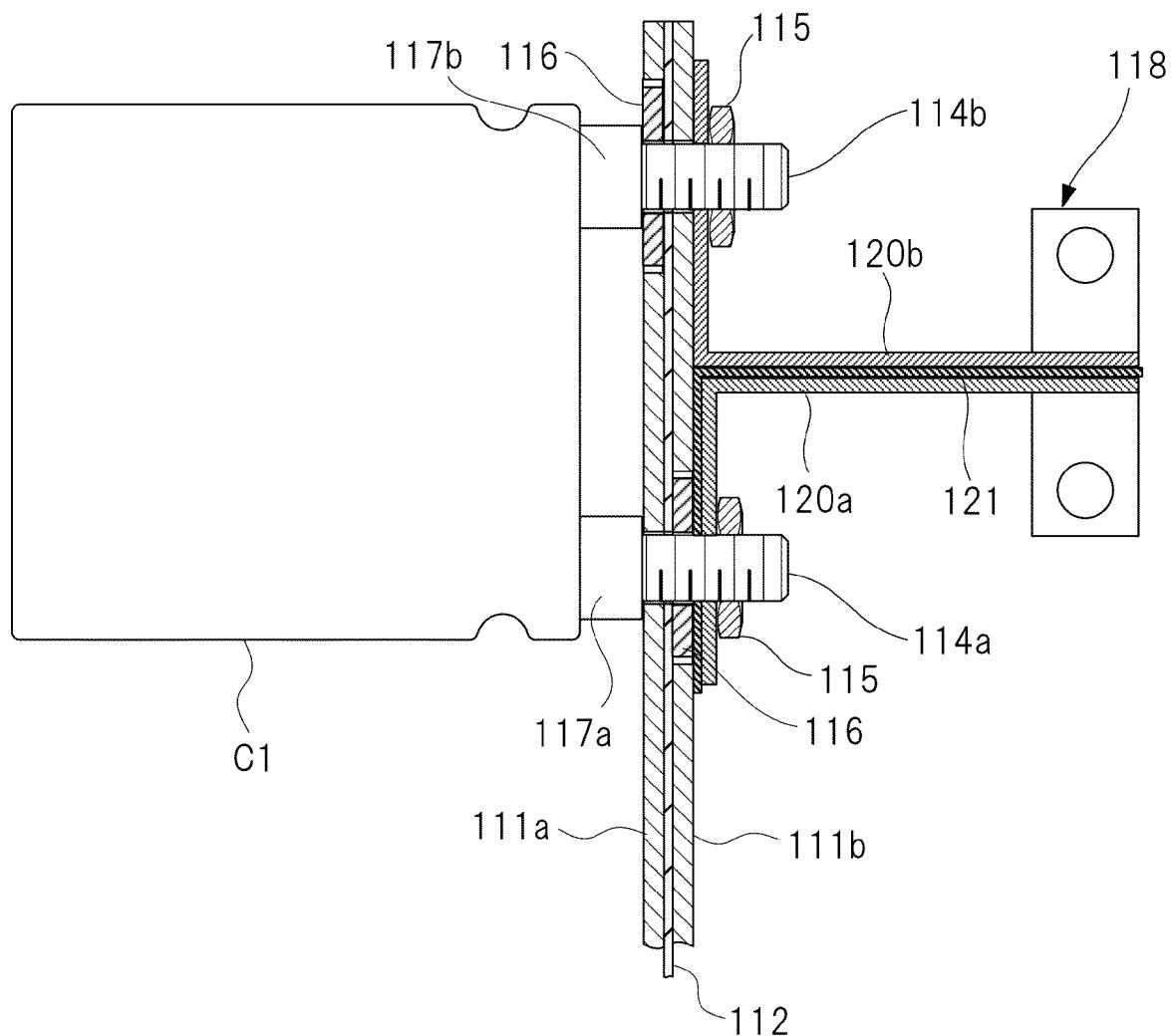
[Fig. 8]



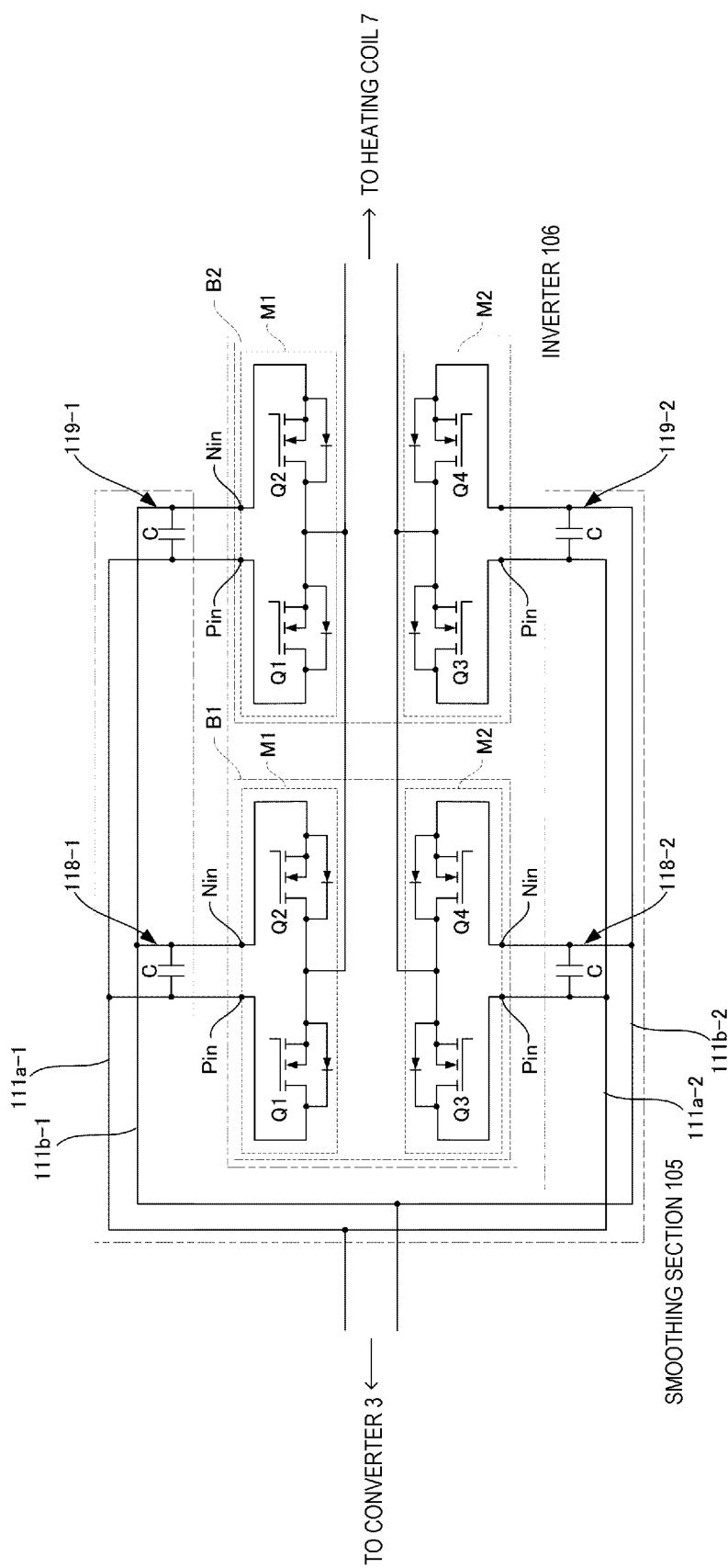
[Fig. 9]



[Fig. 10]



[Fig. 11]



INTERNATIONAL SEARCH REPORT

International application No
PCT/JP2016/004105

A. CLASSIFICATION OF SUBJECT MATTER INV. H05B6/04 H02M7/42 ADD.		
According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED Minimum documentation searched (classification system followed by classification symbols) H02M H05B		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched		
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used) EPO-Internal, WPI Data		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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Y	JP 2003 319665 A (TOYOTA MOTOR CORP) 7 November 2003 (2003-11-07) abstract; figures 4,6 -----	2,3
X	JP 2002 016202 A (DENSO CORP) 18 January 2002 (2002-01-18) abstract; figures 1,4 -----	1
X	JP 2000 152662 A (DENSO CORP) 30 May 2000 (2000-05-30) abstract; figures 1,2 ----- -/-	1
<input checked="" type="checkbox"/> Further documents are listed in the continuation of Box C.		<input checked="" type="checkbox"/> See patent family annex.
<p>* Special categories of cited documents :</p> <p>"A" document defining the general state of the art which is not considered to be of particular relevance</p> <p>"E" earlier application or patent but published on or after the international filing date</p> <p>"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)</p> <p>"O" document referring to an oral disclosure, use, exhibition or other means</p> <p>"P" document published prior to the international filing date but later than the priority date claimed</p> <p>"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention</p> <p>"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone</p> <p>"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art</p> <p>"&" document member of the same patent family</p>		
Date of the actual completion of the international search	Date of mailing of the international search report	
16 November 2016	25/11/2016	
Name and mailing address of the ISA/ European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Authorized officer Gea Haupt, Martin	

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