(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
30 December 2015 (30.12.2015)

WIPO | PCT

(10) International Publication Number
WO 2015/200454 A1

(51) International Patent Classification:
H05B 33/08 (2006.01)

(21) International Application Number:
PCT/US2015/037372

(22) International Filing Date:
24 June 2015 (24.06.2015)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
62/018,531 27 June 2014 (27.06.2014) US
14/748,175 23 June 2015 (23.06.2015) US

(71) Applicant: **MICROCHIP TECHNOLOGY INC.** [US/US]; 2355 West Chandler Blvd., Chandler, AZ 85224 (US).

(72) Inventor: **LYNCH, Scott**; 2098 Touraine Lane, Half Moon Bay, CA 94019 (US).

(74) Agent: **YAMASHITA, Brent**; Dla Piper LLP US, 2000 University Avenue, East Palo Alto, CA 94303 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

(54) Title: SEQUENTIAL LINEAR LED SYSTEM WITH LOW OUTPUT RIPPLE

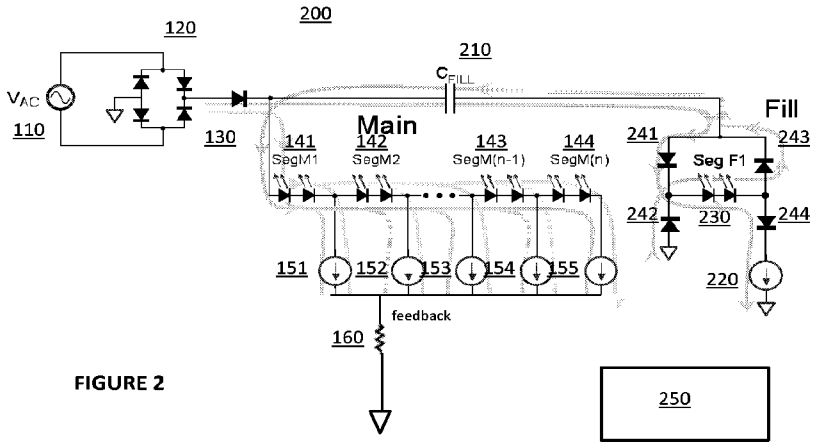


FIGURE 2

(57) Abstract: A sequential linear light emitting diode (LED) system with a low output ripple is disclosed. In one embodiment, the a sequential linear LED system comprises a bridge rectifier for generating a DC voltage, a diode for receiving the DC voltage, a capacitor coupled to the diode, a current regulator coupled to the capacitor for controlling the charging of the capacitor, and a plurality of segments coupled to the diode, each segment comprising an LED string and current regulator.

WO 2015/200454 A1

SEQUENTIAL LINEAR LED SYSTEM WITH LOW OUTPUT RIPPLE

CROSS REFERENCE TO RELATED APPLICATION

[0001] This patent application claims priority to U.S. Provisional Application No. 62/018,531, filed on June 27, 2014, and titled "Sequential Linear LED System with Low Output Ripple," which is incorporated herein by reference in its entirety.

TECHNICAL FIELD

[0002] A sequential linear light emitting diode (LED) driver with a low output ripple is disclosed.

BACKGROUND OF THE INVENTION

[0003] With reference to Figure 1, prior art LED system 100 is depicted. Prior art LED system 100 comprises AC voltage source 110, bridge rectifier 120, and diode 130. Prior art LED system 100 further comprises a plurality of LED strings, here shown as LED string 141, LED string 142, LED string 143, and LED string 144. A current regulator is attached after each LED string, here shown as current regulator 151, current regulator 152, current regulator 153, current regulator 154, and current regulator 155. It is to be understood that prior art LED system 100 can comprise a greater or fewer number of LED strings and current regulators than what is shown.

[0004] As the voltage output of bridge rectifier 120 increases from 0V, LED string 141 is forward biased such that the LEDs in LED string 141 emit light and current is controlled by current regulator 151. When the voltage becomes sufficiently high, LED string 142 also will become forward biased such that the LEDs in both LED string 141 and LED string 142 emit light. At that point, current regulator 152 will cause current regulator 151 to shut down. As the voltage increases

further, the same happens for the remaining LED strings and current regulators, until LED strings 141, 142, 143, and 144 are emitting light, current is drawn by current regulator 155, and current regulators 151, 152, 153, and 154 are turned off.

[0005] One drawback of prior art LED system 100 is that when the voltage provided by AC voltage source 110 approaches 0V, the total light output from all LED strings will be zero. That is, LED system 100 will stop emitting light, which results in a "strobing" or "ripple" effect. This is extremely undesirable from a user's point of view.

[0006] What is needed is an improved LED system with a decreased strobing or ripple effect.

SUMMARY OF THE INVENTION

[0007] The present invention reduces or eliminates the strobing or ripple effect through the use of a fill capacitor that is charged by a current regulator.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] Figure 1 depicts a prior art LED system.

[0009] Figure 2 depicts an embodiment of an LED system comprising a fill capacitor charged by a current regulator.

[0010] Figure 3 depicts another embodiment of an LED system comprising a fill capacitor charged by a current regulator.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[0011] With reference to Figure 2, LED system 200 is depicted. LED system 200 comprises many of the same components in prior art LED system 100 shown in Figure 1. LED system 200 further

comprises fill capacitor 210, current regulator 220, LED string 230, and diodes 241, 242, 243, and 244. LED string 230 is optional and does not need to be used. If used, LED string 230 could comprise one LED or multiple LEDs. Moreover, one or more additional LED strings could be added to LED string 230. Current regulators 151, 152, 153, 154, and 155 are coupled to resistor 160, which in turn is coupled to ground. Thus, current regulators 151, 152, 153, 154, and 155 share a common path to ground.

[0012] During operation, as the voltage from bridge rectifier 120 increases from 0V, current will flow into fill capacitor 210 and through diode 241, through LED string 230, through diode 244, and through current regulator 220. Current also will flow into the lower circuit, starting with LED string 141 and current regulator 151. By controlling current regulator 220 and current regulators 151, 152, 153, 154, and 155 using control circuit 250, the system can allocate current between charging fill capacitor 210 and providing power to LED strings 141, 142, 143, and 144 and can maximize the power factor of LED system 200 (such that voltage and current usage are in phase with one another). Thus, current regulator 220 can be used to control the charging of fill capacitor to maintain a high input power factor.

[0013] When the voltage output by bridge rectifier 120 approaches the zero crossings (the situation in which prior art LED system 100 would emit no light), the charge stored in fill capacitor can be used to power LED strings 141, 142, 143, and 144. Current will flow from ground through diode 242, LED string 230, diode 243, through fill capacitor 210 and into LED strings 141, 142, 143, and 144. The voltage provided by fill capacitor 210 will be at the peak voltage of fill capacitor 210. Thus, unlike in the prior art, LED strings 141, 142, 143, and 144 can continue to emit light even in periods when AC voltage source 110 is producing a voltage near 0 V.

[0014] As fill capacitor 210 is discharged, its voltage will decrease. As the voltage of fill capacitor 210 decreases, LED strings 141, 142, 143, and 144 will stop conducting one-by-one, in reverse order starting with LED string 144. Thus, LED string 144 will stop emitting light when the voltage of fill capacitor 210 drops below a certain level. At that point, current regulator 155 will stop drawing current and will activate current regulator 154. Current regulator 154 will then draw current until LED string 143 stops emitting light, at which point current regulator 154 will stop drawing current and will activate current regulator 153. This process continues until only LED string 141 and current regulator 151 are active, although at some point the voltage from bridge rectifier 120 will exceed the voltage being provided by fill capacitor 210.

[0015] With reference to Figure 3, another embodiment is depicted. LED system 300 comprises many of the same components as LED system 200. LED system 300 also comprises LED string 310, diode 130, current regulator 320, and control circuit 350. Control circuit 350 controls current regulators 151, 152, 153, 154, 155, 220, and 320. The purpose of LED string 210 and current regulator 320 is to reduce the total harmonic distortion (THD) of the system and to maintain total light output over time.

[0016] LED system 200 and LED system 300 minimize or eliminate the output ripple and "strobe effect" of prior art LED system 100. In addition, a greater power factor is achieved. LED system 300 further reduces the THD of the system.

What Is Claimed Is:

1. A light emitting diode (LED) system comprising:

an alternating current voltage source;

a bridge rectifier coupled to the alternating current voltage source;

a plurality of LED strings coupled to an output of the bridge rectifier, each of the plurality of LED strings comprising one or more LEDs;

a plurality of current regulators, each of the plurality of current regulators coupled to one of the plurality of LED strings to control current through that LED string;

a capacitor coupled to the output of the bridge rectifier and to an ancillary current regulator;

wherein when the output of the bridge rectifier is reverse-biased, the capacitor provides a positive voltage to the plurality of LED strings to initially cause one or more the plurality of LED strings to emit light after the output of the bridge rectifier becomes reverse-biased.

2. The system of claim 2, further comprising a control circuit for controlling the plurality of current regulators and the ancillary current regulator coupled to the capacitor to allocate current between charging the capacitor and providing power to the plurality of LED strings.

3. The system of claim 2, wherein the control circuit allocates current between charging the capacitor and providing power to the plurality of LED strings to maintain a high input power factor.

4. The system of claim 1, further comprising a resistor coupled to each of the plurality of current regulators to provide a common path to ground.

5. The system of claim 1, further comprising an ancillary LED string comprising one or more LEDs coupled between the capacitor and the ancillary current regulator.

6. The system of claim 5, further comprising a diode coupled between the capacitor and the ancillary LED string and a diode between the ancillary LED string and the ancillary current regulator.

7. The system of claim 6, further comprising a diode coupled between ground and the ancillary LED string and another diode coupled between the capacitor and ancillary LED string.

8. The system of claim 7, wherein when the main diode is reverse-biased, current initially flows from ground through a diode, the ancillary LED string, a diode, the capacitor, and one or more of the plurality of LED strings.

9. The system of claim 1, further comprising a second ancillary LED string coupled between the bridge rectifier and main diode.

10. The system of claim 9, further comprising a current regulator coupled to the second ancillary LED string and to the control circuit.

11. A method of operating a light emitting diode (LED) system comprising:

concurrently provide current to a capacitor and a first LED string, the first LED string comprising one or more LEDs;

while an output of a bridge rectifier is still forward biased, providing current to a first LED string and one or more additional LED strings, each of the one or more additional LED strings comprising one or more LEDs;

reverse biasing the output of the bridge rectifier and providing current from the capacitor to the first LED string and the one or more additional LED strings;

when the output of the bridge rectifier is still reverse biased, providing current from the capacitor only to the first LED string

12. The method of claim 11, further comprising:

allocating, by a control circuit, current between charging the capacitor and providing power to the first LED string and the one or more additional LED strings.

13. The method of claim 12, wherein the allocating step maintains a high input power factor.

14. The method of claim 11, wherein a resistor coupled to the first LED string and the one or more additional LED strings provides a common path to ground.

15. The method of claim 11, further comprising:

when the output of the bridge rectifier is forward biased, providing current to an ancillary LED string comprising one or more LEDs coupled to the capacitor.

16. The method of claim 15, wherein a diode is coupled between the capacitor and the ancillary LED string.

17. The method of claim 16, wherein a diode is coupled between ground and the ancillary LED string and a diode is coupled between the capacitor and the ancillary LED string.

18. The method of claim 17, further comprising:

when the output of the bridge rectifier is reverse-biased, providing current from ground through a diode, the ancillary LED string, a diode, the capacitor, and at least the first LED string.

19. The method of claim 11, further comprising:

providing current to a second ancillary LED string coupled between the bridge rectifier and main diode.

20. The method of claim 19, further comprising:

allocating, by a control circuit, current between charging the capacitor and providing power to the first LED string, the one or more additional LED strings, and the second ancillary LED string.

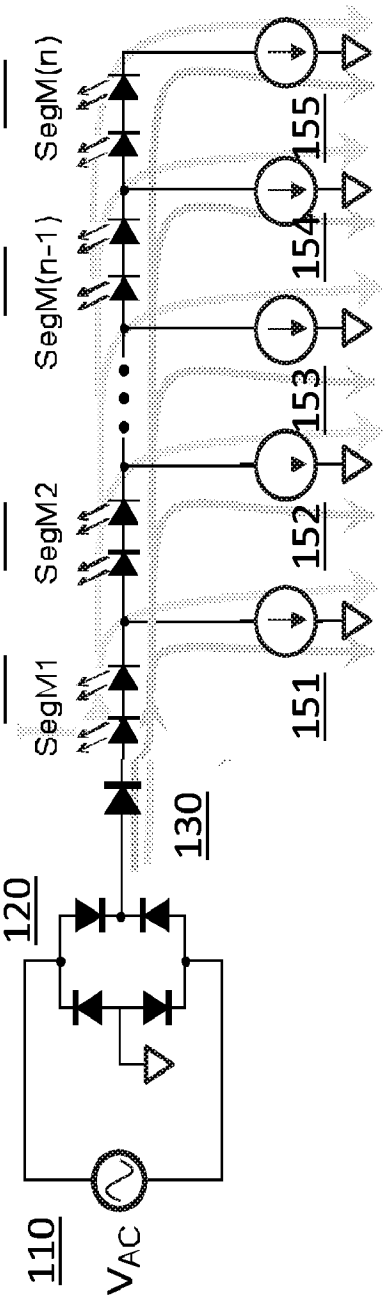


FIGURE 1 (PRIOR ART)

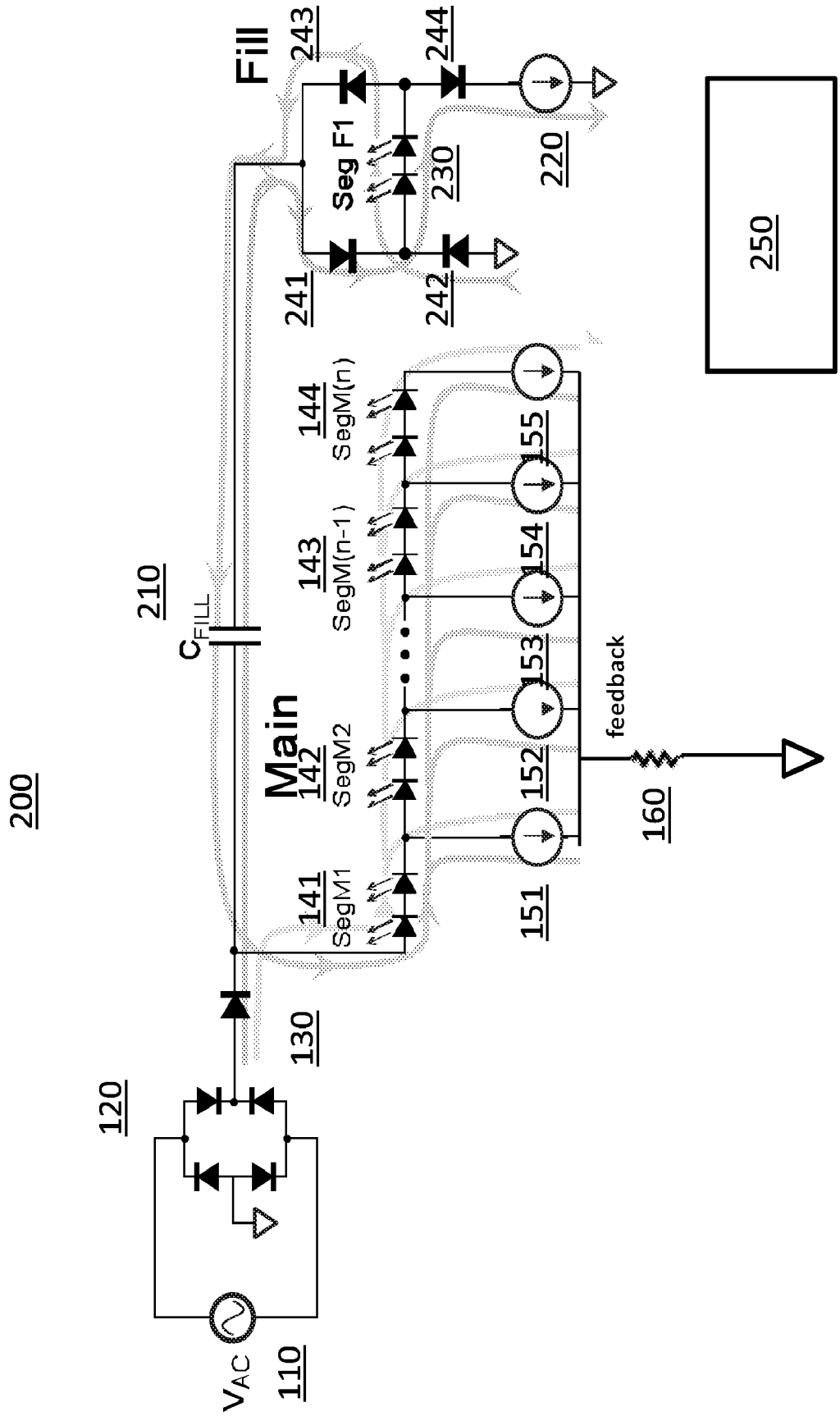

200
Fill
243
244
Seg F1
230
220
241
242
250
210
C_{FILL}
144
SegM(n)
143
SegM(n-1)
Main
142
SegM2
141
SegM1
155
154
153
152
151
feedback
160
130
120
V_{AC}
110

FIGURE 2

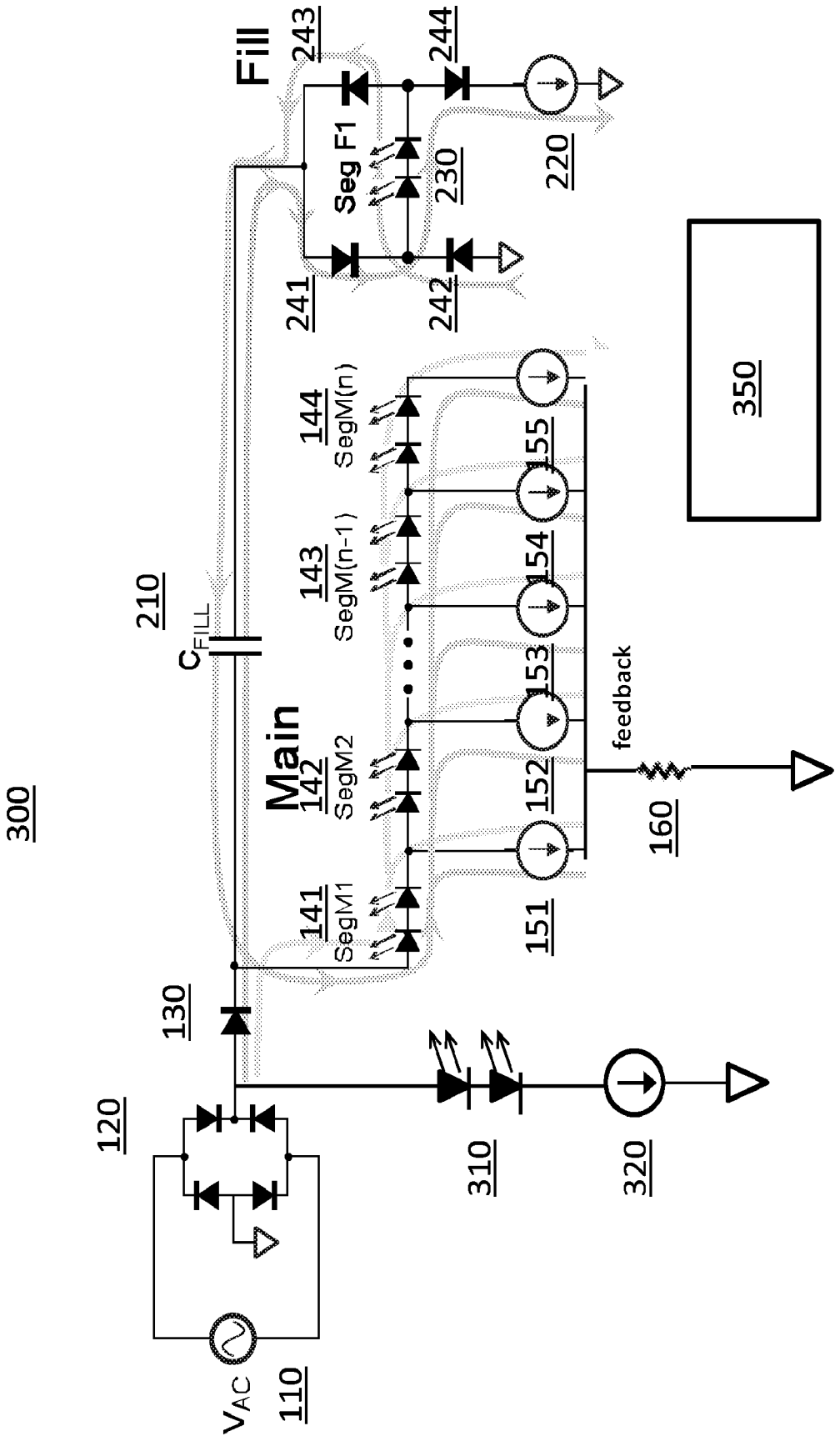

300
Fill
243
244
Seg F1
230
220
241
242
350
144
SegM(n)
155
143
SegM(n-1)
154
210
C_{FILL}
Main
142
SegM2
153
feedback
152
160
141
SegM1
151
130
120
310
320
V_{AC}
110

FIGURE 3

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2015/037372

A. CLASSIFICATION OF SUBJECT MATTER
INV. H05B33/08
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H05B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X A	US 2013/200802 A1 (SAKURAGI HARUMI [JP] ET AL) 8 August 2013 (2013-08-08) paragraphs [0057] - [0124]; figures 1-7	1-6, 11-16 7-10, 17-20

X	US 2013/313984 A1 (MAIWALD HUBERT [DE]) 28 November 2013 (2013-11-28)	1-3,5-7, 9-13, 15-17, 19,20
A	paragraphs [0059] - [0112]; figures 2,3	4,8,14, 18

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
31 August 2015	04/09/2015

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Waters, Duncan

1

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2015/037372

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2013200802 A1	08-08-2013	CN 103249217 A	14-08-2013
		JP 2013179288 A	09-09-2013
		TW 201352065 A	16-12-2013
		US 2013200802 A1	08-08-2013
US 2013313984 A1	28-11-2013	CN 103348767 A	09-10-2013
		DE 102011003931 A1	16-08-2012
		EP 2668822 A2	04-12-2013
		US 2013313984 A1	28-11-2013
		WO 2012107293 A2	16-08-2012