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(71) Applicant: **INTERNATIONAL BUSINESS MACHINES CORPORATION** [US/US]; New Orchard Road, Armonk, New York 10504 (US).

(71) Applicant (for MG only): **IBM DEUTSCHLAND GMBH** [DE/DE]; IBM-Allee 1, 71139 Ehningen (DE).

(72) Inventors: **DIAL, Oliver**; c/o IBM Thomas J Watson Research, 1101 Kitchawan Road, P.O. Box 218, Yorktown Heights, New York 10598 (US). **GAMBETTA, Jay**; c/o IBM Thomas J Watson Research, 1101 Kitchawan Road, P.O. Box 218, Yorktown Heights, New York 10598 (US). **JOHNSON, Blake**; c/o IBM Thomas J Watson Research, 1101 Kitchawan Road, P.O. Box 218, Yorktown Heights, New York 10598 (US). **CHOW, Jerry**; c/o IBM Thomas J Watson Research, 1101 Kitchawan Road, P.O. Box 218, Yorktown Heights, New York 10598 (US). **ORCUTT, Jason**; c/o IBM Thomas J Watson Research, 1101 Kitchawan Road, P.O. Box 218, Yorktown Heights, New York 10598 (US). **ABRAHAM, David**; c/o IBM Thomas J Watson Research, 1101 Kitchawan Road, P.O. Box 218, Yorktown Heights, New York 10598 (US).

(74) Agent: **LAUX, Felix**; c/o IBM Deutschland GmbH, Patentwesen und Urheberrecht, IBM-Allee 1, 71139 Ehningen (DE).

(54) Title: MODULAR QUANTUM SYSTEM WITH DISCRETE LEVELS OF CONNECTIVITY

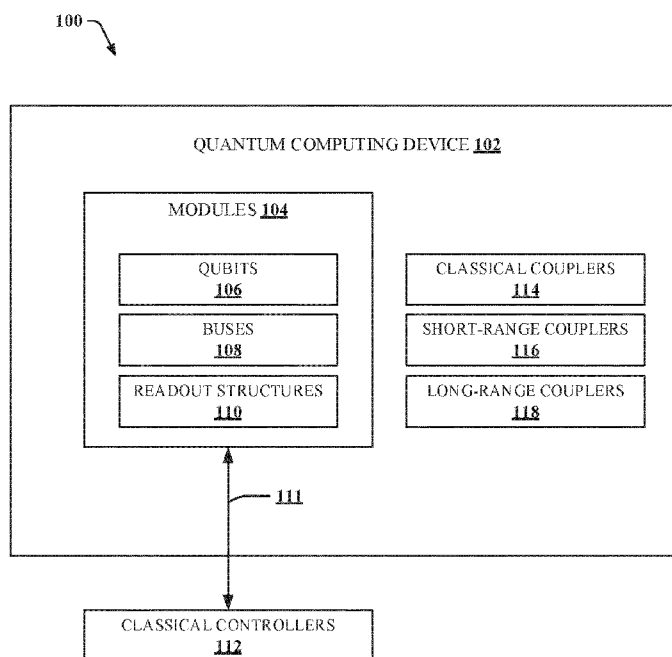


FIG. 1

(57) Abstract: Devices and methods that facilitate modular quantum systems with discrete levels of connectivity are provided. In various embodiments, a quantum computing device can comprise one or more modules comprising at least qubits, buses, and readout structures; a plurality of couplers, wherein the plurality of couplers comprises at least two couplers selected from a group consisting of: classical couplers, short-range couplers, and long-range couplers, that are adapted for coupling a plurality of the at least qubits, buses, and readout structures; and a connection from the one or more modules to one or more classical controllers external to a cryogenic environment comprising the one or more modules.

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MODULAR QUANTUM SYSTEM WITH DISCRETE LEVELS OF CONNECTIVITY

BACKGROUND

[0001] The subject disclosure relates to quantum computing processors, and more specifically to modular quantum systems with discrete levels of connectivity.

[0002] Quantum computing is generally the use of quantum-mechanical phenomena to perform computing and information processing functions. Quantum computing can be viewed in contrast to classical computing, which generally operates on binary values with transistors. That is, while classical computers can operate on bit values that are either 0 or 1, quantum computers operate on quantum bits (qubits) that comprise superpositions of both 0 and 1. Quantum computing has the potential to solve problems that, due to computational complexity, cannot be solved or can only be solved slowly on a classical computer.

[0003] On a large scale, quantum computing cloud service providers can execute millions of quantum jobs for users during a year. Each quantum job can include the execution of one or more quantum programs at a physical logic circuit. Physical, real-world, quantum logic circuits controlled by a quantum system can include a plurality of qubits.

SUMMARY

[0004] The following presents a summary to provide a basic understanding of one or more embodiments of the invention. This summary is not intended to identify key or critical elements, or delineate any scope of the particular embodiments or any scope of the claims. Its sole purpose is to present concepts in a simplified form as a prelude to the more detailed description that is presented later. In one or more embodiments described herein, devices, systems, computer-implemented methods, apparatus and/or computer program products that can facilitate modular quantum systems with discrete levels of connectivity.

[0005] According to an embodiment, a quantum computing device can comprise one or more modules comprising at least qubits, buses, and readout structures; a plurality of couplers, wherein the plurality of couplers comprises at least two couplers selected from a group consisting of: classical couplers, short-range couplers, and long-range couplers, that are adapted for coupling a plurality of the at least qubits, buses, and readout structures; and a

connection from the one or more modules to at least two classical controllers external to a cryogenic environment comprising the one or more modules.

[0006] According to an embodiment, a method can comprise coupling a plurality of at least qubits, buses, and readout structures using a plurality of couplers, wherein the plurality of couplers comprises at least two couplers selected from a group consisting of: classical couplers, short-range couplers, and long-range couplers, and wherein the plurality of at least qubits, buses and readout structures are comprised by one or more modules.

[0007] According to an embodiment, a quantum computing device can comprise one or more modules comprising at least qubits, buses, and readout structures; a plurality of couplers, wherein the plurality of couplers comprises at least two couplers selected from a group consisting of: classical couplers, short-range couplers, and long-range couplers, that are adapted for coupling a plurality of the at least qubits, buses, and readout structures; and a connection from the one or more modules to a classical controller external to a cryogenic environment comprising the one or more modules.

[0008] Approaches described herein can relate to a quantum computing device. The quantum computing device can comprise modules which can contain a number of qubits, buses, and readout elements or structures, a plurality of which can be coupled together using a combination of classical couplers, short-range couplers, and long-range couplers that can be adapted to respectively provide classical, near-range, and medium-range connections. It is to be appreciated that the classical couplers, short-range couplers, and long-range couplers are hereafter referred to as p-type couplers, m-type couplers, and l-type couplers, respectively. Thus, the m-type couplers can be characterized as being of short length (e.g., less than twice the wavelength of the characteristic frequency of the qubits and/or buses (about 1cm or less)) and as having a defined number of channels between at least two connected modules of the one or more modules, while l-type couplers can be characterized as being longer (e.g., from 5 cm to several meters in length). The modules may comprise individual quantum processing units comprising the qubits, busses, and readout structures. The quantum computing device may comprise a connection from one or more of the modules to a classical controller external to a cryogenic environment.

[0009] The p-type couplers can refer to a classical mode of communication which can be connected to the plurality of modules, and which can transmit information from any of the modules, analyze the data received, and transmit instructions to any of the other modules, all within a time window which is of the order of a coherence time (T_1) of qubits

contained in the modules. A quantum computing system comprised of modules with at least two or all three types of connectivity (p-type, m-type and l-type) can offer significant advantages in computational capabilities. For example, by combining different modularities using a combination of classical, short-range and/or long-range couplers, issues with limits in scaling by cooling density, running dynamic circuits across a chip and/or running substantial algorithms (i.e., entanglement distillation) requiring a larger number of qubit chips can be overcome.

[0010] According to one or more embodiments, utilization of all types of connectivity (p-type, m-type and l-type) can permit computations involving very large numbers of qubits.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] FIG. 1 illustrates a schematic view of a system, in accordance with one or more embodiments described herein.

[0012] FIG. 2 illustrates an example, non-limiting schematic of an exemplary qubit lattice with couplers between adjacent qubit chips in accordance with one or more embodiments described herein.

[0013] FIG. 3A illustrates an example, non-limiting arrangement of a qubit lattice that can be extended via l-type couplers and m-type couplers in accordance with one or more embodiments described herein.

[0014] FIG. 3B illustrates an example, non-limiting arrangement of an extended qubit lattice in accordance with one or more embodiments described herein.

[0015] FIG. 4 illustrates a p-level modularity in accordance with one or more embodiments described herein.

[0016] FIG. 5A illustrates a dilution refrigerator in accordance with one or more embodiments described herein.

[0017] FIG. 5B further illustrates a dilution refrigerator in accordance with one or more embodiments described herein.

[0018] FIG. 6A illustrates an exemplary qubit chip in accordance with one or more embodiments described herein.

[0019] FIG. 6B further illustrates an exemplary qubit chip in accordance with one or more embodiments described herein.

[0020] FIG. 6C further illustrates an exemplary qubit chip in accordance with one or more embodiments described herein.

[0021] FIG. 7 illustrates multiple qubit chips (quantum processing chips or QPUs) that can be connected in a p-level modularity in accordance with one or more embodiments discussed herein.

[0022] FIG. 8A illustrates classical parallelization of QPUs in accordance with one or more embodiments described herein.

[0023] FIG. 8B further illustrates classical parallelization of QPUs via p-type couplers in accordance with one or more embodiments described herein.

[0024] FIG. 9 illustrates classical parallelization of QPUs in accordance with one or more embodiments described herein.

[0025] FIG. 10A further illustrates classical parallelization of QPUs in accordance with one or more embodiments described herein.

[0026] FIG. 10B further illustrates classical parallelization of QPUs in accordance with one or more embodiments described herein.

[0027] FIG. 11 illustrates an l-level modularity in accordance with one or more embodiments described herein.

[0028] FIG. 12 illustrates a dilution refrigerator in accordance with one or more embodiments described herein.

[0029] FIG. 13 illustrates multiple qubit chips that can be connected in an l-level modularity via long range cables, in accordance with one or more embodiments described herein.

[0030] FIG. 14A illustrates quantum parallelization of QPUs in accordance with one or more embodiments described herein.

[0031] FIG. 14B further illustrates quantum parallelization of QPUs in accordance with one or more embodiments described herein.

[0032] FIG. 14C further illustrates quantum parallelization of QPUs in accordance with one or more embodiments described herein.

[0033] FIG. 15 further illustrates quantum parallelization of QPUs in accordance with one or more embodiments described herein.

- [0034] FIG. 16 illustrates an m-level modularity in accordance with one or more embodiments described herein.
- [0035] FIG. 17 illustrates coupling of multichip QPUs in an m-level modularity, in accordance with one or more embodiments described herein.
- [0036] FIG. 18A further illustrates coupling of multichip QPUs in an m-level modularity, in accordance with one or more embodiments described herein.
- [0037] FIG. 18B further illustrates coupling of multichip QPUs in an m-level modularity, in accordance with one or more embodiments described herein.
- [0038] FIG. 19 further illustrates coupling of multichip QPUs in an m-level modularity, in accordance with one or more embodiments described herein.
- [0039] FIG. 20A illustrates quantum parallelization of multichip QPUs via an m+l-level modularity in accordance with one or more embodiments described herein.
- [0040] FIG. 20B further illustrates quantum parallelization of multichip QPUs via an m+l-level modularity in accordance with one or more embodiments described herein.
- [0041] FIG. 21 further illustrates QPUs connected via an m+l+p-level modularity in accordance with one or more embodiments described herein.
- [0042] FIG. 22 illustrates a summary of classical parallelization of quantum processing units, multi-chip quantum processors with chip-to-chip couplers, and quantum parallelization of quantum processors in accordance with one or more embodiments described herein.
- [0043] FIG. 23 illustrates an example, non-limiting method that facilitates modular quantum systems with discrete levels of connectivity.
- [0044] FIG. 24 illustrates a block diagram of an example, non-limiting, operating environment in which one or more embodiments described herein can be facilitated.

DETAILED DESCRIPTION

- [0045] The following detailed description is merely illustrative and is not intended to limit embodiments and/or application or uses of embodiments. Furthermore, there is no intention to be bound by any expressed or implied information presented in the preceding Background or Summary sections, or in the Detailed Description section.

[0046] Modular quantum processors can be required to solve challenges experienced with increasing the number of qubits on monolithic chips. These problems can relate to difficulty of chip test/screening, device yield, reliability, and manufacturability. Further advantages can be offered by use of modularities for relieving input/output (I/O) bottlenecks in dense qubit arrays, sidestepping the capacity requirements associated with available dilution refrigerators, easy replacement or upgrading of portions of the system, and allowing the exploration (or taking advantage of) heterogeneous systems.

[0047] Approaches described herein can provide different levels of modularities, namely, a p-level modularity, an l-level modularity and an m-level modularity, and combinations thereof, wherein a combination of the modularities can be more powerful than individual modularities. An l-level modularity can permit quantum communication over relatively long distances. A p-level modularity can permit use of classical communication between quantum processors. An m-level modularity can permit quantum computation between different quantum processors that can be separate and distinct and that can reside on separate and distinct substrates, while preserving the underlying lattice symmetry across the quantum processor chips. Each type of modularity can have distinct advantages. Therefore, a desirable solution can be the implementation of a combination of at least any two types of a p-level modularity, an m-level modularity, or an l-level modularity.

[0048] It is to be appreciated that the terms “qubit chip/s”, “module/s”, “quantum processing chip/s”, and “quantum processing unit/s” are used interchangeably throughout the scope of this specification. Thus, a quantum processor can comprise one or more qubit chips (quantum processing chips or quantum processing units). It is to be further appreciated that terms “l-level coupler/s”, “l-couplers”, and “l-type coupler/s” are used interchangeably, and the terms “m-level coupler/s”, “m-couplers”, and “m-type coupler/s” are also used interchangeably throughout the scope of this specification. Similarly, the terms “p-level coupler/s”, “p-couplers”, and “p-type coupler/s” are used interchangeably throughout the scope of this specification. Thus, l-level couplers, l-couplers, or l-type couplers can facilitate l-level coupling and modularity, m-level couplers, m-couplers, or m-type couplers can facilitate m-level coupling and modularity, and p-level couplers, p-couplers, or p-type couplers can facilitate p-level coupling and modularity.

[0049] In various embodiments of the invention discussed in this application, high fidelity multi-qubit devices across separate quantum processor chips, including quantum processor chips on separate and distinct substrates, can allow for the realization of scalable

quantum processors out of smaller modular units with higher yield, and reduced tolerances on frequency control. Such systems can be field repaired in cases where there are broken or defective modules, without having to replace the entire quantum processor, which can further facilitate modular qubit devices wherein qubits can be connected to transmission line resonators, wherein the transmission line resonators can be either capacitively or inductively coupled to each other. In an embodiment, the qubits and transmission line resonators can be on separate physical chips with no galvanic connection between them to enable modularity.

[0050] In various embodiments of the invention, devices, systems and/or methods for generating a pulse to affect a qubit can relate to a first qubit chip and a second qubit chip electrically coupled to the first qubit chip via a plurality of coupling elements via capacitive, inductive, and/or galvanic coupling.

[0051] One or more embodiments are now described with reference to the drawings, wherein like referenced numerals are used to refer to like elements throughout. In the following description, for purposes of explanation, numerous specific details are set forth in order to provide a more thorough understanding of the one or more embodiments. It is evident, however, in various cases, that the one or more embodiments can be practiced without these specific details.

[0052] Further, it will be appreciated that the embodiments depicted in one or more figures described herein are for illustration only, and as such, the architecture of embodiments is not limited to the devices and/or components depicted therein, nor to any particular order, connection and/or coupling of devices and/or components depicted therein.

[0053] FIG. 1 illustrates a schematic view of a system, in accordance with one or more embodiments described herein. FIG. 1 illustrates environment 100, wherein environment 100 can be a quantum computing environment comprising quantum computing device 102. Quantum computing device 102 can comprise one or more of modules 104. Modules 104 can further comprise at least qubits 106, buses 108, and readout structures 110, wherein at least the qubits 106, buses 108, and readout structures 110 can be coupled by any combination of classical couplers 114, short-range couplers 116 and/or long-range couplers 118. Modules 104 can further comprise wiring, readout filters and other components that are not illustrated in FIG. 1. Modules 104 can be connected to one or more of classical controllers 112, via a connection 111, external to a cryogenic environment of modules 104. In one or more embodiments, the qubits 106, buses 108, and readout structures 110 can be

connected by one or more of any one type of coupler out of the group comprising classical couplers 114, short-range couplers 116 and long-range couplers 118.

[0054] FIG. 2 illustrates an example, non-limiting schematic of an exemplary qubit lattice 200 with couplers between adjacent qubit chips in accordance with one or more embodiments described herein. FIG. 2 illustrates qubits 201, m-couplers 202, and l-couplers 203.

[0055] With m-level coupling and m-level modularity (illustrated at the center of FIG. 2, between adjacent qubit chips 204) provided by m-couplers 202, and l-level coupling and l-level modularity (illustrated at the right-hand side of FIG. 2) provided by l-couplers 203, the connectivity of qubits 201 on qubit chips 204 and arrangement of the modular couplers can permit qubit lattice 200 to be extended to encompass multiple quantum processor chips such as qubit chips 204. M-couplers 202 can be provided in the form of capacitive, inductive, or galvanic coupling.

[0056] FIG. 3A illustrates an example, non-limiting arrangement of a qubit lattice 300 that can be extended via l-type couplers and m-type couplers in accordance with one or more embodiments described herein. FIG. 3B illustrates an example, non-limiting arrangement of an extended qubit lattice 310 in accordance with one or more embodiments described herein. Repetitive description of like elements and/or processes employed in respective embodiments is omitted for sake of brevity.

[0057] The qubit lattice 300 can be a heavy hex lattice ($d=13$ nodes) that can be extended by m-couplers 302 and l-couplers 303. It is to be appreciated that the disclosure is not limited to a heavy hex lattice such as qubit lattice 300. Further, the extended qubit lattice 310 illustrates 9 qubit chips 304, with 3 qubit chips in each column. Adding 15 qubits to a core lattice (e.g., a core lattice of 433 qubits ($d=13$ nodes)) for "m-level" tileability and adding 7 qubits associated with the "l-type" connectivity (455 qubits total) can facilitate extension of the heavy hex lattice (e.g., qubit lattice 300), wherein l-coupler interface qubits such as interface qubits 301 can be treated as part of the l-coupler such as l-couplers 303. Such a connection can facilitate permeating information through the qubit chips such that the interconnectedness and the geometrical integrity of a qubit lattice such as qubit lattice 300 can be preserved.

[0058] As discussed in one or more embodiments herein, the m-type couplers can be characterized as being of short length (e.g., less than twice the wavelength of the

characteristic frequency of the qubits and/or buses (about 1 cm or less)) and as having a defined number of channels between at least two connected modules of the one or more modules, while l-type couplers can be characterized as being longer (e.g., from 5 cm to several meters in length). Herein, the number of channels can depend on the layout of the qubit chip. For example, for a heavy hexagonal arrangement of the chips, the m-couplers can be placed in the lattice so as to replace the other types of couplers (i.e., p-type couplers and l-type couplers). This can further depend on how the qubit lattice is cut, and it can be advantageous to choose a cut that can minimize the connections required between two modules. For example, FIG. 3A shows 13 m-couplers along the top of the array, however, the number of channels required can depend on the number of qubits and a layout of the qubits (i.e., how the qubits are laid out and connected). This can also hold true for l-type couplers.

[0059] FIG. 4 illustrates a p-level modularity in accordance with one or more embodiments described herein. Repetitive description of like elements and/or processes employed in respective embodiments is omitted for sake of brevity.

[0060] A p-level modularity can be a structure in which more than one qubit chip, for example qubit chips 403, can be connected to a classical mode of communication, such as bus 401, via one or more classical qubit controllers, such as controllers 402. In the case of one controller (e.g., one of the controllers 402), the controller can measure the state of a qubit on one chip (e.g., one of the qubit chips 403) and conditioned on that measurement, conditionally perform one or more operations on another chip (e.g., another one of the qubit chips 403). The latency of this operation can be less than 1 microsecond(s) (μ s), and thus the operation can happen more than one time within the coherence time of the qubits on qubit chips 403, wherein the coherence time of the qubits can be greater than 100 μ s. P-level coupling can be achieved, e.g., with classical buses such as bus 401 coupled to microwave I/O interfaces for communicating with qubits.

[0061] In the case of multiple controllers such as controllers 402, the operation of individual controllers can be the same as in the case of a singular controller, but a first controller can read a qubit and the first controller can pass the qubit state on bus 401 to a second controller that can run a conditional operation. The second controller can perform a computation on a qubit state and previously measured state, and bus 401 can have an active processing unit that can perform the computation. This can be further illustrated by the following sequence of figures 5A through 10B.

[0062] FIG. 5A and FIG. 5B illustrate a dilution refrigerator in accordance with one or more embodiments described herein. Repetitive description of like elements and/or processes employed in respective embodiments is omitted for sake of brevity.

[0063] FIGS. 5A and 5B illustrate qubit chips 502 housed within dilution refrigerator 506. FIG. 5A further illustrates classical controller/communication 504, that can be connected to the dilution refrigerator 506. Any combination of the different types of couplers (e.g., classical couplers, short-range couplers, and long-range couplers) discussed in one or more embodiments herein, can extend connectivity of qubit chips comprised within individual dilution refrigerator such as dilution refrigerator 506, to enable quantum computing with classical communications.

[0064] FIG. 6A, FIG. 6B and FIG. 6C illustrate an exemplary qubit chip in accordance with one or more embodiments described herein. Repetitive description of like elements and/or processes employed in respective embodiments is omitted for sake of brevity.

[0065] FIGS. 6A, 6B, and 6C illustrate qubit chip 602 and qubits 604. Qubit chip 602 can be an individual qubit chip that can be housed inside dilution refrigerator 506 of FIGS. 5A and 5B. FIG. 6B further illustrates qubit layer 606, resonator layer 608, and input/output layer 610 (I/O layer 610).

[0066] FIG. 7 illustrates multiple qubit chips (quantum processing chips or QPUs) that can be connected in a p-level modularity in accordance with one or more embodiments discussed herein. Repetitive description of like elements and/or processes employed in respective embodiments is omitted for sake of brevity.

[0067] FIG. 7 comprises three qubit chips 602 of FIG. 6. Subsequently, figures 8A through 8B can illustrate how p-type couplers can facilitate classical parallelization of multiple qubit chips 602.

[0068] FIG. 8A illustrates classical parallelization of QPUs in accordance with one or more embodiments described herein. Repetitive description of like elements and/or processes employed in respective embodiments is omitted for sake of brevity.

[0069] Multiple qubit chips 602 can be connected to one or more classical qubit controllers such as controller 806. Controller 806 can pass the qubit state via universal bus 804, that can comprise classical communication channel 802, to another controller, that can then run a conditional operation. Thus, classical information can leave one quantum fridge

(cryogenically controlled cryostat to achieve low temperatures) and return to the same fridge or travel to a different fridge.

[0070] FIG. 8B further illustrates classical parallelization of QPUs via p-type couplers in accordance with one or more embodiments described herein. Repetitive description of like elements and/or processes employed in respective embodiments is omitted for sake of brevity. Several rows of qubit chips 602 can be arranged to facilitate classical parallelization of quantum processors via classical communication channel 802, universal bus 804, and controller 806. P-type couplers are different from l-type and m-type couplers such that p-type couplers can use existing I/O control and readout lines to send signals to a central processing unit (CPU) at room temperature. The signals can then be processed, and the results can be sent to a separate quantum module at cryogenic temperatures. The operation can happen quickly enough such that quantum information can be held onto each module during the interaction, allowing quantum derived information to span modules (but not quantum coupling per se). Thus, p-type couplers refer to a classical computation unit which is connected to the one or more modules (as opposed to physical connections between modules such as provided by the l-type and m-type couplers).

[0071] FIG. 9 illustrates classical parallelization of QPUs in accordance with one or more embodiments described herein. Repetitive description of like elements and/or processes employed in respective embodiments is omitted for sake of brevity.

[0072] FIG. 9 illustrates the classical parallelization of quantum processors in the context of dilution refrigerator 506 illustrated in FIGS. 5A and 5B. As described in one or more embodiments herein, classical information can leave one quantum fridge (cryogenically controlled cryostat to achieve low temperatures) and return to the same fridge or travel to a different fridge, thereby enabling classical parallelization of quantum processors.

[0073] FIG. 10A and FIG. 10B further illustrate classical parallelization of QPUs in accordance with one or more embodiments described herein. Repetitive description of like elements and/or processes employed in respective embodiments is omitted for sake of brevity.

[0074] FIG. 10A describes three qubit chips 602 arranged in a p-level modularity whereas FIG. 10B describes “n” qubit chips arranged in a p-level modularity. Thus, classical

parallelization of quantum processors can allow for multiple qubit chips to be connected to one another via p-type couplers.

[0075] FIG. 11 illustrates an l-level modularity in accordance with one or more embodiments described herein. In an l-level modularity, multiple qubit chips 1102, each of which can have a multitude of qubits, can be connected by one or more long-range couplers such as l-coupler 1104. The long-range couplers can be much longer than the wavelength of a qubit's frequency (e.g., from 5 cm to several meters in length), and the long-range couplers can permit quantum operations by means of at least resonator-induced phase (RIP) gates, cross resonance (CR) gates, Fast Flux gates, adiabatic state transfer, and dark state transfer in a time less than the coherence time of the qubits. The long-range couplers can be flexible, permitting them to be used to join distant parts of the same cryogenic environment, and they can be made out of one or more of superconducting coaxial cables, striplines, CPWs, twinax, differential stripline, flexible printed circuit boards, or ribbon cables. They can have a loss of less than 1dB.

[0076] In an l-level modularity such as illustrated by FIG. 11 where each qubit chip (e.g., individual qubit chips of qubit chips 1102) can feature two or more connections to other qubit chips permitting the formation of a chain, wherein the network can be a small world network, an expander graph, or a binary tree, and each chip can feature more than one connection to other chips in the network. Those connections can extend the on-chip qubit lattice to another chip, or a part thereof. As before, the qubit chips 1102 can be dematable, and re-routable by moving cables where each qubit chip (e.g., one qubit chip of qubit chips 1102) can have its own classical control wiring. Some l-couplers (e.g., l-couplers 1104) can go back to the same chip reducing the average distance between qubits, whereas other l-couplers (e.g., l-couplers 1104) can run between separate magnetic shielding cans on one dilution refrigeration stack and/or between separate dilution refrigeration stacks within a shared vacuum vessel. This can be further illustrated by the following sequence of figures 12 through 15.

[0077] FIG. 12 illustrates a dilution refrigerator in accordance with one or more embodiments described herein. Repetitive description of like elements and/or processes employed in respective embodiments is omitted for sake of brevity.

[0078] FIG. 12 illustrates qubit chips 1204 housed within dilution refrigerator 1202.

[0079] FIG. 13 illustrates multiple qubit chips that can be connected in an l-level modularity via long range cables (e.g., l-couplers 1104), in accordance with one or more embodiments described herein. Repetitive description of like elements and/or processes employed in respective embodiments is omitted for sake of brevity.

[0080] FIG. 13 illustrates three qubit chips 1302 that can be part of qubit chips 1204 of FIG. 12. Subsequently, figures 12 through 15 can illustrate how l-type couplers (e.g., l-couplers 1104) can facilitate quantum parallelization of multiple qubit chips 1302.

[0081] FIG. 14A and FIG. 14B illustrate quantum parallelization of QPUs in accordance with one or more embodiments described herein. Repetitive description of like elements and/or processes employed in respective embodiments is omitted for sake of brevity.

[0082] As discussed in one or more embodiments herein, multiple qubit chips 1204 can be connected via several long-range cables (e.g., l-couplers 1402) to facilitate quantum parallelization of quantum processors. For example, L-couplers 1402 can form a quantum communication link between qubit chips 1302 of FIG. 13, thereby facilitating an l-level modularity and quantum communication at 1404 between qubit chips 1302.

[0083] L-couplers 1402 can be about 1 meter long and they can facilitate introducing physical space into a quantum computing system. The long-range cables (e.g., l-couplers 1402) can enable l-level modularity, and they can be at the same cryogenic temperatures as qubits on qubit chips 1302. L-coupling can be achieved, for example, using cryogenically cooled cables having internal wires that connect one qubit chip 1302 with another qubit chip 1302, for example, via capacitive coupling or inductive coupling or galvanic coupling.

[0084] FIG. 14C further illustrates quantum parallelization of QPUs in accordance with one or more embodiments described herein. FIG. 14C illustrates quantum parallelization of qubit chips 1204 in the context of dilution refrigerator 1202 illustrated in FIG. 12. At 1406, l-couplers 1402 can facilitate inter QPU quantum communications links between multiple QPUs on separate magnetic shielding cans on one dilution refrigeration stack.

[0085] FIG. 15 further illustrates quantum parallelization of QPUs in accordance with one or more embodiments described herein. Repetitive description of like elements and/or processes employed in respective embodiments is omitted for sake of brevity.

[0086] As discussed in one or more embodiments herein, qubit chips 1302 can be connected in a flexible manner via long range cables (e.g., l-couplers 1402) wherein the long-range cables can permit quantum operations by means of RIP, CR, Fast Flux, adiabatic state transfer, dark state transfer, etc. in much less time than the coherence time of the qubits.

[0087] FIG. 16 illustrates an m-level modularity in accordance with one or more embodiments described herein. In an m-level modularity, multiple qubit chips 1602 can be joined together by m-couplers 1604 that are short range links, less than 2 wavelengths long at the qubit frequency, and quantum gates (RIP, CR, fast flux, adiabatic, etc.) can be performed across those links.

[0088] Similar to the l-level modularity and the p-level modularity discussed in one or more embodiments, the gates in an m-level modularity can be substantially as fast as gates on the chip, permitting an extension of the fabric of one qubit chip onto another. The connections can extend the lattice on the qubit chip or extend only part of the lattice on the qubit chip. Each qubit chip can be mechanically separable and rematable, and each qubit chip can have its own classical control wiring. This can be further illustrated by the following sequence of figures 17 through 19.

[0089] FIG. 17 illustrates coupling of multichip QPUs in an m-level modularity, in accordance with one or more embodiments described herein. Repetitive description of like elements and/or processes employed in respective embodiments is omitted for sake of brevity.

[0090] FIG. 17 illustrates m-couplers 1704, wherein m-type couplers 1704 are chip-to-chip couplers that can facilitate multi-chip quantum processors that can facilitate quantum communication between qubit chips 1702. M-type couplers (e.g., m-couplers 1704) are short-range and the chip-to-chip connections can be a capacitive or other low-loss connection.

[0091] FIG. 18A and FIG. 18B further illustrate coupling of multichip QPUs in an m-level modularity, in accordance with one or more embodiments described herein. Repetitive description of like elements and/or processes employed in respective embodiments is omitted for sake of brevity.

[0092] FIG. 18B further illustrates, at 1802, quantum communication via two qubit gates between separate chips. By employing individual qubit gates between qubits on separate qubit chips such as qubit chips 1702, quantum communication between the qubit

chips can be enabled via m-couplers 1704. The qubit gates can be high fidelity and they can be run at nearly the same speed and a similar mechanism as the on-chip gates.

[0093] FIG. 19 further illustrates coupling of multichip QPUs in an m-level modularity, in accordance with one or more embodiments described herein. Repetitive description of like elements and/or processes employed in respective embodiments is omitted for sake of brevity.

[0094] While FIG. 19 illustrates three qubit chips that can be coupled via m-couplers 1704 (e.g., m-couplers 1704), it is to be appreciated that more than three qubit chips can be connected via m-type couplers.

[0095] FIG. 20A and FIG. 20B illustrate quantum parallelization of multichip QPUs via an m+l-level modularity in accordance with one or more embodiments described herein. Repetitive description of like elements and/or processes employed in respective embodiments is omitted for sake of brevity.

[0096] In accordance with one or more embodiments discussed herein, QPUs with an m+l-level modularity such as used for coupling qubit chips 2002 can comprise both l-level and m-level modularities. In an m+l-level modularity, devices joined by an m-level modularity, such as m-type couplers 2006, can share refrigeration and control infrastructure, while those joined by an l-level modularity, l-type couplers 2004, can be on independent refrigeration and control infrastructure. Additionally, an m-level modularity can be used to make uniform patches of qubits for error correcting codes, and an l-level modularity can be used to create a high-rate code out of the encoded qubits, wherein l-type couplers 2004 can permit non-local connections between qubit chips coupled by m-type couplers 2006, thereby reducing the average qubit-to-qubit distance. M-type couplers 2006 and l-type couplers 2004 can enable orthogonal directions of lattice connectivity in accordance with FIG. 20A. At 2008 in FIG. 20B, l-type couplers 2004 facilitate quantum communication between qubit chips 2002.

[0097] In accordance with one or more embodiments discussed herein, QPUs with an l+p-level modularity used for coupling qubit chips can comprise both l-level and p-level modularities. An l+p-level modularity can be facilitated by a protocol where an entangled state can be prepared between two qubits or logical qubits across an l-link (via l-couplers), and quantum teleportation can be performed between qubit chips using a p-link (via p-couplers) to perform the teleportation. In the protocol, lattice surgery can be performed

between two chips, using the p-link (provided by p-type couplers) to share stabilizer measurements. Where the latency of the p-link can be much less than the coherence time of the qubits but substantially the same as the speed of the l-coupler, it can allow synchronized classical and quantum information.

[0098] In accordance with one or more embodiments described herein, QPUs with an m+p-level modularity can comprise both m-level and p-level modularities and can behave the same as an l+p-level modularity.

[0099] FIG. 21 illustrates QPUs connected via an m+l+p-level modularity in accordance with one or more embodiments herein. Repetitive description of like elements and/or processes employed in respective embodiments is omitted for sake of brevity.

[00100] An m+l+p-level modularity can behave the same as an m+l-level modularity combined with an l+p-level modularity. FIG. 21 illustrates, at 2102, classical communication via p-type couplers, quantum communication via l-type couplers at 2104, and quantum communication via short-range m-type couplers at 2106. FIG. 21 illustrates a multi-chip quantum processor 2108 wherein multiple individual QPUs can be connected via short-range chip-to-chip couplers (e.g. m-level modularity), and wherein individual multi-chip quantum processors can be connected via p-level (at 2102) and l-level modularities (at 2104). The three levels of modularity can address various limitations observed with using individual levels of modularities, as discussed in one or more embodiments herein. The three levels of modularities can facilitate building a quantum system that can coexist at different length scales, such as illustrated by FIG. 21.

[00101] FIG. 22 illustrates a summary of classical parallelization of quantum processors, multi-chip quantum processors with chip-to chip couplers, and quantum parallelization of quantum processing units in accordance with one or more embodiments described herein. FIG. 22 illustrates classical parallelization of quantum processors at 2202, multi-chip quantum processors with chip-to-chip couplers at 2204, and quantum parallelization of quantum processors at 2206.

[00102] FIG. 23 illustrates a flow diagram of an example, non-limiting method that facilitates modular quantum systems with discreet levels of connectivity. Repetitive description of like elements and/or processes employed in respective embodiments is omitted for sake of brevity. Method 2300 can comprise, at 2302, coupling a plurality of at least qubits, buses, and readout structures using a plurality of couplers, wherein the plurality

of couplers comprises at least two couplers selected from a group consisting of: classical couplers, short-range couplers, and long-range couplers, and wherein the plurality of at least qubits, buses and readout structures are comprised by one or more modules.

[00103] Some non-limiting exemplary embodiments are specified in the following numbered clauses:

1. A quantum computing device comprising: a plurality of modules comprising individual quantum processing units (QPUs) comprising at least qubits, busses, and readout structures; a plurality of at least one of p-type couplers, m-type couplers, l-type couplers or a combination thereof, wherein a plurality of the at least qubits, buses and readout structures are coupled using classical (p-type), near-range (m-type) and medium range (l-type) connections. a connection from one or more modules of the plurality of modules to a classical controller external to the cryogenic environment.
2. The quantum computing device of clause 1, comprising a bus external to the cryogenic environment that carries classical information from one controller to another in a time less than the coherence time (T_1) of the qubits, wherein the bus runs between the classical controllers.
3. The quantum computing device of any of clauses 1 to 2, wherein module-to-module connections are less than a defined length to create a longitudinal or transverse coupling between qubits on the edge of modules, and wherein density and arrangement of the qubits extend a qubit lattice from one module to the next.
4. The quantum computing device of any of clauses 1 to 3, further comprising: one or more m-type couplers that are defined as being constrained by less than a defined distance between modules and as containing a defined number of channels between connected modules.; and one or more p-type couplers that facilitate classical parallelization between quantum processors.
5. The quantum computing device of any of clauses 1 to 4, wherein m-type couplers are characterized as being of short length, and wherein p-type couplers refer to a classical computation unit which is connected to the plurality of modules.
6. The quantum computing device of any of clauses 1 to 5, further comprising: a plurality of l-type couplers that are longer than a defined length and that connect the plurality modules.
7. The quantum computing device of any of clauses 1 to 6, wherein each of multiple individual quantum processing units are disposed on separate and distinct

substrates.

[00104] FIG. 24 illustrates a block diagram of an example, non-limiting, operating environment in which one or more embodiments described herein can be facilitated.

[00105] Various aspects of the present disclosure are described by narrative text, flowcharts, block diagrams of computer systems and/or block diagrams of the machine logic included in computer program product (CPP) embodiments. With respect to any flowcharts, depending upon the technology involved, the operations can be performed in a different order than what is shown in a given flowchart. For example, again depending upon the technology involved, two operations shown in successive flowchart blocks may be performed in reverse order, as a single integrated step, concurrently, or in a manner at least partially overlapping in time.

[00106] A computer program product embodiment ("CPP embodiment" or "CPP") is a term used in the present disclosure to describe any set of one, or more, storage media (also called "mediums") collectively included in a set of one, or more, storage devices that collectively include machine readable code corresponding to instructions and/or data for performing computer operations specified in a given CPP claim. A "storage device" is any tangible device that can retain and store instructions for use by a computer processor. Without limitation, the computer readable storage medium may be an electronic storage medium, a magnetic storage medium, an optical storage medium, an electromagnetic storage medium, a semiconductor storage medium, a mechanical storage medium, or any suitable combination of the foregoing. Some known types of storage devices that include these mediums include: diskette, hard disk, random access memory (RAM), read-only memory (ROM), erasable programmable read-only memory (EPROM or Flash memory), static random access memory (SRAM), compact disc read-only memory (CD-ROM), digital versatile disk (DVD), memory stick, floppy disk, mechanically encoded device (such as punch cards or pits / lands formed in a major surface of a disc) or any suitable combination of the foregoing. A computer readable storage medium, as that term is used in the present disclosure, is not to be construed as storage in the form of transitory signals *per se*, such as radio waves or other freely propagating electromagnetic waves, electromagnetic waves propagating through a waveguide, light pulses passing through a fiber optic cable, electrical signals communicated through a wire, and/or other transmission media. As will be understood by those of skill in the art, data is typically moved at some occasional points in time during normal operations of a storage device, such as during access, de-fragmentation

or garbage collection, but this does not render the storage device as transitory because the data is not transitory while it is stored.

[00107] Computing environment 2400 contains an example of an environment for the execution of at least some of the computer code involved in performing the inventive methods, such as quantum computing code 2445. In addition to block 2445, computing environment 2400 includes, for example, computer 2401, wide area network (WAN) 2402, end user device (EUD) 2403, remote server 2404, public cloud 2405, and private cloud 2406. In this embodiment, computer 2401 includes processor set 2410 (including processing circuitry 2420 and cache 2421), communication fabric 2411, volatile memory 2412, persistent storage 2413 (including operating system 2422 and block 2445, as identified above), peripheral device set 2414 (including user interface (UI), device set 2423, storage 2424, and Internet of Things (IoT) sensor set 2425), and network module 2415. Remote server 2404 includes remote database 2430. Public cloud 2405 includes gateway 2540, cloud orchestration module 2441, host physical machine set 2442, virtual machine set 2443, and container set 2444.

[00108] COMPUTER 2401 may take the form of a desktop computer, laptop computer, tablet computer, smart phone, smart watch or other wearable computer, mainframe computer, quantum computer or any other form of computer or mobile device now known or to be developed in the future that is capable of running a program, accessing a network or querying a database, such as remote database 2430. As is well understood in the art of computer technology, and depending upon the technology, performance of a computer-implemented method may be distributed among multiple computers and/or between multiple locations. On the other hand, in this presentation of computing environment 2400, detailed discussion is focused on a single computer, specifically computer 2401, to keep the presentation as simple as possible. Computer 2401 may be located in a cloud, even though it is not shown in a cloud in Figure 24. On the other hand, computer 2401 is not required to be in a cloud except to any extent as may be affirmatively indicated.

[00109] PROCESSOR SET 2410 includes one, or more, computer processors of any type now known or to be developed in the future. Processing circuitry 2420 may be distributed over multiple packages, for example, multiple, coordinated integrated circuit chips. Processing circuitry 2420 may implement multiple processor threads and/or multiple processor cores. Cache 2421 is memory that is located in the processor chip package(s) and is typically used for data or code that should be available for rapid access by the threads or

cores running on processor set 2410. Cache memories are typically organized into multiple levels depending upon relative proximity to the processing circuitry. Alternatively, some, or all, of the cache for the processor set may be located “off chip.” In some computing environments, processor set 2410 may be designed for working with qubits and performing quantum computing.

[00110] Computer readable program instructions are typically loaded onto computer 2401 to cause a series of operational steps to be performed by processor set 2410 of computer 2401 and thereby effect a computer-implemented method, such that the instructions thus executed will instantiate the methods specified in flowcharts and/or narrative descriptions of computer-implemented methods included in this document (collectively referred to as “the inventive methods”). These computer readable program instructions are stored in various types of computer readable storage media, such as cache 2421 and the other storage media discussed below. The program instructions, and associated data, are accessed by processor set 2410 to control and direct performance of the inventive methods. In computing environment 2400, at least some of the instructions for performing the inventive methods may be stored in block 2445 in persistent storage 2413.

[00111] COMMUNICATION FABRIC 2411 is the signal conduction paths that allow the various components of computer 2401 to communicate with each other. Typically, this fabric is made of switches and electrically conductive paths, such as the switches and electrically conductive paths that make up busses, bridges, physical input / output ports and the like. Other types of signal communication paths may be used, such as fiber optic communication paths and/or wireless communication paths.

[00112] VOLATILE MEMORY 2412 is any type of volatile memory now known or to be developed in the future. Examples include dynamic type random access memory (RAM) or static type RAM. Typically, the volatile memory is characterized by random access, but this is not required unless affirmatively indicated. In computer 2401, the volatile memory 2412 is located in a single package and is internal to computer 2401, but, alternatively or additionally, the volatile memory may be distributed over multiple packages and/or located externally with respect to computer 2401.

[00113] PERSISTENT STORAGE 2413 is any form of non-volatile storage for computers that is now known or to be developed in the future. The non-volatility of this storage means that the stored data is maintained regardless of whether power is being supplied to computer 2401 and/or directly to persistent storage 2413. Persistent storage

2413 may be a read only memory (ROM), but typically at least a portion of the persistent storage allows writing of data, deletion of data and re-writing of data. Some familiar forms of persistent storage include magnetic disks and solid state storage devices. Operating system 2422 may take several forms, such as various known proprietary operating systems or open source Portable Operating System Interface type operating systems that employ a kernel. The code included in block 2445 typically includes at least some of the computer code involved in performing the inventive methods.

[00114] PERIPHERAL DEVICE SET 2414 includes the set of peripheral devices of computer 2401. Data communication connections between the peripheral devices and the other components of computer 2401 may be implemented in various ways, such as Bluetooth connections, Near-Field Communication (NFC) connections, connections made by cables (such as universal serial bus (USB) type cables), insertion type connections (for example, secure digital (SD) card), connections made through local area communication networks and even connections made through wide area networks such as the internet. In various embodiments, UI device set 2423 may include components such as a display screen, speaker, microphone, wearable devices (such as goggles and smart watches), keyboard, mouse, printer, touchpad, game controllers, and haptic devices. Storage 2424 is external storage, such as an external hard drive, or insertable storage, such as an SD card. Storage 2424 may be persistent and/or volatile. In some embodiments, storage 2424 may take the form of a quantum computing storage device for storing data in the form of qubits. In embodiments where computer 2401 is required to have a large amount of storage (for example, where computer 2401 locally stores and manages a large database) then this storage may be provided by peripheral storage devices designed for storing very large amounts of data, such as a storage area network (SAN) that is shared by multiple, geographically distributed computers. IoT sensor set 2425 is made up of sensors that can be used in Internet of Things applications. For example, one sensor may be a thermometer and another sensor may be a motion detector.

[00115] NETWORK MODULE 2415 is the collection of computer software, hardware, and firmware that allows computer 2401 to communicate with other computers through WAN 2402. Network module 2415 may include hardware, such as modems or Wi-Fi signal transceivers, software for packetizing and/or de-packetizing data for communication network transmission, and/or web browser software for communicating data over the internet. In some embodiments, network control functions and network forwarding

functions of network module 2415 are performed on the same physical hardware device. In other embodiments (for example, embodiments that utilize software-defined networking (SDN)), the control functions and the forwarding functions of network module 2415 are performed on physically separate devices, such that the control functions manage several different network hardware devices. Computer readable program instructions for performing the inventive methods can typically be downloaded to computer 2401 from an external computer or external storage device through a network adapter card or network interface included in network module 2415.

[00116] WAN 2402 is any wide area network (for example, the internet) capable of communicating computer data over non-local distances by any technology for communicating computer data, now known or to be developed in the future. In some embodiments, the WAN may be replaced and/or supplemented by local area networks (LANs) designed to communicate data between devices located in a local area, such as a Wi-Fi network. The WAN and/or LANs typically include computer hardware such as copper transmission cables, optical transmission fibers, wireless transmission, routers, firewalls, switches, gateway computers and edge servers.

[00117] END USER DEVICE (EUD) 2403 is any computer system that is used and controlled by an end user (for example, a customer of an enterprise that operates computer 2401), and may take any of the forms discussed above in connection with computer 2401. EUD 2403 typically receives helpful and useful data from the operations of computer 2401. For example, in a hypothetical case where computer 2401 is designed to provide a recommendation to an end user, this recommendation would typically be communicated from network module 2415 of computer 2401 through WAN 2402 to EUD 2403. In this way, EUD 2403 can display, or otherwise present, the recommendation to an end user. In some embodiments, EUD 2403 may be a client device, such as thin client, heavy client, mainframe computer, desktop computer and so on.

[00118] REMOTE SERVER 2404 is any computer system that serves at least some data and/or functionality to computer 2401. Remote server 2404 may be controlled and used by the same entity that operates computer 2401. Remote server 104 represents the machine(s) that collect and store helpful and useful data for use by other computers, such as computer 2401. For example, in a hypothetical case where computer 2401 is designed and programmed to provide a recommendation based on historical data, then this historical data may be provided to computer 2401 from remote database 2430 of remote server 2404.

[00119] PUBLIC CLOUD 2405 is any computer system available for use by multiple entities that provides on-demand availability of computer system resources and/or other computer capabilities, especially data storage (cloud storage) and computing power, without direct active management by the user. Cloud computing typically leverages sharing of resources to achieve coherence and economies of scale. The direct and active management of the computing resources of public cloud 2405 is performed by the computer hardware and/or software of cloud orchestration module 2441. The computing resources provided by public cloud 2405 are typically implemented by virtual computing environments that run on various computers making up the computers of host physical machine set 2442, which is the universe of physical computers in and/or available to public cloud 2405. The virtual computing environments (VCEs) typically take the form of virtual machines from virtual machine set 2443 and/or containers from container set 2444. It is understood that these VCEs may be stored as images and may be transferred among and between the various physical machine hosts, either as images or after instantiation of the VCE. Cloud orchestration module 2441 manages the transfer and storage of images, deploys new instantiations of VCEs and manages active instantiations of VCE deployments. Gateway 2440 is the collection of computer software, hardware, and firmware that allows public cloud 2405 to communicate through WAN 2402.

[00120] Some further explanation of virtualized computing environments (VCEs) will now be provided. VCEs can be stored as “images.” A new active instance of the VCE can be instantiated from the image. Two familiar types of VCEs are virtual machines and containers. A container is a VCE that uses operating-system-level virtualization. This refers to an operating system feature in which the kernel allows the existence of multiple isolated user-space instances, called containers. These isolated user-space instances typically behave as real computers from the point of view of programs running in them. A computer program running on an ordinary operating system can utilize all resources of that computer, such as connected devices, files and folders, network shares, CPU power, and quantifiable hardware capabilities. However, programs running inside a container can only use the contents of the container and devices assigned to the container, a feature which is known as containerization.

[00121] PRIVATE CLOUD 2406 is similar to public cloud 2405, except that the computing resources are only available for use by a single enterprise. While private cloud 2406 is depicted as being in communication with WAN 2402, in other embodiments a

private cloud may be disconnected from the internet entirely and only accessible through a local/private network. A hybrid cloud is a composition of multiple clouds of different types (for example, private, community or public cloud types), often respectively implemented by different vendors. Each of the multiple clouds remains a separate and discrete entity, but the larger hybrid cloud architecture is bound together by standardized or proprietary technology that enables orchestration, management, and/or data/application portability between the multiple constituent clouds. In this embodiment, public cloud 2405 and private cloud 2406 are both part of a larger hybrid cloud.

CLAIMS

1. A quantum computing device comprising:
 - one or more modules comprising at least qubits, buses, and readout structures;
 - a plurality of couplers, wherein the plurality of couplers comprises at least two couplers selected from a group consisting of: classical couplers, short-range couplers, and long-range couplers, that are adapted for coupling a plurality of the at least qubits, buses, and readout structures; and
 - a connection from the one or more modules to at least two classical controllers external to a cryogenic environment comprising the one or more modules.
2. The quantum computing device of claim 1, wherein a bus external to the cryogenic environment and running between the at least two classical controllers is adapted to carry classical information between the at least two classical controllers.
3. The quantum computing device of claim 2, wherein the bus is adapted to carry the classical information in a time less than a coherence time (T_1) of qubits.
4. The quantum computing device of any of the preceding claims, wherein connections between at least two consecutive modules of the one or more modules are less than a defined length to create a longitudinal or transverse coupling between the qubits on edges of modules.
5. The quantum computing device of any of the preceding claims, wherein the qubits extend a qubit lattice between at least two modules of the one or more modules.
6. The quantum computing device of any of the preceding claims, wherein the short-range couplers are characterized as being shorter than a defined length, and wherein the short-range couplers are characterized as having a defined number of channels between at least two connected modules of the one or more modules.
7. The quantum computing device of any of the preceding claims, wherein the classical couplers are adapted to provide classical parallelization between individual modules, and wherein the classical couplers refer to a classical computation unit which is connected to the

one or more modules.

8. The quantum computing device of any of the preceding claims, wherein the long-range couplers are characterized as being longer than a defined length, and wherein individual modules of the one or more modules are respectively disposed on separate and distinct substrates.

9. The quantum computing device of any of the preceding claims, wherein a combination of the classical couplers and the short-range couplers, and the combination of the classical couplers and the long-range couplers allow synchronization of classical and quantum information between at least two modules of the one or more modules.

10. A method, comprising:
coupling a plurality of at least qubits, buses, and readout structures using a plurality of couplers, wherein the plurality of couplers comprises at least two couplers selected from a group consisting of: classical couplers, short-range couplers, and long-range couplers, and wherein the plurality of at least qubits, buses and readout structures are comprised by one or more modules.

11. The method of claim 10, further comprising:
creating a longitudinal or transverse coupling between the qubits on edges of modules using connections between at least two consecutive modules of the one or more modules, wherein the connections are less than a defined length.

12. The method of any of claims 10 to 11, wherein the qubits extend a qubit lattice between at least two modules of the one or more modules.

13. The method of any of claims 10 to 12, wherein the short-range couplers are characterized as being shorter than a defined length.

14. The method of any of claims 10 to 13, wherein the short-range couplers are characterized as having a defined number of channels between at least two connected modules of the one or more modules.

15. The method of any of claims 10 to 14, wherein the classical couplers refer to a classical computation unit which is connected to the one or more modules.
16. The method of any of claims 10 to 15, wherein the long-range couplers are characterized as being longer than a defined length.
17. The method of any of claims 10 to 16, wherein individual modules of the one or more modules are respectively disposed on separate and distinct substrates.
18. A quantum computing device, comprising:
one or more modules comprising at least qubits, buses, and readout structures;
a plurality of couplers, wherein the plurality of couplers comprises at least two couplers selected from a group consisting of: classical couplers, short-range couplers, and long-range couplers, that are adapted for coupling a plurality of the at least qubits, buses, and readout structures; and
a connection from the one or more modules to a classical controller external to a cryogenic environment comprising the one or more modules.
19. The quantum computing device of claim 18, wherein the classical controller measures a state of a qubit on a first module of the one or more modules.
20. The quantum computing device of claim 19, wherein based on a measurement of the state of the qubit, the classical controller conditionally performs one or more operations on a second module of the one or more modules, via a bus external to the cryogenic environment.

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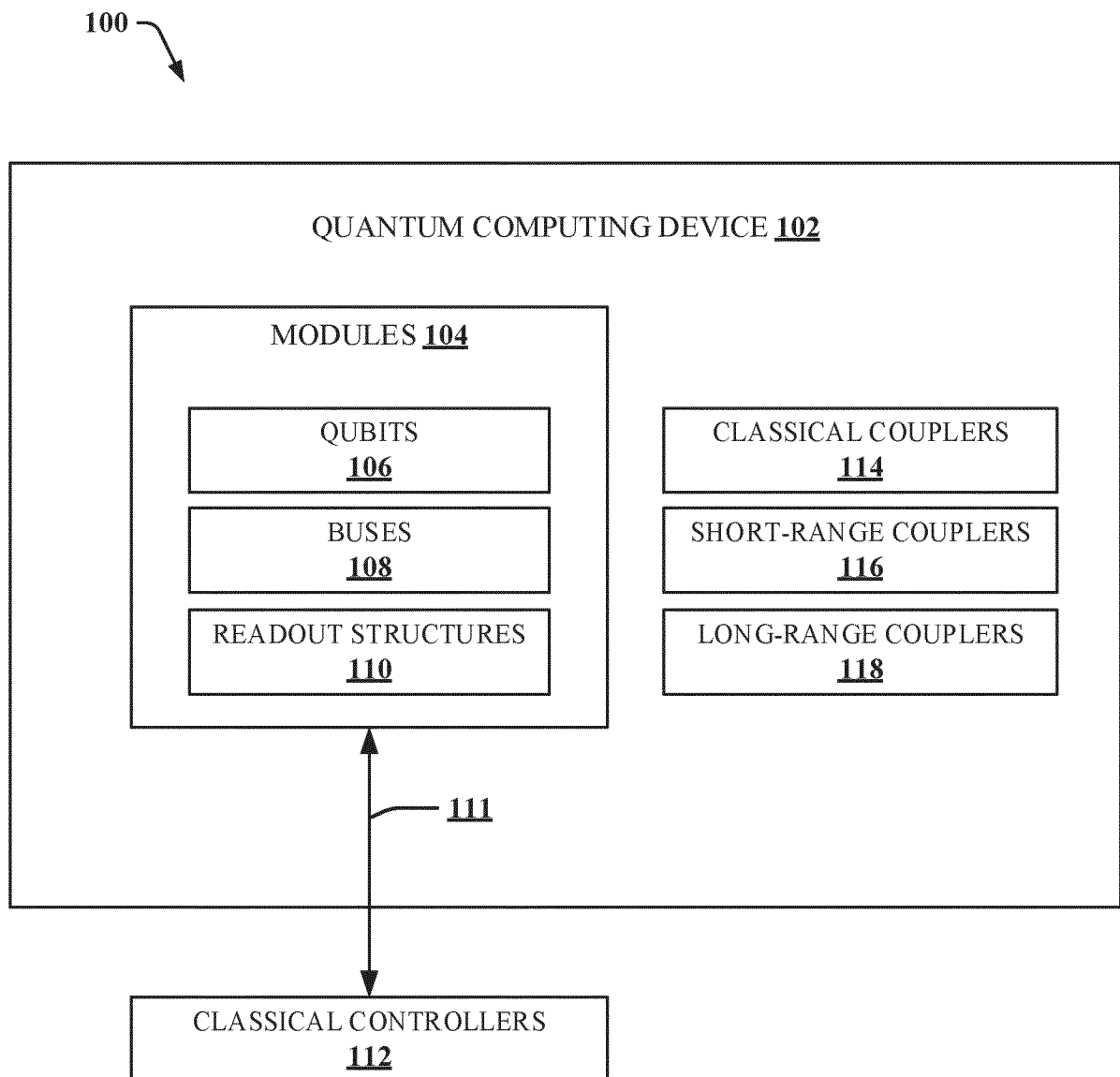


FIG. 1

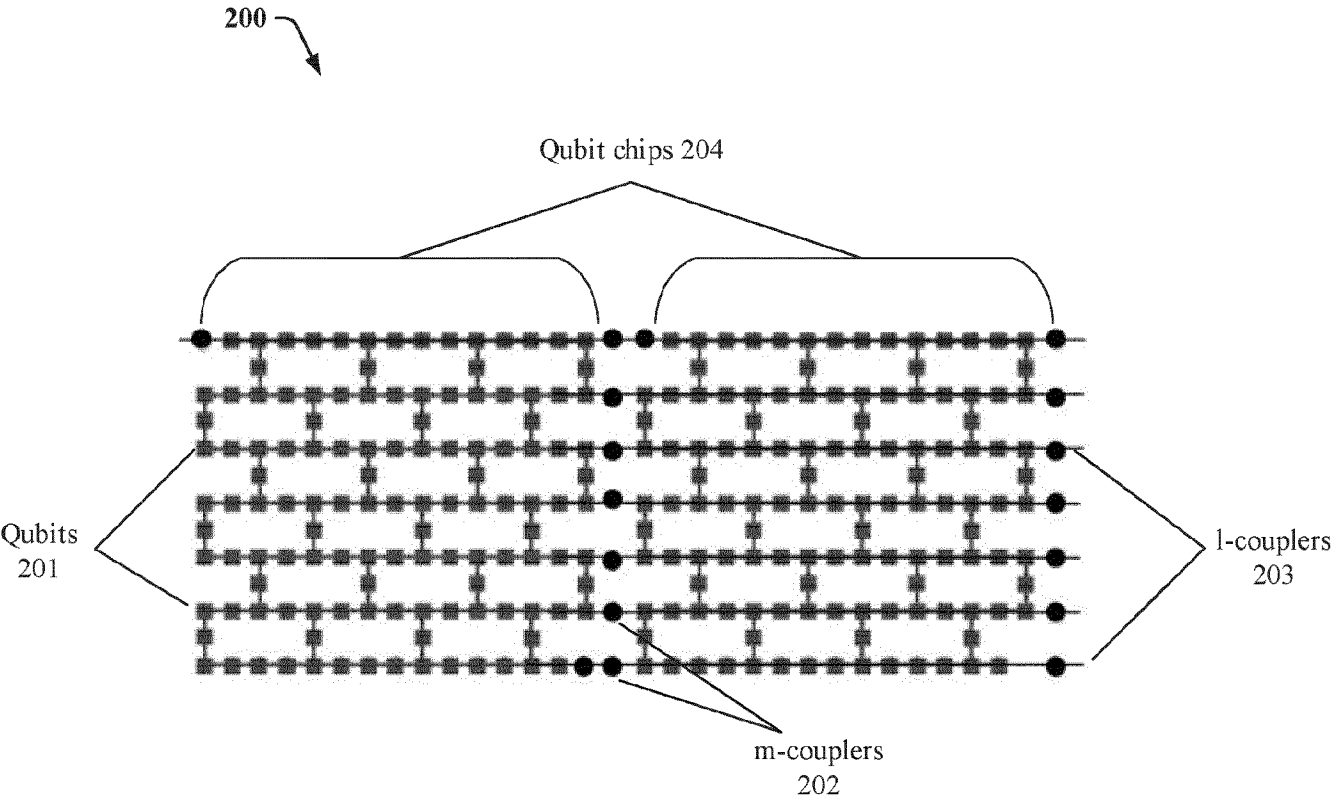


FIG. 2

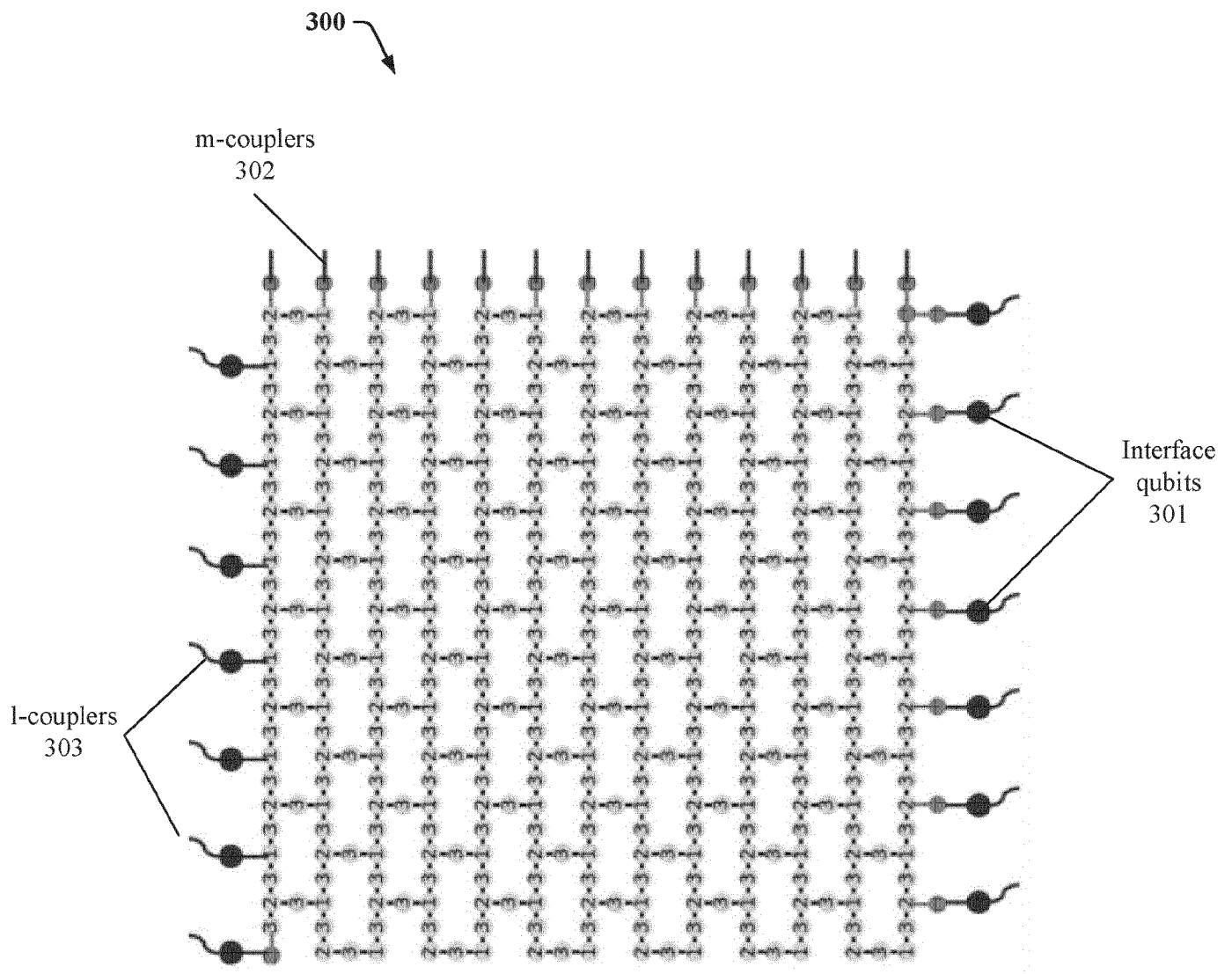


FIG. 3A

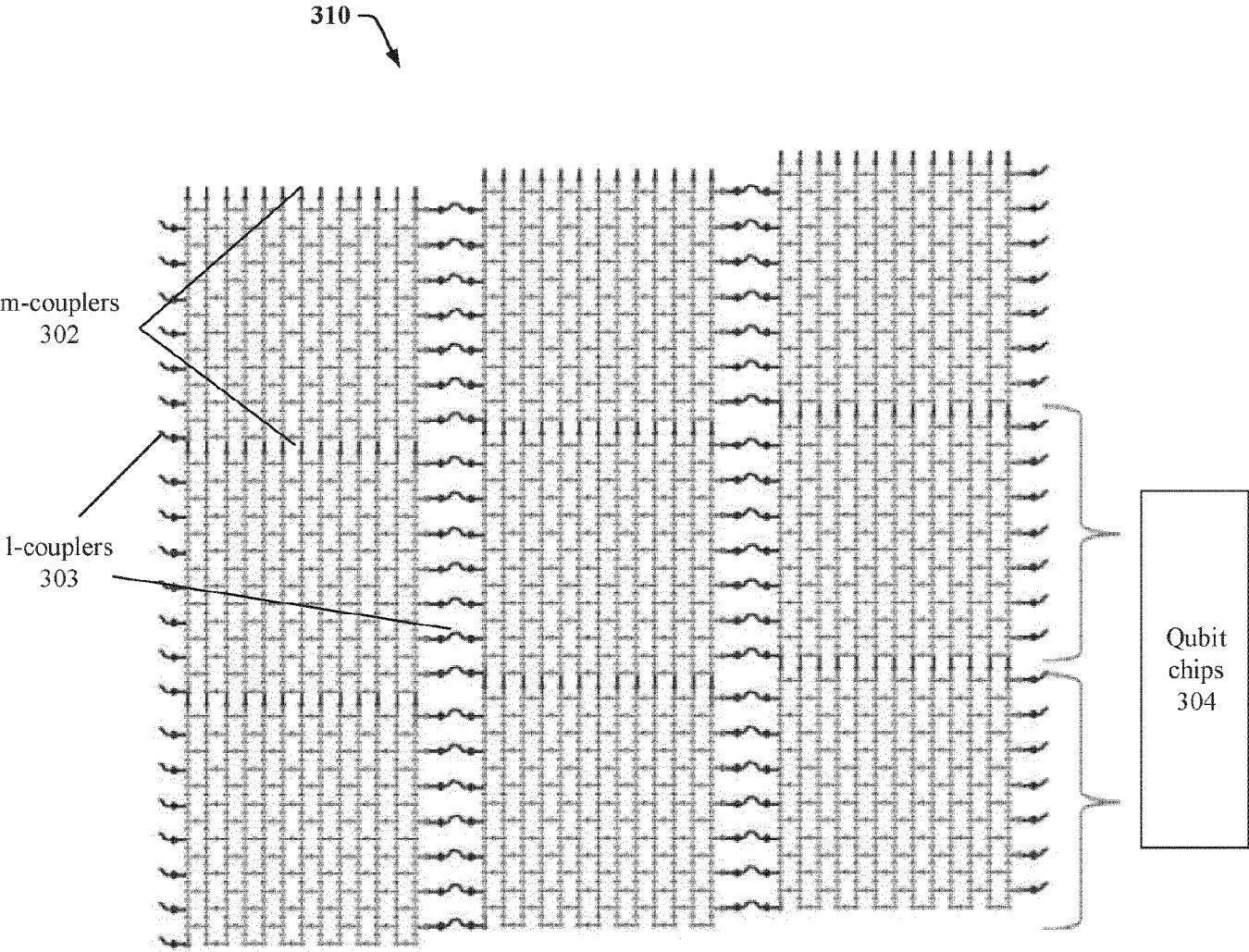


FIG. 3B

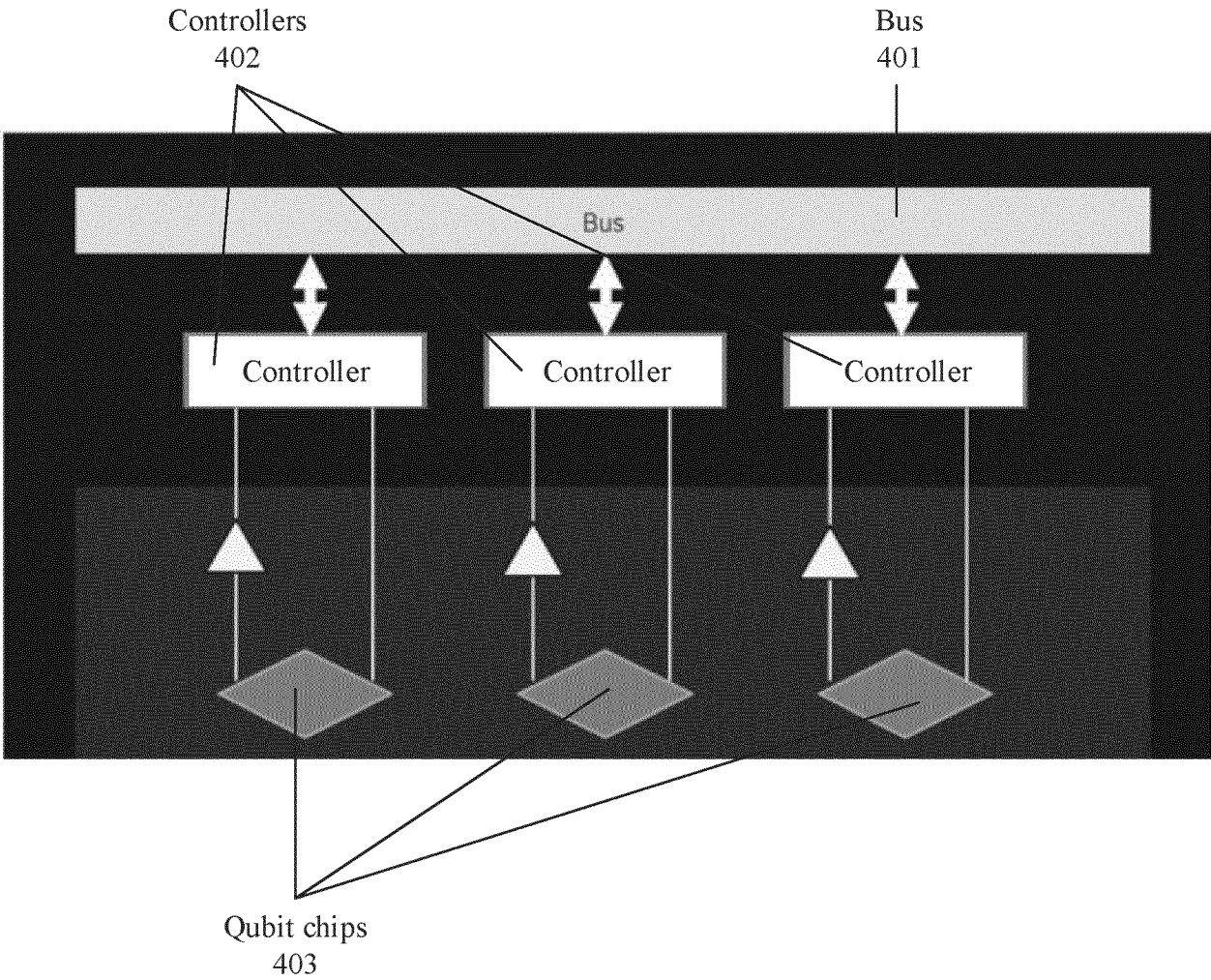


FIG. 4

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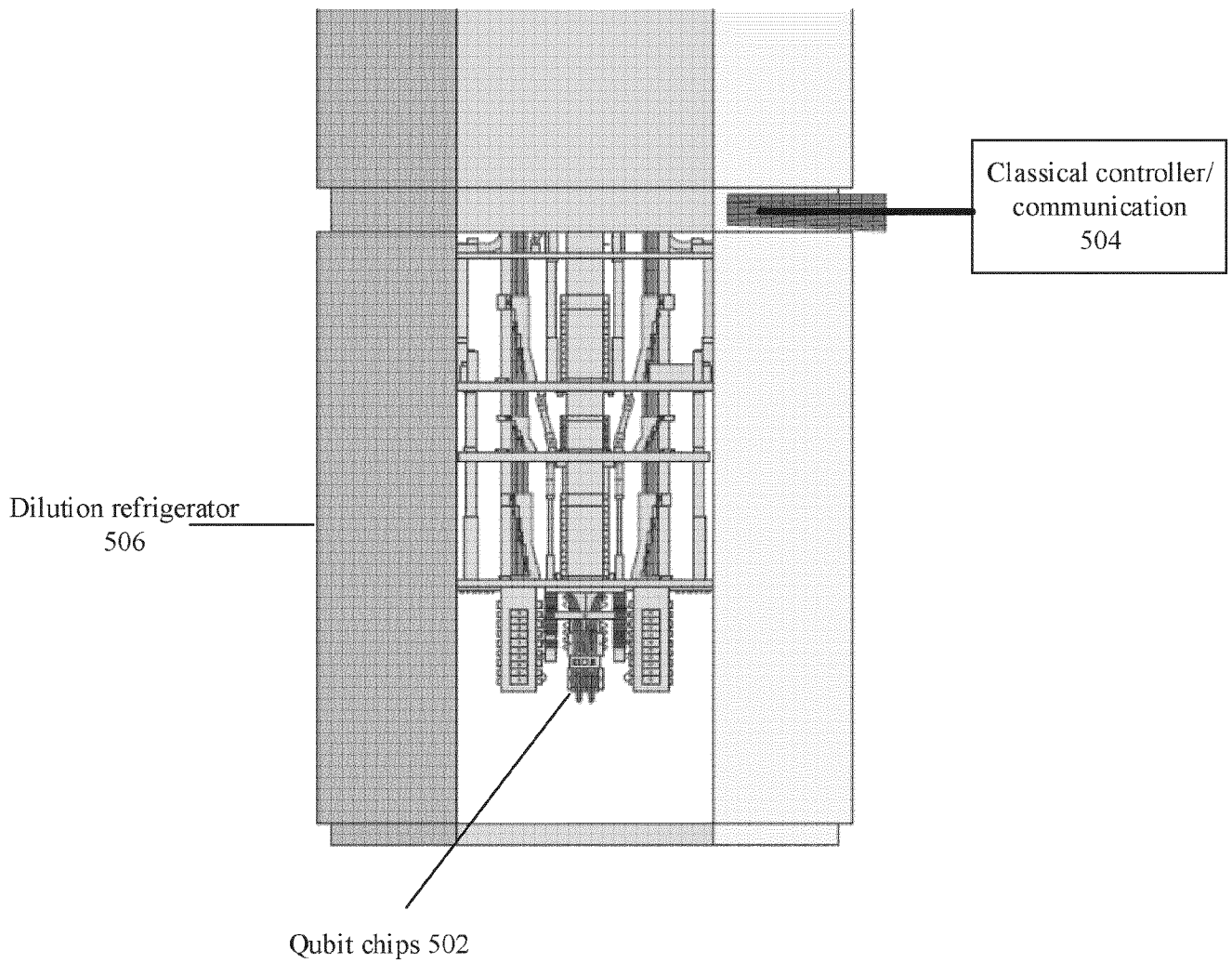


FIG. 5A

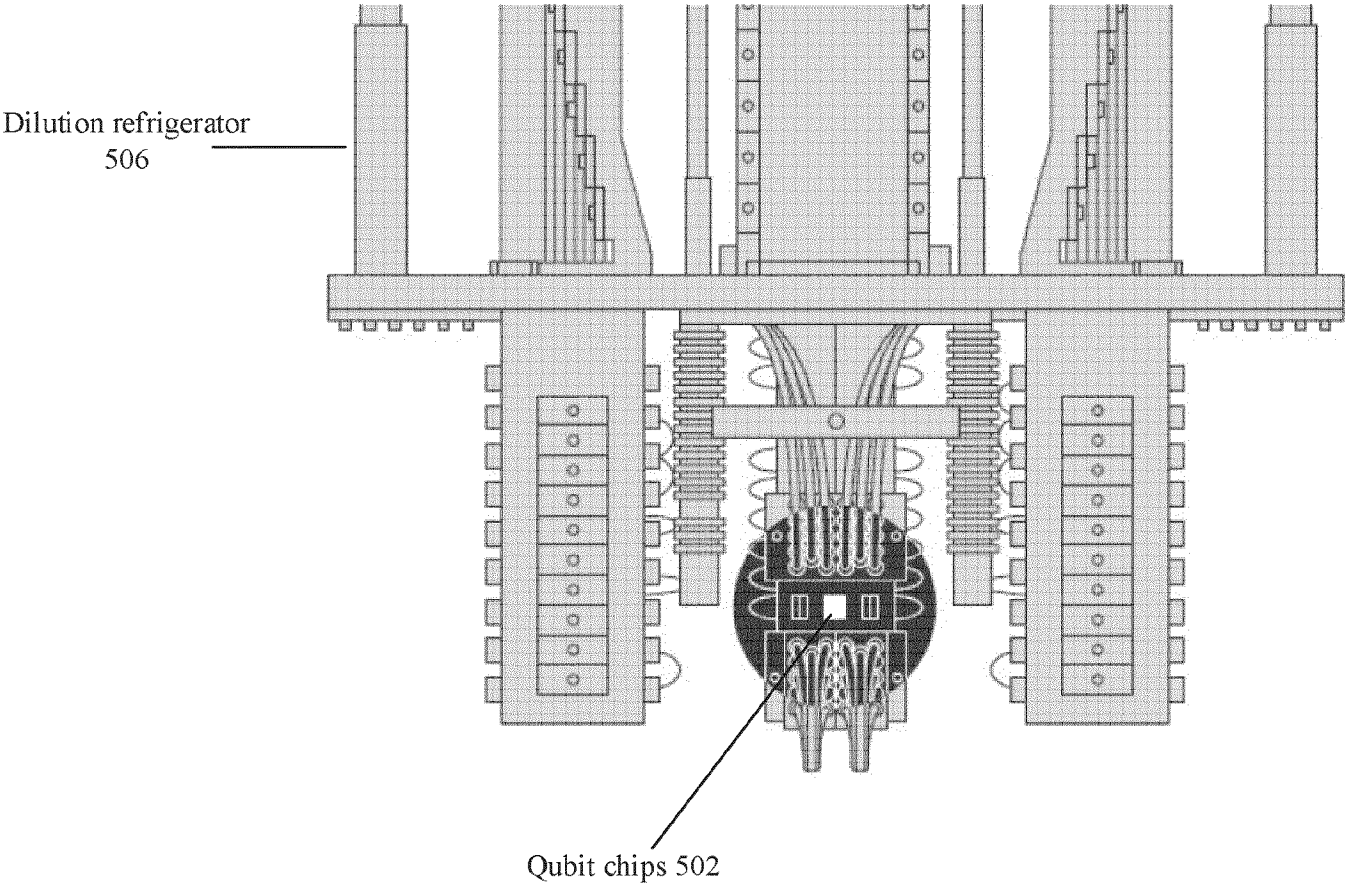


FIG. 5B

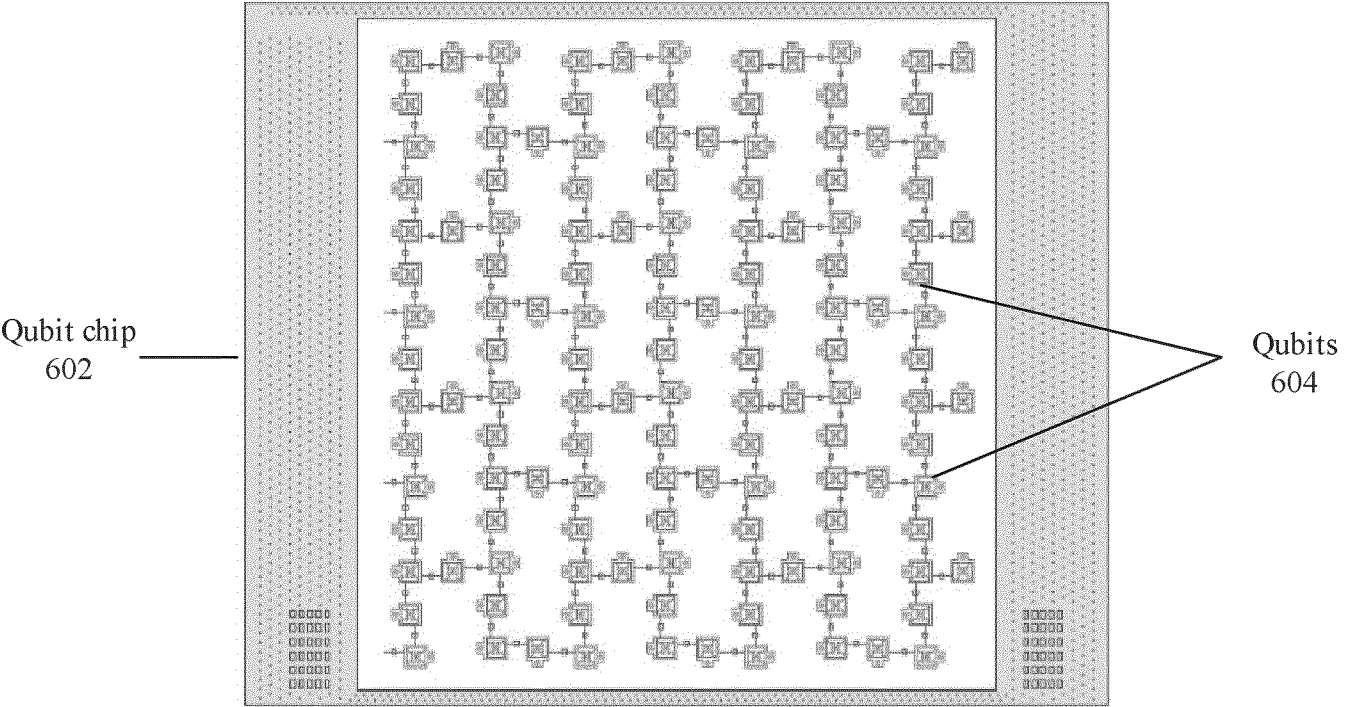


FIG. 6A

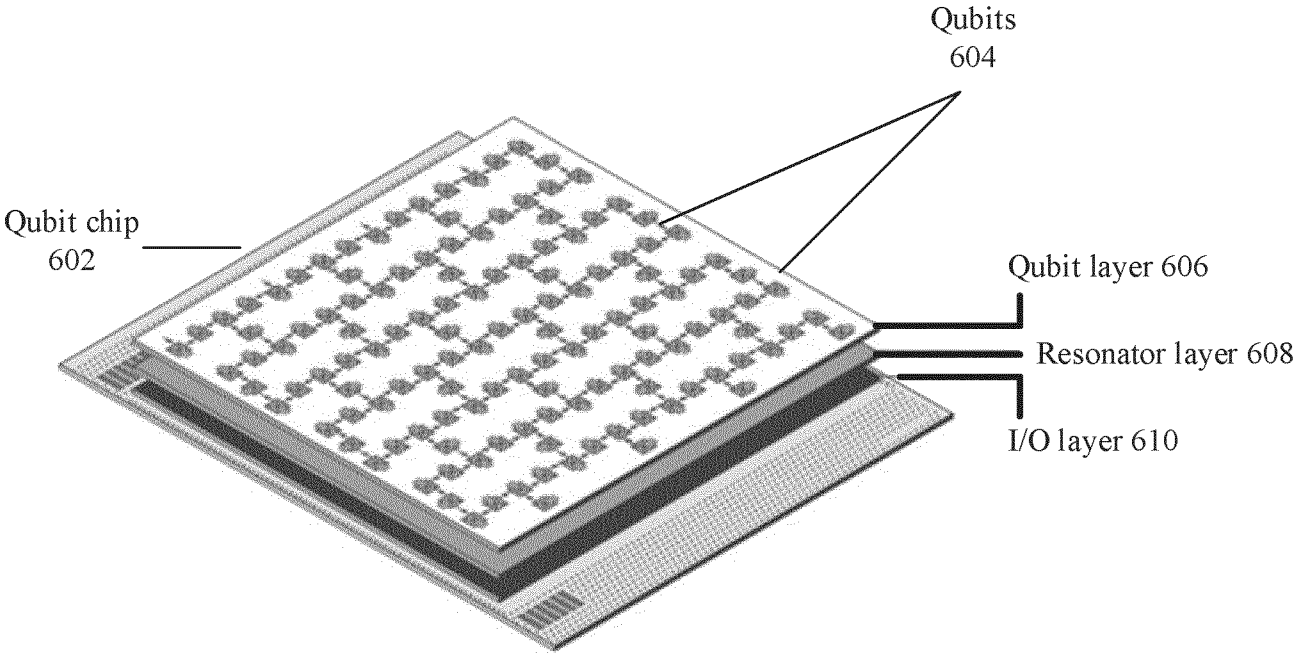


FIG. 6B

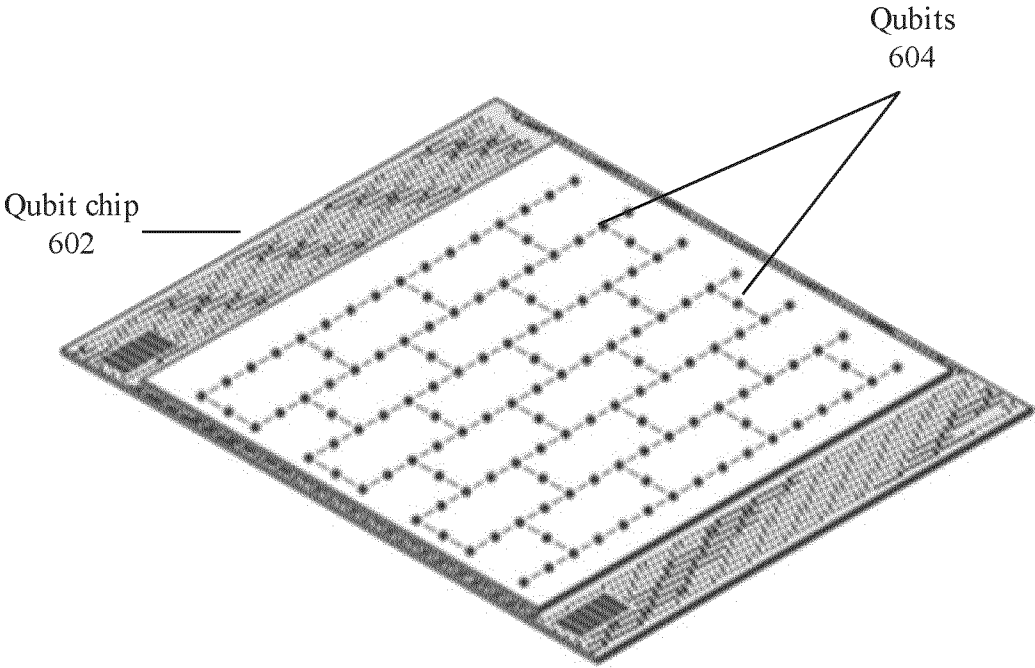


FIG. 6C

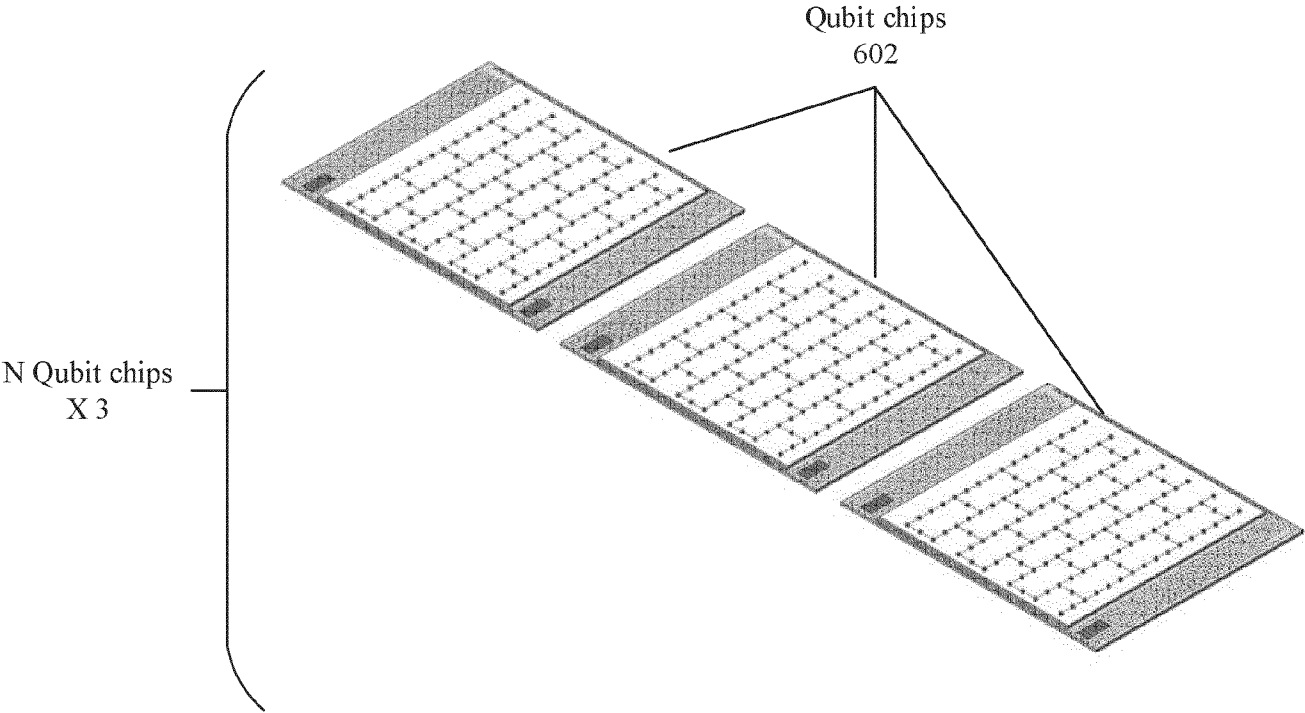


FIG. 7

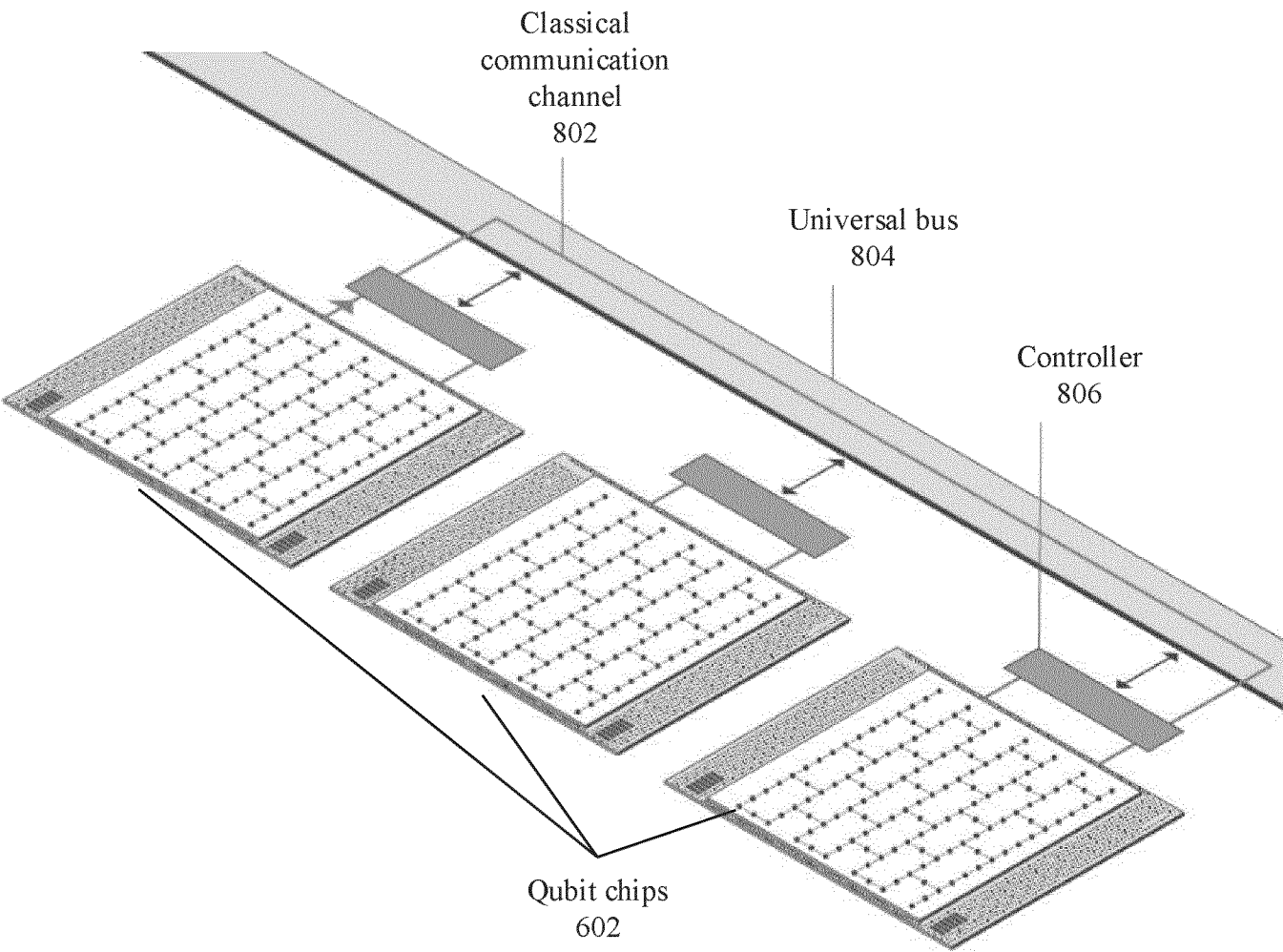


FIG. 8A

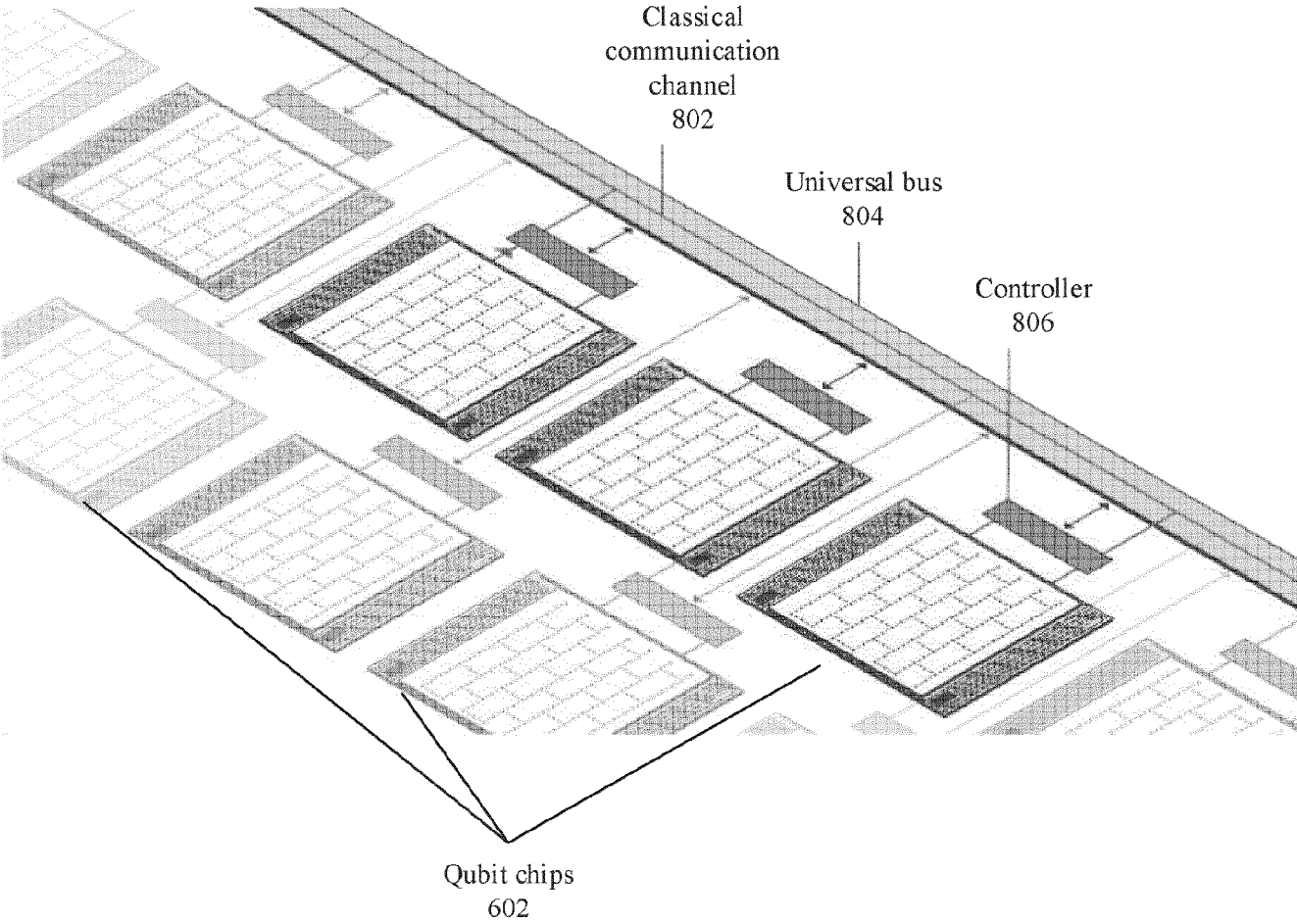


FIG. 8B

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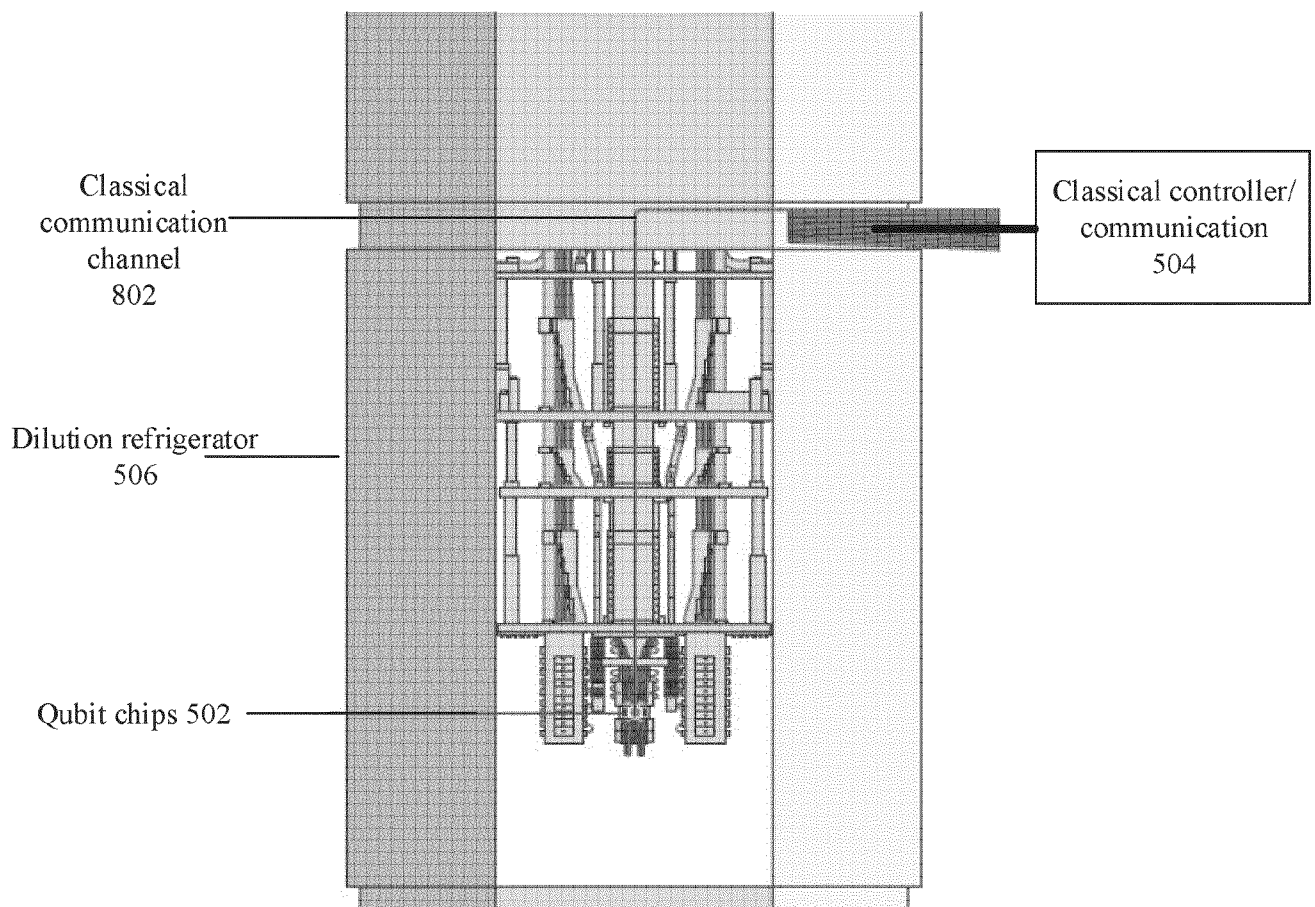


FIG. 9

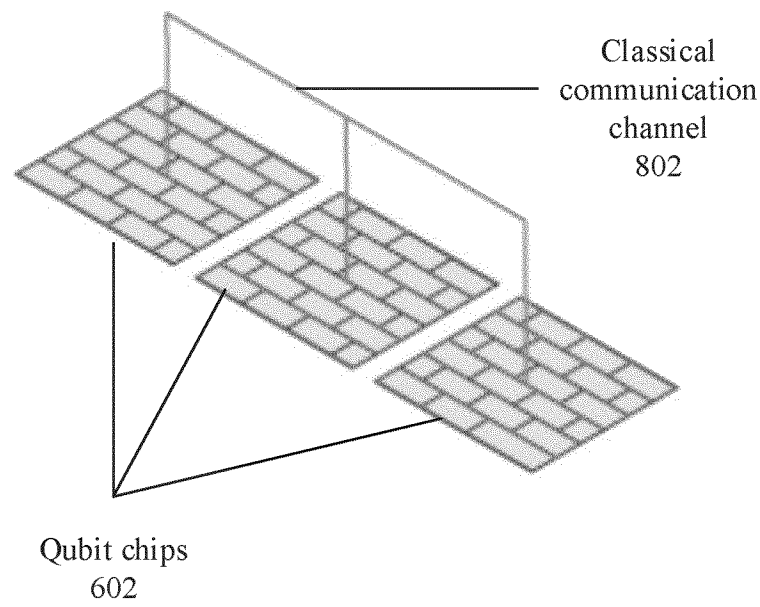


FIG. 10A

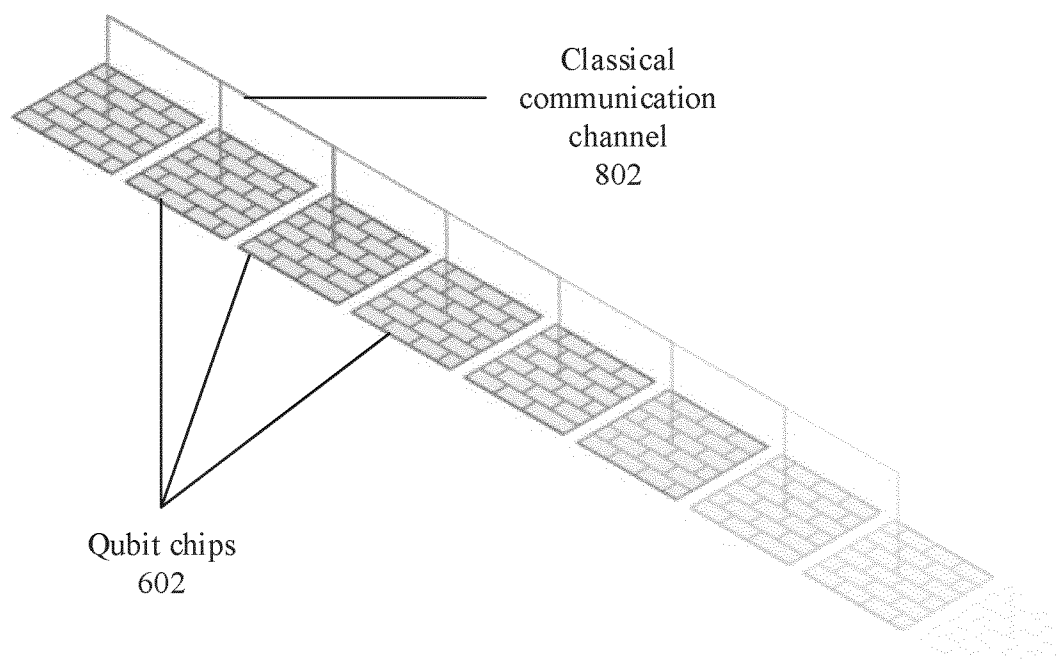


FIG. 10B

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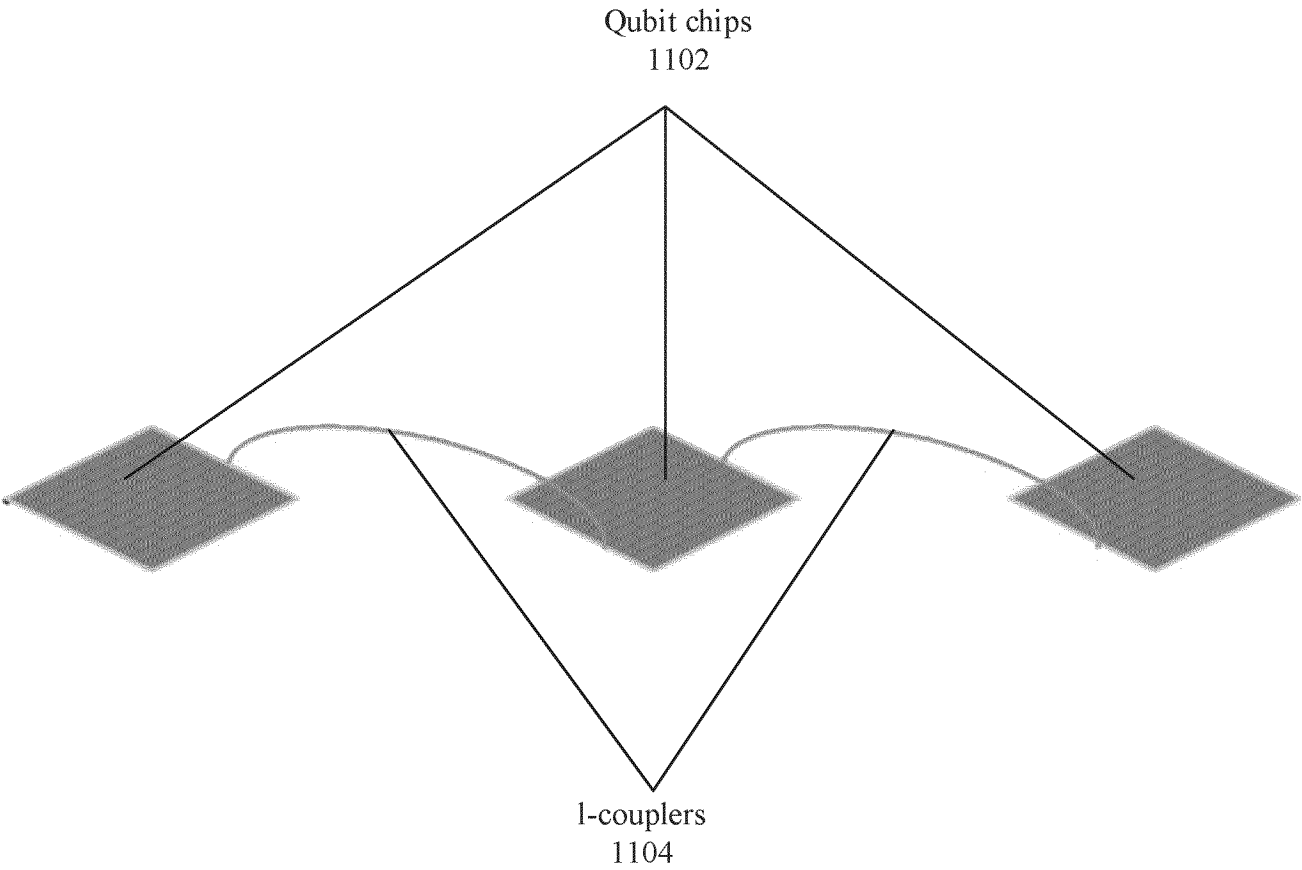


FIG. 11

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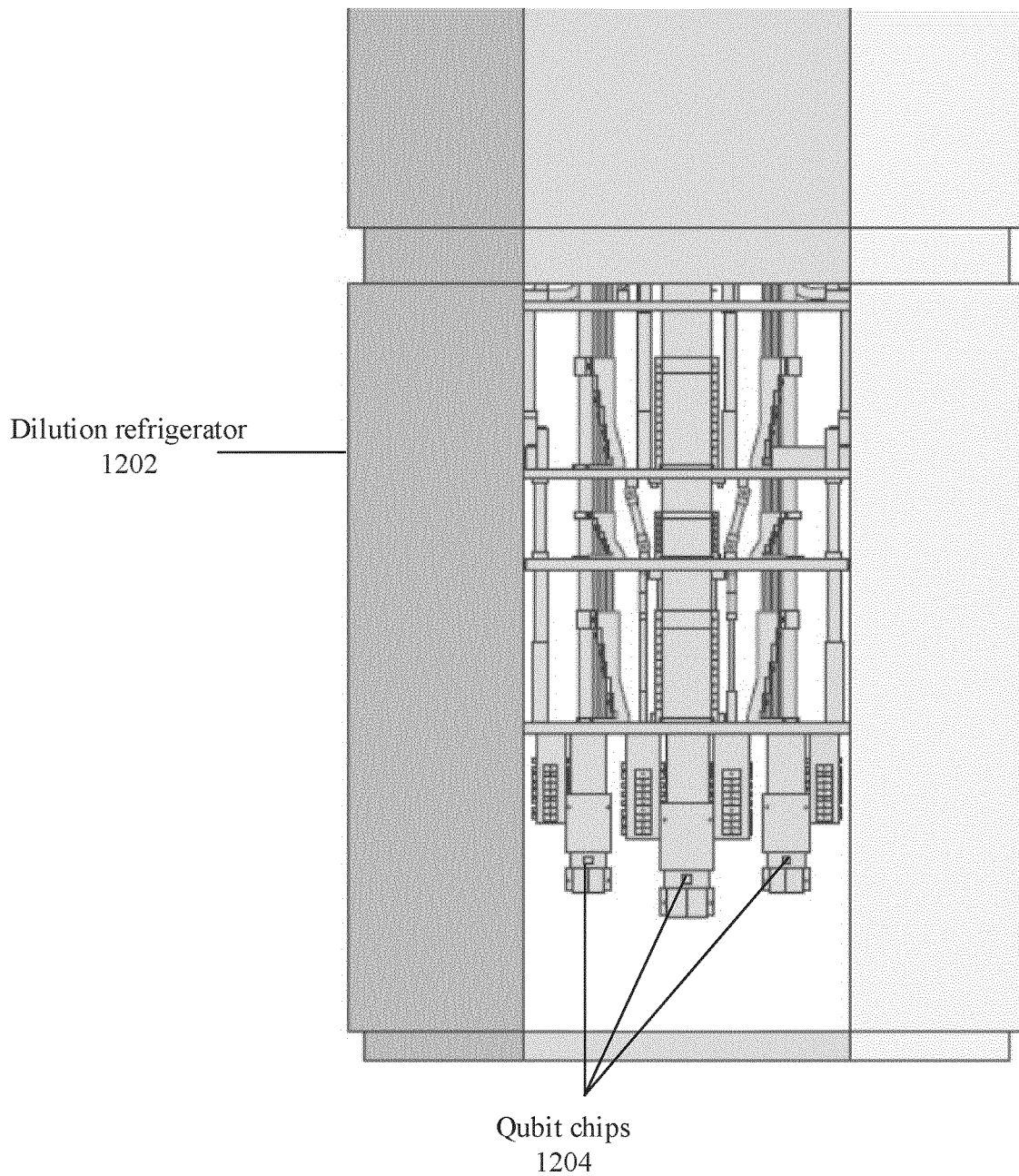


FIG. 12

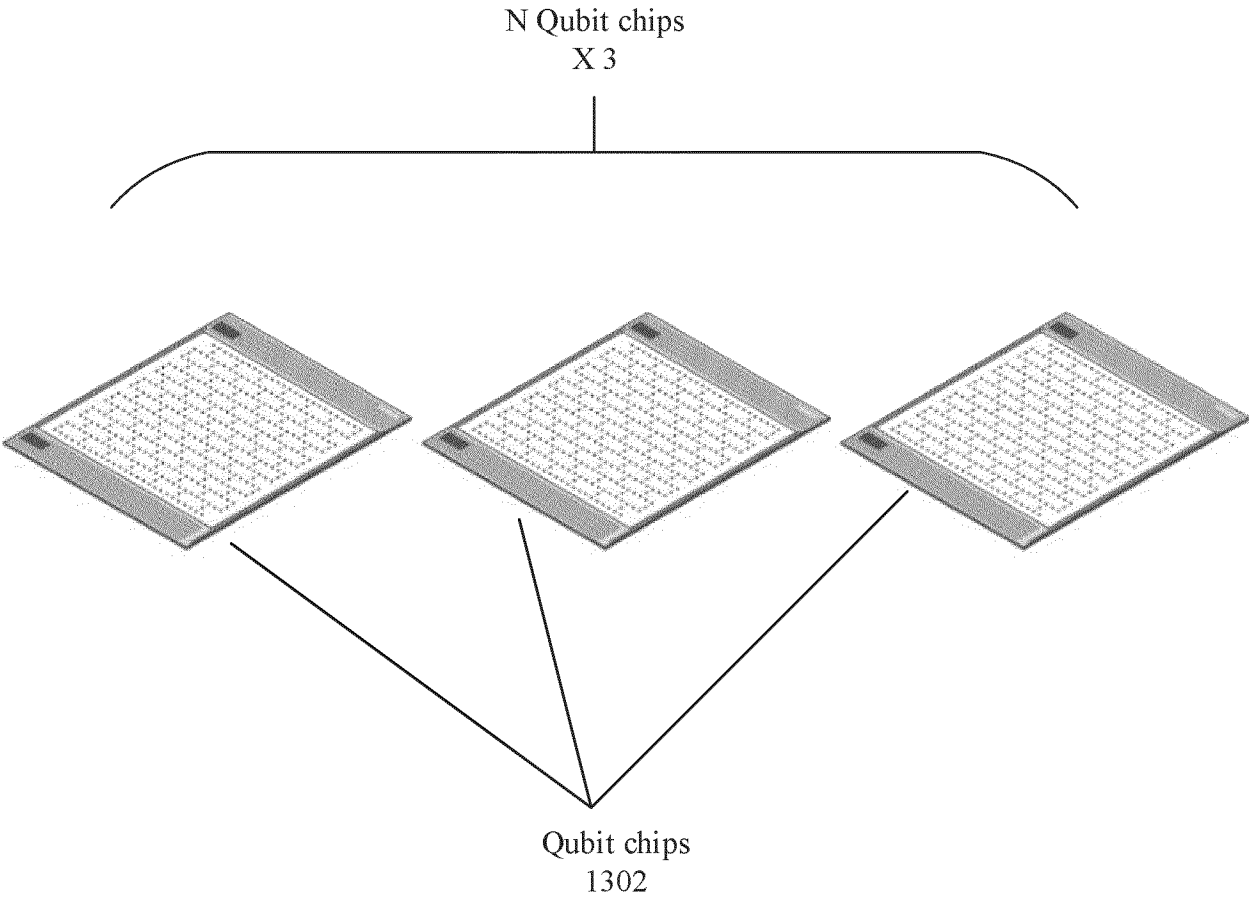


FIG. 13

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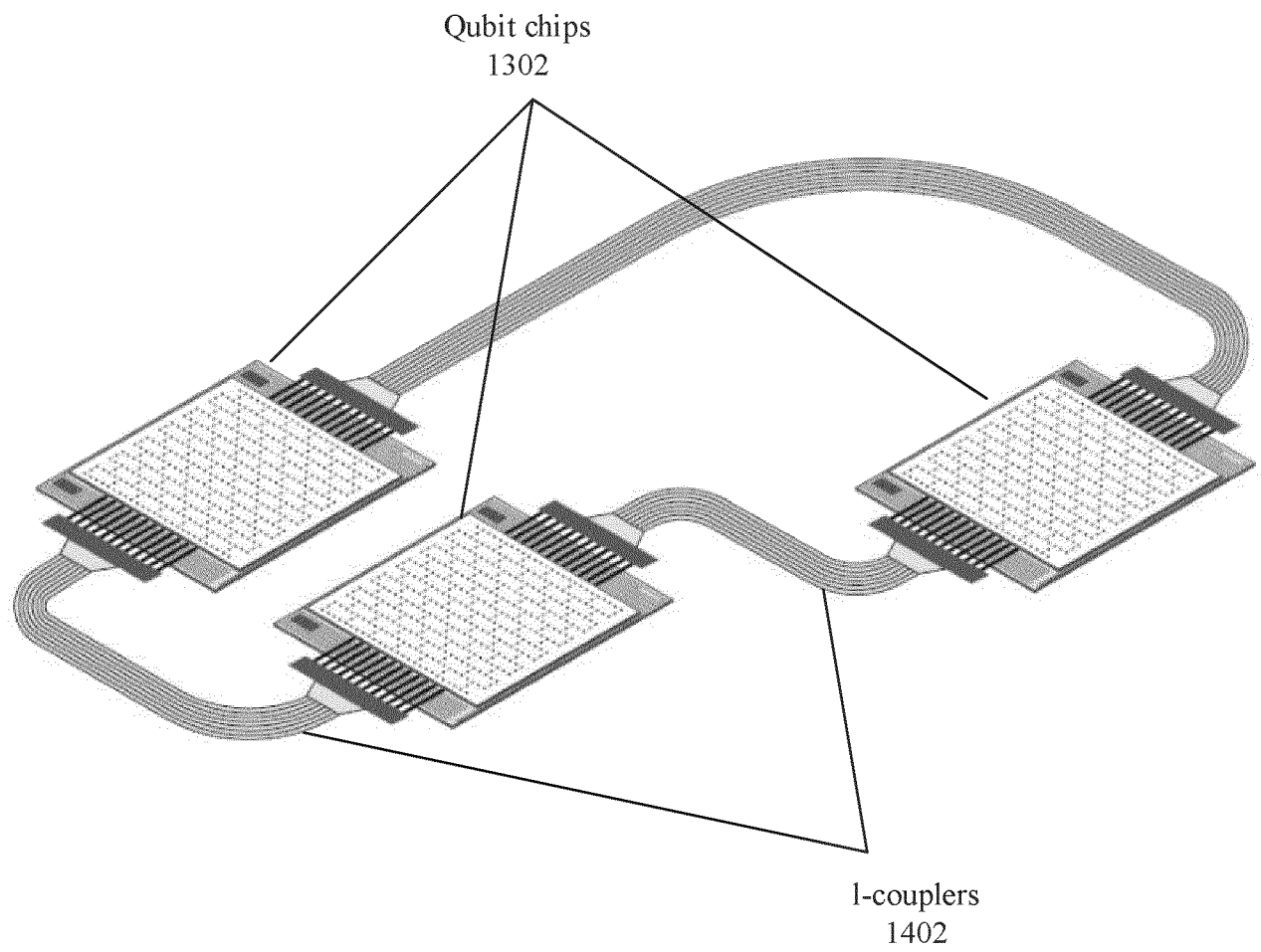


FIG. 14A

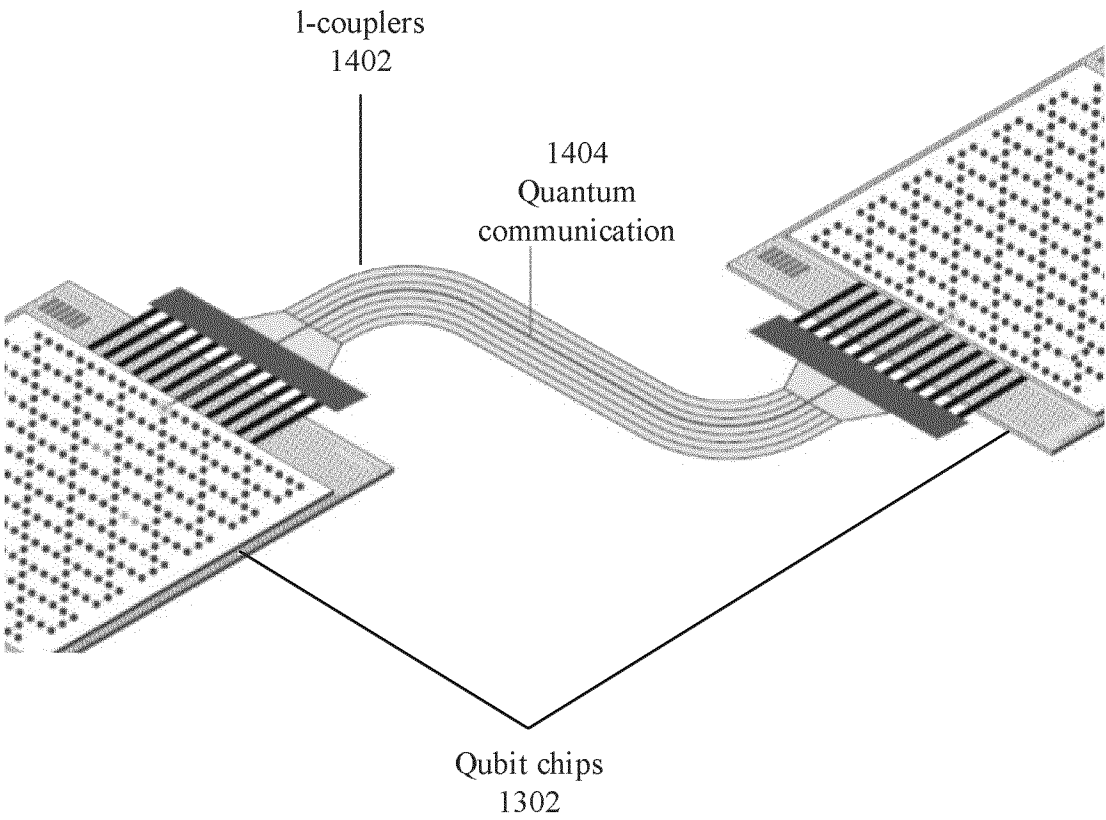


FIG. 14B

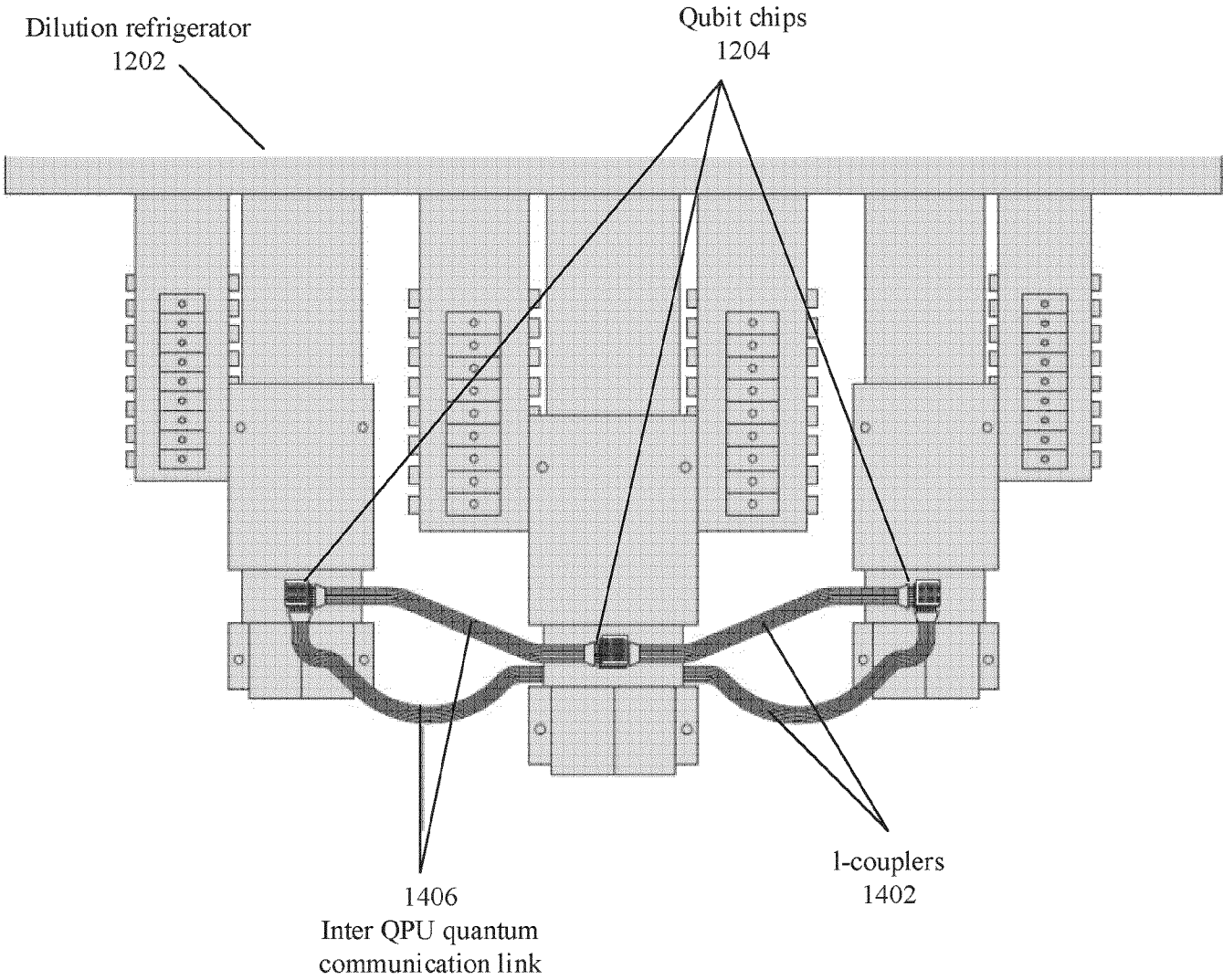


FIG. 14C

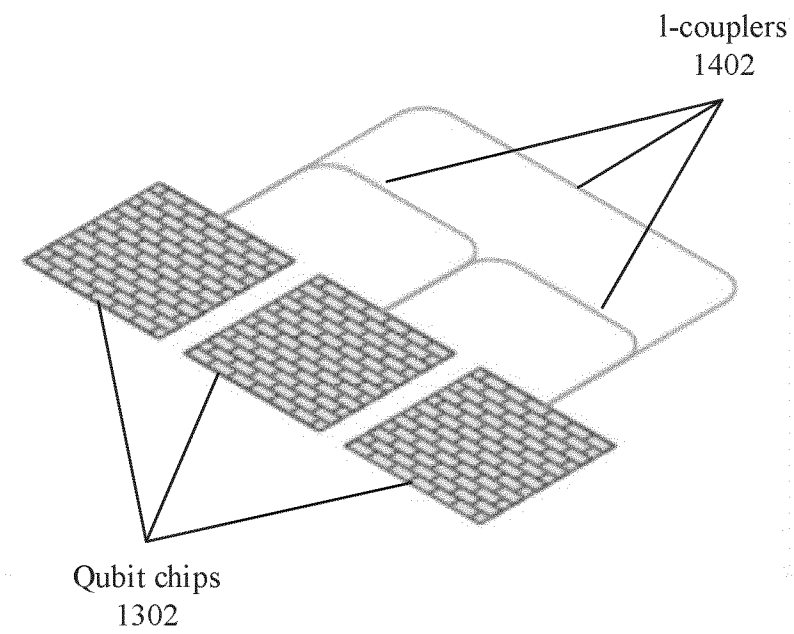


FIG. 15

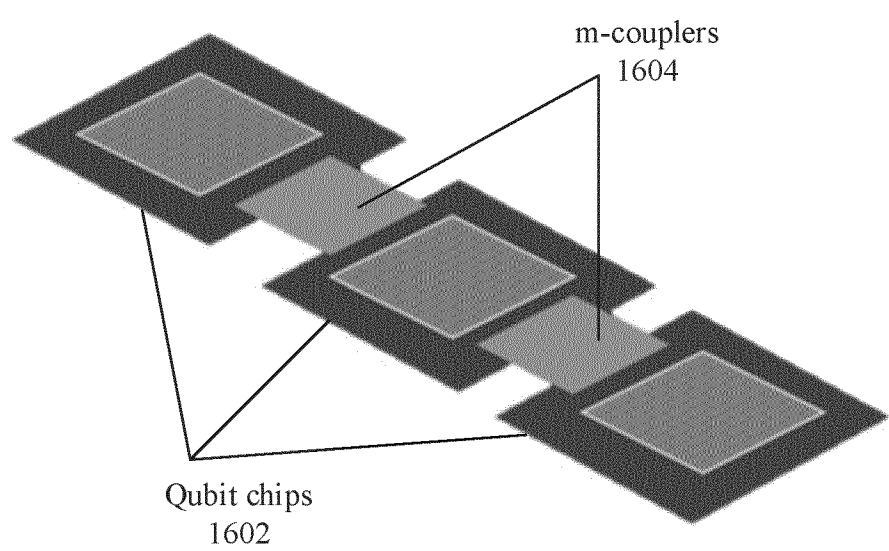


FIG. 16

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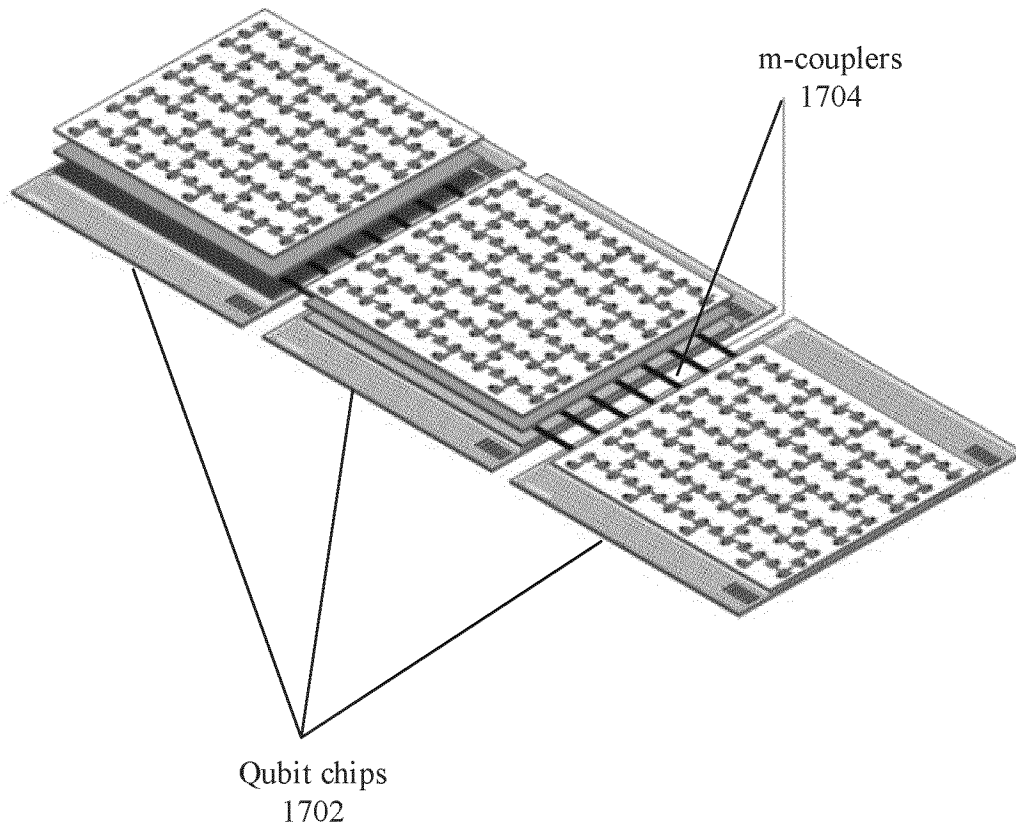


FIG. 17

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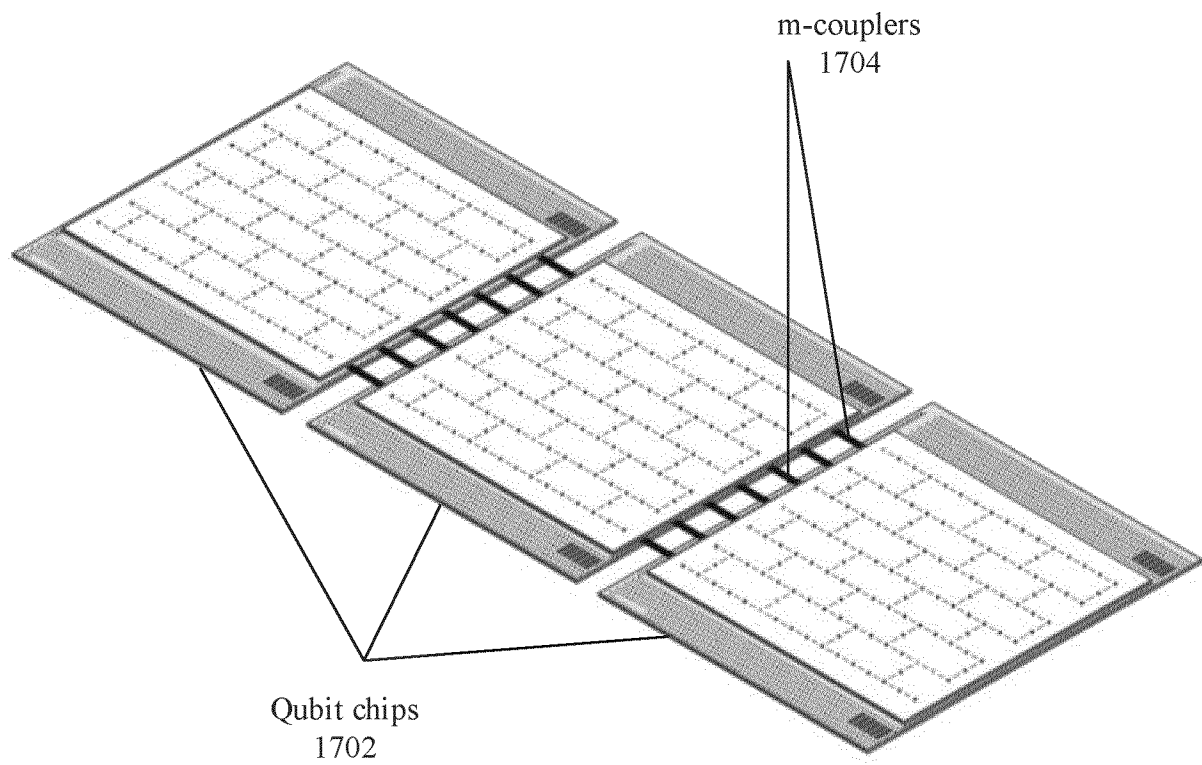


FIG. 18A

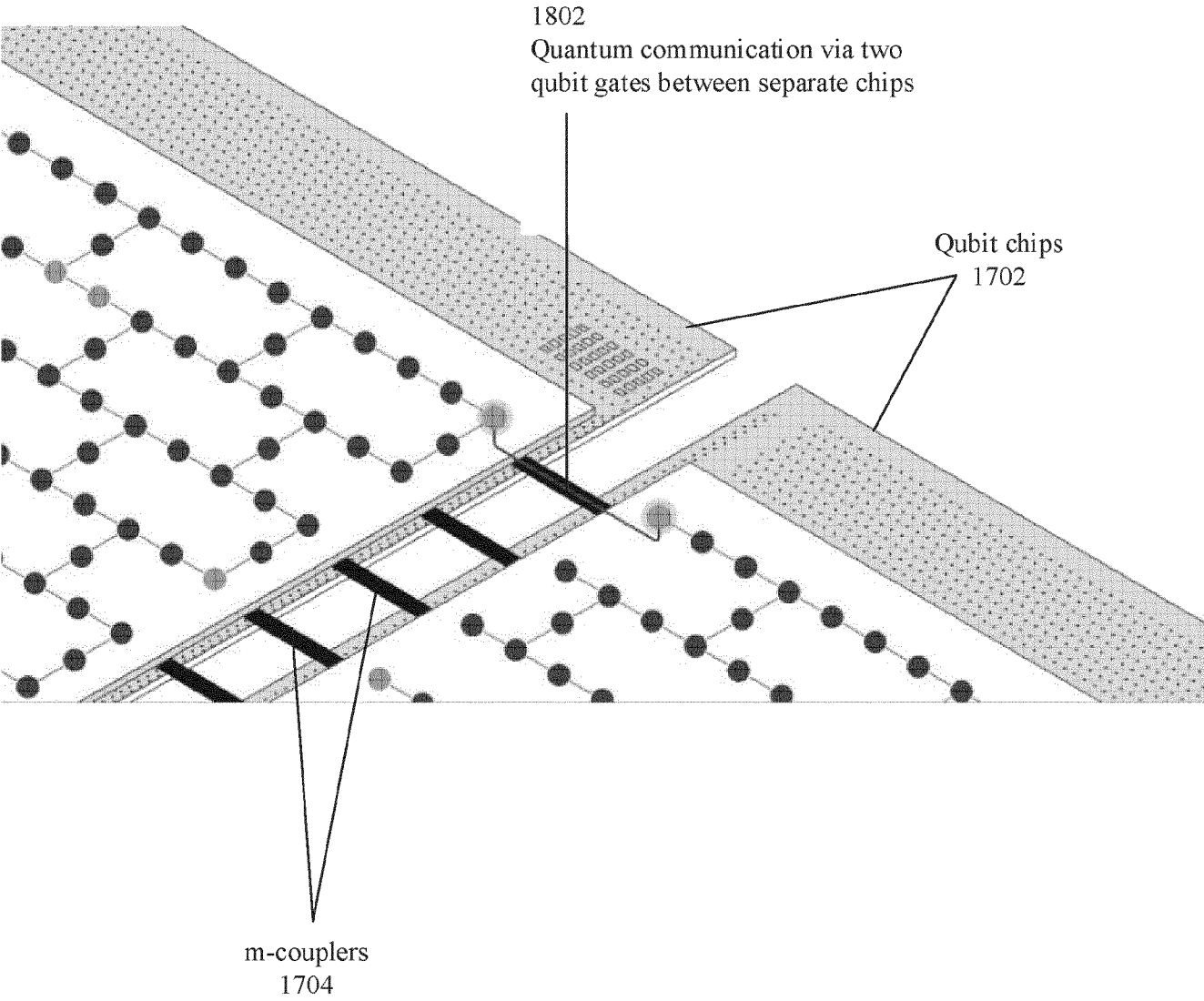


FIG. 18B

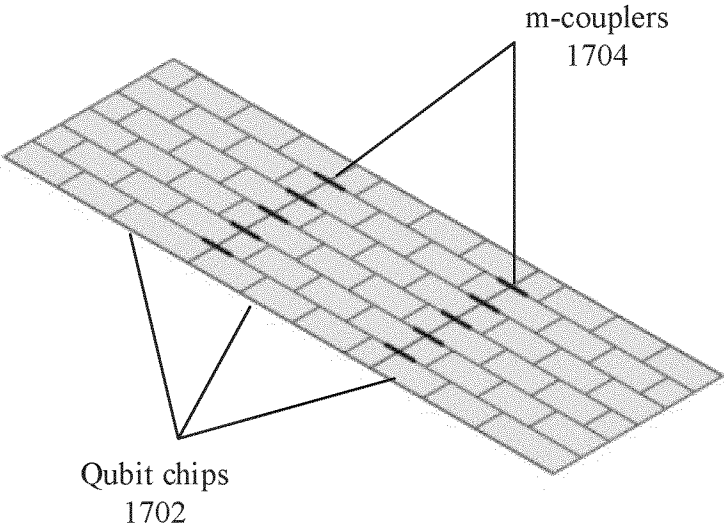


FIG. 19

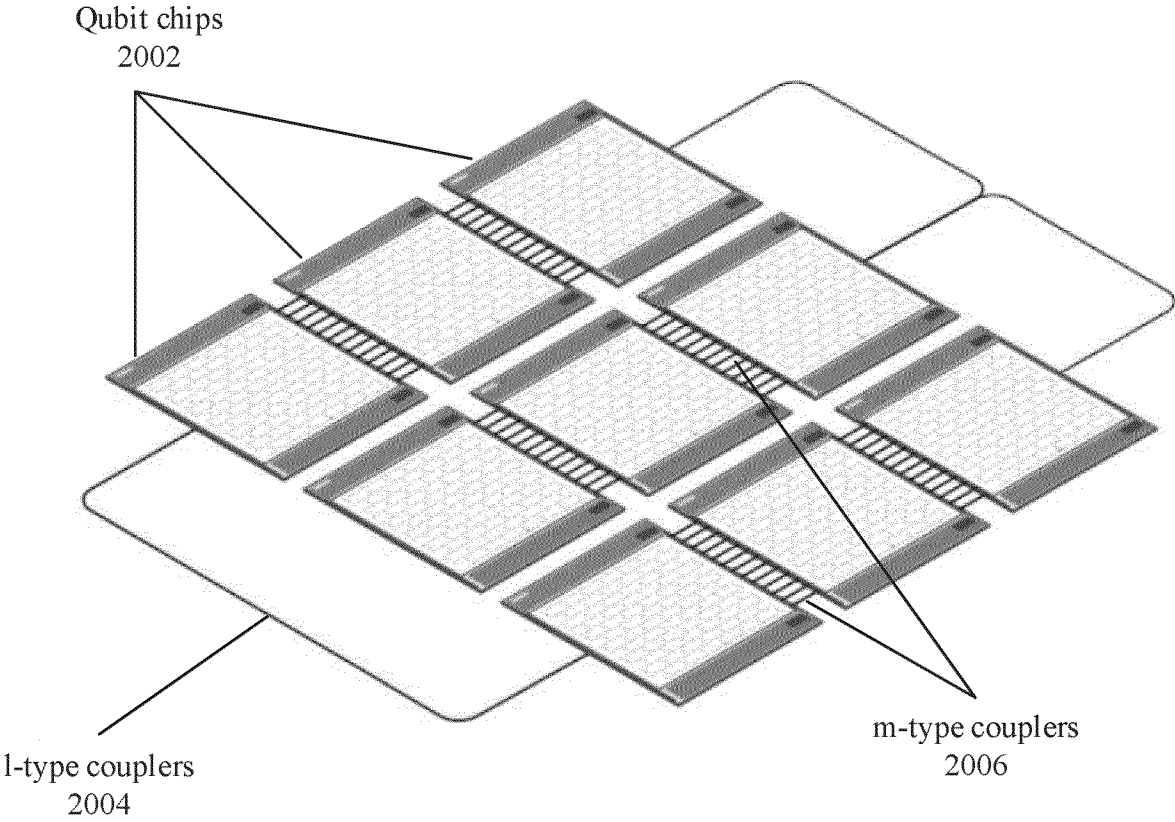


FIG. 20A

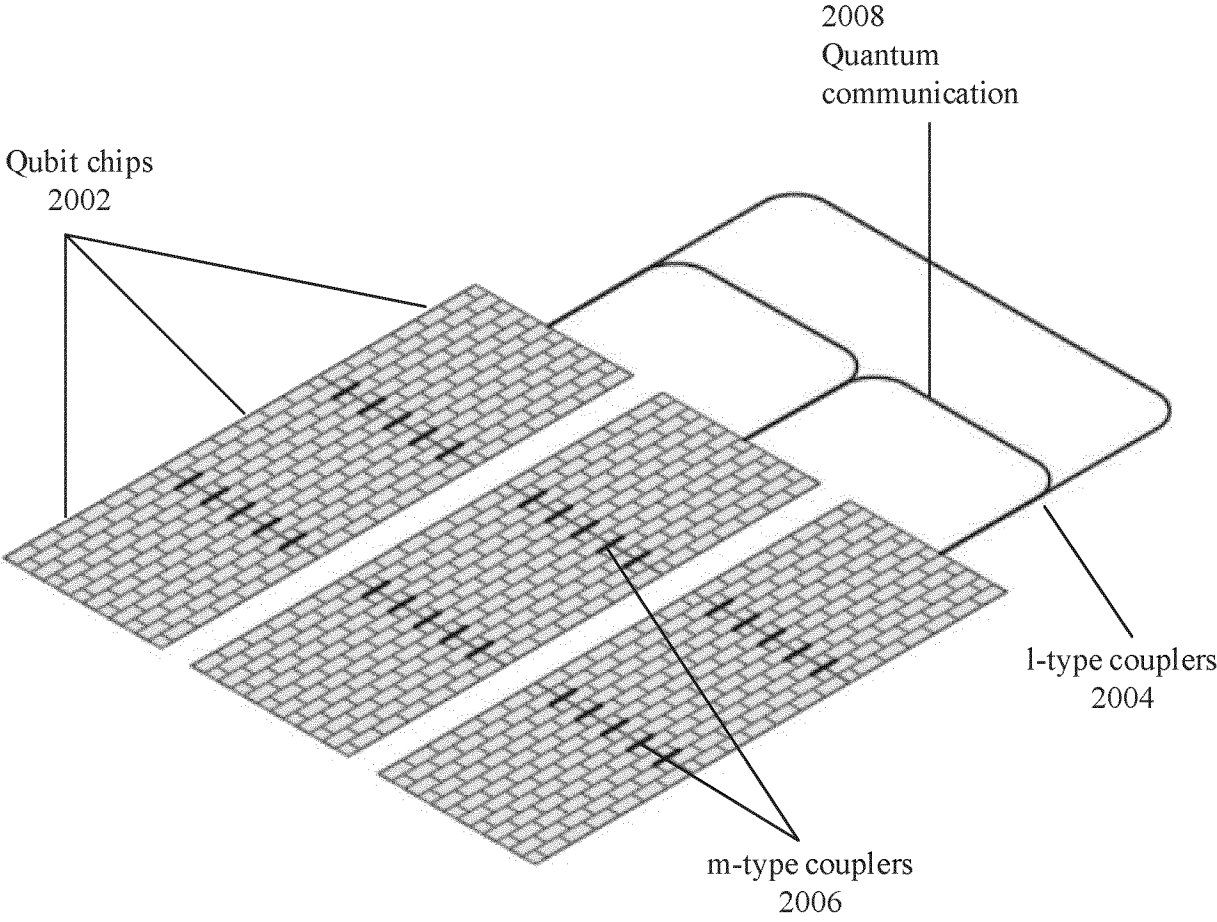


FIG. 20B

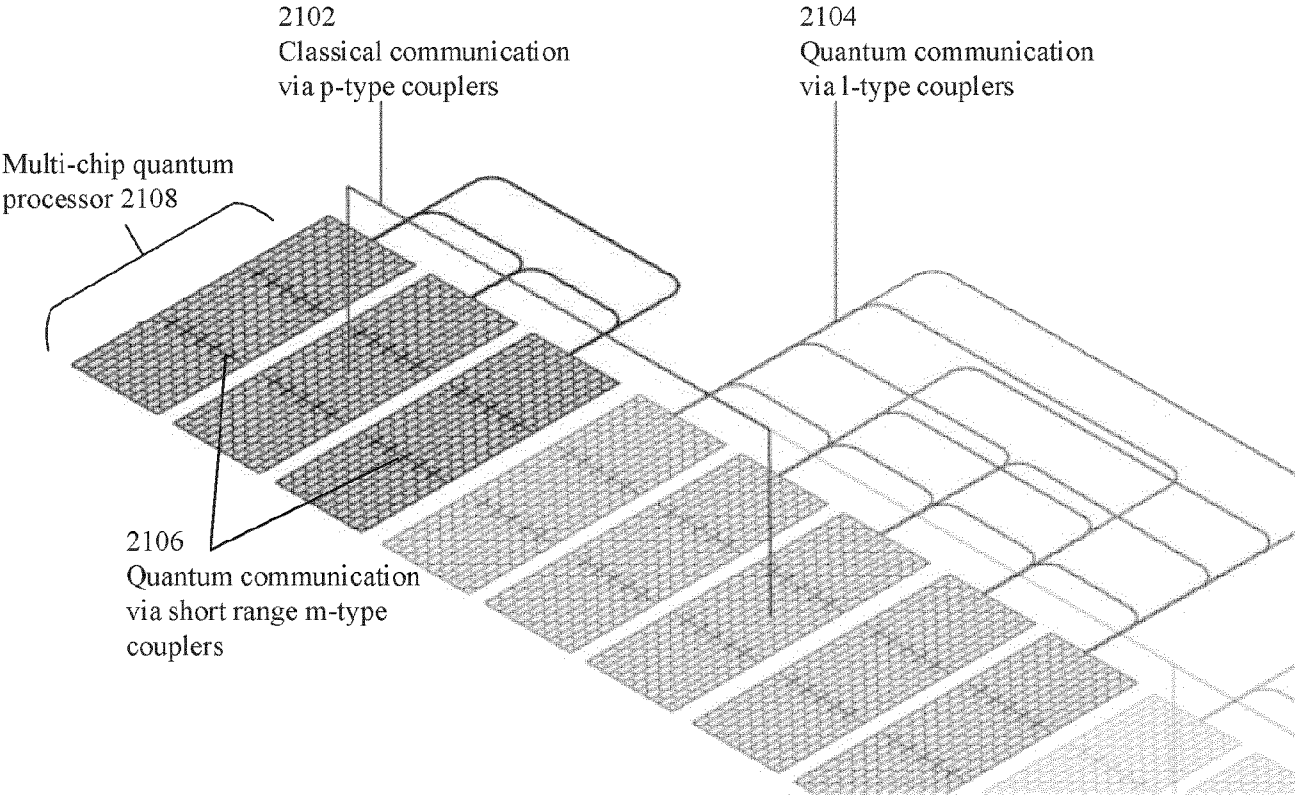


FIG. 21

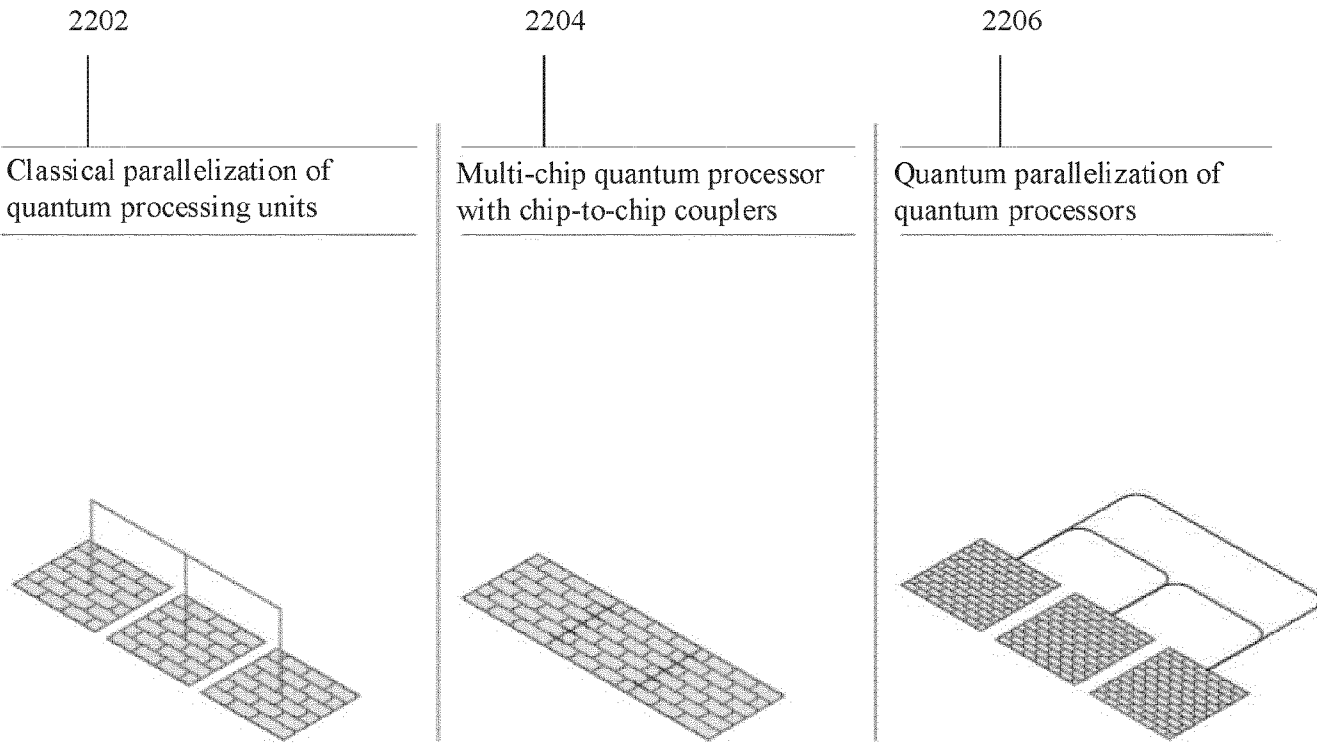


FIG. 22

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2300



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Coupling a plurality of at least qubits, buses, and readout structures using a plurality of couplers, wherein the plurality of couplers comprises at least two couplers selected from a group consisting of: classical couplers, short-range couplers, and long-range couplers, and wherein the plurality of at least qubits, buses and readout structures are comprised by one or more modules

FIG. 23

2400

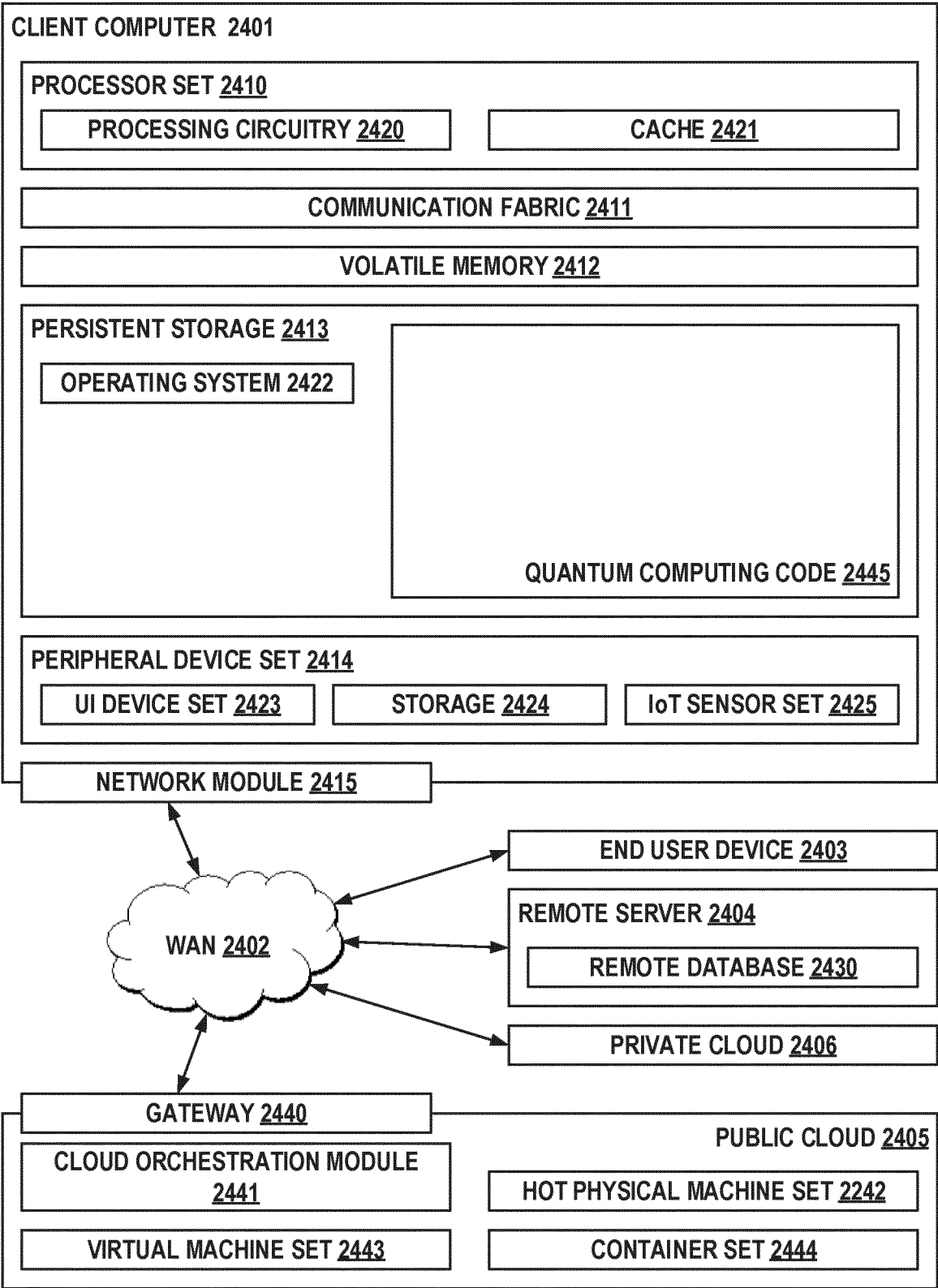


FIG. 24

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2023/062026**A. CLASSIFICATION OF SUBJECT MATTER****INV. G06N10/40****ADD.**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G06N G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 9 892 365 B2 (RIGETTI & CO INC [US]) 13 February 2018 (2018-02-13) figures 2, 3A, 21C, 22C, 23A, 28 claims 1, 2 column 1, line 41 - column 2, line 4 column 4, line 46 - line 48 column 7, line 36 - line 48 column 10, line 1 - line 2 column 14, line 42 - line 48 column 56, line 42 - line 56 column 65, line 4 - line 24 column 76, line 63 - line 67 ----- -/--	1-20



Further documents are listed in the continuation of Box C.



See patent family annex.

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Date of the actual completion of the international search

14 July 2023

Date of mailing of the international search report

24/07/2023

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European Patent Office, P.B. 5818 Patentlaan 2

NL - 2280 HV Rijswijk

Tel. (+31-70) 340-2040,

Fax: (+31-70) 340-3016

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INTERNATIONAL SEARCH REPORT

International application No

PCT/EP2023/062026

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 2022/038205 A1 (IBM [US]; IBM DEUTSCHLAND [DE]) 24 February 2022 (2022-02-24) figures 1A, 2, 3, 9-12 paragraph [0061] - paragraph [0062] paragraph [0055] - paragraph [0057] paragraph [0087] - paragraph [0088] paragraph [0106] - paragraph [0107] -----	1-20
A	PENG ZHAO ET AL: "Tunable coupling of widely separated superconducting qubits: A possible application towards a modular quantum device", ARXIV.ORG, CORNELL UNIVERSITY LIBRARY, 201 OLIN LIBRARY CORNELL UNIVERSITY ITHACA, NY 14853, 25 April 2022 (2022-04-25), XP091196372, the whole document -----	1-20

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/EP2023/062026

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