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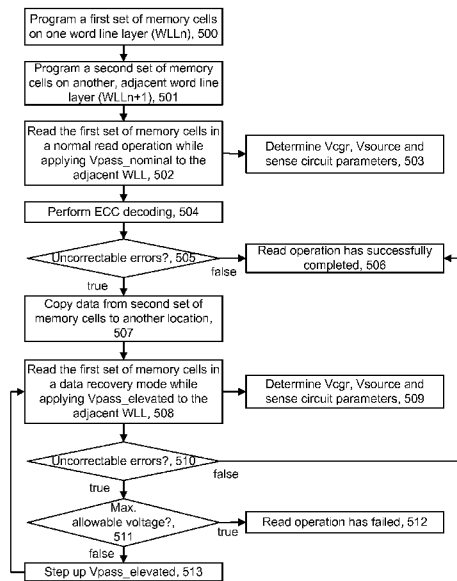
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[Continued on next page]

(54) Title: NEIGHBORING WORD LINE PROGRAM DISTURB COUNTERMEASURE FOR CHARGE-TRAPPING STACKED MEMORY

Fig. 5A



(57) Abstract: Techniques are provided for reading data from memory cells arranged along a common charge trapping layer, e.g., in a 3D stacked non-volatile memory device. Memory cells on a word line layer WLLn are disturbed by programming of memory cells on an adjacent word line layer WLLn+1, resulting in uncorrectable errors. The memory cells on WLLn can be read in a data recovery read operation which applies an elevated pass voltage to WLLn+1. The elevated pass voltage causes a decrease and narrowing of the threshold voltage distribution on WLLn which facilitates reading. The operation compensates for the lower threshold voltages by lowering the control gate voltage, raising the source voltage or adjusting a sensing period, demarcation level or pre-charge level in sensing circuitry. The elevated pass voltage can be stepped up in repeated read attempts until there are no uncorrectable errors or a limit is reached.

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## NEIGHBORING WORD LINE PROGRAM DISTURB COUNTERMEASURE FOR CHARGE-TRAPPING STACKED MEMORY

[0001] The present technology relates to techniques for reading memory cells in a 3D non-volatile memory device.

[0002] Recently, ultra high density storage devices have been proposed using a 3D stacked memory structure sometimes referred to as a Bit Cost Scalable (BiCS) architecture. For example, a 3D NAND stacked memory device can be formed from an array of alternating conductive and dielectric layers. A memory hole is drilled in the layers to define many memory layers simultaneously. A NAND string is then formed by filling the memory hole with materials including a charge trapping layer. A straight NAND string extends in one memory hole, while a pipe- or U-shaped NAND string (P-BiCS) includes a pair of vertical columns of memory cells which extend in two memory holes and which are joined by a bottom back gate. Control gates of the memory cells are provided by the conductive layers. However, various challenges are presented in operating such memory devices.

### BRIEF DESCRIPTION OF THE DRAWINGS

[0003] Like-numbered elements refer to common components in the different figures.

[0004] FIG. 1A is a perspective view of a 3D stacked non-volatile memory device.

[0005] FIG. 1B is a functional block diagram of the 3D stacked non-volatile memory device 100 of FIG. 1A.

[0006] FIG. 2A depicts a top view of a U-shaped NAND embodiment of a block 200, showing example SGD line subsets SGDL-SB0 and SGDL-SB1, as an example implementation of BLK0 in FIG. 1A.

[0007] FIG. 2B1 depicts the block 200 FIG. 2A, showing example word line subsets WL23D-SB and WL23S-SB and example bit line subsets BL-SB0 and BL-SB1.

[0008] FIG. 2B2 depicts the block 200 FIG. 2A, showing example sets of NAND strings 210-215.

[0009] FIG. 2C depicts an embodiment of a stack 230 showing a cross-sectional view of the portion 209 of the block 200 of FIG. 2A, along line 220.

[0010] FIG. 3A depicts a close-up view of the region 236 of the column C0 of FIG. 2C, showing example memory cells MC23D, MC22D, MC23S and MC22S.

[0011] FIG. 3B depicts a cross-sectional view along line 302 of FIG. 3A.

[0012] FIG. 3C depicts one embodiment of a circuit 301 in a 3D stacked non-volatile memory device.

[0013] FIG. 4A depicts a top view of a straight NAND string embodiment (block 480) of the block BLK0 of FIG. 1A, showing example SGD line subsets SGDL-SB0A and SGDL-SB1A.

[0014] FIG. 4B1 depicts the block BLK0 of FIG. 4A, showing an example WL line subset WL23-SB and example bit line subsets BL-SB0A and BL-SB1A.

[0015] FIG. 4B2 depicts the block BLK0 of FIG. 4A, showing example sets of NAND strings 216-219, 221 and 222.

[0016] FIG. 4C depicts a cross-sectional view of the portion 488 of the block 480 of FIG. 4A along line 486.

[0017] FIG. 5A depicts a process for programming and reading memory cells in a memory device.

[0018] FIG. 5B depicts an example of a programming operation consistent with step 500 of FIG. 5A.

[0019] FIGs. 6A and 6B depict a one pass programming operation with four data states consistent with FIG. 5B.

[0020] FIGs. 7A to 7C depict a two-pass programming operation with four data states consistent with FIG. 5B.

[0021] FIG. 8 depicts program and verify voltages in a programming operation, consistent with FIG. 5B.

[0022] FIG. 9A depicts a change in a  $V_t$  distribution of a first set of memory cells on a word line layer  $WLL_n$  after programming of an adjacent second set of memory cells on a word line layer  $WLL_{n+1}$ .

[0023] FIG. 9B depicts a change in a threshold voltage ( $V_t$ ) distribution of the first set of memory cells in a second read operation (a first data recovery read operation) which follows FIG. 9A.

[0024] FIG. 9C depicts a change in a  $V_t$  distribution of the first set of memory cells in a third read operation (a second data recovery read operation) which follows FIG. 9B.

[0025] FIG. 9D depicts the  $V_t$  distributions 703, 713, 723 and 733 of FIG. 9C aligned with the  $V_t$  distributions 700, 710, 720 and 730 of FIG. 9A.

[0026] FIG. 10A depicts a  $V_t$  distribution from test data of a first set of memory cells on  $WLL_n$  before and after programming of an adjacent second set of memory cells on  $WLL_{n+1}$ ,

where: (1) WLLn+1 is unprogrammed and Vpass\_nominal is used on WLLn+1 when WLLn is read, and (2) WLLn+1 is programmed and Vpass\_nominal is used on WLLn+1 when WLLn is read.

[0027] FIG. 10B depicts a close up view of a portion of the example memory cells MC22D and MC23D of FIG. 3B, showing electron injection in a charge trapping layer between memory cells.

[0028] FIG. 10C depicts a Vt distribution from test data of a second set of memory cells on WLLn+1 after programming to an all C state data pattern using: (3) a lower verify level (e.g., 4.5 V, see line 1030) and (4) a higher verify level (e.g., 5.5 V, see line 1031).

[0029] FIG. 10D depicts a Vt distribution from test data of a first set of memory cells on WLLn where: (5) WLLn+1 is unprogrammed and Vpass\_nominal is used on WLLn+1 when WLLn is read, (6) WLLn+1 is programmed using the low verify of case (3) and Vpass\_nominal is used on WLLn+1 when WLLn is read, and (7) WLLn+1 is programmed using the high verify of case (4) and Vpass\_nominal is used on WLLn+1 when WLLn is read.

[0030] FIG. 10E depicts a Vt distribution from test data of a first set of memory cells on WLLn where: (8) WLLn+1 is unprogrammed and Vpass\_nominal is used on WLLn+1 when WLLn is read, (9) WLLn+1 is programmed and Vpass\_nominal is used on WLLn+1 when WLLn is read, (10) WLLn+1 is unprogrammed and Vpass\_elevated is used on WLLn+1 when WLLn is read, and (11) WLLn+1 is programmed and Vpass\_elevated is used on WLLn+1 when WLLn is read.

[0031] FIG. 10F depicts a Vt distribution from test data of a first set of memory cells on WLLn where: (12) WLLn+1 is programmed and Vpass\_nominal is used on WLLn+1 when WLLn is read, (13) WLLn+1 is programmed and Vpass\_elevated is used on WLLn+1 when WLLn is read.

[0032] FIG. 10G depicts a Vt distribution from test data of a first set of memory cells on WLLn where: (14) WLLn+1 is unprogrammed and Vpass\_nominal is used on WLLn+1 when WLLn is read, (15) WLLn+1 is programmed and Vpass\_nominal is used on WLLn+1 when WLLn is read, and (16) WLLn+1 is programmed and Vpass\_elevated is used on WLLn+1 when WLLn is read, and the Vt distribution is aligned with the Vt distributions of cases (14) and (15).

[0033] FIG. 11A depicts a control gate voltage on WLLn as a function of time during a read operation for distinguishing four data states in a first set of memory cells on WLLn, consistent with FIG. 5A.

[0034] FIG. 11B depicts  $V_{pass\_elevated}$  on  $WLL_{n+1}$  and  $V_{pass\_nominal}$  on remaining unselected word line layers as a function of time during a read operation for a first set of memory cells on  $WLL_n$ , time-aligned with FIG. 11A, and consistent with FIG. 5A.

[0035] FIG. 11C depicts  $V_{pass\_elevated}$  on  $WLL_{n+1}$  during a second read operation (a first data recovery read operation) for a first set of memory cells on  $WLL_n$ , as a function of a number of errors during a first (normal) read operation, and consistent with FIG. 5A.

[0036] FIG. 11D depicts a step size for  $V_{pass\_elevated}$  during a data recovery read operation for a first set of memory cells on  $WLL_n$ , as a function of a number of errors during a previous read operation, and consistent with FIG. 5A.

[0037] FIG. 11E depicts  $V_{cgr}$  on  $WLL_n$  during a data recovery read operation for a first set of memory cells on  $WLL_n$ , as a function of  $V_{pass\_elevated}$ , and consistent with FIG. 5A.

[0038] FIG. 11F depicts  $V_{source}$  during a data recovery read operation for a first set of memory cells on  $WLL_n$ , as a function of  $V_{pass\_elevated}$ , and consistent with FIG. 5A.

[0039] FIG. 11G depicts a sensing period (SP) in sensing circuitry during a data recovery read operation as for a first set of memory cells on  $WLL_n$ , as a function of  $V_{pass\_elevated}$ , and consistent with FIG. 5A.

[0040] FIG. 11H depicts voltage demarcation level (DL) in sensing circuitry during a data recovery read operation for a first set of memory cells on  $WLL_n$ , as a function of  $V_{pass\_elevated}$ , and consistent with FIG. 5A.

[0041] FIG. 11I depicts pre-charge level (PL) in sensing circuitry during a data recovery read operation for a first set of memory cells on  $WLL_n$ , as a function of  $V_{pass\_elevated}$ , and consistent with FIG. 5A.

[0042] FIG. 11J depicts an optimum  $V_{cgr\_A}$  in a first read operation, an optimum  $V_{cgr\_A}$  in a second read operation, and a reference  $V_{cgr\_A}$  in the second read operation, consistent with FIG. 5A.

[0043] FIG. 11K depicts an adjustment to  $V_{pass\_elevated}$  step size as a function of delta  $V_{cgr\_A}$  in the second read operation, consistent with FIG. 11J.

[0044] FIG. 12A depicts a configuration of a NAND string and sensing circuitry when current sensing is used.

[0045] FIG. 12B depicts waveforms associated with FIG. 12A.

[0046] FIG. 12C depicts a sensing process which applies to the current sensing circuitry of FIG. 12A or the voltage sensing circuitry of FIG. 12A.

[0047] FIG. 12D depicts a voltage drop with time for different lines of fixed current.

[0048] FIG. 13A depicts a configuration of a NAND string and sensing circuitry when voltage sensing is used.

[0049] FIG. 13B depicts waveforms associated with FIG. 13A.

#### DETAILED DESCRIPTION

[0050] Techniques are provided for reading memory cells which are subject to program disturb due to the trapping of charge in a charge trapping layer between memory cells.

[0051] One example implementation involves reading cells in a 3D stacked non-volatile memory device. In such a memory device, memory cells are formed along memory holes which extend through alternating conductive layers (word line layers) and dielectric layers in a stack. The memory cells are typically arranged in NAND strings. The memory holes comprise a charge trapping layer which holds charges after a cell is programmed.

[0052] However, as such memory devices are scaled down in size, the distance (e.g., a vertical distance) between adjacent cells on a common charge trapping layer becomes smaller. As the spacing is reduced, a special type of program disturb referred to as neighboring word line program disturb becomes significant. With this disturb, a victim memory cell on an  $n$ th word line layer (WLL $n$ ) is disturbed by the programming of an adjacent memory cell. For example, the adjacent memory cell may be directly above the victim memory cell, e.g., on WLL $n+1$  and on the same NAND string. This disturb is caused by the high programming voltage ( $V_{pgm}$ ) used to program the memory cells on WLL $n+1$  to higher data states. For example, this can be the C state in a four state memory device which stores data in erased (E), A, B and C states. As another example, this can be the F and G states in an eight state memory device which stores data in erased (Er), A, B, C, D, E, F and G states. This programming results in a fringing field which injects electrons into a portion of the charge trapping layer which is between the adjacent memory cells. Moreover, electron injection can also be caused by the pass voltage which is applied to WLL $n$  when WLL $n+1$  is programmed. The trapped charges act as a parasitic cell which impairs the ability to read back data from the cells on WLL $n$ . Moreover, the cells on each word line layer can be disturbed in turn as each successive word line layer is programmed and parasitic cells are formed between each adjacent pair of cells along a common charge trapping layer.

[0053] Techniques provided herein address the above-mentioned issues. In one approach, the data stored in the cells can be coded using an error correction code (ECC). When the data is read, the ECC code is used to determine if there are uncorrectable errors. If there are one or

more uncorrectable errors, a data recovery read operation is used to attempt to recover the data. In this approach, the data on WLL<sub>n+1</sub> may first be copied to another location since it may be disturbed by the data recovery read operation. The data recovery read operation attempts to read the cells on WLL<sub>n</sub> while applying an elevated pass voltage on WLL<sub>n+1</sub>. The elevated pass voltage causes a decrease and narrowing of the V<sub>t</sub> distribution on WLL<sub>n</sub> which facilitates reading. The data recovery read operation compensates for the lower V<sub>t</sub> distribution by lowering the control gate voltage, raising the source voltage or adjusting a sensing period, demarcation level or pre-charge voltage level in sensing circuitry. The elevated pass voltage can be stepped up in repeated read attempts until there are no uncorrectable errors or a maximum allowable pass voltage is reached.

**[0054]** Advantages of the above-mentioned techniques include providing the ability to read data which has been subject to program disturb.

**[0055]** The following discussion provides details of the construction of a memory device and of related programming and sensing techniques which address the above-mentioned issues.

**[0056]** FIG. 1A is a perspective view of a 3D stacked non-volatile memory device. The memory device 100 includes a substrate 101. On the substrate are example blocks BLK0 and BLK1 of memory cells and a peripheral area 104 with circuitry for use by the blocks. The substrate 101 can also carry circuitry under the blocks, along with one or more lower metal layers which are patterned in conductive paths to carry signals of the circuitry. The blocks are formed in an intermediate region 102 of the memory device. In an upper region 103 of the memory device, one or more upper metal layers are patterned in conductive paths to carry signals of the circuitry. Each block comprises a stacked area of memory cells, where alternating levels of the stack represent word lines. In one possible approach, each block has opposing tiered sides from which vertical contacts extend upward to an upper metal layer to form connections to conductive paths. While two blocks are depicted as an example, additional blocks can be used, extending in the x- and/or y-directions.

**[0057]** In one possible approach, the length of the plane, in the x-direction, represents a direction in which signal paths to word lines extend in the one or more upper metal layers (a word line or SGD line direction), and the width of the plane, in the y-direction, represents a direction in which signal paths to bit lines extend in the one or more upper metal layers (a bit line direction). The z-direction represents a height of the memory device.

**[0058]** FIG. 1B is a functional block diagram of the 3D stacked non-volatile memory device 100 of FIG. 1A. The memory device 100 may include one or more memory die 108.



The memory die 108 includes a 3D (three-dimensional) stacked memory array or structure 126 of memory cells, e.g., including the blocks BLK0 and BLK1, control circuitry 110, and read/write circuits 128. The memory array 126 is addressable by word lines via a row decoder 124 and by bit lines via a column decoder 132. The read/write circuits 128 include multiple sense blocks 130 (sensing circuitry) and allow a page of memory cells to be read or programmed in parallel. Typically a controller 122 is included in the same memory device 100 (e.g., a removable storage card) as the one or more memory die 108. Commands and data are transferred between the host and controller 122 via lines 120 and between the controller and the one or more memory die 108 via lines 118.

**[0059]** The control circuitry 110 cooperates with the read/write circuits 128 to perform memory operations on the memory array 126, and includes a state machine 112, an on-chip address decoder 114, and a power control module 116. The state machine 112 provides chip-level control of memory operations. The on-chip address decoder 114 provides an address interface between that used by the host or a memory controller to the hardware address used by the decoders 124 and 132. The power control module 116 controls the power and voltages supplied to the word lines and bit lines during memory operations. It can include drivers for WLLs, drain- and source-side select gate drivers (referring, e.g., to drain- and source-sides or ends of a string of memory cells such as a NAND string, for instance) and source lines. The sense blocks 130 can include bit line drivers, in one approach.

**[0060]** A storage location 113 may be provided for read parameters. As described further below, this can include pass voltages for unselected word lines, control gate read voltages,  $V_{source}$  and parameters in a sensing circuitry such as sensing period, demarcation level or pre-charge level. The read parameters can also be used to implement the plots of FIG. 11B-11K. The read parameters can include data which is predetermined and data which is determined at the time of a read operation. The storage locations may use ROM fuses or data registers, for example, for the predetermined data.

**[0061]** In some implementations, some of the components can be combined. In various designs, one or more of the components (alone or in combination), other than memory array 126, can be thought of as at least one control circuit. For example, a control circuit may include any one of, or a combination of, control circuitry 110, state machine 112, decoders 114/132, power control module 116, sense blocks 130, read/write circuits 128, and controller 122, and so forth.

[0062] In another approach, a non-volatile memory system uses dual row/column decoders and read/write circuits. Access to the memory array 126 by the various peripheral circuits is implemented in a symmetric fashion, on opposite sides of the array, so that the densities of access lines and circuitry on each side are reduced by half. Thus, the row decoder is split into two row decoders and the column decoder into two column decoders. Similarly, the read/write circuits are split into read/write circuits connecting to bit lines from the bottom and read/write circuits connecting to bit lines from the top of the memory array 126. In this way, the density of the read/write modules is reduced by one half.

[0063] Other types of non-volatile memory in addition to NAND flash memory can also be used.

[0064] FIG. 2A depicts a top view of a U-shaped NAND embodiment of a block 200, showing example SGD line subsets SGDL-SB0 and SGDL-SB1, as an example implementation of BLK0 in FIG. 1A. The view is of a representative layer among the multiple WLLs in a stack. Referring also to FIG. 2C, the stack includes alternating dielectric and conductive layers. The dielectric layers include D0 to D25 and may be made of SiO<sub>2</sub>, for instance. The conductive layers include BG, which is a back gate layer, WLL0 to WLL23, which are conductive paths to control gates of the memory cells at the layer, and SG, which is a select gate layer, e.g., a conductive path to control gates of select gate transistors of NAND strings. FIG. 2A may represent any one of WLL0 to WLL23, for instance, in an example with twenty-four WLLs. The conductive layers may include doped polysilicon, metal silicide or a metal, for instance. An example voltage of 5-10 V may be applied to the back gate to maintain a conductive state which connects the drain- and source-side columns.

[0065] For each block, the WLL is divided into two portions 202 and 204. Each block includes a slit pattern. A slit is a void which extends vertically in the stack, typically from an etch stop layer at the bottom to at least a top layer of the stack. The slit can be filled with insulation to insulate words line layer portions from one another. A slit 206 is a single continuous slit which extends in a zig-zag pattern in the block so that the block is divided into two portions, 202 and 204, which are insulated from one another. This approach can provide greater flexibility in controlling the memory cells since the WLL portions can be driven independently.

[0066] Each block includes rows of columnar, e.g., vertical, memory holes or pillars, represented by circles. Each row represents a vertical group of columns in the figure. The memory holes extend vertically in the stack and include memory cells such as in a vertical

NAND string. Example columns of memory cells along a line 220 include C0 to C11. The figure represents a simplification, as many more rows of memory holes will typically be used, extending to the right and left in the figure. Also, the figures are not necessarily to scale. The columns of memory cells can be arranged in subsets such as sub-blocks.

[0067] Subsets of memory cells can be of different types, such as WL subsets, SGD line subsets and BL subsets.

[0068] A portion 209 of the block is depicted in further detail in connection with FIG. 2C.

[0069] FIG. 2B1 depicts the block 200 FIG. 2A, showing example word line subsets WL23D-SB and WL23S-SB and example bit line subsets BL-SB0 and BL-SB1. This example assumes that the WLL23 layer is depicted. WLL23S-SB is a WLL portion in communication with one memory cell in the source-side of each U-shaped NAND string, and WLL23D-SB is a WLL portion in communication with one memory cell in the drain-side of each U-shaped NAND string.

[0070] When U-shaped NAND strings are used, each SGD line subset can include two adjacent rows of columns of memory cells. In a subset, the adjacent rows are separated by the slit. The columns of memory cells on one side of the slit are drain-side columns (e.g., C0, C3, C4 and C7 in FIG. 2C) of NAND strings, and the columns of memory cells on the other side of the slit are source-side columns (e.g., C1, C2, C5 and C6 in FIG. 2C) of the NAND strings. Note that the pattern of two source-side columns between two drain-side columns repeats in the y-direction.

[0071] Word line drivers can independently provide signals such as voltage waveforms to the WLL portions 202 and 204.

[0072] The drawings are not to scale and do not show all memory columns. For example, a more realistic block might have twelve memory columns in the y direction as shown, but a very large number such as 32k memory columns in the x direction, for a total of 384k memory columns in a block. With U-shaped NAND strings, 192k NAND strings are provided in this example. With straight NAND strings, 384k NAND strings are provided in this example. Assuming there are twenty-four memory cells per column, there are  $384k \times 24 = 9,216k$  memory cells in the set. Sets of NAND strings 210-215 are also depicted.

[0073] FIG. 2B2 depicts the block 200 FIG. 2A, showing example sets of NAND strings 210-215. The set of NAND strings 210 includes an example NAND string NS0, such as depicted in FIG. 2B5 and example memory cells MCD23-0, MCD23-1, MCD23-2, ..., MCD23-14, as depicted in FIG. 2B6. In this notation, "MC" denotes a memory cell, "D"

denotes a drain side of the NAND strings, and the number (0,1,2,...,14) denotes a number of the NAND string based on its position in the stack. NAND strings NS0, NS0-1, NS0-2,..., NS0-14 are also depicted.

**[0074]** FIG. 2C depicts an embodiment of a stack 230 showing a cross-sectional view of the portion 209 of the block 200 of FIG. 2A, along line 220. In one approach, the WLLs have a uniform thickness and the memory holes have another uniform thickness. Lcg represents a control gate length for the memory cells, which is the same as the thickness or height of each WLL. Columns of memory cells C0 to C7 are depicted in the multi-layer stack. The stack 230 includes the substrate 101, an insulating film 250 on the substrate, and a back gate layer BG, which is a conductive layer, on the insulating film. A trench is provided in portions of the back gate below pairs of columns of memory cells of a U-shaped NAND string. Layers of materials which are provided in the columns to form the memory cells are also provided in the trenches, and the remaining space in the trenches is filled with a semiconductor material to provide connecting portions 263 to 266 which connect the columns. The back gate thus connects the two columns of each U-shaped NAND string. For example, NS0 (NS=NAND string) includes columns C0 and C1 and connecting portion 263, and has a drain end 232 and a source end 240. NS1 includes columns C2 and C3 and connecting portion 264, and has a drain end 244 and a source end 242. NS2 includes columns C4 and C5 and connecting portion 265. NS3 includes columns C6 and C7 and connecting portion 266.

**[0075]** MH0, corresponding to C0, is depicted for reference. The memory hole is shown as becoming progressively and gradually narrower from the top 237 to the bottom 238 of the stack. The memory holes are columnar and extend at least from a top word line layer (WLL23) of the plurality of WLLs to a bottom word line layer (WLL0) of the plurality of WLLs.

**[0076]** The source line SL0 is connected to the source ends 240 and 242 of two adjacent memory strings NS0 and NS1. SL0 is also connected to other sets of memory strings which are behind NS0 and NS1 in the x direction. Additional U-shaped NAND strings in the stack 230 (e.g., NS0-1, NS0-2,..., NS0-14 from FIG. 2B6) extend behind the U-shaped NAND strings depicted in the cross-section, e.g., along the x-axis, in a SGD line direction. The U-shaped NAND strings NS0 to NS3 are each in a different SGD line subset, but are in a common BL subset.

**[0077]** The slit 206 from FIG. 2A is also depicted as an example. In the cross-section, multiple slit portions are seen, where each slit portion is between the drain- and source-side columns of a U-shaped NAND string. A portion of the bit line BL0 is also depicted.

[0078] A region 236 of the stack is shown in greater detail in FIG. 3A.

[0079] Word line layers WLL0-WLL23 and dielectric layers D0-D24 extend alternately in the stack. The SG layer is between D24 and D2. Each WLL has a drain-side portion and a source-side portion. For example, WL23S-SB is a source-side sub-block of WLL23, and WL23D-SB is a drain-side sub-block of WLL23, consistent with FIG. 2B1. In each WLL, the diagonal line patterned region represents the source-side sub-block, and the unpatterned region represents the drain-side sub-block.

[0080] FIG. 3A depicts a close-up view of the region 236 of the column C0 of FIG. 2C, showing example memory cells MC23D, MC22D, MC23S and MC22S. The region also shows portions D24D and D24S of the dielectric layer D24, portions D23D and D23S of the dielectric layer D23, and portions D22D and D22S of the dielectric layer D22. The region also shows portions WLL24D and WLL24S of the conductive layer WLL24, portions WLL23D and WLL23S of the conductive layer WLL23, and portions WLL22D and WLL22S of the conductive layer WLL22.

[0081] A number of layers can be deposited along the sidewalls of the column and within each word line layer. These layers can include oxide-nitride-oxide (O-N-O) and polysilicon layers which are deposited, e.g., using atomic layer deposition. For example, the column includes a charge trapping layer or film (CTL) 297 such as SiN or other nitride, a tunnel oxide (TNL) 298, a polysilicon body or channel (CH) 299, and a core filler dielectric 300. The word line layer includes a block oxide (BOX) 296, a block high-k material 295, a barrier metal 294, and a conductive metal such as W 293. In another approach, all of these layers except the W are provided in the column. Additional memory cells are similarly formed throughout the columns.

[0082] When a memory cell is programmed, electrons are stored in a portion of the CTL which is associated with the memory cell. These electrons are drawn into the CTL from the channel, and through the TNL. The  $V_{th}$  of a memory cell is increased in proportion to the amount of stored charge. See also FIG. 10B.

[0083] Each respective memory cell of the first set of memory cells is adjacent to, and is arranged along a common charge trapping layer with, a respective memory cell of the second set of memory cells. For example, MC23D is adjacent to, and is arranged along a common charge trapping layer 297 with, MC22D. Also, MC23S is adjacent to, and is arranged along a common charge trapping layer 297 with, MC22S.

[0084] FIG. 3B depicts a cross-sectional view along line 302 of FIG. 3A. Each layer is ring-shaped in one possible approach, except the core filler, which is a cylinder.

[0085] FIG. 3C depicts one embodiment of a circuit 301 in a 3D stacked non-volatile memory device. As a simplification, four memory cells are provided per column.

[0086] NAND strings NS0, NS1, NS2 and NS3 are in communication with a bit line BL0, and NAND strings NS0A, NS1A, NS2A and NS3A are in communication with a bit line BL1. In this example, each NAND string has a drain-side column with four memory cells and a SGD transistor, and a source-side column with four memory cells and a SGS transistor. The filled in circles indicate control gates of the select transistor and the memory cells on the drain side of a NAND string. The open circles indicate control gates of the select transistor and the memory cells on the source side of a NAND string.

[0087] For example, NS0 has a drain side column C0D comprising memory cells M00, M01, M02 and M03 and an SGD transistor SGD0, and a source side column C0S comprising memory cells M10, M11, M12 and M13 and an SGS transistor SGS0. NS1 has a drain side comprising memory cells M30, M31, M32 and M33 and an SGD transistor SGD1, and a source side comprising memory cells M20, M21, M22 and M23 and an SGS transistor SGS1. NS2 has a drain side comprising memory cells M40, M41, M42 and M43 and an SGD transistor SGD2, and a source side comprising memory cells M50, M51, M52 and M53 and an SGS transistor SGS2. NS3 has a drain side comprising memory cells M70, M71, M72 and M73 and an SGD transistor SGD3, and a source side comprising memory cells M60, M61, M62 and M63 and an SGS transistor SGS3.

[0088] Similarly, NS0A has a drain side comprising memory cells M00A, M01A, M02A and M03A and an SGD transistor SGD0A, and a source side comprising memory cells M10A, M11A, M12A and M13A and an SGS transistor SGS0A. NS1A has a drain side comprising memory cells M30A, M31A, M32A and M33A and an SGD transistor SGD1A, and a source side comprising memory cells M20A, M21A, M22A and M23A and an SGS transistor SGS1A. NS2A has a drain side comprising memory cells M40A, M41A, M42A and M43A and an SGD transistor SGD2A, and a source side comprising memory cells M50A, M51A, M52A and M53A and an SGS transistor SGS2A. NS3A has a drain side comprising memory cells M70A, M71A, M72A and M73A and an SGD transistor SGD3A, and a source side comprising memory cells M60A, M61A, M62A and M63A and an SGS transistor SGS3A.

[0089] Each NAND string has a back gate (BG0 for NS0, BG1 for NS1, BG2 for NS2, BG3 for NS3, BG0A for NS0A, BG1A for NS1A, BG2A for NS2A, BG3A for NS3A). The control gates of all of the back gates in the circuit may be connected to one another.

[0090] In one approach, the source side of each SGS transistor is connected to a common source line of the circuit.

[0091] A sets of memory cells includes cells that can be programmed or read together. For example, a set of memory cells can include cells connected to a common word line layer (WLL) portion and to a common SGD line. For example, Set0 includes cells M00-M00A, Set1 includes cells M01-M01A, Set2 includes cells M02-M02A, and Set3 includes cells M03-M03A.

[0092] At each level of the circuit, the control gates of the drain-side memory cells are connected to one another by a common WLL. For example, at the top WLL, M03, M03A, M33, M33A, M43, M43A, M73 and M73A have control gates connected by a word line layer. Similarly, the control gates of the source-side memory cells are connected to one another by a common WLL. For example, at the top WLL, M13, M13A, M23, M23A, M53, M53A, M63 and M63A have control gates connected by a word line layer.

[0093] Additionally, control gates of the SGD transistors are connected to one another. For example, control gates of SGD0, ..., SGD0A are connected, control gates of SGD1, ..., SGD1A are connected, control gates of SGD2, ..., SGD2A are connected, and control gates of SGD3, ..., SGD3A are connected.

[0094] The control gates of the SGS transistors are connected to one another in the x-direction. For example, control gates of SGS0, ..., SGS0A are connected, control gates of SGS1, ..., SGS1A are connected, control gates of SGS2, ..., SGS2A are connected, and control gates of SGS3, ..., SGS3A are connected.

[0095] FIG. 4A depicts a top view of a straight NAND string embodiment (block 480) of the block BLK0 of FIG. 1A, showing example SGD line subsets SGDL-SB0A and SGDL-SB1A. In this configuration, a NAND string has only one column, and the source-side select gate is on the bottom of the column instead of on the top, as in a U-shaped NAND string. Moreover, a given level of a block has one WLL which is connected to each of the memory cells of the layer.

[0096] For example, FIG. 4B1 depicts the block BLK0 of FIG. 4A, showing an example WL line subset WL23-SB and example bit line subsets BL-SB0A and BL-SB1A. A number of slits, such as example slit 482, can also be used. These insulation-filled slits are used in the

fabrication process to provide structural support for the stack when undoped polysilicon layers are removed by a wet etch and a dielectric is deposited to form the alternating dielectric layers. A dashed line 486 extends through columns C12 to C17. A cross-sectional view along line 486 of portion 488 is shown in FIG. 4C.

[0097] FIG. 4B2 depicts the block BLK0 of FIG. 4A, showing example sets of NAND strings 216-219, 221 and 222. Example NAND strings NS0A-NS3A in the portion 488 are also depicted.

[0098] FIG. 4C depicts a cross-sectional view of the portion 488 of the block 480 of FIG. 4A along line 486. Columns of memory cells corresponding to NAND strings NS0A-NS3A in FIG. 4B2 are depicted in the multi-layer stack. In the portion, a stack 490 which includes a substrate 101, an insulating film 250 on the substrate, and a portion of a source line SL0A. Recall that the additional straight NAND strings in a SGD line subset extend in front of and in back of the NAND strings depicted in the cross-section, e.g., along the x-axis. NS0A has a source end 494 and a drain end 492. The slit 482 from FIG. 4A is also depicted with other slits. A portion of the bit line BL0A is also depicted. Dashed lines depict memory cells and select gate transistors. The techniques described herein can be used with a U-shaped or straight NAND. Word line layers WLL0-WLL23A are arranged alternately with dielectric layers D0A-D24A in the stack. An SGD layer, SGDA, an SGS layer, SGSA, and an additional dielectric layer DS are also depicted. SGDA is between D24A and D25A.

[0099] FIG. 5A depicts a process for programming and reading memory cells in a memory device. Step 500 involves programming a first set of memory cells on one word line layer (WLL<sub>n</sub>). Step 501 involves programming a second set of memory cells on another word line layer (WLL<sub>n+1</sub>) which is adjacent to (e.g., above or below) the one word line layer (WLL). In one example programming sequence, the programming proceeds one word line layer at a time starting from a bottom word line layer, and moving sequentially to each next higher word line layer. In this case, the programming of cells on a particular word line layer causes program disturb to the cells on the word line below the particular word line layer. Step 502 includes reading the first set of cells in a normal read operation while applying V<sub>pass\_nominal</sub> (e.g., 8 V) to the adjacent WLL. A normal read operation refers to a read operation in which it has not yet been determined that the cells contain one or more uncorrectable errors. In connection with step 502, step 503 determines V<sub>cg</sub>, V<sub>source</sub> and sensing circuit parameters. These parameters can be set at nominal levels. A nominal level is used during a normal read operation.



**[00100]** Step 504 performs ECC decoding on the data read from the first set of memory cells, e.g., to correct errors and to determine if there are one or more uncorrectable errors. Various types of ECC codes can be used. Some codes have the ability to detect and correct errors. In some cases, the number of errors which can be detected exceeds the number of errors which can be corrected. Thus, some errors are correctable and some are uncorrectable. For example, Hamming codes have a minimum distance of 3, which means that the code can detect and correct a single bit error, or detect but not correct two bit errors. The extended Hamming code adds an extra parity bit to increase the minimum distance to 4. This code can distinguish between single bit errors and two-bit errors. Thus, the code can detect and correct a single error and at the same time detect (but not correct) a two-bit error. Or, the code can detect up to 3 errors without correction. In practice, a unit of data such as a page can be encoded using ECC by a control or state machine and stored in a set of memory cells in an encoded form. The corresponding decoding process is performed on the unit of data when it is read. In this example, one bit error can be corrected and two bit errors can be detected.

**[00101]** In another example, portions of the unit of data such as sub-pages are encoded separately using the ECC. The corresponding decoding process is performed on each portion of the unit of data when it is read. In this example, one bit error can be corrected and two bit errors can be detected for each portion. For example, with eight portions, a total of eight bit errors can be corrected and sixteen bit errors can be detected for the unit of data. A count of errors can include uncorrectable errors only, or both uncorrectable and correctable errors.

**[00102]** Decision step 505 determines if there are one or more uncorrectable errors. This situation is generally unacceptable since the data which was read will not be the same as the data which was programmed. If decision step 505 is false, the read operation has successfully completed at step 506. If decision step 505 is true, data from the second set of memory cells is copied from WLL<sub>n+1</sub> to another location (e.g., a backup location), such as another WLL in the same sub-block or block, or in another block, at step 507. This preserves the data from the second set of memory cells so that it is not corrupted by the use of an elevated V<sub>pass</sub> on WLL<sub>n+1</sub>. If V<sub>pass\_elevated</sub> becomes too high, it can cause read disturb on the cells of WLL<sub>n+1</sub>.

**[00103]** Subsequently, the first set of memory cells is read in a data recovery mode in which V<sub>pass\_elevated</sub> is applied to the adjacent WLL, at step 508. The effect of applying an elevated V<sub>pass</sub> in place of the nominal V<sub>pass</sub> is discussed further below. Generally, it helps to narrow and separate the V<sub>t</sub> distributions of each data state stored by the first set of memory cells so

that it is more probable that the data can be read without uncorrectable errors. In connection with step 508, step 509 determines  $V_{cgr}$ ,  $V_{source}$  and sensing circuit parameters. These parameters can be set at levels which are different than the nominal levels, as discussed further below.

**[00104]** Decision step 510 determines if there are one or more uncorrectable errors. If decision step 510 is false, the read operation has successfully completed at step 506. If decision step 510 is true, decision step 511 determines whether a maximum allowable voltage has been reached by  $V_{pass\_elevated}$ . Alternatively, a maximum allowable number of data recovery read operations may be enforced. If decision step 511 is true, the read operation has failed, at step 512. If decision step 511 is false, step 513 steps up  $V_{pass\_elevated}$  and another data recovery read operation is performed at step 508.  $V_{pass\_elevated}$  can be stepped up using various approaches, as discussed further below. Moreover,  $V_{pass\_elevated}$  can be tailored to the level of  $V_{cgr}$  or to the data states being distinguished, as discussed further below.

**[00105]** FIG. 5B depicts an example of a programming operation consistent with step 500 of FIG. 5A. A programming operation begins at step 520. Step 521 includes applying  $V_{pgm}$  to a set of memory cells on a selected WLL. Step 522 includes performing a verify test for the set of memory cells. For example, sensing circuitry which is connected to the bit lines can be used to sense a conductive or non-conductive state of the cells. A cell which is in a non-conductive state has passed a verify test and is locked out from further programming. Decision step 523 determines whether the set of memory cells has passed the verify test. Typically, this requires that all, or almost all of the cells have passed their respective verify tests. If decision step 523 is false, a next programming pulse is applied at step 521. If decision step 523 is true, decision step 524 determines whether there is a next WLL to program. If decision step 524 is false, the programming operation has ended at step 525. If decision step 524 is true, a next programming pulse is applied at step 521.

**[00106]** FIGs. 6A and 6B depict a one pass programming operation with four data states consistent with FIG. 5B. One pass programming involves a sequence of multiple program-verify operations which are performed starting from an initial  $V_{pgm}$  level and proceeding to a final  $V_{pgm}$  level until the threshold voltages of a set of selected memory cells reach one or more respective verify levels of respective target data states. All memory cells are initially in an erased state. Some of the memory cells are not programmed and remain in the erased state while others are programmed to higher target data states.

**[00107]** Example  $V_{th}$  distributions for the memory cell array are provided for a case where each memory cell stores two bits of data. Each graph depicts  $V_{th}$  on the horizontal axis and a number or population of memory cells in a  $V_{th}$  distribution on the vertical axis. One bit represents the LP data and the other bit represents the UP data. A bit combination can be denoted by the UP bit followed by the LP bit, e.g., 11 denotes UP=1 and LP=1, 01 denotes UP=0 and LP=1, 00 denotes UP=0 and LP=0 and 10 denotes UP=1 and LP=0. A first  $V_{th}$  distribution 600 is provided for erased (Er) state memory cells. Three  $V_{th}$  distributions 604, 606 and 608 represent target data states A, B and C, respectively, which are reached by memory cells when their  $V_{th}$  exceeds the verify level  $V_{vA}$ ,  $V_{vB}$  or  $V_{vC}$ , respectively. In this case, each memory cell can store two bits of data in one of four possible  $V_{th}$  ranges, referred to as states Er (or E), A, B and C.

**[00108]** The specific relationship between the data programmed into a memory cell and the  $V_{th}$  level of the memory cell depends upon the data encoding scheme adopted for the memory cells. In one embodiment, data values are assigned to the  $V_{th}$  ranges using a Gray code assignment so that if the  $V_{th}$  of a floating gate erroneously shifts to its neighboring physical state, only one bit will be affected. One example assigns “11,” “01,” “00” and “10” to the E, A, B- and C-states. Read reference voltages which are between the distributions are used for reading data from the memory cells. By testing whether the  $V_{th}$  of a given memory cell is above or below one or more of the read reference voltages, the system can determine the data state which is represented by a memory cell.

**[00109]** FIGS. 7A to 7C depict a two-pass programming operation with four data states consistent with FIG. 5B. Each pass can be used to program a page of data. For example, programming of lower and upper pages in two-bit, four-level memory cells is provided. Programming can be performed one logical page at a time, with the lower page followed by the upper page. Initially, all memory cells are in the Er state, represented by the distribution 700 in FIG. 7A.

**[00110]** FIG. 7B depicts programming of a lower page of data. If the lower page has a bit=1, the associated memory cell remains in the distribution 700 and the data is represented by x1, where x is an upper page bit that is not yet known. If the lower page has a bit=0, the memory cell is programmed to a higher  $V_{th}$  as represented by distribution 702, which is an interim distribution (INT), using a verify level  $V_{v1}$ . The data of these memory cells is represented by x0. Note that the interim distribution can be relatively wide since it is not a final distribution and does not represent a final data state.

[00111] FIG. 7C depicts programming of an upper page of data. If UP/LP=11, the associated memory cell in the distribution 700 remains in the distribution 700 and stores data bits 11. If UP/LP=01, the memory cells in the distribution 700 are programmed to the distribution 704. If UP/LP=10, the memory cells in the distribution 702 are programmed to the distribution 708 (state C). If UP/LP=00, the memory cells in the distribution 702 are programmed to the distribution 706 (state B).

[00112] Programming can be similarly extended to three or more bits per memory cell.

[00113] FIG. 8 depicts program and verify voltages in a programming operation, consistent with FIG. 5B. A programming operation may include multiple program-verify iterations or loops, where each program-verify iteration includes a programming portion comprising a program pulse and a following verify operation comprising one or more verify voltages. The program pulse and verify voltages are applied to a selected WLL.

[00114] In one approach, the program pulses are stepped up in successive iterations by a step size,  $dV_{pgm}$ . Moreover, each program pulse may include a first portion which has a pass voltage ( $V_{pass}$ ) level, e.g., 6-8 V, followed by a second, peak amplitude portion at a program level, e.g., 12-25 V. For example, this programming pass includes program pulses 801-805 and associated sets of verify pulses 811-815, respectively. The initial program pulse has a magnitude of  $V_{pgm\_initial}$ . In this example, the verify pulses have a magnitude of  $V_{vA}$ ,  $V_{vB}$  and  $V_{vC}$ .

[00115] FIG. 9A depicts a change in a  $V_t$  distribution of a first set of memory cells on a word line layer  $WLL_n$  after programming of an adjacent second set of memory cells on a word line layer  $WLL_{n+1}$ . The  $V_t$  distributions 700, 710, 720 and 730 are depicted for the E, A, B and C states, respectively, of the first set of memory cells, before programming the second set of memory cells. The  $V_t$  distributions 701, 711, 721 and 731 are depicted for the E, A, B and C states, respectively, of the first set of memory cells, after programming the second set of memory cells. The  $V_t$  distributions of FIG. 9A-9D are simplifications. Actual test data is provided further below. Generally, the  $V_t$  distributions are widened due to program disturb caused by programming the adjacent cells.

[00116] If the set of control read voltages which includes  $V_{rA}$ ,  $V_{rB}$  and  $V_{rC}$  is used to read the cells after they have been disturbed, a large number of errors can result because these read voltages are optimized for a non-disturbed set of cells. To reduce the number of errors, the read levels can be adaptively set based on the current  $V_t$  distribution, in a first (normal) read operation. In this approach, several sensing operations are performed to an optimum read level

between adjacent data states. For example, sensing operations can be performed using control gate voltages of VrA0a, VrA0b, VrA0, VrA0c and VrA0d. Error correction decoding is performed on data read for each control gate voltage of a plurality of different control gate voltages, and an optimum control gate voltage (e.g., VrA0) which results in a minimum number of errors is selected from among the plurality of different control gate voltages. Typically, the optimum control gate voltage will be at a minimum point in the Vt distribution between adjacent data states. Similarly, VrB0 is an optimum read voltage between the A and B states, and VrC0 is an optimum read voltage between the B and C states.

[00117] However, even with the optimum read levels, there will be some read errors. For example, for some of the E state cells, the Vt exceeds VrA0 and these cells will be incorrectly read as being A state cells. For some of the A state cells, the Vt is less than VrA0 and these cells will be incorrectly read as being E state cells.

[00118] FIG. 9B depicts a change in a Vt distribution of the first set of memory cells in a second read operation (a first data recovery read operation) which follows FIG. 9A. When Vpass\_elevated is applied to second set of memory cells, this causes a shift in the Vt distribution of the first set of memory cells. In particular, the Vt distribution is lowered and somewhat narrowed. The effect is more pronounced for the lower data states. The Vt distributions 701, 711, 721 and 731 of FIG. 9A become the Vt distributions 702, 712, 722 and 732 of FIG. 9B. The optimum read voltages can again be adaptively determined, this time as VrA1, VrB1 and VrC1.

[00119] FIG. 9C depicts a change in a Vt distribution of the first set of memory cells in a third read operation (a second data recovery read operation) which follows FIG. 9B. When a stepped up Vpass\_elevated is applied to second set of memory cells, this cause a further lowering and narrowing in the Vt distribution of the first set of memory cells. The Vt distributions 702, 712, 722 and 732 of FIG. 9B become the Vt distributions 703, 713, 723 and 733 of FIG. 9C. The optimum read voltages can again be adaptively determined, this time as VrA2, VrB2 and VrC2. Note that the optimum read voltages also typically become lower with each successive read operation.

[00120] FIG. 9D depicts the Vt distributions 703, 713, 723 and 733 of FIG. 9C aligned with the Vt distributions 700, 710, 720 and 730 of FIG. 9A. The aligned Vt distributions are 704, 714, 724 and 734. This indicates that the Vt distributions are somewhat wider than the non-disturbed distributions 700, 710, 720 and 730 of FIG. 9A, but advantageously narrower than the disturbed distributions 701, 711, 721 and 731 of FIG. 9A.

[00121] FIG. 10A depicts a  $V_t$  distribution from test data of a first set of memory cells on WLL $_n$  before and after programming of an adjacent second set of memory cells on WLL $_{n+1}$ , where: (1) WLL $_{n+1}$  is unprogrammed and  $V_{pass\_nominal}$  is used on WLL $_{n+1}$  when WLL $_n$  is read (see line 1000 with the square symbols), and (2) WLL $_{n+1}$  is programmed and  $V_{pass\_nominal}$  is used on WLL $_{n+1}$  when WLL $_n$  is read (see line 1001 with the circle symbols). The plot depicts the  $V_t$  of a set of cells on WLL $_n$  on the horizontal x-axis and a number of cells on the vertical axis using a logarithmic scale.

[00122] The plot indicates that the  $V_t$  is widened for each state. The widening is greatest for the A state, and less for the B and C states. Moreover, the C state distribution is widened primarily on its lower end. The widening of the  $V_t$  distribution is due to program disturb. In particular, this program disturb is not observed until the spacing between memory cells becomes very small, such as less than 20nm. For example, the program disturb was not observed for a cell spacing of 25-40 nm.

[00123] FIG. 10B depicts a close up view of a portion of the example memory cells MC22D and MC23D of FIG. 3B, showing electron injection in a charge trapping layer between memory cells. In this program disturb model, when MC23D on a neighbor WLL (e.g., WLL $_{n+1}$ ) is programmed, a strong fringing field is caused by the use of a high  $V_{pgm}$  on WLL $_{n+1}$ . The application of  $V_{pgm}$  results in a primary electromagnetic field  $E_2$  which causes electron injection from the channel 299 to a portion 1008 of the charge trapping layer 297 which is within the memory cell MC23D, e.g., adjacent to the WLL. See example electron 1005. However, fringing fields  $E_1$  and  $E_3$  are also generated which cause electron injection from the channel 299 to portions of the charge trapping layer 297 which are outside the memory cell MC23D. See example electron 1006 in a portion 1007 of the charge trapping layer which is between the memory cells MC23D and MC22D.

[00124] These charges can result in a parasitic memory cell which has a threshold voltage. As a result, during a read operation on WLL $_n$ , a higher control gate voltage may be needed to provide a fringing field from MC22D which causes the parasitic cell to become conductive and to thereby allow sensing of MC22D. The control gate voltages used for the lower data states may not be sufficient to cause the parasitic cell to become highly conductive. As a result, reading of lower data states can be significantly impaired. On the other hand, the control gate voltages used for the higher data states may be sufficient to cause the parasitic cell to become highly conductive, so that reading of higher data states is impaired by a smaller amount.

[00125] Note that the charge trapping layer extends vertically in this example and the word line layers extend horizontally. However, other configurations are possible. For example, the charge trapping layer could extend horizontally while the word line layers extend vertically.

[00126] FIG. 10C depicts a  $V_t$  distribution from test data of a second set of memory cells on WLL<sub>n+1</sub> after programming to an all C state data pattern using: (3) a lower verify level (e.g., 4.5 V, see line 1030) and (4) a higher verify level (e.g., 5.5 V, see line 1031). The plot depicts the  $V_t$  of a set of cells on WLL<sub>n+1</sub> on the horizontal x-axis and a number of cells on the vertical axis using a logarithmic scale. This figure shows programming on WLL<sub>n+1</sub> to determine the amount of program disturb on WLL<sub>n</sub> (FIG. 10D).

[00127] FIG. 10D depicts a  $V_t$  distribution from test data of a first set of memory cells on WLL<sub>n</sub> where: (5) WLL<sub>n+1</sub> is unprogrammed and  $V_{pass\_nominal}$  is used on WLL<sub>n+1</sub> when WLL<sub>n</sub> is read (see line 1040), (6) WLL<sub>n+1</sub> is programmed using the low verify of case (3) and  $V_{pass\_nominal}$  is used on WLL<sub>n+1</sub> when WLL<sub>n</sub> is read (see line 1041), and (7) WLL<sub>n+1</sub> is programmed using the high verify of case (4) and  $V_{pass\_nominal}$  is used on WLL<sub>n+1</sub> when WLL<sub>n</sub> is read (see line 1042). The plot depicts the  $V_t$  of a set of cells on WLL<sub>n</sub> on the horizontal x-axis and a number of cells on the vertical axis using a logarithmic scale.

[00128] Specifically, case (5) represents the original  $V_t$  distribution of the cells on WLL<sub>n</sub> after completion programming on WLL<sub>n</sub>. The cells on WLL<sub>n</sub> were programmed to an all B state data pattern using a verify level of 3 V. Case (6) represents a change in the distribution of case (5) due to programming of the cells of WLL<sub>n+1</sub> to an all C state data pattern using a verify level of 4.5 V. Case (7) represents a change in the distribution of case (5) due to programming of the cells of WLL<sub>n+1</sub> to an all C state data pattern using a verify level of 5.5 V. The  $V_t$  of the cells on WLL<sub>n</sub> increase by about 0.2 V in case (6) and by about 0.5 V in case (7), at the three-sigma point of the  $V_t$  distributions 1041 and 1042, respectively. Since a voltage change on WLL<sub>n+1</sub> of  $4.5-3=1.5$  V causes a 0.2 V change on WLL<sub>n</sub>, and a voltage change on WLL<sub>n+1</sub> of  $5.5-3=2.5$  V causes a 0.5 V change on WLL<sub>n</sub>, the increase in  $V_t$  due to program disturb is non-linear with the programming depth (voltage swing) of the cells on WLL<sub>n+1</sub>. That is, the ratio of program disturb to the voltage change on WLL<sub>n</sub> is  $0.2/1.5=0.13$  in one case and  $0.5/2.5=0.20$  in another case. This indicates the program disturb effect cannot be resolved by countermeasures for linear program disturb effects such as might be seen in floating gate cells.

[00129] FIG. 10E depicts a  $V_t$  distribution from test data of a first set of memory cells on WLL<sub>n</sub> where: (8) WLL<sub>n+1</sub> is unprogrammed and  $V_{pass\_nominal}$  is used on WLL<sub>n+1</sub> when

WLL<sub>n</sub> is read (see line 1052 and the upright triangle symbols), (9) WLL<sub>n+1</sub> is programmed and V<sub>pass\_nominal</sub> is used on WLL<sub>n+1</sub> when WLL<sub>n</sub> is read (see line 1050 and the circle symbols), (10) WLL<sub>n+1</sub> is unprogrammed and V<sub>pass\_elevated</sub> is used on WLL<sub>n+1</sub> when WLL<sub>n</sub> is read (see line 1053 and the inverted triangle symbols), and (11) WLL<sub>n+1</sub> is programmed and V<sub>pass\_elevated</sub> is used on WLL<sub>n+1</sub> when WLL<sub>n</sub> is read (see line 1051 and the square symbols). The plot depicts the V<sub>t</sub> of a set of cells on WLL<sub>n</sub> on the horizontal x-axis and a number of cells on the vertical axis using a logarithmic scale.

**[00130]** This graph shows the effect of using V<sub>pass\_elevated</sub> on WLL<sub>n+1</sub>, when reading the cells on WLL<sub>n</sub>. There is not a significant difference in the V<sub>t</sub> of the cells on WLL<sub>n</sub> based on whether V<sub>pass\_nominal</sub> or V<sub>pass\_elevated</sub> is applied to WLL<sub>n+1</sub>, when the cells of WLL<sub>n+1</sub> have not been programmed (cases (8) and (10) are similar). This is true because no parasitic cell has been created. However, there is a narrowing of the V<sub>t</sub> of the cells on WLL<sub>n</sub>, especially for the A state, when V<sub>pass\_elevated</sub> instead of V<sub>pass\_nominal</sub> is applied to WLL<sub>n+1</sub>, and when the cells of WLL<sub>n+1</sub> have been programmed so that a parasitic cell has been created. As an example, V<sub>pass\_nominal</sub> is about 8 V and V<sub>pass\_elevated</sub> is about 12 V.

**[00131]** For a given data state, the V<sub>t</sub> distribution is narrowed because V<sub>pass\_elevated</sub> causes a larger downshift in the high part of the distribution than in the low part. As mentioned, a parasitic cell is created between a memory cell on WLL<sub>n</sub> and a memory cell on WLL<sub>n+1</sub> when the cell on WLL<sub>n+1</sub> is programmed using a high V<sub>pgm</sub>. The parasitic cell acts as a resistance between the memory cells and the resistance is higher when the cell on WLL<sub>n+1</sub> is programmed to a higher state such as the C state). This causes a higher upshift in the V<sub>t</sub> of the cell on WLL<sub>n</sub> than if the cell on WLL<sub>n+1</sub> was programmed to a low state such as the A state. Further, there may be no upshift in the V<sub>t</sub> of the cell on WLL<sub>n</sub> if the cell on WLL<sub>n+1</sub> remains in the erase state. See also FIG. 9A. Subsequently, when V<sub>pass\_elevated</sub> is applied to WLL<sub>n+1</sub> while reading the cell on WLL<sub>n</sub>, the parasitic cell is provided in a less resistive, conducive state so that the effect of the parasitic cell is largely removed. As a result, there is a large downshift in the V<sub>t</sub> of the cells in the high part of the distribution than in the V<sub>t</sub> of the cells in the low part of the distribution, resulting in a narrowing of the V<sub>t</sub> distribution. The narrowing effect due to V<sub>pass\_elevated</sub> is therefore stronger when the widening effect due to the parasitic cell is stronger.

**[00132]** The techniques provided herein provide a system-level data rescue solution for highly-scaled 3D stacked non-volatile memory devices. In these techniques, when the ECC decoding indicates there are one or more uncorrectable errors in the data read from the cells on



WLLn while WLLn+1 is biased at Vpass\_nominal, a recovery process is initiated. The process can involve multiple read attempts, where Vpass\_elevated becomes progressively higher with each attempt, until the ECC decoding indicates there are no uncorrectable errors, or until Vpass\_elevated reaches a limit. As mentioned, the initial value of Vpass\_elevated can be significantly higher than Vpass\_nominal, e.g., 12 V vs. 8 V. Vpass\_elevated can increase in steps of 3 V, for instance, so that the next value of Vpass\_elevated is 15 V and then 18 V, which may be the maximum allowed value. In this case, up to three data recovery read operations can be used.

**[00133]** As mentioned, the Vt distribution is shifted lower on the cells of WLLn by the use of Vpass\_elevated on WLLn+1. To compensate, Vcgr can also be shifted lower. In the adaptive approach, an optimum Vcgr can be determined for distinguishing between each pair of adjacent data states. In another approach, Vcgr can be shifted lower by predetermined amounts for each pair of adjacent data states. The shifts can be the same or vary for each data recovery read operation. Further, the shifts can be different for the different states, with the lower states having a larger shift.

**[00134]** The amount of the shift can be expressed by  $Y=nX$ , where n is the sensitivity of the Vt of the cells on WLLn to Vcgr on WLLn+1, and is specific to the memory device. X is the difference between Vpass\_elevated – Vpass\_nominal. For example, if n is 0.1 V/V and Vpass\_elevated – Vpass\_nominal = 12-8=4 V, then Y=0.4 V. Y is the difference in Vcgr on WLLn.

**[00135]** Another option to compensate for the Vt distribution being shifted lower is to increase Vsource, the bias of the source end of the NAND string and of the source terminals of the cells being read, above a nominal level by the above-mentioned voltage Y. Other options to compensate for the Vt distribution being shifted lower on the cells of WLLn include adjusting parameters in the sensing circuitry, as discussed further below.

**[00136]** FIG. 10F depicts a Vt distribution from test data of a first set of memory cells on WLLn where: (12) WLLn+1 is programmed and Vpass\_nominal is used on WLLn+1 when WLLn is read (see line 1060 and the square symbols), (13) WLLn+1 is programmed and Vpass\_elevated is used on WLLn+1 when WLLn is read (see line 1061 and the circle symbols). The plot depicts the Vt of a set of cells on WLLn on the horizontal x-axis and a number of cells on the vertical axis using a logarithmic scale.

**[00137]** Referring also to FIG. 10G, in this example, the cells of WLLn were programmed while biasing WLLn+1 at Vpass\_nominal, then the cells of WLLn+1 were programmed while

biasing WLLn at Vpass\_nominal. In case (12), the cells of WLLn were read while biasing WLLn+1 at Vpass\_nominal. In case (13), the cells of WLLn were read while biasing WLLn+1 at Vpass\_elevated. These results show the decrease in the Vt of the cells on WLLn due to the use of Vpass\_elevated.

**[00138]** FIG. 10G depicts a Vt distribution from test data of a first set of memory cells on WLLn where: (14) WLLn+1 is unprogrammed and Vpass\_nominal is used on WLLn+1 when WLLn is read (see line 1070 and the square symbols), (15) WLLn+1 is programmed and Vpass\_nominal is used on WLLn+1 when WLLn is read (see line 1072 and the triangle symbols), and (16) WLLn+1 is programmed and Vpass\_elevated is used on WLLn+1 when WLLn is read, and the Vt distribution is aligned with the Vt distributions of cases (14) and (15) (see line 1071 and the circle symbols). The plot depicts the Vt of a set of cells on WLLn on the horizontal x-axis and a number of cells on the vertical axis using a logarithmic scale. These results show that the Vt distribution of the cells on WLLn was successfully narrowed with the Vpass\_elevated applied to WLLn+1. By narrowing the Vt distribution, the number of read errors can be reduced.

**[00139]** FIG. 11A depicts a control gate voltage on WLLn as a function of time during a read operation for distinguishing four data states in a first set of memory cells on WLLn, consistent with FIG. 5A. The horizontal axis depicts time and the vertical axis depicts a voltage on WLLn. In a read operation, each selected cell to be read is biased in a way which indicates the Vt of the cell. The terminals of a cell include the control gate, drain and source. In one approach, the selected cell is in a NAND string, one end of the NAND string is connected to sensing circuitry via a bit line and the other end of the NAND string is connected to a source line. By providing the unselected cells in the NAND string in a conductive state, the drain of the selected cell can be biased by a voltage at the sensing circuitry and the source of the selected cell can be biased by a voltage at the source line. The control gate of the selected cell can be biased by a control gate read voltage (Vcgr) on WLLn. To distinguish between n=4 different data states, n-1=3 different levels of Vcgr can be applied to WLLn in turn.

**[00140]** To distinguish between the E and A states (E/A read), Vcgr\_A is applied to WLLn and the sensing circuitry is used to determine whether each cell is in a conductive state. If a cell is in a conductive state, this indicates its  $V_t > V_{cgr\_A}$ . If a cell is in a non-conductive state, this indicates its  $V_t \leq V_{cgr\_A}$ . Similarly, to distinguish between the A and B states (A/B read), Vcgr\_B is applied to WLLn, and to distinguish between the B and C states (B/C read), Vcgr\_C is applied to WLLn.

[00141] As mentioned, a higher  $V_{pass}$  on  $WLL_{n+1}$  results in a decrease in the  $V_t$  distribution on  $WLL_n$ . Accordingly,  $V_{cgr}$  will be lower for each successive read operation.  $V_{cgr}$  can also be lowered for each successive read operation by setting it adaptively or based on predetermined decreases. Thus, during the first read operation, the E/A read is performed in which  $V_{cgr\_A}$  is applied to  $WLL_n$  at the level of line 1101, the A/B read is performed in which  $V_{cgr\_B}$  is applied to  $WLL_n$  at the level of line 1102, and the B/C read is performed in which  $V_{cgr\_C}$  is applied to  $WLL_n$  at the level of line 1103. During the second read operation, the E/A read is performed in which  $V_{cgr\_A}$  is applied to  $WLL_n$  at the level of line 1104, the A/B read is performed in which  $V_{cgr\_B}$  is applied to  $WLL_n$  at the level of line 1105, and the B/C read is performed in which  $V_{cgr\_C}$  is applied to  $WLL_n$  at the level of line 1105. During the third read operation, the E/A read is performed in which  $V_{cgr\_A}$  is applied to  $WLL_n$  at the level of line 1107, the A/B read is performed in which  $V_{cgr\_B}$  is applied to  $WLL_n$  at the level of line 1108, and the B/C read is performed in which  $V_{cgr\_C}$  is applied to  $WLL_n$  at the level of line 1109.

[00142] FIG. 11B depicts  $V_{pass\_elevated}$  on  $WLL_{n+1}$  and  $V_{pass\_nominal}$  on remaining unselected word line layers as a function of time during a read operation for a first set of memory cells on  $WLL_n$ , time-aligned with FIG. 11A, and consistent with FIG. 5A. The horizontal axis depicts time and the vertical axis depicts  $V_{pass\_elevated}$ . This example shows the first read operation which is a normal read operation, a second read operation which is a first data recovery read operation, and a third read operation which is a second data recovery read operation.  $V_{pass\_nominal}$  is also depicted. In one example,  $V_{pass\_nominal}$  is about 6-8 V and  $V_{pass\_elevated}$  is between 10-18 V. Additionally, for each demarcation of adjacent data states in each read operation, two options are provided for  $V_{cgr}$ : a lower voltage is represented by a solid line and a higher voltage is represented by a dashed line. The higher or lower voltage, or an intermediate voltage, may be selected based on a factor such as a number of errors detected in the previous read operation.

[00143] For example, it may be desirable to provide a higher  $V_{pass\_elevated}$  when there are a relatively large number of errors detected in the previous read operation. In this situation, a higher  $V_{pass\_elevated}$  is used to more quickly bring down the number of errors. The initial level of  $V_{pass\_elevated}$  as well as the step size of  $V_{pass\_elevated}$  in a read operation may be a function of the number of errors in the previous read operation.

[00144] Additionally, the initial level of  $V_{pass\_elevated}$  and the step size of  $V_{pass\_elevated}$  can be a function of the data states being demarcated in a read operation. Generally, the initial

level of  $V_{\text{pass\_elevated}}$  and the step size of  $V_{\text{pass\_elevated}}$  can be relatively higher when the amount of program disturb is higher, e.g., for a read which attempts to demarcate between adjacent lower data states (e.g., E/A read). The lower data states encompass an associated range of threshold voltages which are lower an associated range of threshold voltages for higher data states. The initial level of  $V_{\text{pass\_elevated}}$  and the step size of  $V_{\text{pass\_elevated}}$  can be relatively lower when the amount of program disturb is lower, e.g., for a read which attempts to demarcate between adjacent higher data states (e.g., A/B and B/C reads). The initial level of  $V_{\text{pass\_elevated}}$  and the step size of  $V_{\text{pass\_elevated}}$  can thus be inversely proportional to the level of  $V_{\text{cgr}}$  in a read operation.

**[00145]** Thus, during the first read operation, the E/A read is performed in which  $V_{\text{cgr\_A}}$  is applied to  $WLL_n$  and  $V_{\text{pass\_elevated}}$  at the level of line 1110 or 1111 is applied to  $WLL_{n+1}$ .  $V_{\text{pass\_nominal}}$  may be applied to the remaining word line layers, in one approach. The A/B read is performed in which  $V_{\text{cgr\_B}}$  is applied to  $WLL_n$  and  $V_{\text{pass\_elevated}}$  at the level of line 1112 or 1113 is applied to  $WLL_{n+1}$ . The B/C read is performed in which  $V_{\text{cgr\_C}}$  is applied to  $WLL_n$  and  $V_{\text{pass\_elevated}}$  at the level of line 1114 or 1115 is applied to  $WLL_{n+1}$ .

**[00146]** During the second read operation, the E/A read is performed in which  $V_{\text{cgr\_A}}$  is applied to  $WLL_n$  and  $V_{\text{pass\_elevated}}$  at the level of line 1116 or 1117 is applied to  $WLL_{n+1}$ . The A/B read is performed in which  $V_{\text{cgr\_B}}$  is applied to  $WLL_n$  and  $V_{\text{pass\_elevated}}$  at the level of line 1118 or 1119 is applied to  $WLL_{n+1}$ . The B/C read is performed in which  $V_{\text{cgr\_C}}$  is applied to  $WLL_n$  and  $V_{\text{pass\_elevated}}$  at the level of line 1120 or 1121 is applied to  $WLL_{n+1}$ .

**[00147]** During the third read operation, the E/A read is performed in which  $V_{\text{cgr\_A}}$  is applied to  $WLL_n$  and  $V_{\text{pass\_elevated}}$  at the level of line 1122 or 1123 is applied to  $WLL_{n+1}$ . The A/B read is performed in which  $V_{\text{cgr\_B}}$  is applied to  $WLL_n$  and  $V_{\text{pass\_elevated}}$  at the level of line 1124 or 1125 is applied to  $WLL_{n+1}$ . The B/C read is performed in which  $V_{\text{cgr\_C}}$  is applied to  $WLL_n$  and  $V_{\text{pass\_elevated}}$  at the level of line 1126 or 1127 is applied to  $WLL_{n+1}$ .

**[00148]** FIG. 11C depicts  $V_{\text{pass\_elevated}}$  on  $WLL_{n+1}$  during a second read operation (a first data recovery read operation) for a first set of memory cells on  $WLL_n$ , as a function of a number of errors during a first (normal) read operation, and consistent with FIG. 5A. The horizontal axis depicts a number of errors in a first (normal) read operation and the vertical axis depicts  $V_{\text{pass\_elevated}}$  in a second read operation. As mentioned, the initial value of  $V_{\text{pass\_elevated}}$  can be a function of the number of errors from the ECC decoding in the normal read operation. The initial value of  $V_{\text{pass\_elevated}}$  can be adaptively set in proportion to the number of errors. The number of errors can be the number of uncorrectable errors, the number

of detected errors or some other error metric. Generally, a higher number of errors indicates that a more aggressive  $V_{\text{pass\_elevated}}$  is appropriate in the next read operation. This approach can result in completing the data recovery process with fewer read operations than when a less aggressive  $V_{\text{pass\_elevated}}$  is used.

[00149] Furthermore, the initial value of  $V_{\text{pass\_elevated}}$  can be a function of the data states which are being distinguished, e.g., a function of  $V_{\text{cgr}}$ , such that the initial value of  $V_{\text{pass\_elevated}}$  is relatively higher when relatively lower data states are being distinguished. The initial value of  $V_{\text{pass\_elevated}}$  is inversely proportional to  $V_{\text{cgr}}$ .

[00150] FIG. 11D depicts a step size for  $V_{\text{pass\_elevated}}$  during a data recovery read operation for a first set of memory cells on WLLn, as a function of a number of errors during a previous read operation, and consistent with FIG. 5A. The horizontal axis depicts a number of errors in a previous read operation and the vertical axis depicts  $V_{\text{pass\_elevated}}$  step size in a current read operation. As mentioned, the step size can be a function of the number of errors from the ECC decoding in the previous read operation. The step size can be proportional to the number of errors. Generally, a higher number of errors indicates that a more aggressive step size is appropriate in the next read operation. This approach can result in completing the data recovery process with fewer read operations than when a less aggressive step size is used. This approach adaptively sets the step size in proportion to the number of errors.

[00151] Furthermore, the step size can be a function of the data states which are being distinguished, e.g., a function of  $V_{\text{cgr}}$ , such that the step size is relatively higher when relatively lower data states are being distinguished. The step size is inversely proportional to  $V_{\text{cgr}}$ .

[00152] FIG. 11E depicts  $V_{\text{cgr}}$  on WLLn during a data recovery read operation for a first set of memory cells on WLLn, as a function of  $V_{\text{pass\_elevated}}$ , and consistent with FIG. 5A. The horizontal axis depicts  $V_{\text{pass\_elevated}}$  and the vertical axis depicts  $V_{\text{cgr}}$ . As mentioned, one approach to optimizing  $V_{\text{cgr}}$  is to perform multiple sensing operations using different values for  $V_{\text{cgr}}$  to determine which value results in a minimum number of errors. However, this consumes time. To save time,  $V_{\text{cgr}}$  can be set for each data recovery read operation based on a predetermined decrease from a baseline level or from the level of a previous read operation. In this case,  $V_{\text{cgr}}$  can be optimized by making it inversely proportional to the level of  $V_{\text{pass\_elevated}}$ .  $V_{\text{cgr}}$  can also depend on the data states which are being distinguished, such that  $V_{\text{cgr}}$  is lower and decreases more quickly when relatively lower data states are being distinguished. See also FIG. 11A. Thus, the magnitude of the slope of  $V_{\text{cgr}}/V_{\text{pass\_elevated}}$  is higher for the E/A read than for the B/C read.

[00153] FIG. 11F depicts  $V_{source}$  during a data recovery read operation for a first set of memory cells on WLLn, as a function of  $V_{pass\_elevated}$ , and consistent with FIG. 5A. The horizontal axis depicts  $V_{pass\_elevated}$  and the vertical axis depicts  $V_{source}$ . As an alternative to decreasing  $V_{cgr}$  for each read operation,  $V_{source}$  can be increase. The conductive state of a cell is based on  $V_{cgr}-V_{source}$ , so that increasing  $V_{source}$  is equivalent to decreasing  $V_{cgr}$ . In this case,  $V_{source}$  is proportional to the level of  $V_{pass\_elevated}$ .  $V_{source}$  can also depend on the data states which are being distinguished, such that  $V_{source}$  is higher and increases more quickly when relatively lower data states are being distinguished. Thus, the magnitude of the slope of  $V_{source}/V_{pass\_elevated}$  is higher for the E/A read than for the B/C read.

[00154] FIG. 11G depicts a sensing period (SP) in sensing circuitry during a data recovery read operation as for a first set of memory cells on WLLn, as a function of  $V_{pass\_elevated}$ , and consistent with FIG. 5A. The horizontal axis depicts  $V_{pass\_elevated}$  and the vertical axis depicts SP. As mentioned, the  $V_t$  of a cell can be determined by applying different levels of  $V_{cgr}$  to the cell and using sensing circuitry to determine whether the cell is in a conductive state. This approach assume the sensing circuitry uses a consistent sensing process. As an alternative to decreasing  $V_{cgr}$  for each read operation as a function of  $V_{pass\_elevated}$ , a sensing period in the sensing circuitry can be reduced in proportion to  $V_{pass\_elevated}$ . SP can also depend on the data states which are being distinguished, such that SP is lower and decreases more quickly when relatively lower data states are being distinguished. Details regarding the use of SP in sensing circuitry are discussed further below.

[00155] FIG. 11H depicts voltage demarcation level (DL) in sensing circuitry during a data recovery read operation for a first set of memory cells on WLLn, as a function of  $V_{pass\_elevated}$ , and consistent with FIG. 5A. The horizontal axis depicts  $V_{pass\_elevated}$  and the vertical axis depicts DL. As an alternative to decreasing  $V_{cgr}$  for each read operation as a function of  $V_{pass\_elevated}$ , a demarcation level (DL) in the sensing circuitry can be decreased in proportion to  $V_{pass\_elevated}$ . DL can also depend on the data states which are being distinguished, such that DL is lower and decreases more quickly when relatively lower data states are being distinguished.

[00156] FIG. 11I depicts pre-charge level (PL) in sensing circuitry during a data recovery read operation for a first set of memory cells on WLLn, as a function of  $V_{pass\_elevated}$ , and consistent with FIG. 5A. The horizontal axis depicts  $V_{pass\_elevated}$  and the vertical axis depicts PL. As an alternative to decreasing  $V_{cgr}$  for each read operation as a function of  $V_{pass\_elevated}$ , a pre-charge level in the sensing circuitry can be increased in proportion to

Vpass\_elevated. PL can also depend on the data states which are being distinguished, such that PL is lower and decreases more quickly when relatively lower data states are being distinguished. Details regarding the use of PL in sensing circuitry are discussed further below.

**[00157]** In various options, one or more of Vcgr, Vsource, SP, DL or PL can be adjusted in each read operation to compensate for decreases in the Vt of cells on WLLn caused by the use of Vpass\_elevated on WLLn+1.

**[00158]** FIG. 11J depicts an optimum Vcgr\_A in a first read operation, an optimum Vcgr\_A in a second read operation, and a reference Vcgr\_A in the second read operation, consistent with FIG. 5A. The horizontal axis depicts time and the vertical axis depicts Vcgr\_A. As mentioned, an optimum Vcgr for distinguishing between two adjacent data states can be determined adaptively by determining a Vcgr which results in the fewest errors. Typically, this Vcgr is at a minimum in the Vt distribution between the two adjacent data states. This can be done for each read operation. Line 1130 represents an optimum level of Vcgr\_A for a first read operation on WLLn, in which Vpass\_nominal is applied on WLLn+1. Line 1131 represents an optimum level of Vcgr\_A for a second read operation on WLLn, in which an initial level of Vpass\_elevated is applied on WLLn+1. Further, line 1132 represents a predetermined reference level of Vcgr\_A for the second read operation. This reference level could be determined from testing of different memory devices, or of different WLLs in one memory device. This reference level may represent an expected level for an average memory device or WLL.

**[00159]** However, a given WLL may behave differently from the average. A difference between the reference Vcgr\_A and the adaptively determined optimum of Vcgr\_A, referred to as delta Vcgr\_A, is a function of a degree of sensitivity of the Vt of the cells on WLLn relative to Vpass\_elevated on WLLn+1. This is similar to the sensitivity discussed in connection with FIG. 10E.

**[00160]** Delta Vcgr\_A is inversely proportional to the sensitivity. It can be useful to adjust the step size for Vpass\_elevated so that uniform results are achieved for data recovery operations for different WLLs with different sensitivities. For example, with a higher sensitivity, the step size can be lower. With a lower sensitivity, the step size can be higher. Since line 1131 is higher than line 1132, the sensitivity is lower than average. This means the step size for Vpass\_elevated can be adjusted to be higher than when the sensitivity is average.

**[00161]** The above technique can be extended to the Vcgr used for other data states, such as for the A/B and B/C reads. However, the sensitivity, and variations in the sensitivity, will

typically be strongest for the E/A read. The above technique could also be extended to later read operations, e.g., third, fourth and so forth. The value of  $\Delta V_{cgr\_A}$  from the second read operation can be used to adjust the step size of  $V_{pass\_elevated}$  in the second read operation and optionally, the third, fourth and later read operations. Or, a new value of  $\Delta V_{cgr\_A}$  from the third read operation, for instance, can be used to adjust the step size of  $V_{pass\_elevated}$  in the third read operation and optionally, the fourth and later read operations.

**[00162]** FIG. 11K depicts an adjustment to  $V_{pass\_elevated}$  step size as a function of  $\Delta V_{cgr\_A}$  in the second read operation, consistent with FIG. 11J. The horizontal axis depicts  $\Delta V_{cgr\_A}$  as discussed in connection with FIG. 11J, e.g.,  $V_{cgr\_A}$  (2<sup>nd</sup> read reference) –  $V_{cgr\_A}$  (2<sup>nd</sup> read optimum) and the vertical axis depicts a positive or negative adjustment to  $V_{pass\_elevated}$  step size. The origin of the axes represents  $\Delta V_{cgr\_A}=0$  and adjustment=0. Note that the step size is non-zero regardless of the adjustment. The adjustment is inversely proportional to  $\Delta V_{cgr\_A}$ .

**[00163]** This is an example of a second voltage ( $V_{pass\_elevated}$ ) being based on a difference between the optimum control gate voltage (line 1131) and a reference control gate voltage (line 1132).

**[00164]** The adjustment of sensing parameters can be understood further in view of the following example sensing circuits and control schemes.

**[00165]** FIG. 12A depicts a configuration of a NAND string and sensing circuitry when current sensing is used. A simple NAND string 1212 includes four storage elements which are in communication with word lines WL0, WL1, WL2 and WL3, respectively. A bit line 1210 having a voltage  $V_{bl}$  is depicted, in addition to sensing circuitry 1200. A BLS (bit line sense) transistor 1206, coupled to the bit line 1210, is a high voltage transistor, and is made conductive in response to a control 1208 during sense operations. A BLC (bit line clamp) transistor 1204 is a low voltage transistor which is made conductive in response to the control 1208 at a start of a sensing period to allow the bit line to communicate with a current sensing module 1202. During a sense operation, such as a read or verify operation, a pre-charge operation occurs in which a capacitor in the current sensing module 1202 is charged. The BLC transistor 1204 may be made conductive to allow the pre-charging. The pre-charge level in the current sensing module 1202 can be a sensing parameter, for example. The BLC transistor can be used to set a bit line voltage as  $V_{bl}=V_{blc} - V_{th}$ , where the  $V_{th}$  is of the BLC transistor. The selected word line receives a read or verify control gate voltage, and  $V_{source}$  is set.



[00166] At the drain side of the NAND string 1230, the BLS transistor 1210 is made conductive. Additionally,  $V_{blc}$  is applied to the BLC transistor 1204 to allow the current sensing module 1202 to communicate with the bit line. The pre-charged capacitor in the current sensing module 1202 discharges through the bit line and into the source so that the source acts as a current sink. The pre-charged capacitor at the drain of the NAND string may be pre-charged to a potential which exceeds a potential of the source so that a current flows through the selected non-volatile storage element and sinks into the source when the selected storage element is in the conductive state.

[00167]  $V_{source}$  is provided on a source line 1211.

[00168] If the selected storage element is in a conductive state due to the application of the control gate verify or read voltage, a relatively high current will flow in the NAND string. If the selected storage element is in a non-conductive state, no or relatively little current will flow. The current sensing module 1202 can sense the cell/storage element current,  $i_{cell}$ . In one possible approach, the current sensing module determines a voltage drop which is tied to a fixed current flow by the relationship  $\Delta V = i \cdot t / C$ , where  $\Delta V$  is the voltage drop,  $i$  is the fixed current,  $t$  is a discharge/sensing time period and  $C$  is the capacitance of the pre-charged capacitor in the current sensing module. The sensing period can be an adjustable sensing parameter, as discussed.

[00169] See also FIG. 12D, which depicts a voltage drop with time for different lines of fixed current. The greater voltage drops represent higher currents. At the end of the sensing period, since  $i$  and  $C$  are fixed,  $\Delta V$  for a given current can be determined. In one approach, a p-MOS transistor is used to determine a level of  $\Delta V$  relative to a demarcation value. In another possible approach, a cell current discriminator serves as a discriminator or comparator of current levels by determining whether the conduction current is higher or lower than a given demarcation current.

[00170] The current sensing module 1202 thus can determine whether the selected storage element is in a conductive or non-conductive state by the level of current. Generally, a higher current will flow when the selected storage element is in a conductive state and a lower current will flow when the selected storage element is in a non-conductive state. A  $V_{th}$  of the selected storage element is above or below the control gate voltage, such as a verify level or a read level, when it is in a non-conductive state or a conductive state, respectively.

[00171] FIG. 12B depicts waveforms associated with FIG. 12A. In one approach, different sensing periods are used, and a fixed pre-charge level is used. Waveform 1220 depicts  $V_{blc}$

and waveform 1222 depicts  $V_{bl}$ , when a longer sensing period (sensing period1) is used. Waveform 1221 depicts  $V_{blc}$  and waveform 1223 depicts  $V_{bl}$ , when a shorter sensing period (sensing period2) is used. Waveform 1224 depicts  $V_{bls}$ .

[00172] Waveforms 1226 and 1227 depict a sense voltage when the longer sensing period is used, and a sensed storage element is non-conductive. Waveforms 1226 and 1229 depict a sense voltage when the longer sensing period is used, and a sensed storage element is conductive. Waveforms 1228 and 1227 depict a sense voltage when the shorter sensing period is used, and a sensed storage element is non-conductive. Waveforms 1228 and 1230 depict a sense voltage when the shorter sensing period is used, and a sensed storage element is conductive. Waveform 1231 depicts a discharge level.

[00173]  $V_{bl}$  increases with  $V_{blc}$  between  $t_1$  and  $t_2$ . At  $t_2$ , the pre-charged capacitor is discharged. In practice, after rising,  $V_{bl}$  will drop slightly (not shown) if current flows in the NAND string. For example,  $V_{bl}$  may rise to 1 V when  $V_{blc} = 2$  V and the  $V_{th}$  of the BLC transistor is 1 V. When sensing, if current flows,  $V_{bl}$  may drop from 1 V to 0.9 V, for instance. Thus, the capacitor can start to discharge at  $t_{2a}$  when the longer sensing period is used, or at  $t_{2b}$  when the shorter sensing period is used.  $t_3$  is a sense time, at an end of the sensing or discharge period. A determination can be made at  $t_3$  as to whether the sensed voltage exceeds a demarcation level. It can be concluded that the selected storage element is conductive when the voltage drops below the demarcation level (DL1), or that the selected storage element is non-conductive if the voltage does not drop below the demarcation level.

[00174] In another approach, a fixed sensing period is used, but different pre-charge levels are used. Waveforms 1240 and 1241 depict a sense voltage when a higher pre-charge level is used, and a sensed storage element is non-conductive. Waveforms 1240 and 1244 depict a sense voltage when the higher pre-charge level is used, and the sensed storage element is conductive. Waveforms 1242 and 1245 depict a sense voltage when a lower pre-charge level is used, and a sensed storage element is non-conductive. Waveforms 1242 and 1243 depict a sense voltage when the lower pre-charge level is used, and a sensed storage element is conductive. Waveform 1246 depicts a discharge level. The demarcation level (DL1) is also depicted.

[00175] FIG. 12C depicts a sensing process which applies to the current sensing circuitry of FIG. 12A or the voltage sensing circuitry of FIG. 12A. A sense operation, such as a read or verify operation, begins at step 1250. Step 1252 includes setting a charge-storing element in the sensing circuitry to a desired level which is optionally based on a group number of the

storage element being sensed in the associated NAND string. Step 1254 includes allowing the charge-storing element to communicate with the bit line and the NAND string during a sensing period which is optionally based on the group number. Step 1256 includes determining whether the storage element is conductive or non-conductive using current sensing. If another sense operation is to be performed, at decision step 1258, the control flow continues at step 1250. Otherwise, the process ends at step 1260. As mentioned, one or more sensing parameters can be adjusted in the sensing operation.

**[00176]** In another approach, voltage sensing can be used. Note that the terms "current sensing" and "voltage sensing" are used informally since both can involve sensing a voltage. In contrast to current sensing, voltage sensing does not involve sensing a voltage drop which is tied to a fixed current. Instead, voltage sensing involves determining whether charge sharing occurs between a capacitor in a voltage sensing module and a capacitance of the bit line. Current is not fixed or constant during the sensing. Little or no charge sharing occurs when the selected storage element is conductive, in which case the voltage of the capacitor in the voltage sensing module does not drop significantly. Charge sharing occurs when the selected storage element is non-conductive, in which case the voltage of the capacitor in the voltage sensing module drops significantly.

**[00177]** FIG. 13A depicts a configuration of a NAND string and sensing circuitry when voltage sensing is used. An example NAND string 1312 includes four storage elements which are in communication with word lines WL0, WL1, WL2 and WL3, respectively. A bit line 1310 having a voltage  $V_{bl}$  is depicted, in addition to sensing circuitry 1300. A BLS transistor 1306, which is initially conductive, is coupled to the bit line 1310 via a sense node 1314. The BLS transistor 1306 is a high voltage transistor, and is made conductive in response to a control 1308 during sense operations. A BLC transistor 1304, which is non-conductive initially, is a low voltage transistor which is made conductive in response to the control 1308 to allow the bit line to communicate with a voltage sensing module/circuit 1302. During a sense operation, such as a read or verify operation, a pre-charge operation occurs in which a capacitor in the voltage sensing module 1302 is charged. The BLC transistor 1304 may be made conductive to allow the pre-charging. The pre-charge level of a charge-storing element in the voltage sensing module 1302 can be an adjustable sensing parameter as discussed.

**[00178]** During sensing, the bit line will charge up to a level which is based on the  $V_{th}$  of the selected storage element, and a body effect. After a certain amount of time, all the bit lines reach their DC levels, and the BLC transistor 1304 is made conductive to allow charge sharing

between the voltage sensing module 1302 and the sense node 1314 so that voltage sensing of the threshold voltage of the selected storage element can occur. The voltage sensing module 1302 may perform voltage sensing as part of a reading or verifying operation, for instance.

**[00179]** When voltage sensing occurs, the BLC transistor 1304 is made conductive so that current flows from the voltage sensing module 1302 toward the discharge path 1316, in addition to the current being discharged from the NAND string 1312 flowing toward the discharge path 1316.

**[00180]**  $V_{source}$  is provided on a source line 1311.

**[00181]** FIG. 13B depicts waveforms associated with FIG. 13A. Waveform 1300 depicts  $V_{source}$ , and waveform 1302 depicts  $V_{bls}$ . Waveform 1304 depicts  $V_{blc}$  when a longer sensing period (sensing period1) is used, and waveform 1306 depicts  $V_{blc}$  when a shorter sensing period (sensing period2) is used. In one approach, different sensing periods are used while a fixed pre-charge level is used. Waveform 1314 depicts a sensed voltage when the shorter or longer sensing period is used and the sensed storage element is non-conductive. Waveform 1310 depicts a sensed voltage when the longer sensing period is used and the sensed storage element is conductive. Waveform 1 depicts a sensed voltage when the shorter sensing period is used and the sensed storage element is conductive. Waveform 1316 depicts a discharge level. A demarcation level (DL2) is also depicted. The longer sensing period extends between  $t_{3a}$  and  $t_4$ , while the shorter sensing period extends between  $t_{3b}$  and  $t_4$ .

**[00182]** In another approach, a fixed sensing period is used while different pre-charge levels are used. Waveform 1322 depicts a sensed voltage when a higher pre-charge level is used and the sensed storage element is conductive. Waveform 1320 depicts a sensed voltage when a lower pre-charge level is used and the sensed storage element is conductive. Waveform 1326 depicts a sensed voltage when the higher pre-charge level is used and the sensed storage element is non-conductive. Waveform 1324 depicts a sensed voltage when the lower pre-charge level is used and the sensed storage element is non-conductive. A demarcation level (DL2) is also depicted.

**[00183]** As mentioned, during voltage sensing, charge sharing between the voltage sensing module and the bit line occurs when the selected storage element is non-conductive. This charge sharing lowers the sensed voltage at the voltage sensing module. Little or no charge sharing between the voltage sensing module and the bit line occurs when the selected storage element is conductive so that the sensed voltage at the voltage sensing module remains high.

[00184] At  $t_0$ ,  $V_{bls}$  increases so that the BLS transistor is conductive. At  $t_1$ ,  $V_{source}$  is applied as a common source voltage for a set of NAND strings. At  $t_{3a}$  or  $t_{3b}$ , the BLC transistor is made conductive by increasing  $V_{blc}$  as depicted by waveform 1304 or 1306, respectively, thereby starting the sensing period. The voltage sensing components may use a voltage demarcation level DL2 at a specified sense time  $t_4$ , at the end of the sensing period, to determine whether the selected storage element is conductive or non-conductive.

[00185]  $V_{source}$  is lowered at  $t_5$  and the BLS transistor is made non-conductive at  $t_6$ , indicating the end of the sense operation. The selected word line receives a read or verify control gate voltage while the unselected word lines can receive read pass voltages according to the particular sensing scheme.

[00186] Accordingly, it can be seen that, in one embodiment, a method for reading in a memory device comprises: programming a first set of memory cells connected to one word line layer (WLL $_n$ ) in a set of word line layers in a memory structure; subsequently programming a second set of memory cells connected to another word line layer (WLL $_{n+1}$ ) in the set of word line layers which is adjacent to the one word line layer, where each respective memory cell of the first set of memory cells is adjacent to, and is arranged along a common charge trapping layer with, a respective memory cell of the second set of memory cells; subsequently, in a first read operation, reading data from the first set of memory cells, the first read operation attempts to distinguish between adjacent data states stored by the first set of memory cells, the first read operation biases the another word line layer at a first voltage; determining that the data read in the first read operation comprises one or more uncorrectable errors; and in response to the determining that the data read in the first read operation comprises one or more uncorrectable errors, reading data from the first set of memory cells in a second read operation, the second read operation attempts to distinguish between the adjacent data states, the second read operation biases the another word line layer at a second voltage which is higher than the first voltage, and compensates for lower threshold voltages of the first set of memory cells in the second read operation relative to the first read operation.

[00187] In another embodiment, a memory device comprises: a first set of memory cells connected to one word line layer (WLL $_n$ ) in a set of word line layers in a memory structure; a second set of memory cells connected to another word line layer (WLL $_{n+1}$ ) in the set of word line layers, the another word line layer is adjacent to the one word line layer, and each respective memory cell of the first set of memory cells is adjacent to, and is arranged along a common charge trapping layer with, a respective memory cell of the second set of memory

cells; and a control circuit. The control circuit: programs the first set of memory cells; subsequently programs the second set of memory cells; subsequently, in a first read operation, reads data from the first set of memory cells by attempting to distinguish between adjacent data states stored by the first set of memory cells, the first read operation attempts to distinguish between adjacent data states stored by the first set of memory cells, the first read operation biases the another word line layer at a first voltage; makes a determination that the data read in the first read operation comprises one or more uncorrectable errors; and in response to the determination that the data read in the first read operation comprises one or more uncorrectable errors, reads data from the first set of memory cells in a second read operation, the second read operation attempts to distinguish between the adjacent data states, the second read operation biases the another word line layer at a second voltage which is higher than the first voltage, and compensates for lower threshold voltages of the first set of memory cells in the second read operation relative to the first read operation.

**[00188]** In another embodiment, a method for reading in a memory device comprises: programming a first set of memory cells connected to one word line layer (WLL<sub>n</sub>) in a set of word line layers in a memory structure; subsequently programming a second set of memory cells connected to another word line layer (WLL<sub>n+1</sub>) in the set of word line layers, adjacent to the one word line layer, where each respective memory cell of the first set of memory cells is adjacent to, and is arranged along a common charge trapping layer with, a respective memory cell of the second set of memory cells; subsequently, in a first read operation, reading data from the first set of memory cells by attempting to distinguish between adjacent data states stored by the first set of memory cells while biasing the another word line layer with a first voltage; performing error correction decoding on the data read in the first read operation; determining from the error correction decoding on the data read in the first read operation that the data read in the first read operation comprises one or more uncorrectable errors; and in response to the determining that the data read in the first read operation comprises one or more uncorrectable errors, performing a plurality of additional read operations for the first set of memory cells until data read from the first set of memory cells comprises no uncorrectable errors, or until a maximum allowable voltage has been applied to the another word line layer, each read operation of the plurality of additional read operations attempts to distinguish between the adjacent data states while biasing the another word line layer at a progressively higher voltage.

**[00189]** The foregoing detailed description of the invention has been presented for purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to

the precise form disclosed. Many modifications and variations are possible in light of the above teaching. The described embodiments were chosen in order to best explain the principles of the invention and its practical application, to thereby enable others skilled in the art to best utilize the invention in various embodiments and with various modifications as are suited to the particular use contemplated. It is intended that the scope of the invention be defined by the claims appended hereto.

## CLAIMS

What is claimed is:

1. A method for reading in a memory device, comprising:
  - programming a first set of memory cells (Set0, Set1, Set2, Set3) connected to one word line layer (WLLn ) in a set of word line layers (WLL0-WLL23) in a memory structure (100);
  - subsequently programming a second set of memory cells (Set0, Set1, Set2, Set3) connected to another word line layer (WLLn+1) in the set of word line layers which is adjacent to the one word line layer, where each respective memory cell (MC22D, MC22S) of the first set of memory cells is adjacent to, and is arranged along a common charge trapping layer (297) with, a respective memory cell (MC23D, MC23S) of the second set of memory cells;
  - subsequently, in a first read operation, reading data from the first set of memory cells, the first read operation attempts to distinguish between adjacent data states stored by the first set of memory cells, the first read operation biases the another word line layer at a first voltage (1110, 1111);
  - determining that the data read in the first read operation comprises one or more uncorrectable errors; and
  - in response to the determining that the data read in the first read operation comprises one or more uncorrectable errors, reading data from the first set of memory cells in a second read operation, the second read operation attempts to distinguish between the adjacent data states, the second read operation biases the another word line layer at a second voltage (1116, 1117) which is higher than the first voltage, and compensates for lower threshold voltages of the first set of memory cells in the second read operation relative to the first read operation.
  
2. The method of claim 1, further comprising:
  - determining that the data read in the second read operation comprises one or more uncorrectable errors; and
  - in response to the determining that the data read in the second read operation comprises one or more uncorrectable errors, reading data from the first set of memory cells , in a third read operation, the third read operation attempts to distinguish between the adjacent data states, the third read operation biases the another word line layer at a third voltage (1122,



1123) which is higher than the second voltage, and compensates for lower threshold voltages of the first set of memory cells in the third read operation relative to the second read operation.

3. The method of claim 1 or 2, further comprising:

the second read operation compensates for lower threshold voltages of the first set of memory cells in the second read operation relative to the first read operation by providing a control gate voltage (1104, 1105, 1106) for the first set of memory cells which is lower in the second read operation than in the first read operation.

4. The method of claim 3, further comprising:

the control gate voltage in the second read operation is adaptively determined during the second read operation.

5. The method of claim 3, further comprising:

the control gate voltage in the second read operation is lower by a predetermined amount compared to the first read operation.

6. The method of any one of claims 1 to 5, further comprising:

the second read operation compensates for lower threshold voltages of the first set of memory cells in the second read operation relative to the first read operation by providing a source voltage ( $V_{source}$ ) for the first set of memory cells which is higher in the second read operation than in the first read operation.

7. The method of any one of claims 1 to 6, further comprising:

the second read operation compensates for lower threshold voltages of the first set of memory cells in the second read operation relative to the first read operation by providing at least one of: a sensing period which is shorter in the second read operation than in the first read operation, the sensing period is used by sensing circuitry (1200) which is connected to the first set of memory cells, or a pre-charge level which is lower in the second read operation than in the first read operation, the pre-charge level is used by the sensing circuitry.

8. The method of any one of claims 1 to 7, wherein:

the second voltage is a function of a control gate voltage (1104, 1105, 1106) which is applied to the one word line layer during the second read operation.

9. The method of any one of claims 1 to 8, further comprising:

the determining that the data read in the first read operation comprises one or more uncorrectable errors comprises performing error correction decoding on the data read in the first read operation, the error correction decoding indicates a number of errors in the data read in the first read operation; and

setting the second voltage in proportion to the number of errors indicated by error correction decoding.

10. The method of any one of claims 1 to 9, wherein:

in the first read operation, the attempting to distinguish between the adjacent data states comprises applying a plurality of different control gate voltages to the one word line layer;

error correction decoding is performed on data read from the first set of memory cells for each control gate voltage of the plurality of different control gate voltages; and

an optimum control gate voltage which results in a minimum number of errors is selected from among the plurality of different control gate voltages; and

the second voltage is based on a difference between the optimum control gate voltage and a reference control gate voltage.

11. The method of any one of claims 1 to 10, further comprising:

in response to the determining that the data read in the first read operation comprises one or more uncorrectable errors, copying data from the second set of memory cells to a backup location in the memory structure, before the reading in the second read operation.

12. The method of any one of claims 1 to 11, wherein:

the memory structure is a three-dimensional stacked memory structure in which the set of word line layers comprise word line layers, the word line layers are separated by dielectric layers.

13. A memory device, comprising:

a first set of memory cells (Set0, Set1, Set2, Set3) connected to one word line layer (WLL<sub>n</sub>) in a set of word line layers in a memory structure;

a second set of memory cells (Set0, Set1, Set2, Set3) connected to another word line layer (WLL<sub>n+1</sub>) in the set of word line layers, the another word line layer is adjacent to the

one word line layer, and each respective memory cell (MC22D, MC22S) of the first set of memory cells is adjacent to, and is arranged along a common charge trapping layer (297) with, a respective memory cell (MC23D, MC23S) of the second set of memory cells; and a control circuit (110, 112, 114, 116, 122, 128, 130, 132), the control circuit is configured to:

program the first set of memory cells;

subsequently program the second set of memory cells;

subsequently, in a first read operation, read data from the first set of memory cells by attempting to distinguish between adjacent data states stored by the first set of memory cells, the first read operation attempts to distinguish between adjacent data states stored by the first set of memory cells, the first read operation biases the another word line layer at a first voltage (1110, 1111);

make a determination that the data read in the first read operation comprises one or more uncorrectable errors; and

in response to the determination that the data read in the first read operation comprises one or more uncorrectable errors, read data from the first set of memory cells in a second read operation, the second read operation attempts to distinguish between the adjacent data states, the second read operation biases the another word line layer at a second voltage (1116, 1117) which is higher than the first voltage, and compensate for lower threshold voltages of the first set of memory cells in the second read operation relative to the first read operation.

14. The memory device of claim 13, further comprising:

the second read operation compensates for lower threshold voltages of the first set of memory cells in the second read operation relative to the first read operation by providing a control gate voltage (1104, 1105, 1106) for the first set of memory cells which is lower in the second read operation than in the first read operation.

15. The memory device of claim 13 or 14, wherein:

the second read operation compensates for lower threshold voltages of the first set of memory cells in the second read operation relative to the first read operation by providing a source voltage ( $V_{source}$ ) for the first set of memory cells which is higher in the second read operation than in the first read operation.

**AMENDED CLAIMS**

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1. A method for reading in a 3D charge trapping NAND memory device, comprising:

programming a first set of memory cells (Set0, Set1, Set2, Set3) connected to one word line layer (WLL<sub>n</sub>) in a set of word line layers (WLL0-WLL23) in a memory structure (100);

subsequently programming a second set of memory cells (Set0, Set1, Set2, Set3) connected to another word line layer (WLL<sub>n+1</sub>) in the set of word line layers which is adjacent to the one word line layer, where each respective memory cell (MC22D, MC22S) of the first set of memory cells is adjacent to, and is arranged along a common charge trapping layer (297) with, a respective memory cell (MC23D, MC23S) of the second set of memory cells;

subsequently, in a first read operation, reading data from the first set of memory cells, the first read operation attempts to distinguish between adjacent data states stored by the first set of memory cells, the first read operation biases the another word line layer at a first voltage (1110, 1111);

determining that the data read in the first read operation comprises one or more uncorrectable errors; and

in response to the determining that the data read in the first read operation comprises one or more uncorrectable errors, reading data from the first set of memory cells in a second read operation, the second read operation attempts to distinguish between the adjacent data states, the second read operation biases the another word line layer at a second voltage (1116, 1117) which is higher than the first voltage, and compensates for lower threshold voltages of the first set of memory cells in the second read operation relative to the first read operation, wherein the second read operation compensates for lower threshold voltages of the first set of memory cells in the second read operation relative to the first read operation by providing a control gate voltage (1104, 1105, 1106) for the first set of memory cells which is lower in the second read operation than in the first read operation.

2. The method of claim 1, further comprising:

determining that the data read in the second read operation comprises one or more ~~uncorrectable errors; and~~

in response to the determining that the data read in the second read operation comprises one or more uncorrectable errors, reading data from the first set of memory cells, in a third read operation, the third read operation attempts to distinguish between the adjacent data states, the third read operation biases the another word line layer at a third voltage (1122, 1123) which is higher than the second voltage, and compensates for lower threshold voltages of the first set of memory cells in the third read operation relative to the second read operation.

3. The method of claim 1, wherein the control gate voltage in the second read operation is adaptively determined during the second read operation.

4. The method of claim 1, wherein the control gate voltage in the second read operation is lower by a predetermined amount compared to the first read operation.

5. The method of any one of claims 1 to 4, wherein the second read operation compensates for lower threshold voltages of the first set of memory cells in the second read operation relative to the first read operation by providing a source voltage ( $V_{source}$ ) for the first set of memory cells which is higher in the second read operation than in the first read operation.

6. The method of any one of claims 1 to 5, wherein the second read operation compensates for lower threshold voltages of the first set of memory cells in the second read operation relative to the first read operation by providing at least one of: a sensing period which is shorter in the second read operation than in the first read operation, the sensing period is used by sensing circuitry (1200) which is connected to the first set of memory cells, or a pre-charge level which is lower in the second read operation than in the first read operation, the pre-charge level is used by the sensing circuitry.

7. The method of any one of claims 1 to 6, wherein:  
the second voltage is a function of a control gate voltage (1104, 1105, 1106) which is applied to the one word line layer during the second read operation.

8. The method of any one of claims 1 to 7, wherein the determining that the data read in the first read operation comprises one or more uncorrectable errors comprises performing error correction decoding on the data read in the first read operation, the error correction decoding indicates a number of errors in the data read in the first read operation; and the method further comprises setting the second voltage in proportion to the number of errors indicated by error correction decoding.

9. The method of any one of claims 1 to 8, wherein:

in the first read operation, the attempting to distinguish between the adjacent data states comprises applying a plurality of different control gate voltages to the one word line layer;

error correction decoding is performed on data read from the first set of memory cells for each control gate voltage of the plurality of different control gate voltages; and

an optimum control gate voltage which results in a minimum number of errors is selected from among the plurality of different control gate voltages; and

the second voltage is based on a difference between the optimum control gate voltage and a reference control gate voltage.

10. The method of any one of claims 1 to 9, further comprising:

in response to the determining that the data read in the first read operation comprises one or more uncorrectable errors, copying data from the second set of memory cells to a backup location in the memory structure, before the reading in the second read operation.

11. The method of any one of claims 1 to 10, wherein:

the memory structure is a three-dimensional stacked memory structure in which the set of word line layers comprise word line layers, the word line layers are separated by dielectric layers.

12. A 3D charge trapping NAND memory device, comprising:

a first set of memory cells (Set0, Set1, Set2, Set3) connected to one word line layer (WLL<sub>n</sub>) in a set of word line layers in a memory structure;

~~a second set of memory cells (Set0, Set1, Set2, Set3) connected to another word line layer (WLL<sub>n+1</sub>) in the set of word line layers, the another word line layer is adjacent to the~~

one word line layer, and each respective memory cell (MC22D, MC22S) of the first set of memory cells is adjacent to, and is arranged along a common charge trapping layer (297) with, a respective memory cell (MC23D, MC23S) of the second set of memory cells; and a control circuit (110, 112, 114, 116, 122, 128, 130, 132), the control circuit is configured to:

program the first set of memory cells;

subsequently program the second set of memory cells;

subsequently, in a first read operation, read data from the first set of memory cells by attempting to distinguish between adjacent data states stored by the first set of memory cells, the first read operation attempts to distinguish between adjacent data states stored by the first set of memory cells, the first read operation biases the another word line layer at a first voltage (1110, 1111);

make a determination that the data read in the first read operation comprises one or more uncorrectable errors; and

in response to the determination that the data read in the first read operation comprises one or more uncorrectable errors, read data from the first set of memory cells in a second read operation, the second read operation attempts to distinguish between the adjacent data states, the second read operation biases the another word line layer at a second voltage (1116, 1117) which is higher than the first voltage, and compensate for lower threshold voltages of the first set of memory cells in the second read operation relative to the first read operation, wherein the second read operation compensates for lower threshold voltages of the first set of memory cells in the second read operation relative to the first read operation by providing a control gate voltage (1104, 1105, 1106) for the first set of memory cells which is lower in the second read operation than in the first read operation..

13. The 3D charge trapping NAND memory device of claim 12, wherein:

the second read operation compensates for lower threshold voltages of the first set of memory cells in the second read operation relative to the first read operation by providing a source voltage ( $V_{source}$ ) for the first set of memory cells which is higher in the second read operation than in the first read operation.

Fig. 1A

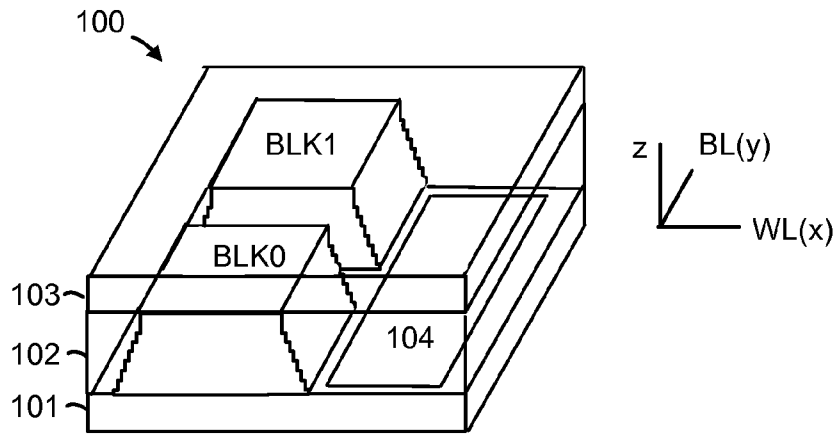


Fig. 1B

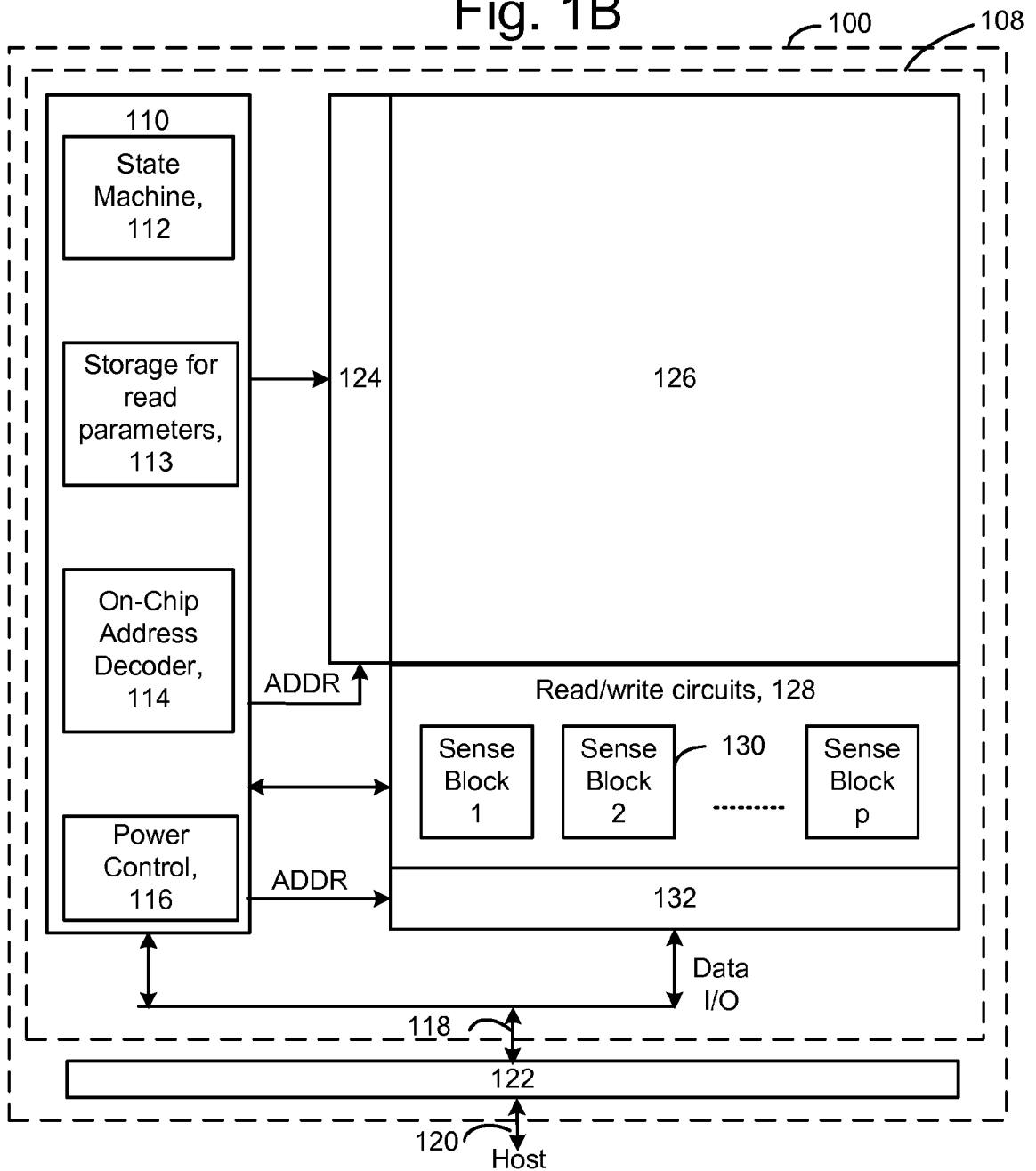




Fig. 2A

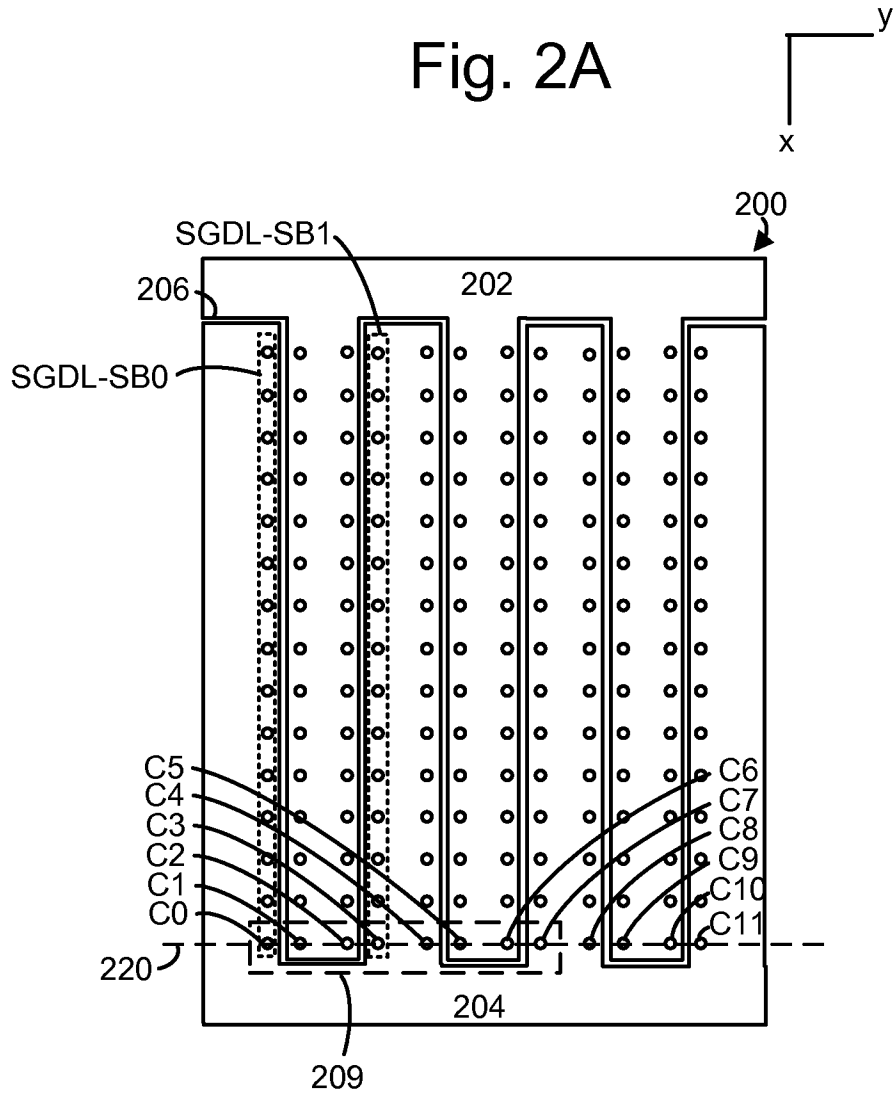


Fig. 2B1

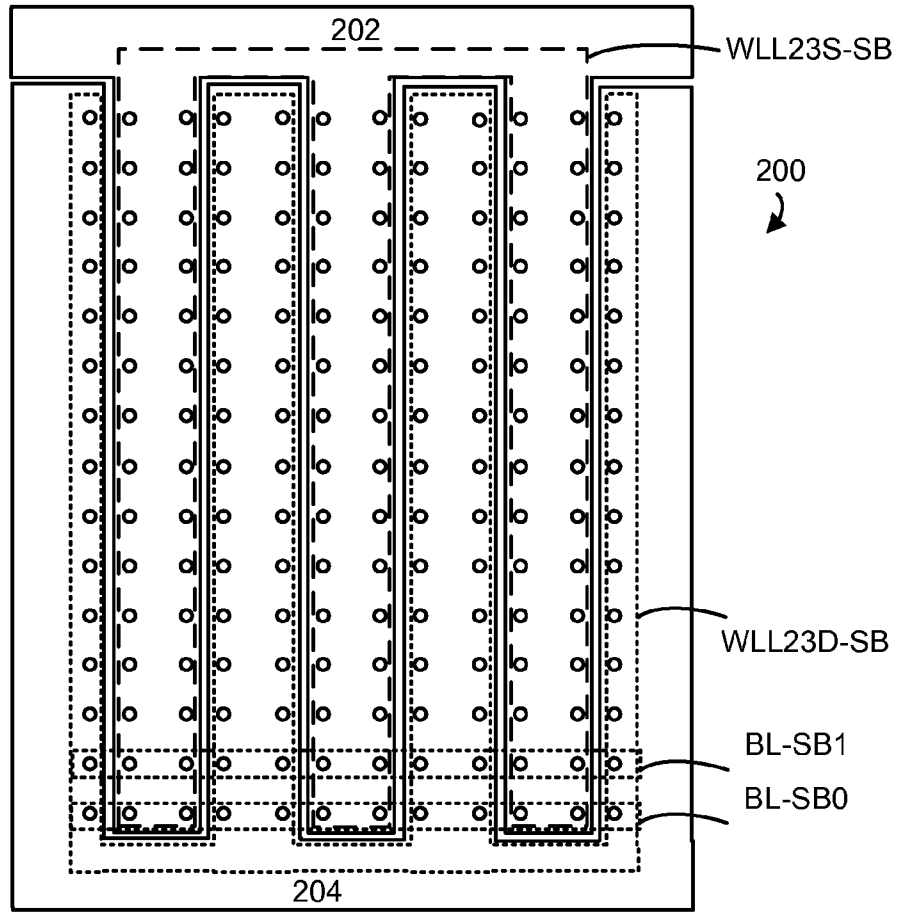
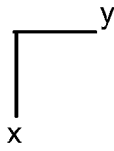


Fig. 2B2

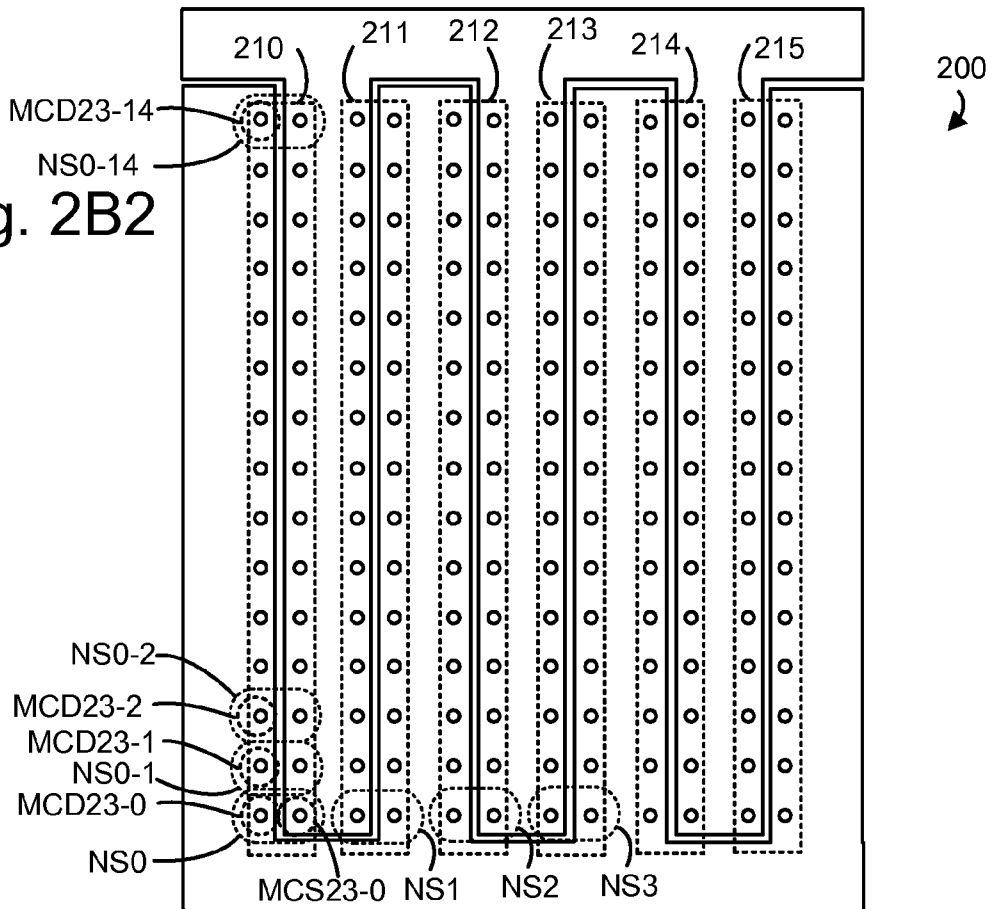
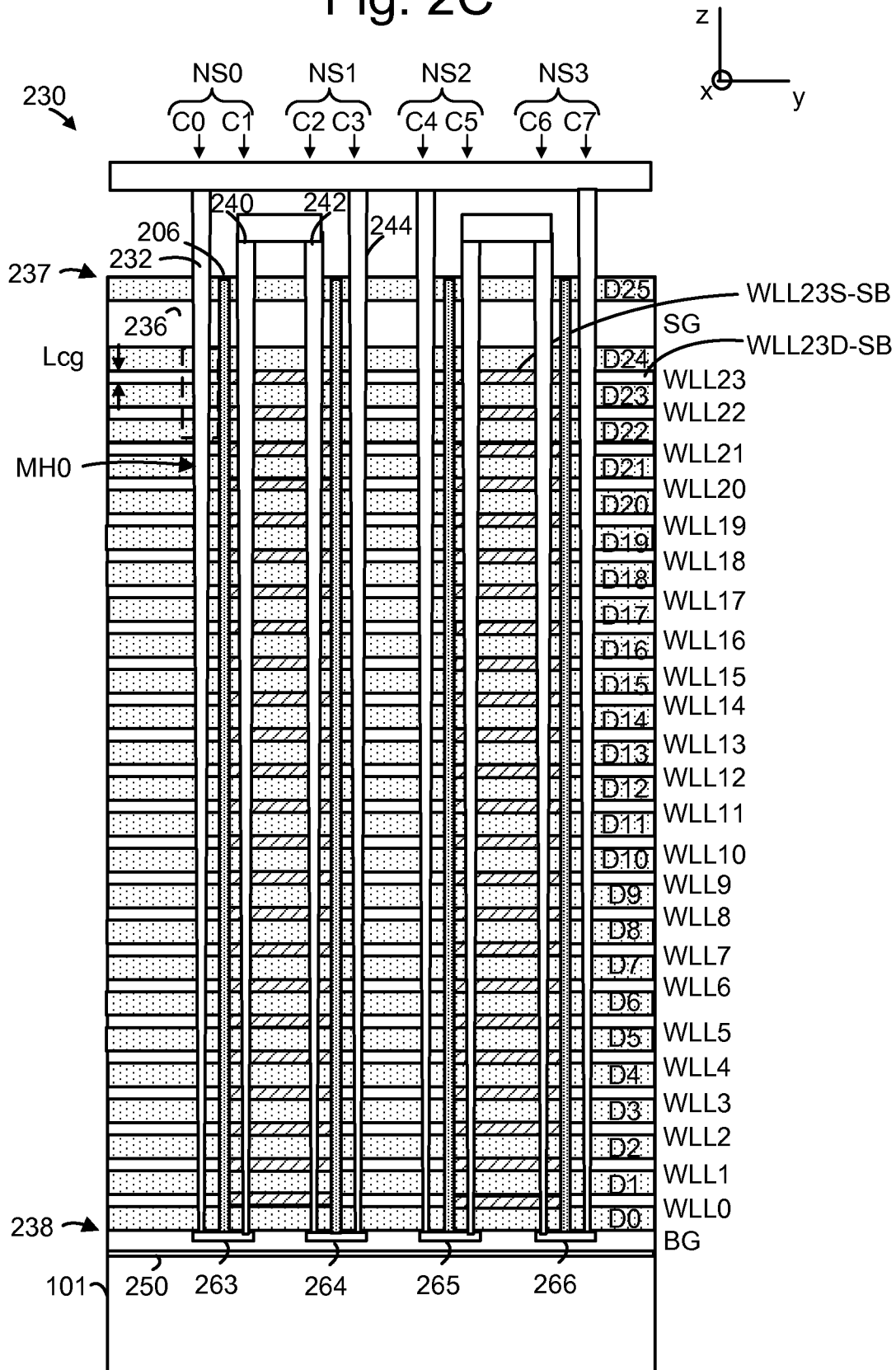
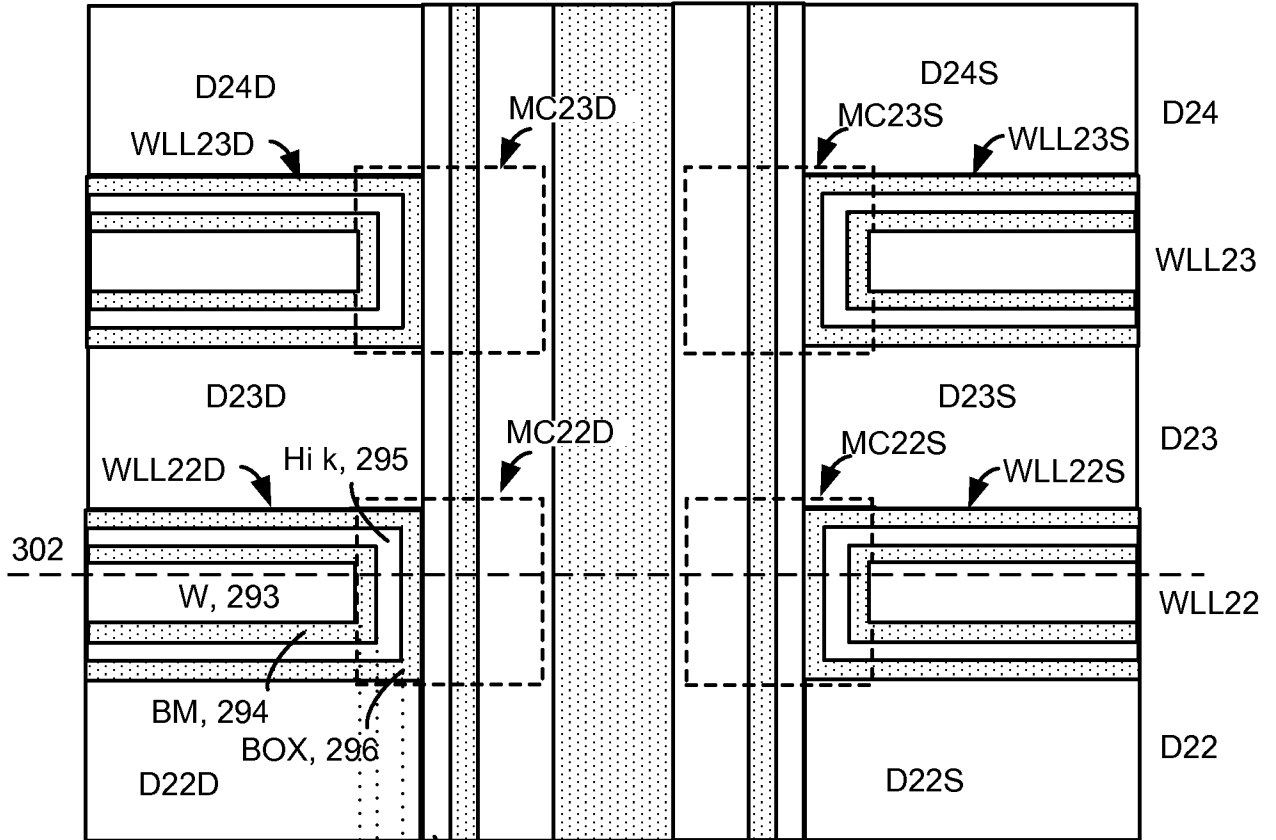


Fig. 2C



236 Fig. 3A



CTL, 297  
TNL, 298  
Ch, 299  
Core, 300

Fig. 3B

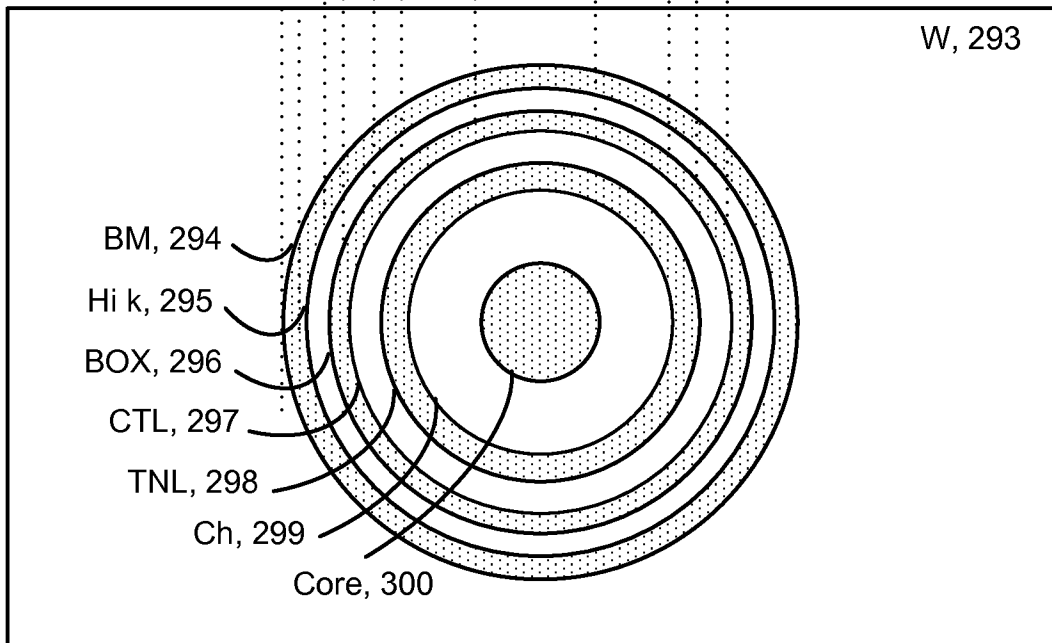


Fig. 3C

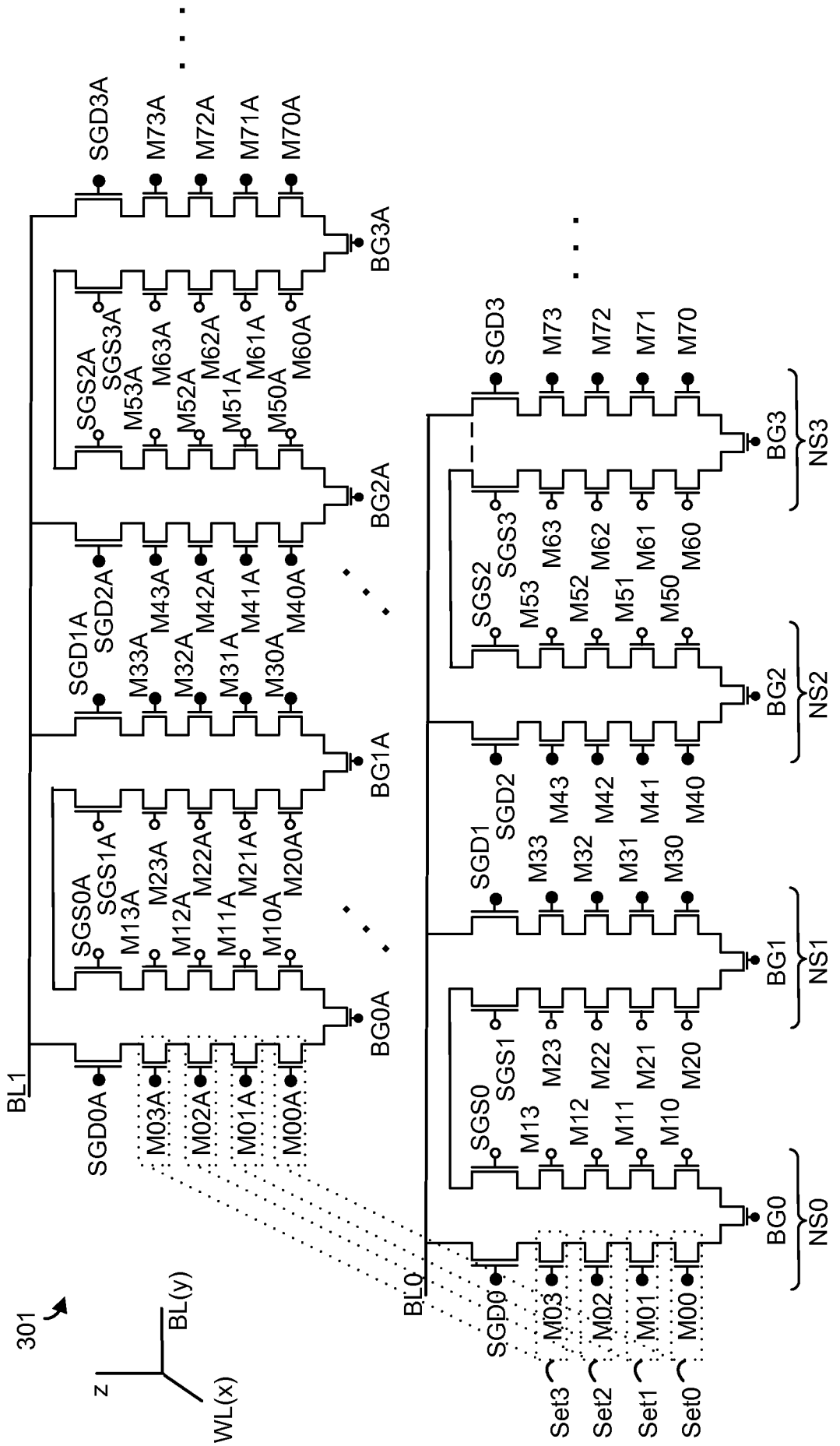


Fig. 4A

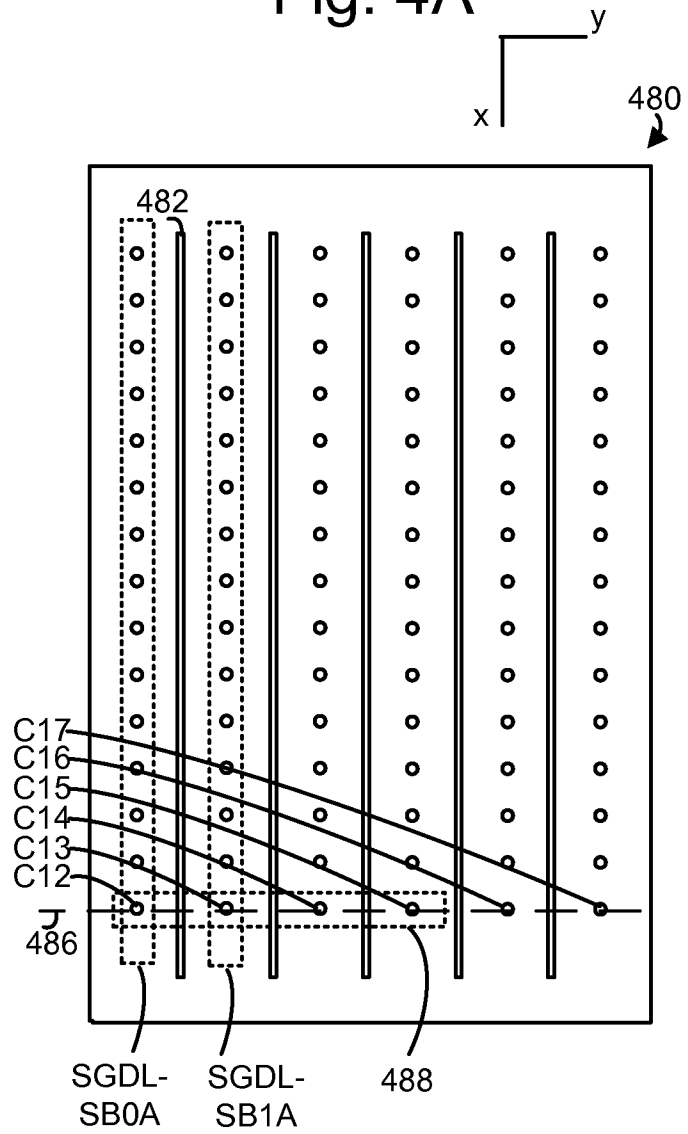


Fig. 4B1

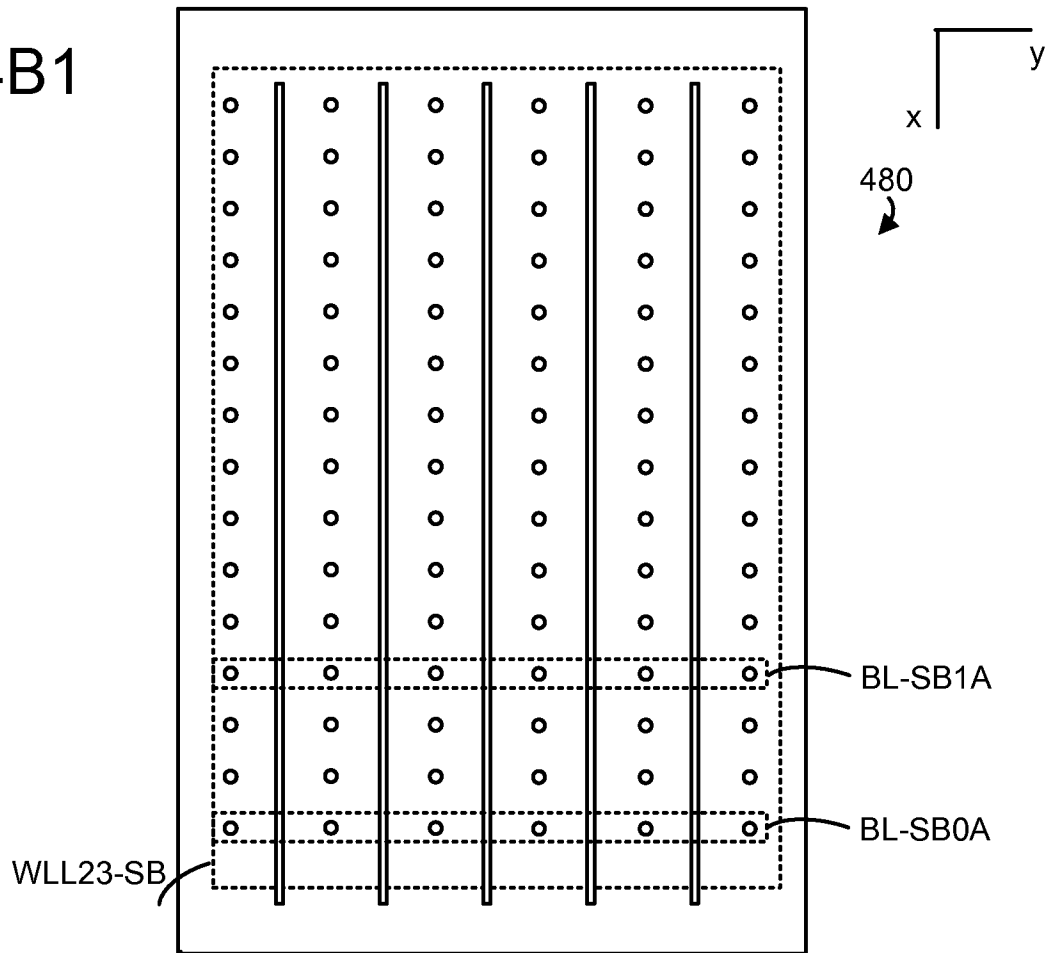


Fig. 4B2

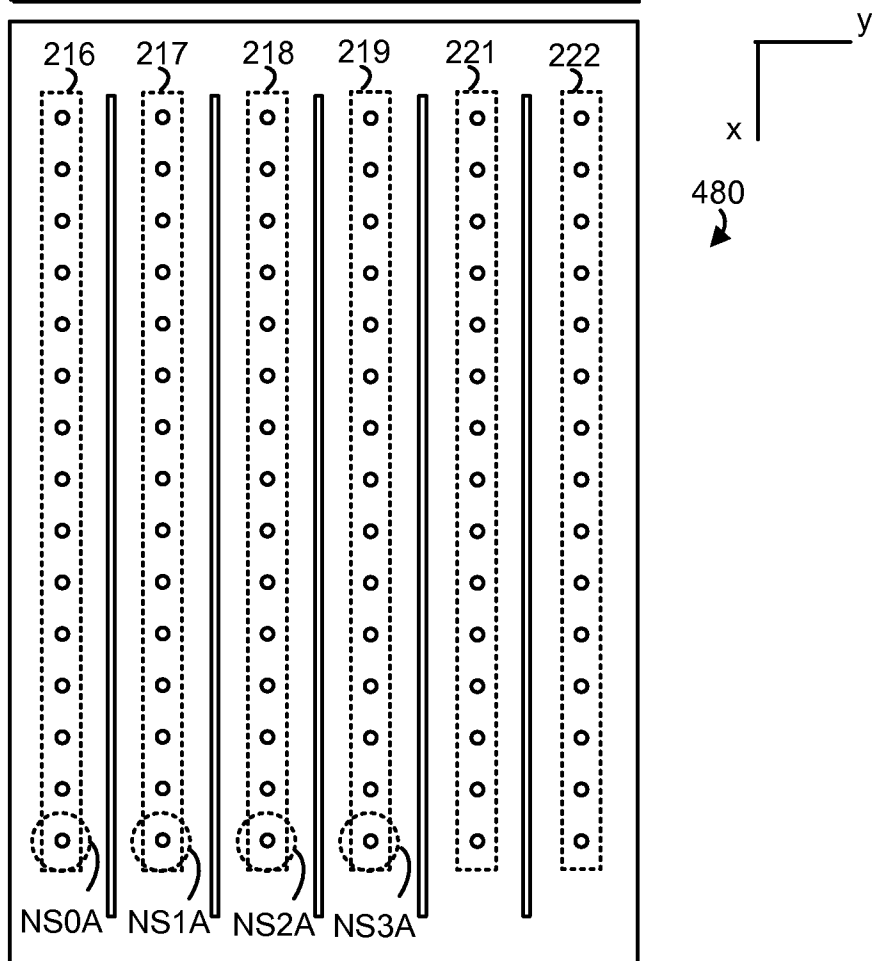


Fig. 4C

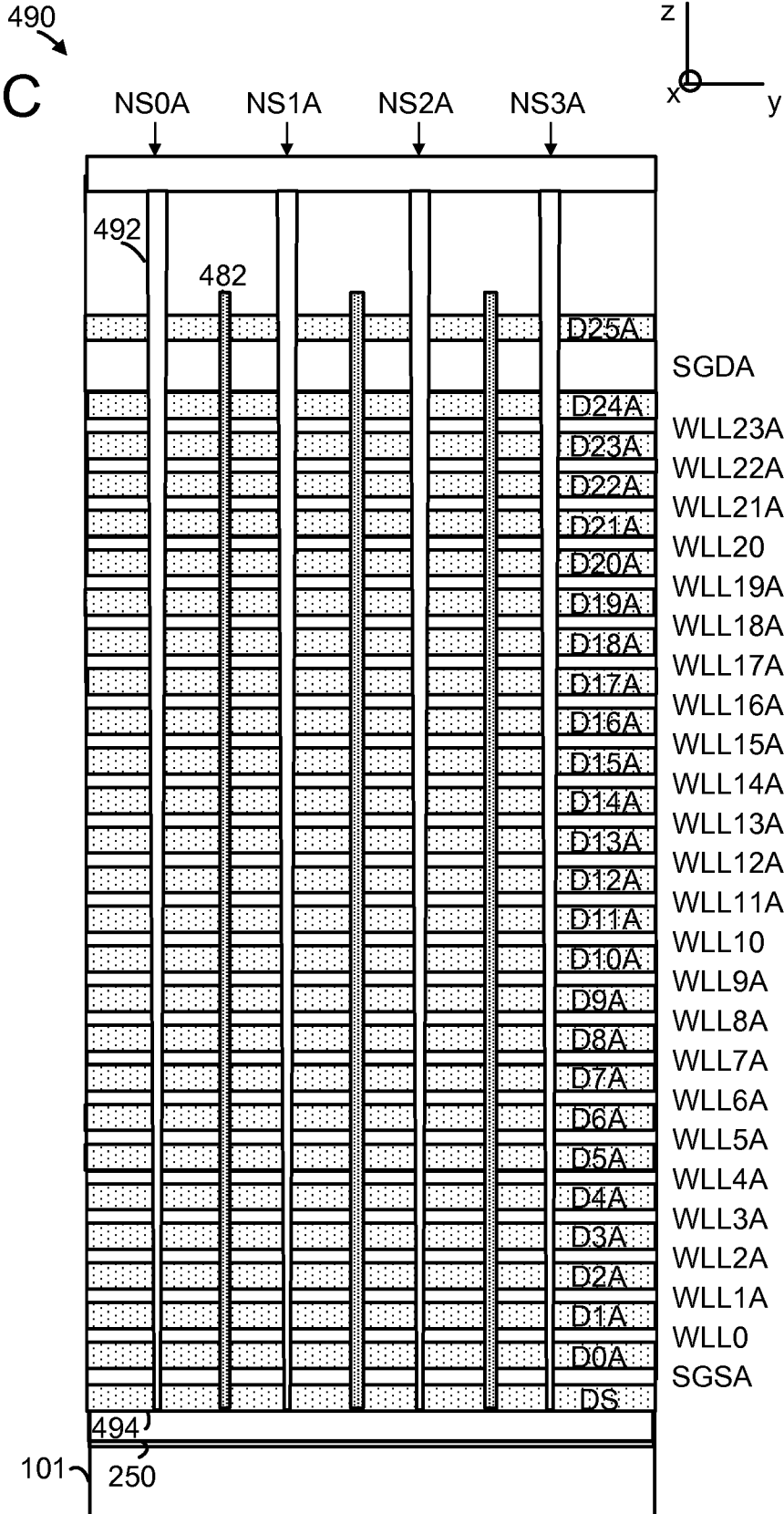




Fig. 5A

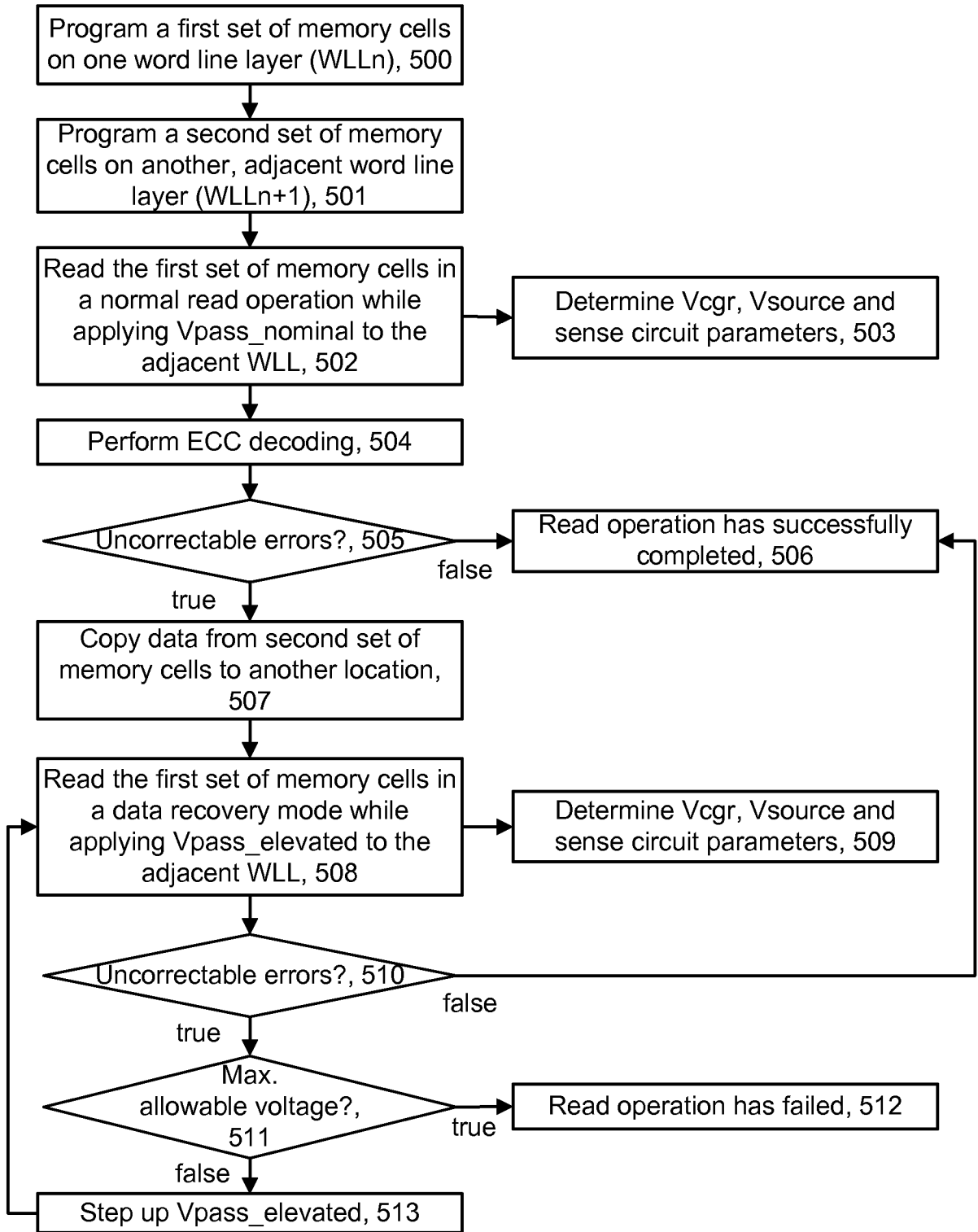
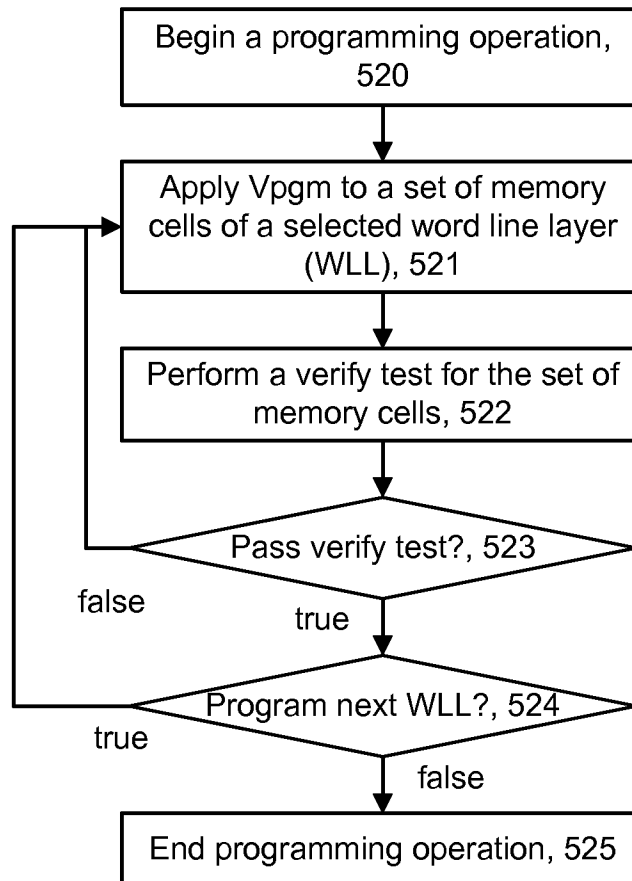
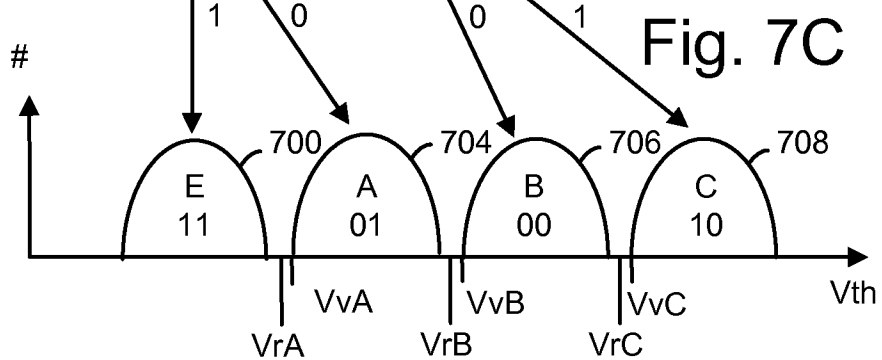
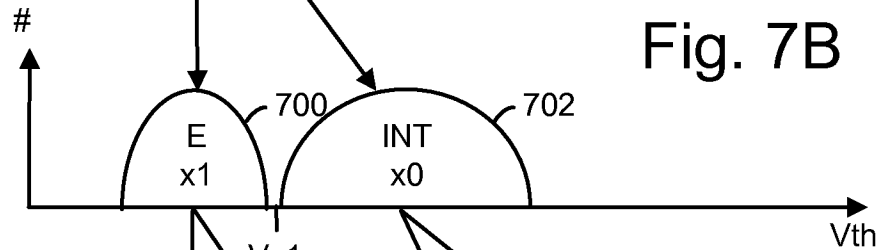
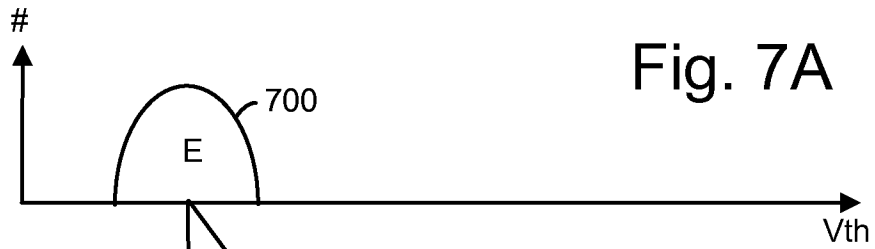
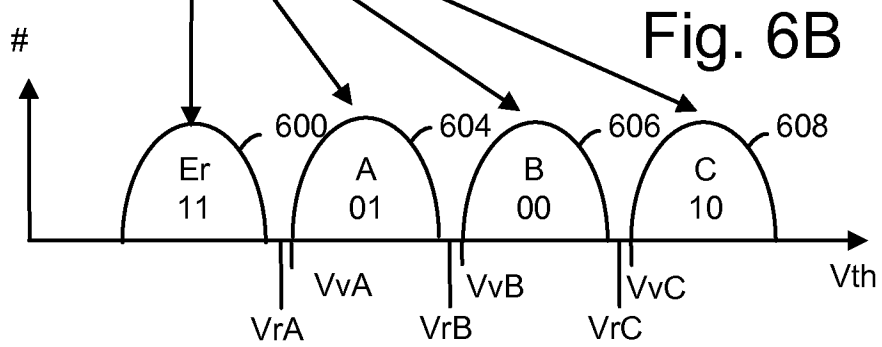
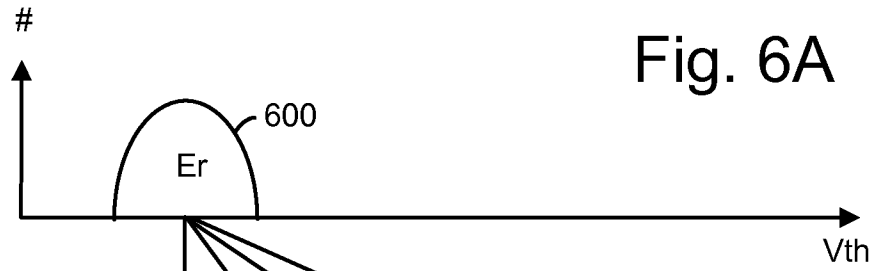
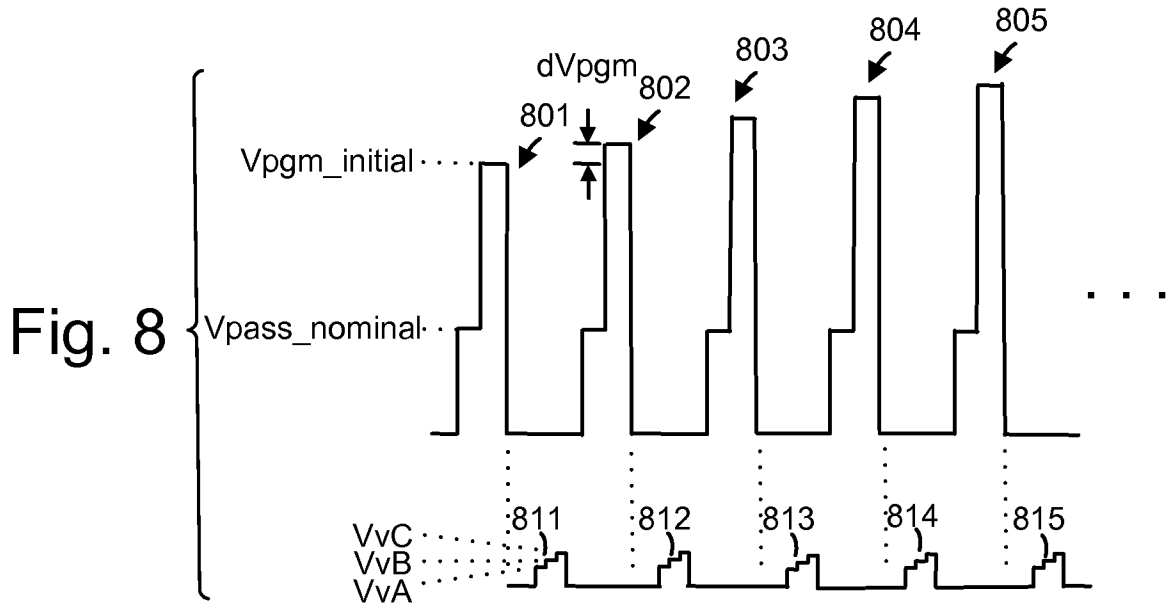


Fig. 5B







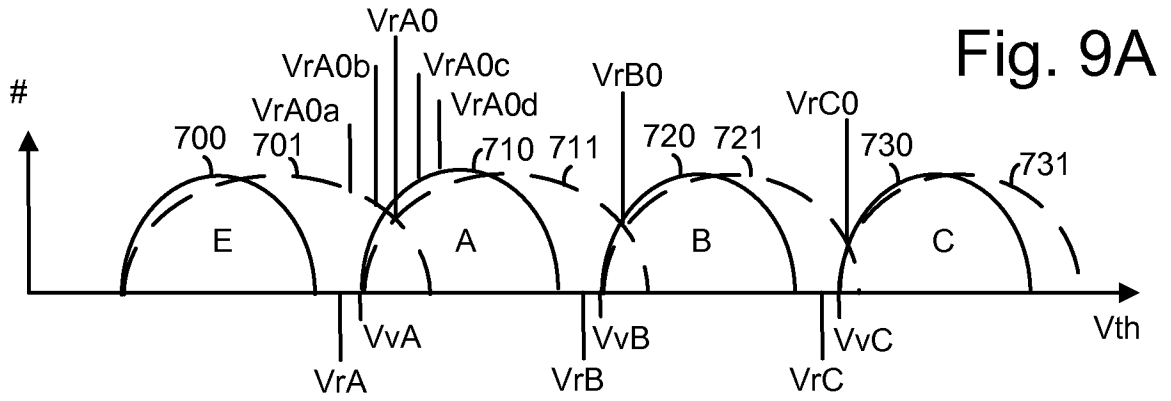


Fig. 9A

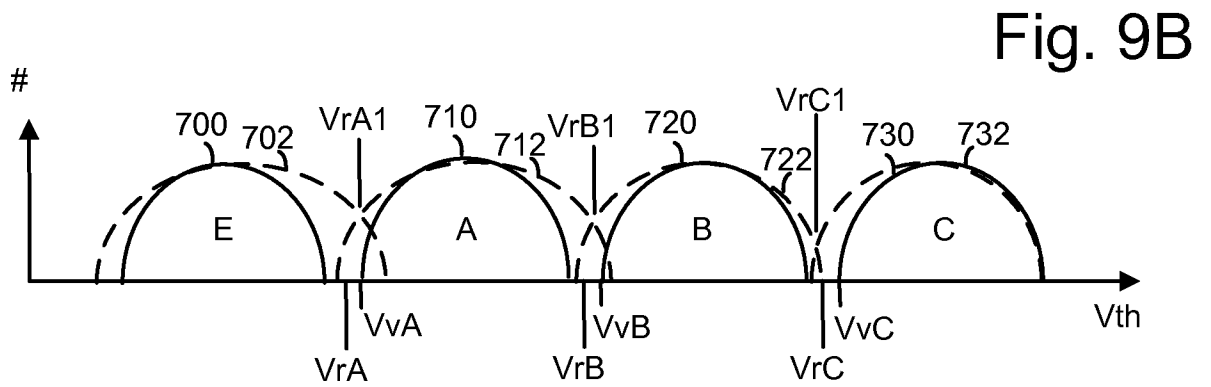


Fig. 9B

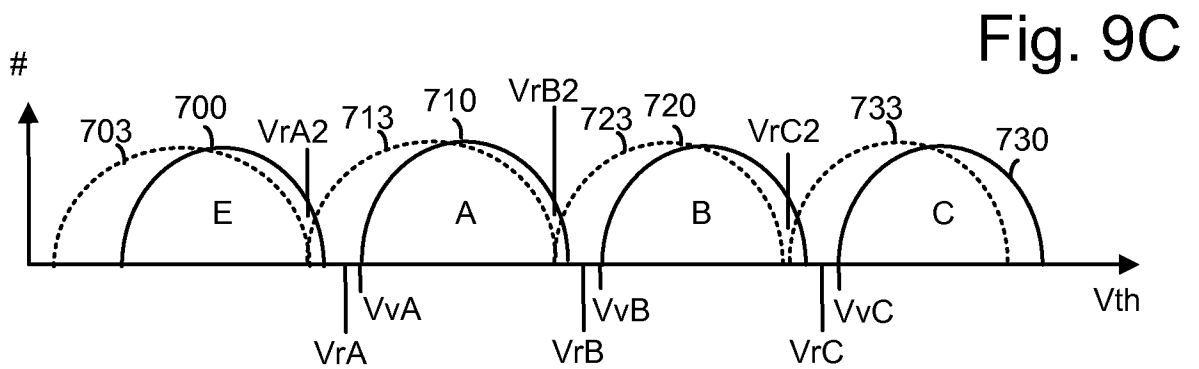


Fig. 9C

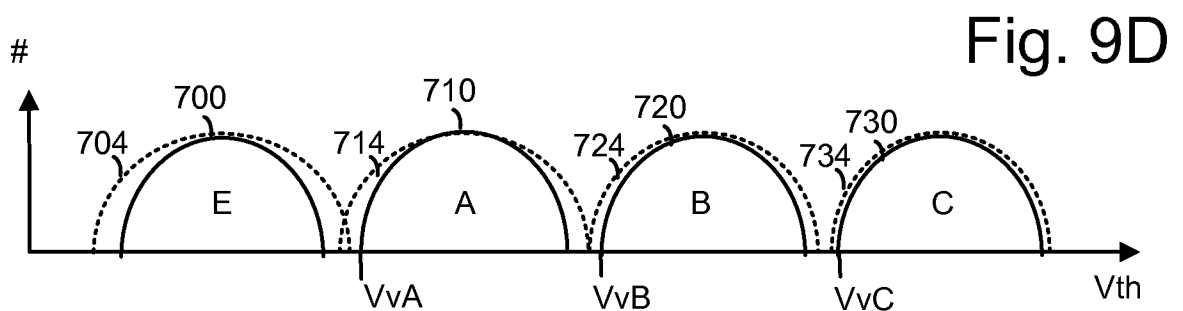


Fig. 9D

Fig. 10A

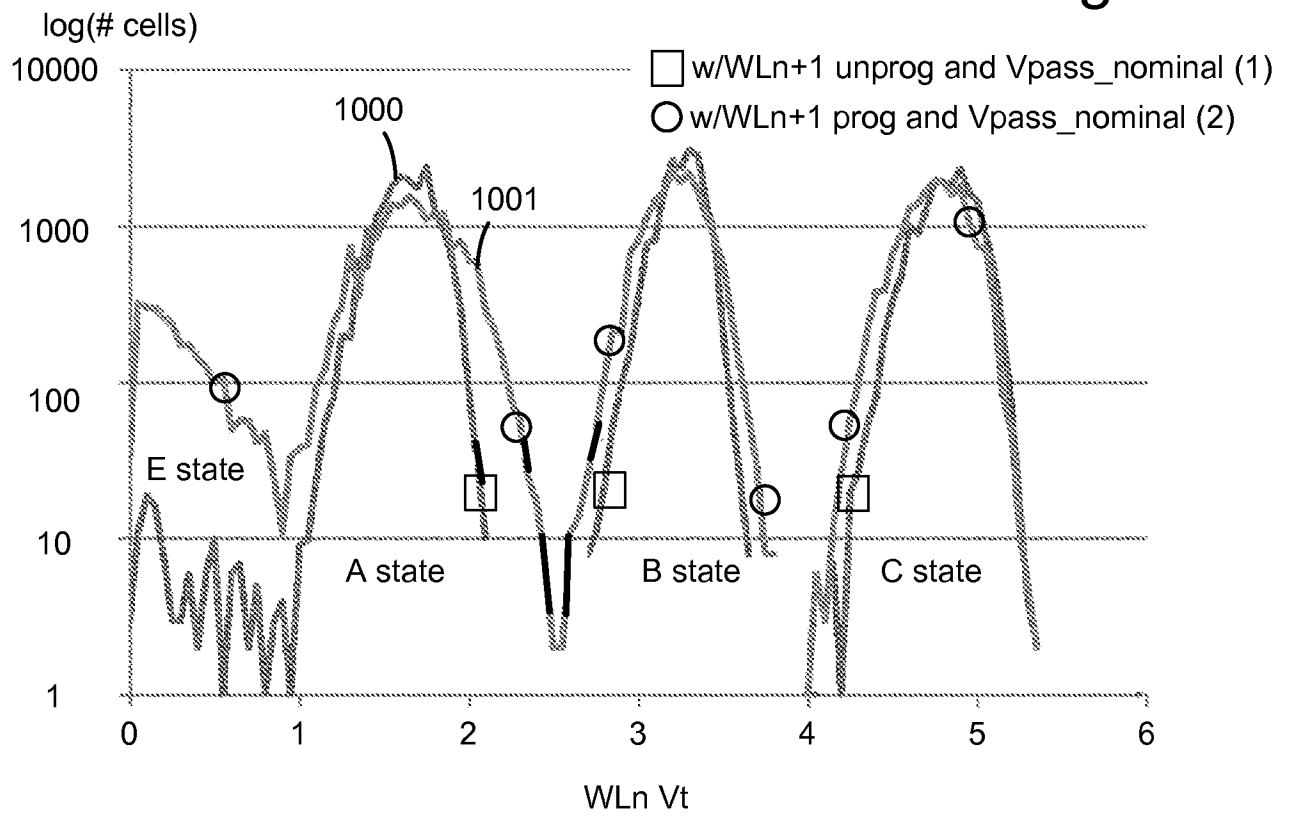
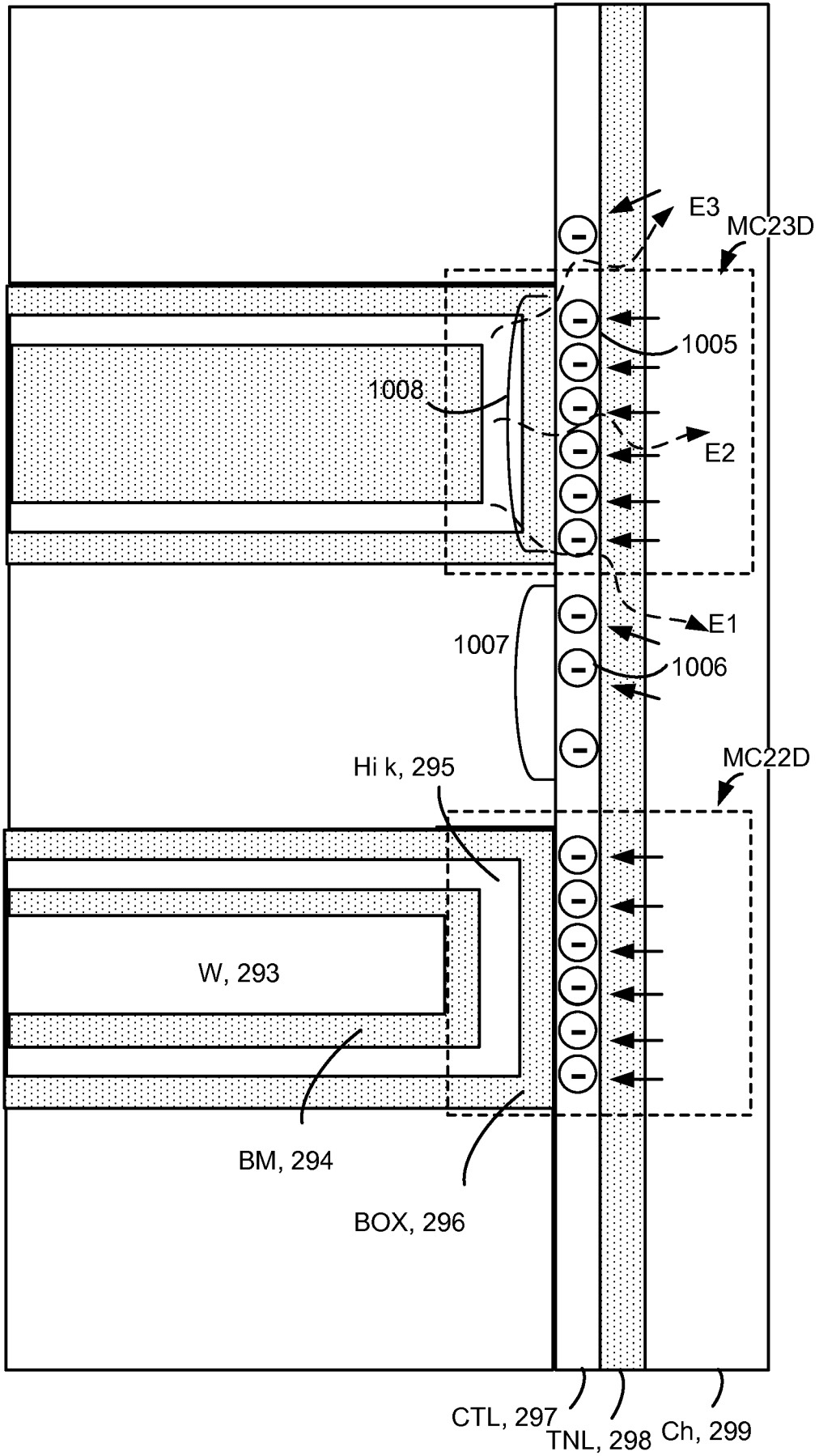


Fig. 10B



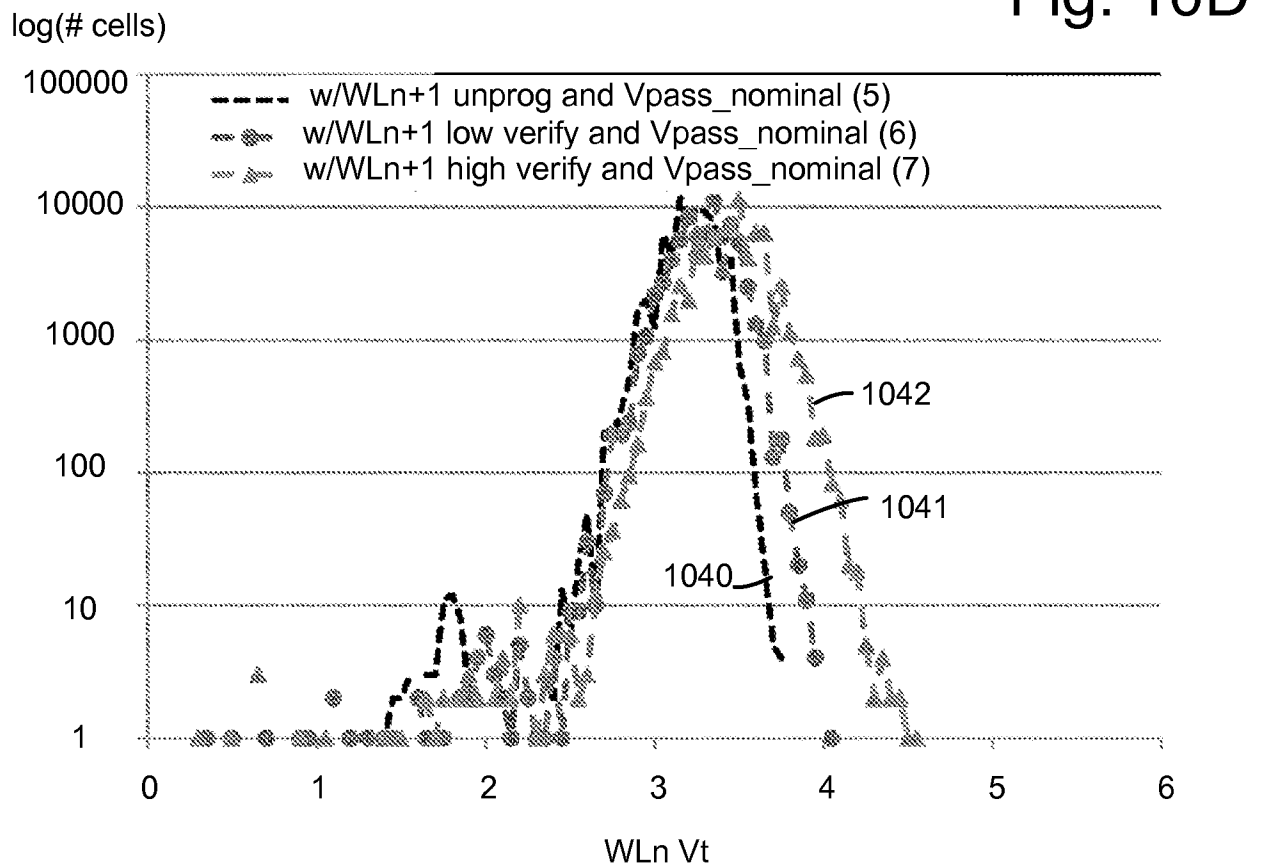
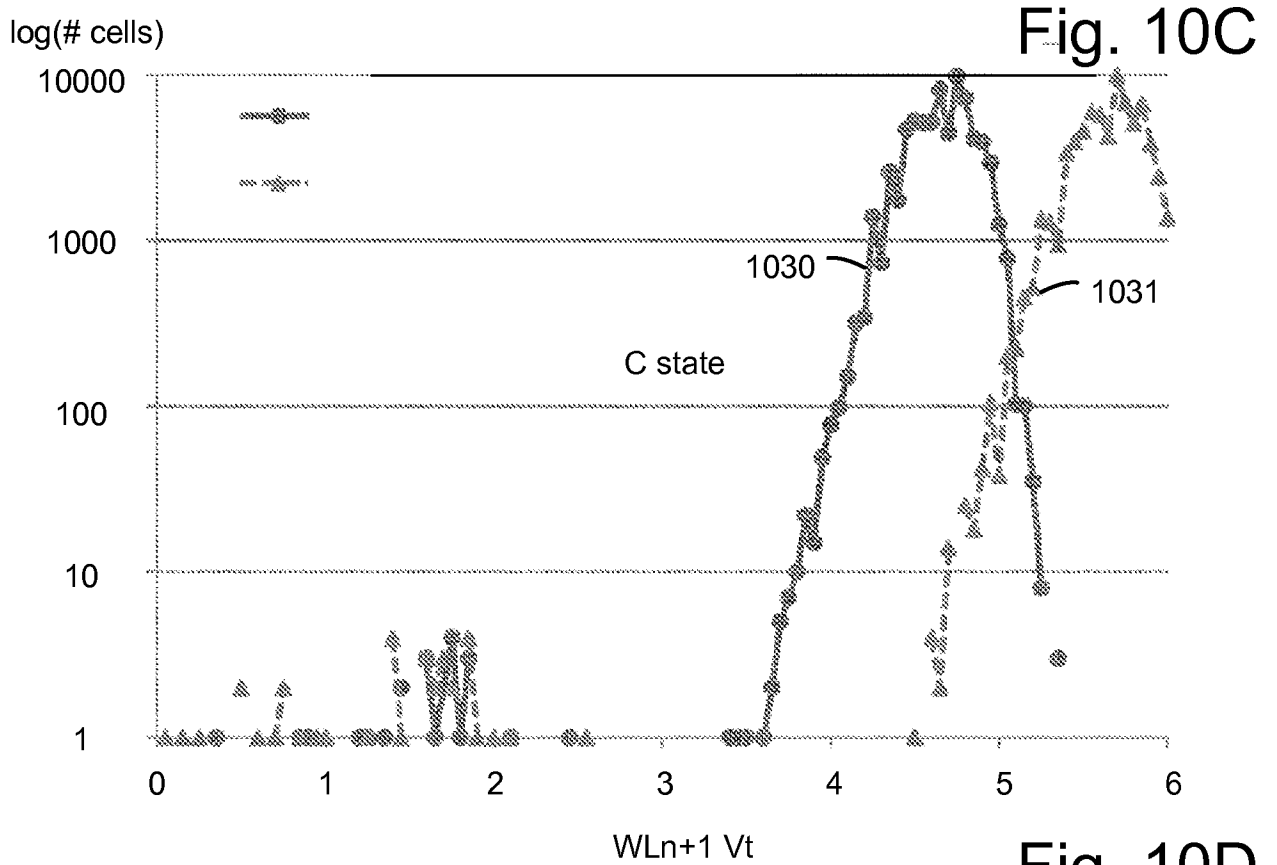
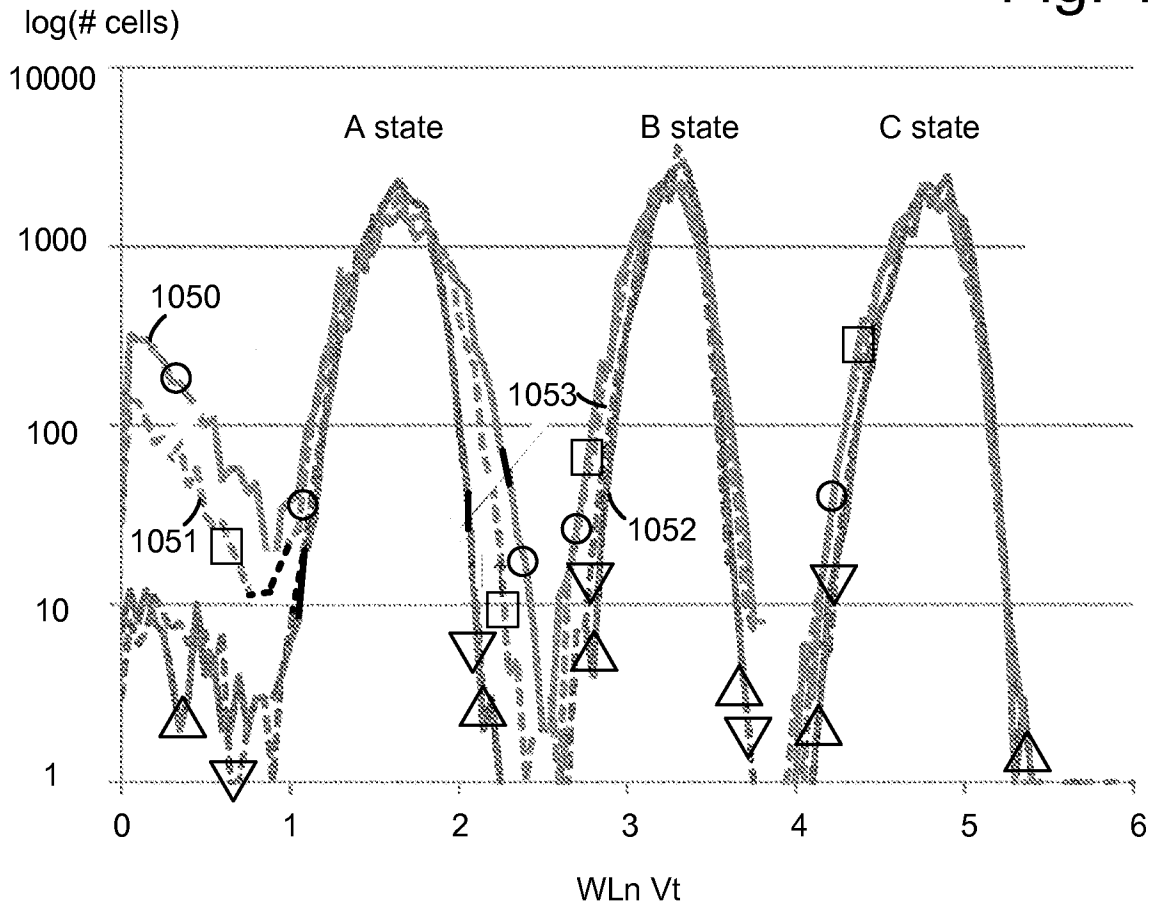




Fig. 10E



- △ w/WLn+1 unprog and Vpass\_nominal (8)
- w/WLn+1 prog and Vpass\_nominal (9)
- ▽ w/WLn+1 unprog and Vpass\_elevated (10)
- w/WLn+1 prog and Vpass\_elevated (11)

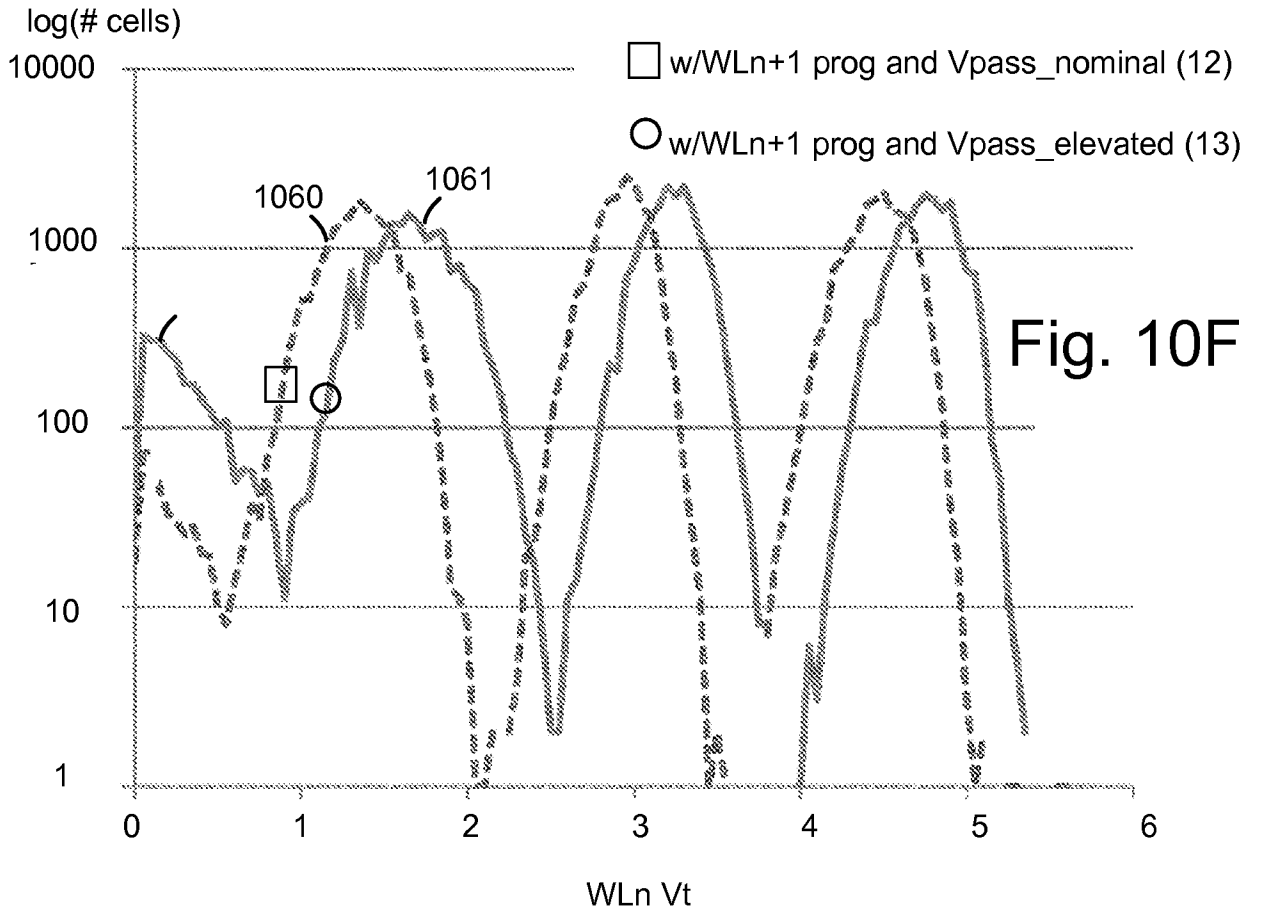


Fig. 10F

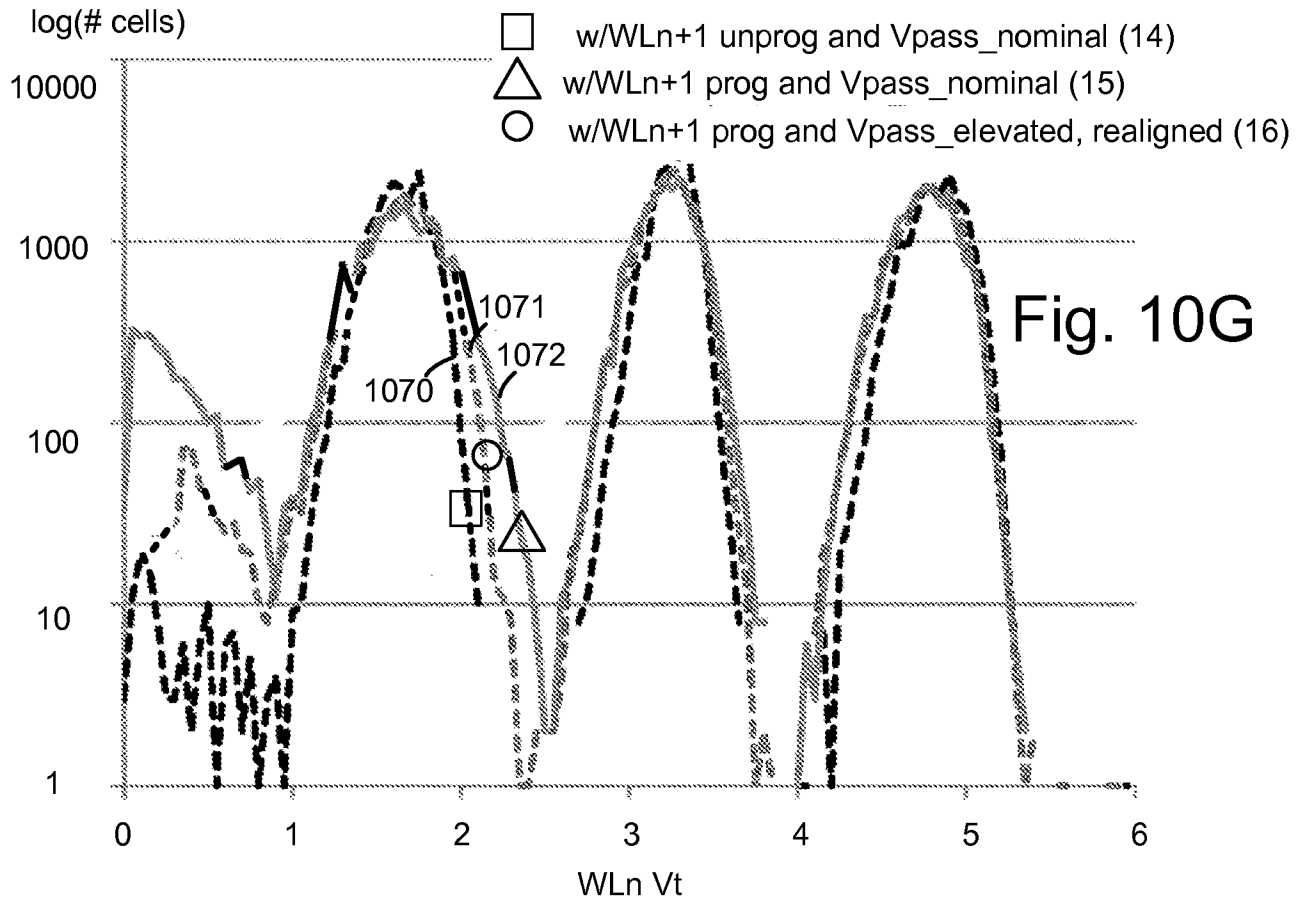


Fig. 10G

Fig. 11A

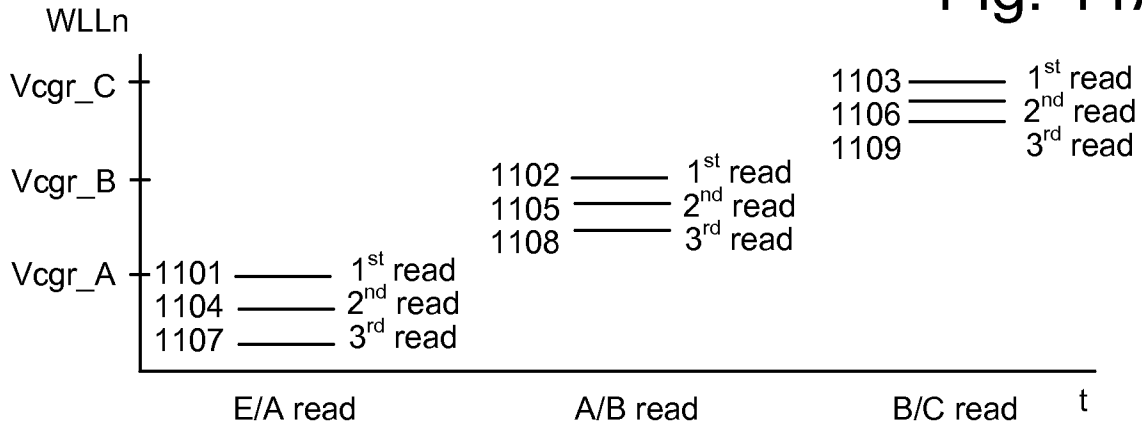


Fig. 11B

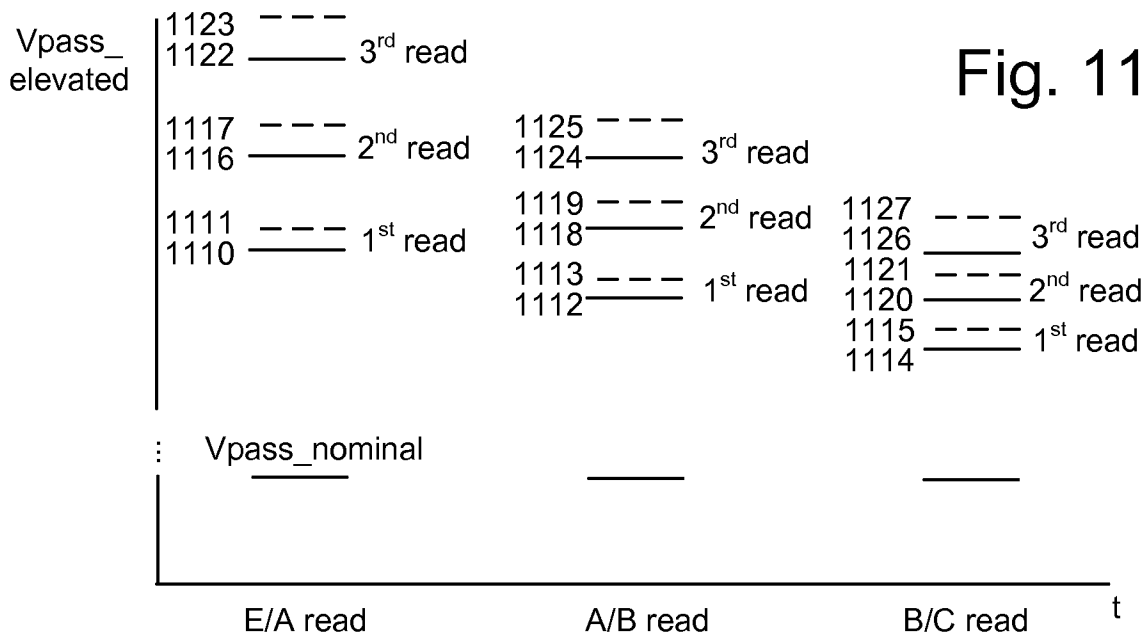


Fig. 11C

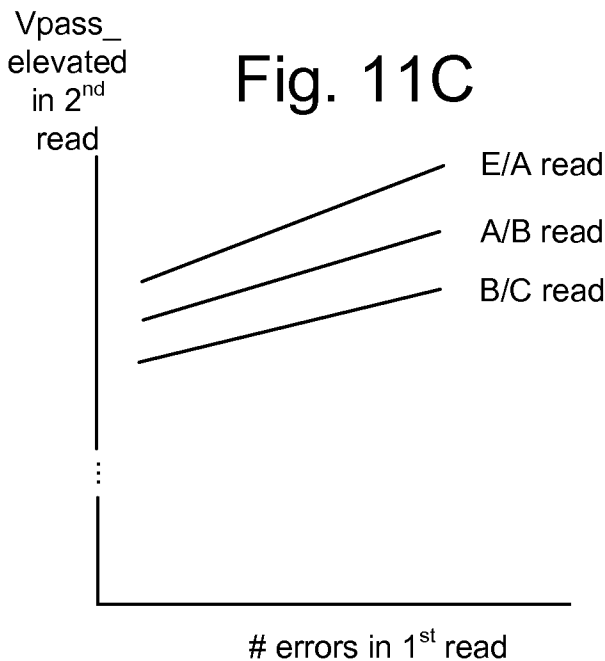


Fig. 11D

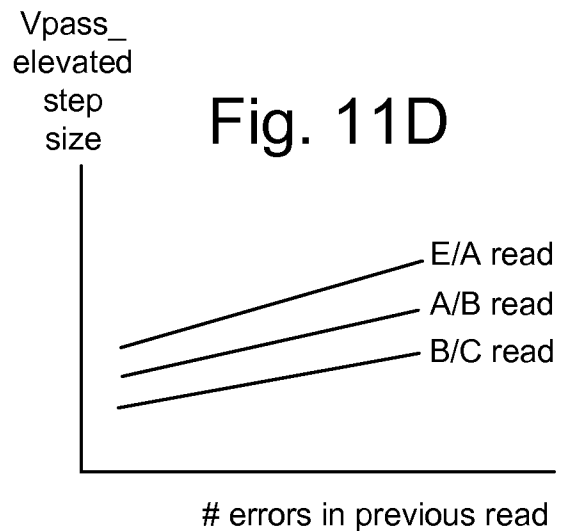


Fig. 11E

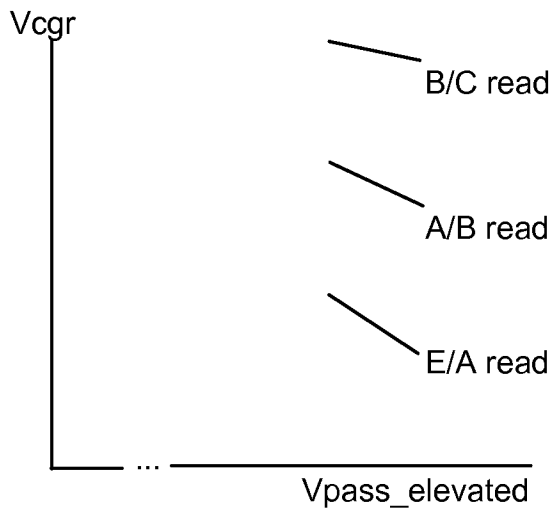


Fig. 11F

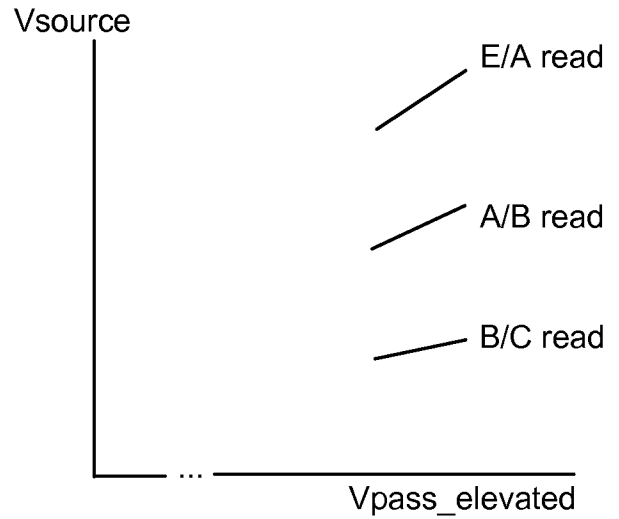


Fig. 11G

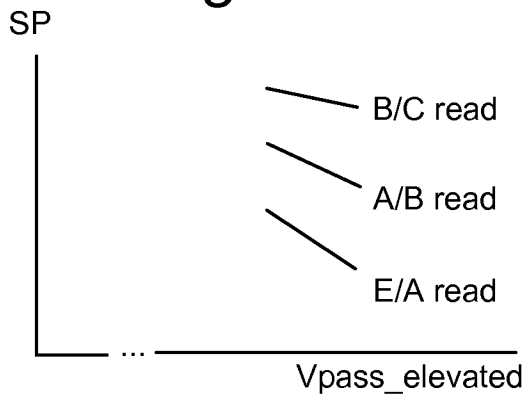


Fig. 11H

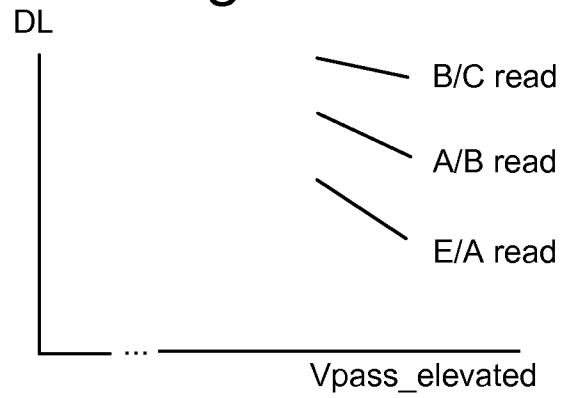


Fig. 11I

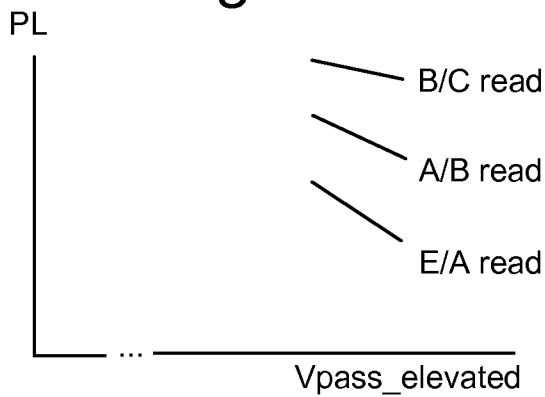


Fig. 11J

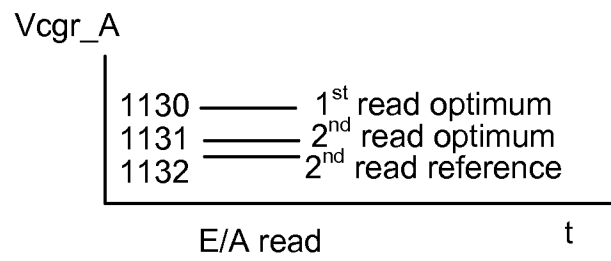


Fig. 11K

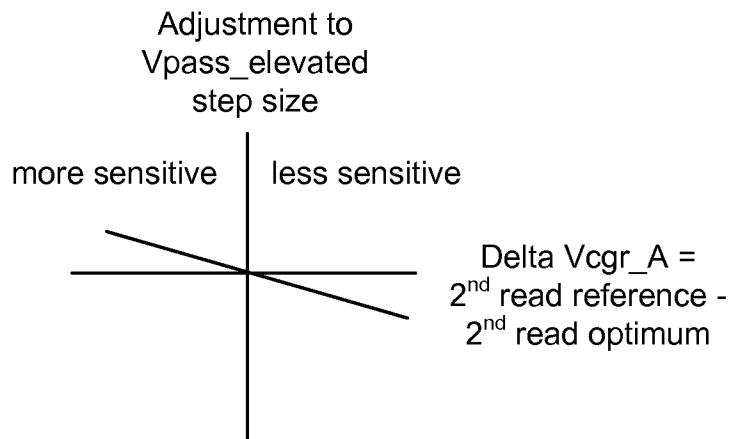


Fig. 12A

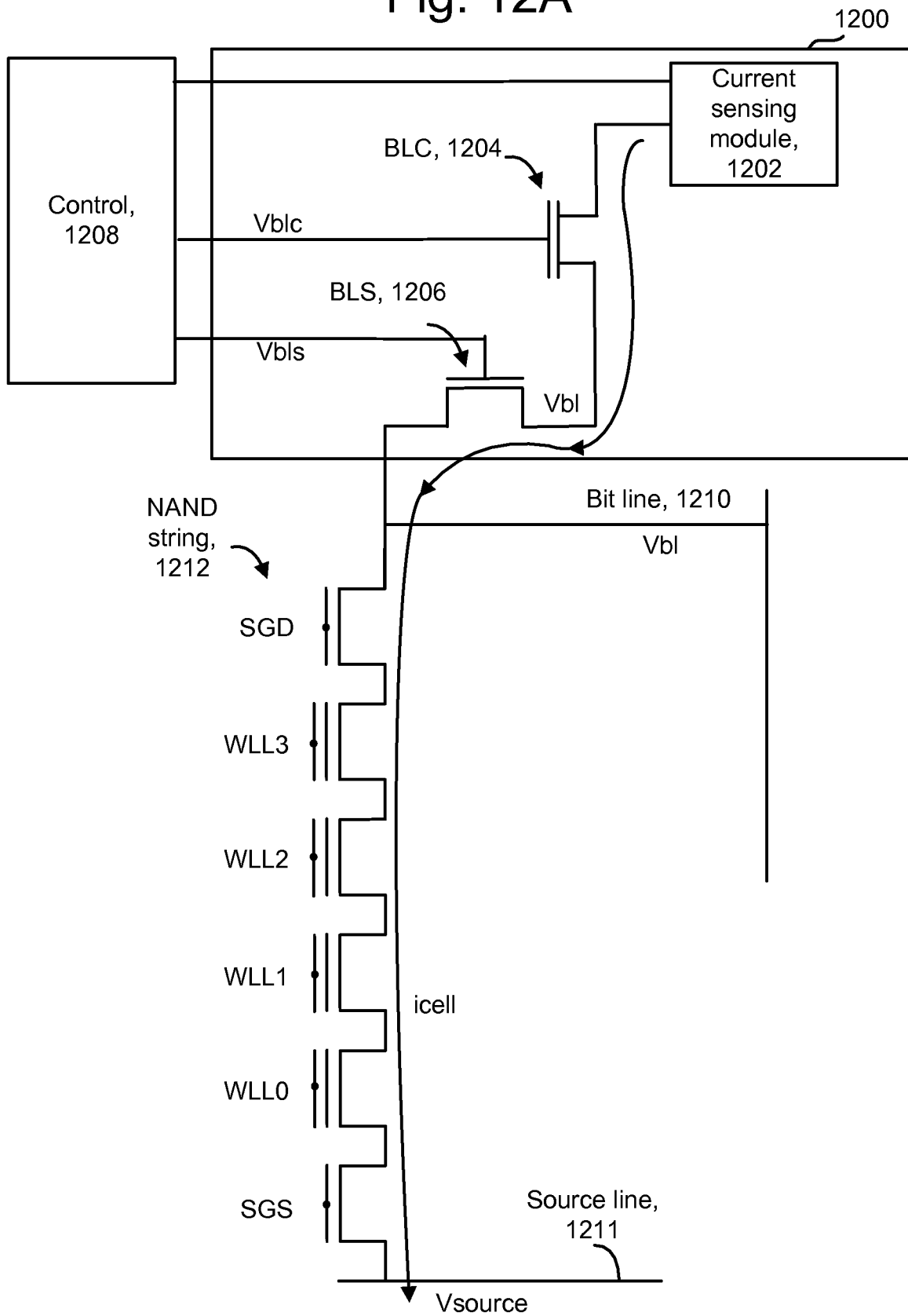


Fig. 12B

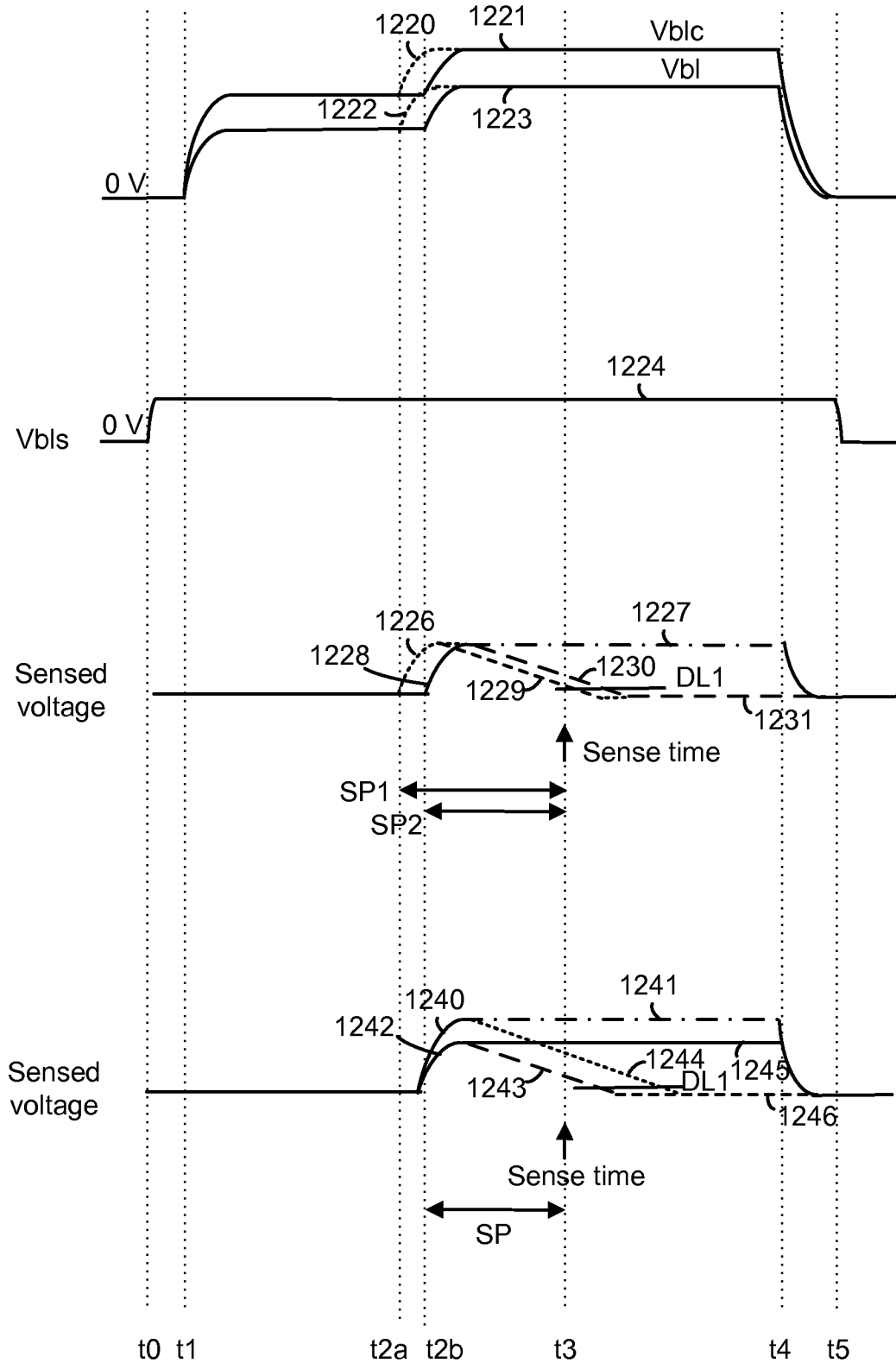


Fig. 12C

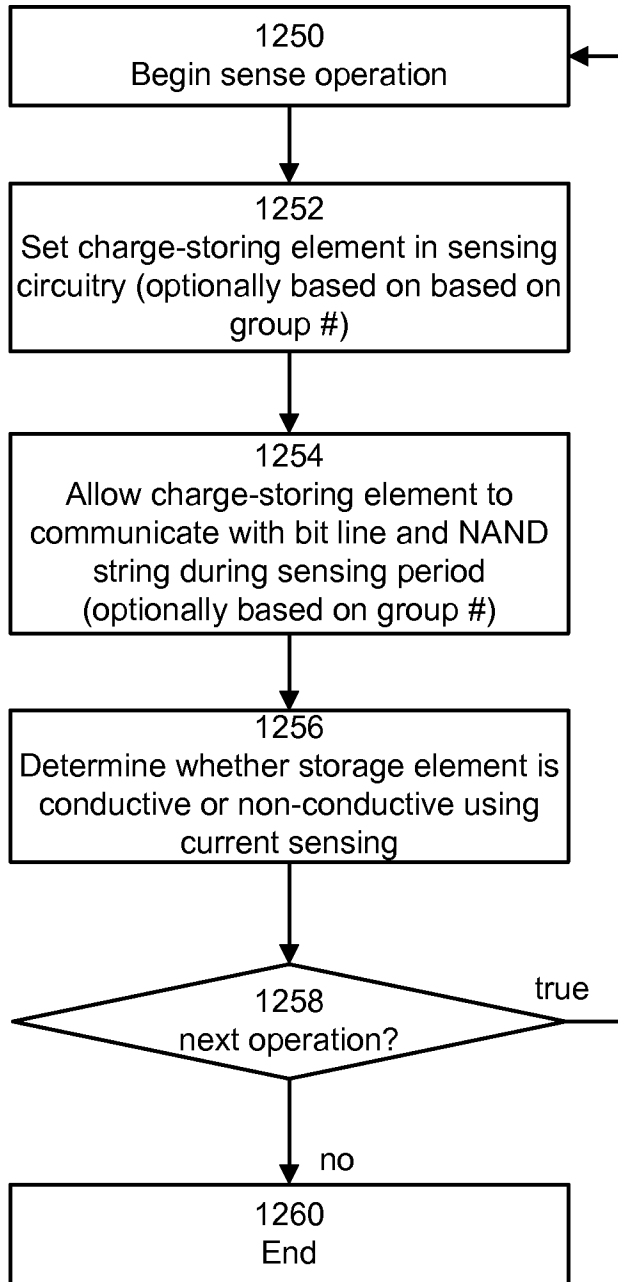


Fig. 12D

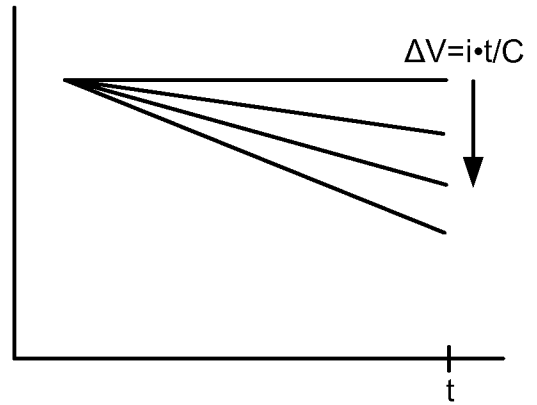




Fig. 13A

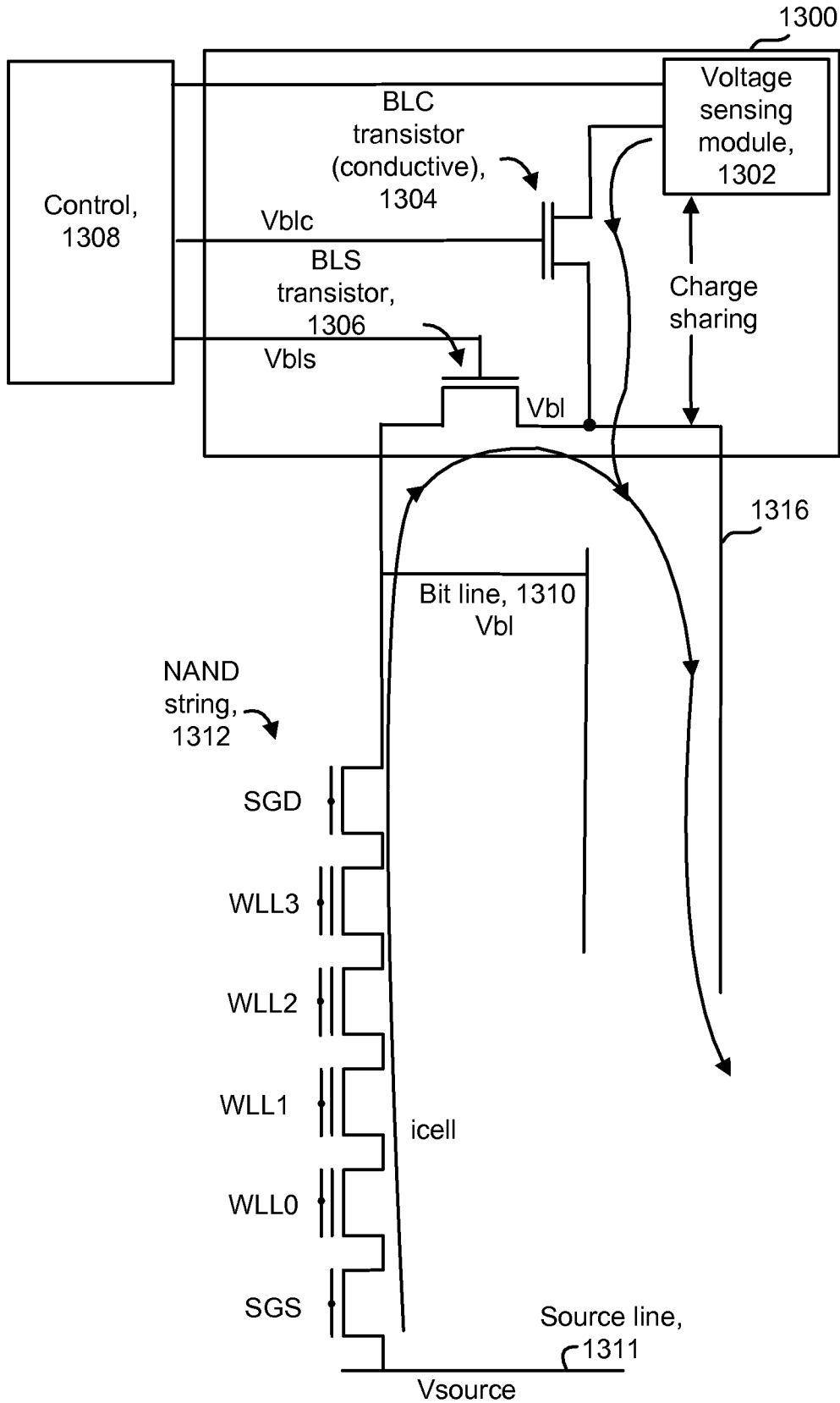
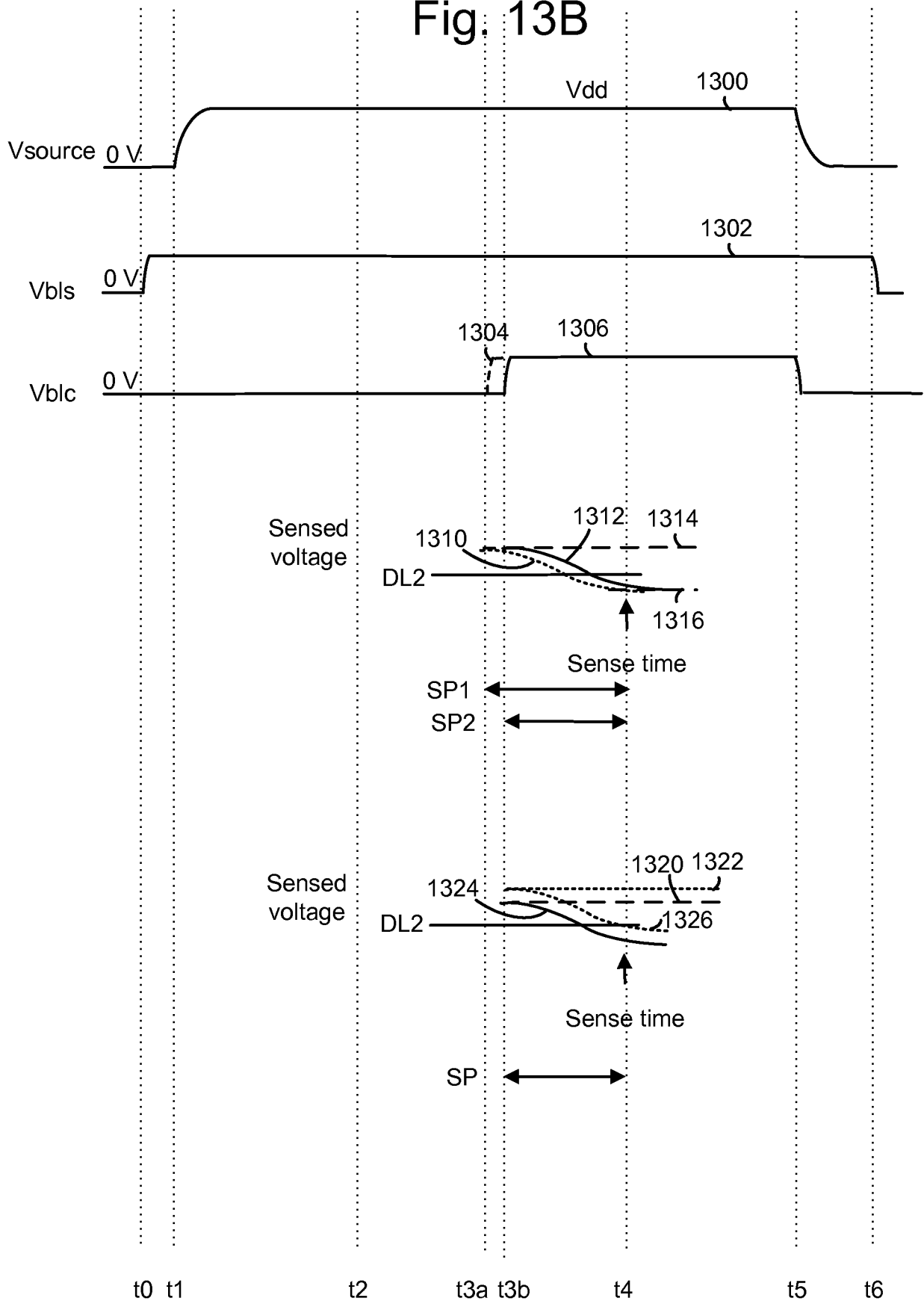


Fig. 13B



INTERNATIONAL SEARCH REPORT

International application No  
PCT/US2015/024273

A. CLASSIFICATION OF SUBJECT MATTER  
INV. G11C11/56 G11C16/26 G11C16/34 H01L27/115  
ADD.  
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED  
Minimum documentation searched (classification system followed by classification symbols)  
G11C H01L  
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)  
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT		
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Further documents are listed in the continuation of Box C.

See patent family annex.

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Date of the actual completion of the international search  21 May 2015	Date of mailing of the international search report  02/06/2015
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Name and mailing address of the ISA/ European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Authorized officer  Kontogiannis, K
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International application No  
PCT/US2015/024273

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
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A	US 2009/073763 A1 (HOSONO KOJI [JP]) 19 March 2009 (2009-03-19) page 7, paragraph 133 -----	1-15
A	WO 2008/083196 A2 (SANDISK CORP [US]; MOKHLESI NIMA [US]) 10 July 2008 (2008-07-10) figure 16 -----	1-15
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