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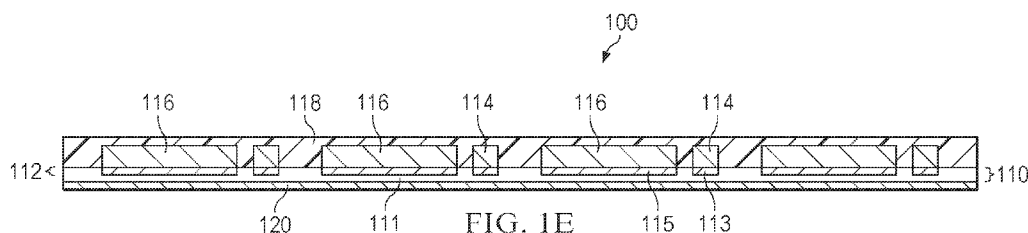
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(54) Title: ELECTRONIC DEVICES WITH SUBSTRATES LESS THAN 50 MICROMETER THICK AND METHODS OF MANUFACTURE



(57) Abstract: A method comprising: molding a structural support coating over the gate pad and source pad at the front side of a wafer; back-side processing the wafer to remove a portion of a silicon layer so that the silicon layer has a post-process thickness, wherein the post-process thickness is less than the pre-process thickness; and removing the structural support coating at the front side of the wafer sufficiently to expose the gate pad and source pad. An electronic device comprising: a silicon layer less than 50 μm thick and defining a back side of the electronic device, a metal layer on the silicon layer, wherein the metal layer defines a front side of the electronic device, wherein the metal layer has a source pad and a gate pad; and a structural support coating between the source pad and the gate pad.

**ELECTRONIC DEVICES WITH SUBSTRATES LESS THAN 50 MICROMETER THICK AND
METHODS OF MANUFACTURE**

PRIORITY

5 This application claims priority to U.S. Provisional Patent Application No. 63/472,953, filed June 14, 2023, the contents of which are hereby incorporated in their entirety.

TECHNICAL FIELD

10 The present disclosure relates to field effect transistors, in particular, field effect transistors with substrates less than 50 μm thick so they may have low RDS (on) values and methods to produce field effect transistors with substrates less than 50 μm thick.

BACKGROUND

15 Relative to metal oxide field effect transistors, RDS(on) stands for “drain-source on resistance,” or the total resistance between the drain and source in a metal oxide field effect transistor (MOSFET) when the MOSFET is fully “on.” There are two prevailing methods for production of vertical MOSFET devices to attain ultra-thin substrates ($> 50 \mu\text{m}$), which have RDS(on) values (> 10 milliohms): (1) grinding a center section of a wafer to an ultra-thin thickness while leaving thicker periphery sections and building the vertical MOSFET on the ultra-thin center section; and (2) adhering a wafer to a support material such as glass, grinding the entire wafer to an ultra-thin thickness, and building the vertical MOSFET on the ultra-thin wafer.

20 The first method is problematic because the thicker periphery sections of the wafer must be cut away after building the vertical MOSFET(s) and the wafer may break into pieces while being cut. There is also a practical limit to how thin the wafer may be ground without breaking during the grinding process. The thicker periphery sections of the wafer are sacrificed, which is a waste of good silicon. Production costs are high because many steps are used to grind and cut the wafer.

25 The second method is problematic because the support material must be removed after building the vertical MOSFET(s) and the wafer may break into pieces while the support material is removed.

30 There is a need for a process for production of vertical MOSFET devices to attain substrates less than 50 μm thick yielding low RDS(on) values that does not tend to break the wafer into pieces.

SUMMARY

Aspects provide a process for production of vertical MOSFET devices to attain substrates less than 50 μm thick yielding low RDS(on) values that does not tend to break the wafer into pieces.

According to an aspect, there is provided a method comprising: providing a wafer
5 having a front side and a back side, a metal layer having a gate pad and a source pad at the front side, and a silicon layer at the back side wherein the silicon layer has a pre-process thickness; molding a structural support coating over the gate pad and source pad at the front side of the wafer; back-side processing the wafer to remove a portion of the silicon layer so that the silicon layer has a post-process thickness, wherein the post-process thickness is less
10 than the pre-process thickness; and removing the structural support coating at the front side of the wafer sufficiently to expose the gate pad and source pad.

An aspect provides the method as in the previous paragraph, wherein the pre-process thickness of the silicon layer is greater than or equal to 700 μm .

An aspect provides the method as in any one of the prior two paragraphs, wherein the
15 post-process thickness of the silicon layer is less than or equal to 50 μm .

An aspect provides the method as in any one of the prior three paragraphs, wherein the structural support coating comprises polymer.

An aspect provides the method as in any one of the prior four paragraphs, wherein the back-side processing comprises grinding and the removing of the structural support coating
20 comprising grinding.

An aspect provides the method as in any one of the prior five paragraphs, comprising plating the front side of the wafer to build up the gate pad and source pad.

An aspect provides the method as in the prior paragraph, wherein the plating comprises plating with copper (Cu).

25 An aspect provides the method as in any one of the prior seven paragraphs, comprising adding a drain pad layer on the back side of the wafer.

An aspect provides the method as in any one of the prior eight paragraphs, comprising plating the front and back sides of the wafer with oxidizing inhibiting layers.

30 An aspect provides the method as in any one of the prior nine paragraphs, comprising singulating the wafer to form individual chips.

An aspect provides a field effect transistor comprising: a silicon layer less than 50 microns thick, a source pad on the silicon layer; a gate pad on the silicon layer; and a structural support coating on the silicon layer between the source pad and the gate pad.

5 According to one aspect, there is provided an electronic device comprising: a silicon layer less than 50 μm thick and defining a back side of the electronic device, a metal layer on the silicon layer, wherein the metal layer defines a front side of the electronic device, wherein the metal layer has a source pad and a gate pad; and a structural support coating on the front side between the source pad and the gate pad.

10 An aspect provides the electronic device as in the prior paragraph, wherein the structural support coating comprises polymer.

An aspect provides the electronic device as in any one of the prior two paragraphs, wherein a surface of the structural support coating, a surface of the source pad, and a surface of the gate pad are coplanar.

15 An aspect provides the electronic device as in any one of the prior three paragraphs, comprising a copper (Cu) layer on the gate pad and source pad on the front side of the wafer.

An aspect provides the electronic device as in any one of the prior four paragraphs, wherein the electronic device has an RDS(on) value less than 10 milliohms.

An aspect provides the electronic device as in any one of the prior five paragraphs, comprising a drain pad layer on the back side of the silicon layer.

20 An aspect provides the electronic device as in any one of the prior six paragraphs, comprising oxidizing inhibiting layers on the front side of the metal layer and the back side of the silicon layer.

An aspect provides the electronic device as in the prior paragraph, wherein the oxidizing inhibiting layers comprise an electroless nickel immersion gold plating.

25 According to an aspect, there is provided a field effect transistor comprising: a silicon layer less than 50 μm thick and defining a back side of the field effect transistor, a metal layer on the silicon layer, wherein the metal layer defines a front side of the field effect transistor, wherein the metal layer has a source pad and a gate pad; a polymer coating on the front side between the source pad and the gate pad; a copper layer on the source pad and the gate pad; a drain pad layer on the back side of the silicon layer; and oxidizing inhibiting layers on the front
30 side of the metal layer and the back side of the silicon layer, wherein the field effect transistor has an RDS(on) value less than 10 milliohms.

An aspect provides the field effect transistor as in the prior paragraph, wherein a surface of the structural support coating, a surface of the source pad, and a surface of the gate pad are coplanar.

BRIEF DESCRIPTION OF THE DRAWINGS

5 The figures illustrate examples of vertical MOSFET devices attaining substrates less than 50 μm thick yielding low $\text{RDS}(\text{on})$ values and methods for manufacturing vertical MOSFET devices attaining low $\text{RDS}(\text{on})$ values via ultra-thin substrates.

FIGURE 1A shows a cross-sectional, side view of a field effect transistor (FET) wafer having a silicon layer and a metal layer on one side of the silicon layer and defines a front side.

10 FIGURE 1B shows a cross-sectional, side view of the FET wafer of FIGURE 1A, wherein a metal is plated on the wafer to build up gate pads and source pads on corresponding portions of the metal layer.

FIGURE 1C shows a cross-sectional, side view of the FET wafer of FIGURE 1B, wherein the FET wafer is overmolded with a structural support coating.

15 FIGURE 1D shows a cross-sectional, side view of the FET wafer of FIGURE 1C, wherein the silicon layer has been ground to a thickness less than 50 μm .

FIGURE 1E shows a cross-sectional, side view of the FET wafer of FIGURE 1D, wherein a drain pad layer is applied to the silicon layer.

20 FIGURE 1F shows a cross-sectional, side view of the FET wafer of FIGURE 1E, wherein the front side of the FET wafer has been ground to remove a portion of the structural support coating, whereby the gate pads and source pads are exposed or revealed.

FIGURE 1G shows a cross-sectional, side view of the FET wafer of FIGURE 1F, wherein plating layers are added to the front and back sides of the FET wafer.

25 FIGURE 1H shows a cross-sectional, side view of the FET wafer of FIGURE 1G, wherein the FET wafer has been singulated or cut into individual chips.

FIGURE 2 shows a flowchart for manufacturing vertical MOSFET devices with substrates less than 50 μm thick yielding low $\text{RDS}(\text{on})$ values.

FIGURE 3 shows a cross-sectional side view of a microchip package comprising MOSFET devices substrates less than 50 μm thick yielding low $\text{RDS}(\text{on})$ values.

30 FIGURES 4A through 4F show a MOSFET device being produced from a wafer. FIGURE 4A is a top view showing a source pad, a gate pad and a die top passivation layer.

FIGURE 4B is a cross-sectional, side view of the MOSFET device shown in FIGURE 4A showing the silicon layer is full thickness.

FIGURE 4C is a cross-sectional, side view of the MOSFET device shown in FIGURES 4A and 4B showing a copper plating on the front side of the wafer forming a source contact on the source pad and a gate contact on the gate pad.

FIGURE 4D is a cross-sectional, side view of the MOSFET device shown in FIGURES 4A through 4C showing a structural support coating over the passivation layer, the source pad, the source contact, the gate pad, and the gate contact.

FIGURE 4E is a cross-sectional, side view of the MOSFET device shown in FIGURES 4A through 4D and shows the silicon layer has been ground to a very thin thickness to attain ultra low RDS(on) values.

FIGURE 4F is a cross-sectional, side view of the MOSFET device shown in FIGURES 4A through 4E and shows the structural support coating has been ground away until the portions of it over the source contact and the gate contact are removed.

The reference number for any illustrated element that appears in multiple different figures has the same meaning across the multiple figures, and the mention or discussion herein of any illustrated element in the context of any particular figure also applies to each other figure, if any, in which that same illustrated element is shown.

DESCRIPTION

According to an aspect, there is provided a process for production of vertical MOSFET devices to attain substrates less than 50 μm thick yielding low RDS(on) values that does not tend to break the wafer into pieces. MOSFET devices with substrates less than 50 μm thick may have RDS(on) values less than 10 milliohms.

By over-molding the MOSFET wafer with a structural support coating prior to a grinding process, the structural support coating provides mechanical support to allow the MOSFET wafer to be ground to an ultra-thin thickness. In some aspects, the MOSFET wafer may be ground to less than 50 μm thickness, and even down to 1 μm thickness. The ultra-thin MOSFET wafer may be plated with a Cu layer to enhance electrical and thermal conductivity.

The wafer thinning process (grinding) may comprise several stages: course grinding, fine grinding, and stress relief by dry polishing or wet polishing.

FIGURE 1A shows a cross-sectional, side view of a field effect transistor (FET) wafer. The FET wafer 100 has a silicon layer 110 and a metal layer 112. The metal layer 112 defines

a front side. The wafer 100 may be an 8-inch, full thickness wafer (thickness between 0.4 mm (400 microns) and 0.8 mm (800 microns)). A metal layer 112 is on one side of the silicon layer 110, wherein the metal may be aluminum or any other metal. The metal layer 112 may define gate pads 113 and source pads 115. A full thickness FET wafer 100 including the silicon layer 110 and the metal layer 112 may be greater than or equal to about 725 microns thick. FIGURE 1A shows a raw die with which one may start the process. A doped region of the silicon layer 110, i.e. the transistor source may be under the source pads 115. An insulation layer may be under the gate pads 113 (there may be a layer of polysilicon below the gate pad and above the insulation layer). The gate pad 113 and insulation layer may act as the gate of the transistor.

FIGURE 1B shows a cross-sectional, side view of the FET wafer 100 of FIGURE 1A. A metal is plated on the wafer 110 to build up gate contacts 114 and source contacts 116 on corresponding gate pads 113 and source pads 115 of the metal layer 112. The metal of the gate contacts 114 and source contacts 116 may be Cu or any other metal. The result may be copper on aluminum. The gate contacts 114 and source contacts 116 may be about 125 microns, so that the entire FET wafer 100 as shown in FIGURE 1B may be 850 microns.

FIGURE 1C shows a cross-sectional, side view of the FET wafer 100 of FIGURE 1B. The FET wafer 100 is overmolded with a structural support coating 118, wherein the structural support coating 118 may be a polymer. The structural support coating 118 may be an epoxy mold compound (EMC) and may be applied using a compression molding process. The structural support coating 118 may be about 75 microns, gate contacts 114 and source contacts 116 may be about 125 microns, and the silicon layer may be about 725 microns, so that the entire FET wafer 100 as shown in FIGURE 1C may be 925 microns.

FIGURE 1D shows a cross-sectional, side view of the FET wafer of FIGURE 1C. The silicon layer 110 may be ground to an ultra-thin thickness (i.e., less than 50 microns, in one example between 2 microns and 25 microns). Because the gate and source pads 114 and 116 and the structural support coating 118 provide structural rigidity and support, a significant portion of the silicon layer 110 may be ground away. In theory, from the perspective of structural rigidity and support provided by the structural support coating 118, the silicon layer 110 may be ground to 1 μ m thick), but some silicon should remain to provide for a “drain.” Drains 111 may be in the remaining silicon layer 110. In an example where the silicon layer 110 is ground to a thickness of less than 50 microns, the gate contacts 114 and source contacts

116 may be about 125 microns, and the structural support coating 118 is about 75 microns, then the entire FET wafer 100 as shown in FIGURE 1D may be 250 microns.

FIGURE 1E shows a cross-sectional, side view of the FET wafer 100 of FIGURE 1D. Depending on the thickness of the silicon layer 110 after grinding, a drain pad layer 120 may be applied to the silicon layer 110. The drain pad layer 120 may be Ti-Cu or other metal and may be applied by a sputter process to the backside of the FET wafer 100. In an example where the drain pad layer 120 is about 2 microns thick, the silicon layer 110 is about 50 microns, the gate contacts 114 and source contacts 116 is about 125 microns, and the structural support coating 118 is about 75 microns, that the entire FET wafer 100 as shown in FIGURE 1E may be 252 microns.

FIGURE 1F shows a cross-sectional, side view of the FET wafer 100 of FIGURE 1E. The front side of the FET wafer 100 has been ground to remove a portion of the structural support coating 118, whereby the gate contacts 114 and source contacts 116 may be exposed or revealed. This may allow other components to be soldered to the gate contacts 114 and source contacts 116. While the structural support coating 118 (see FIGURE 1E) is removed from the front sides of the gate contacts 114 and source contacts 116, material of structural support coating 118 may remain between the gate contacts 114 and source contacts 116 and have the same thickness as the gate contacts 114 and source contacts 116. After grinding, a surface of the structural support coating 118, a surface of the source contact 116, and a surface of the gate contact 114 may be coplanar. In an example, the drain pad layer 120 may be about 2 microns thick, the silicon layer 110 is about 50 microns, and the gate contacts 114 and source contacts 116 may be about 125 microns, so that the entire FET wafer 100 as shown in FIGURE 1F may be 177 microns in thickness.

FIGURE 1G shows a cross-sectional, side view of the FET wafer of FIGURE 1F. A plating layer 122 may be added to the front side of the FET wafer 100 and another plating layer 124 may be added to the back side of the FET wafer 100. These plating layers may inhibit the Cu from oxidizing and may provide common PCB layers for solder and bonding. The plating layers may be electroless nickel immersion gold (ENIG) plating or electroless nickel palladium gold (ENEPIG) plating. The plating of the front and back sides of the wafer may be with oxidizing inhibiting layers. In an example, the plating layers 122 and 124 may be about 2 microns each, the drain pad layer 120 may be about 2 microns thick, the silicon layer 110 may

be about 50 microns, and the gate contacts 114 and source contacts 116 may be about 125 microns, so that the entire FET wafer 100 as shown in FIGURE 1G may be 181 microns.

FIGURE 1H shows a cross-sectional, side view of the FET wafer 100 of FIGURE 1G. The FET wafer 100 may be singulated or cut into individual chips 126.

5 FIGURE 2 shows a flowchart for manufacturing vertical MOSFET devices with substrates less than 50 μm thick yielding low $\text{RDS}(\text{on})$ values. A wafer is provided 202 having a front side and a back side, a metal layer having a gate pad and a source pad at the front side, and a silicon layer at the back side wherein the silicon layer has a pre-process thickness. See FIGURE 1A. A structural support coating is molded 204 over the gate pad and source pad at
10 the front side of the wafer. See FIGURE 1C. The wafer is back-side processed 206 to remove a portion of the silicon layer so that the silicon layer has a post-process thickness, wherein the post-process thickness is less than the pre-process thickness. See FIGURE 1D. The structural support coating is removed 208 at the front side of the wafer sufficiently to expose the gate pad and source pad. See FIGURE 1F.

15 FIGURE 3 shows a cross-sectional side view of a microchip package 300 comprising two MOSFET devices 302 and 304. The MOSFET devices 302 and 304 are mounted on a printed circuit board 306. Because the MOSFET devices 302 and 304 have substrates less than 50 μm thick, the overall thickness 308 of the microchip package 300 is small.

FIGURES 4A through 4F show a MOSFET device being produced from a wafer.
20 FIGURE 4A is a top view showing a source pad 115, a gate pad 113 and a die top passivation layer 119.

FIGURE 4B is a cross-sectional, side view of the MOSFET device shown in FIGURE 4A. FIGURE 4B shows the silicon layer 110 is full thickness (about 723 μm), which is a typical fab-out thickness. Top aluminum bond pads are at the front side of the silicon layer 110 forming
25 a source pad 115 and a gate pad 113. A drain 111 is in the silicon layer 110.

FIGURE 4C is a cross-sectional, side view of the MOSFET device shown in FIGURES 4A and 4B. FIGURE 4C shows a copper plating on the front side of the wafer forming a source contact 116 on the source pad 115 and a gate contact 114 on the gate pad 113.

FIGURE 4D is a cross-sectional, side view of the MOSFET device shown in FIGURES
30 4A through 4C. FIGURE 4D shows a structural support coating 118 over the passivation layer 119, the source pad 115, the source contact 116, the gate pad 113, and the gate contact 114. The silicon layer 110 is full thickness (about 723 μm).

FIGURE 4E is a cross-sectional, side view of the MOSFET device shown in FIGURES 4A through 4D. FIGURE 4E shows a structural support coating 118 over the passivation layer 119, the source pad 115, the source contact 116, the gate pad 113, and the gate contact 114. The silicon layer 110 has been ground to a very thin thickness (less than or equal to 50 μm and as thin as 1 μm) to attain ultra low RDS(on) values less than 10 milliohms. The drain 111 is in the thin thickness silicon layer 110.

FIGURE 4F is a cross-sectional, side view of the MOSFET device shown in FIGURES 4A through 4E. FIGURE 4F shows the structural support coating 118 has been ground away until the portions of it over the source contact 116 and the gate contact 114 are removed. However, the structural support coating 118 adjacent the source contact 116 and the gate contact 114 remains. In particular, the structural support coating 118 between the source contact 116 and the gate contact 114 remains. The drain 111 is in the thin thickness silicon layer 110.

Although examples have been described above, other variations and examples may be made from this disclosure without departing from the spirit and scope of these disclosed examples.

CLAIMS

1. A method comprising:

providing a wafer having a front side and a back side, a metal layer having a gate pad
5 and a source pad at the front side, and a silicon layer at the back side wherein
the silicon layer has a pre-process thickness;

molding a structural support coating over the gate pad and source pad at the front side
of the wafer;

back-side processing the wafer to remove a portion of the silicon layer so that the silicon
10 layer has a post-process thickness, wherein the post-process thickness is less
than the pre-process thickness; and

removing the structural support coating at the front side of the wafer sufficiently to
expose the gate pad and source pad.

15 2. The method as in claim 1, wherein the pre-process thickness of the silicon layer is greater
than or equal to 700 μm .

3. The method as in any one of claims 1 to 2, wherein the post-process thickness of the silicon
layer is less than or equal to 50 μm .

20 4. The method as in any one of claims 1 to 3, wherein the structural support coating comprises
polymer.

5. The method as in any one of claims 1 to 4, wherein the back-side processing comprises
25 grinding and the removing of the structural support coating comprising grinding.

6. The method as in any one of claims 1 to 5, comprising plating the front side of the wafer to
build up the gate pad and source pad.

30 7. The method as in claim 6, wherein the plating comprises plating with copper (Cu).

8. The method as in any one of claims 1 to 7, comprising adding a drain pad layer on the back side of the wafer.

9. The method as in any one of claims 1 to 8, comprising plating the front and back sides of the wafer with oxidizing inhibiting layers.

10. The method as in any one of claims 1 to 9, comprising singulating the wafer to form individual chips.

11. An electronic device comprising:

a silicon layer less than 50 μm thick and defining a back side of the electronic device,
a metal layer on the silicon layer, wherein the metal layer defines a front side of the electronic device, wherein the metal layer has a source pad and a gate pad; and
a structural support coating on the front side between the source pad and the gate pad.

12. The electronic device as in claim 11, wherein the structural support coating comprises polymer.

13. The electronic device as in any one of claims 11 to 12, wherein a surface of the structural support coating, a surface of the source pad, and a surface of the gate pad are coplanar.

14. The electronic device as in any one of claims 11 to 13, comprising a copper (Cu) layer on the gate pad and source pad on the front side of the wafer.

15. The electronic device as in any one of claims 11 to 14, wherein the electronic device has an RDS(on) value less than 10 milliohms.

16. The electronic device as in any one of claims 11 to 15, comprising a drain pad layer on the back side of the silicon layer.

17. The electronic device as in any one of claims 11 to 16, comprising oxidizing inhibiting layers on the front side of the metal layer and the back side of the silicon layer.

18. The electronic device as in claim 17, wherein the oxidizing inhibiting layers comprise an electroless nickel immersion gold plating.

19. A field effect transistor comprising:

5 a silicon layer less than 50 μm thick and defining a back side of the field effect transistor,

 a metal layer on the silicon layer, wherein the metal layer defines a front side of the field effect transistor, wherein the metal layer has a source pad and a gate pad;

 a polymer coating on the front side between the source pad and the gate pad;

10 a copper layer on the source pad and the gate pad;

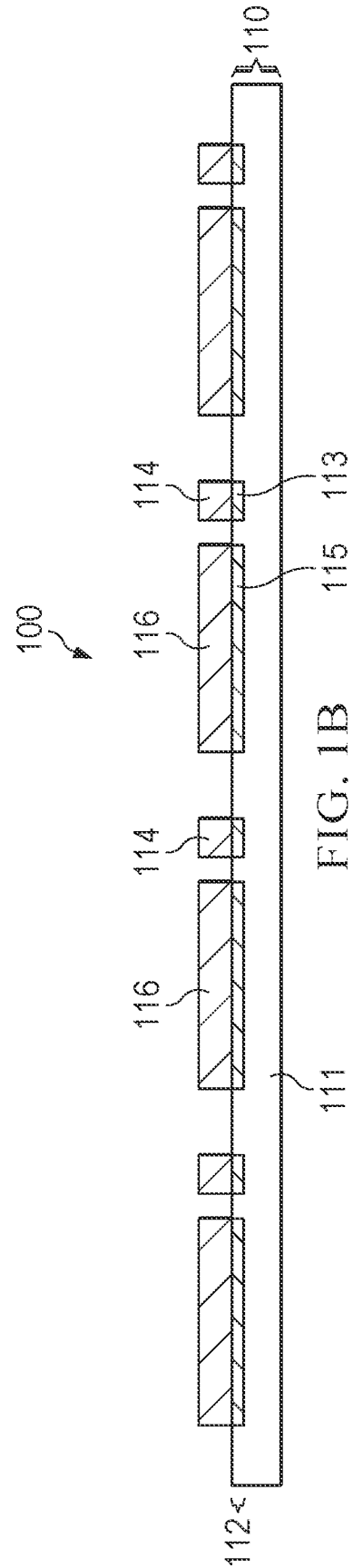
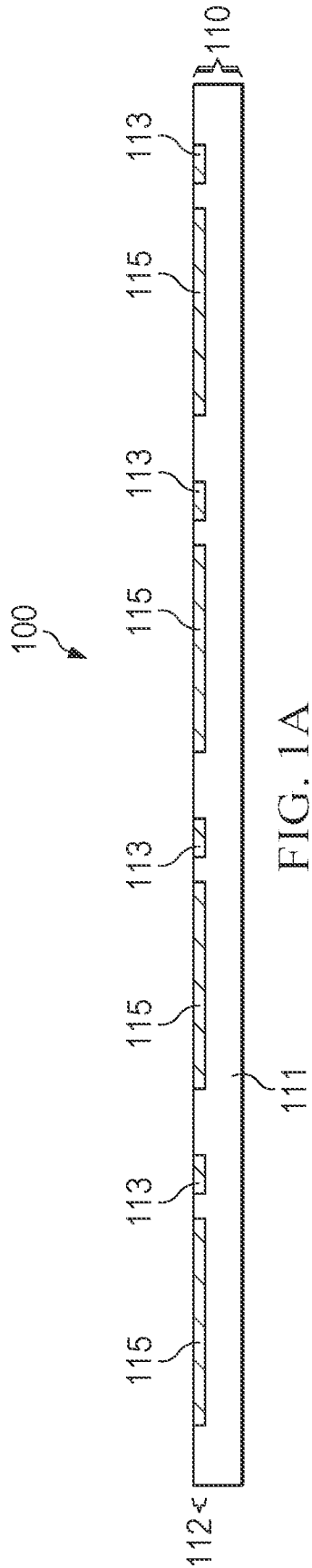
 a drain pad layer on the back side of the silicon layer; and

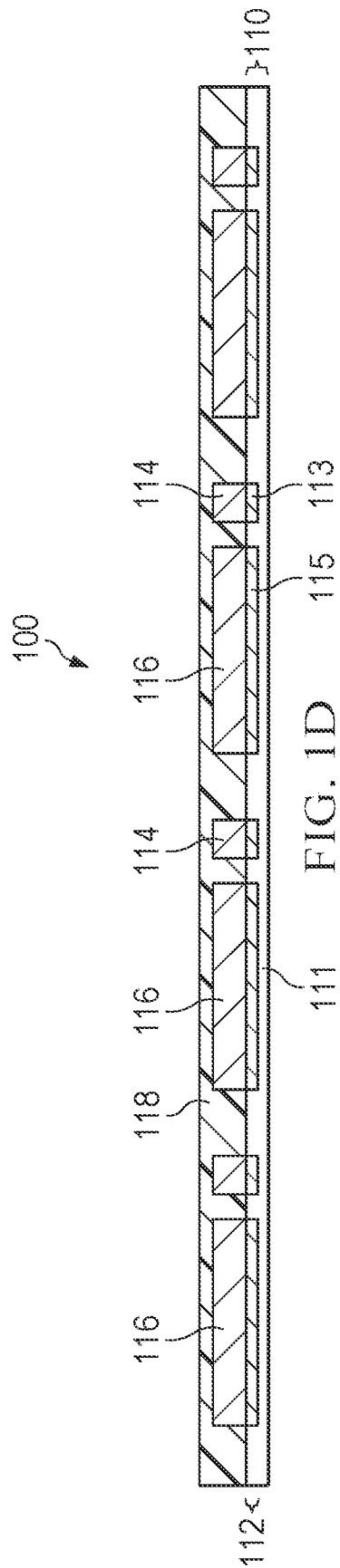
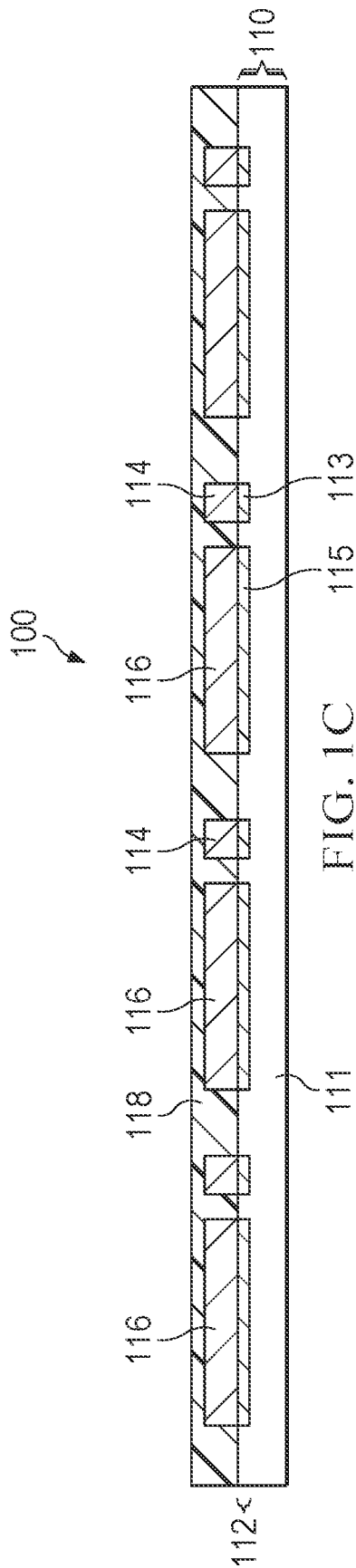
 oxidizing inhibiting layers on the front side of the metal layer and the back side of the silicon layer,

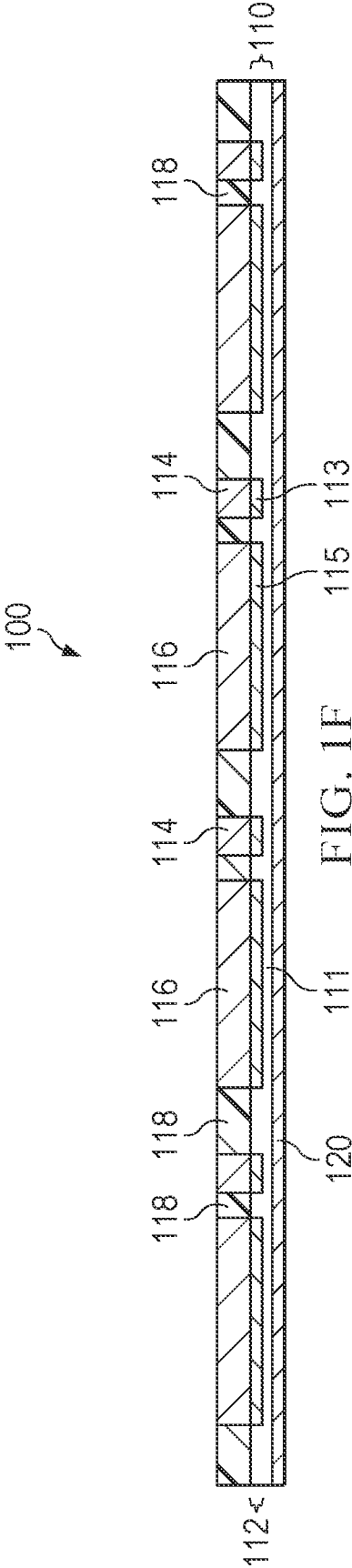
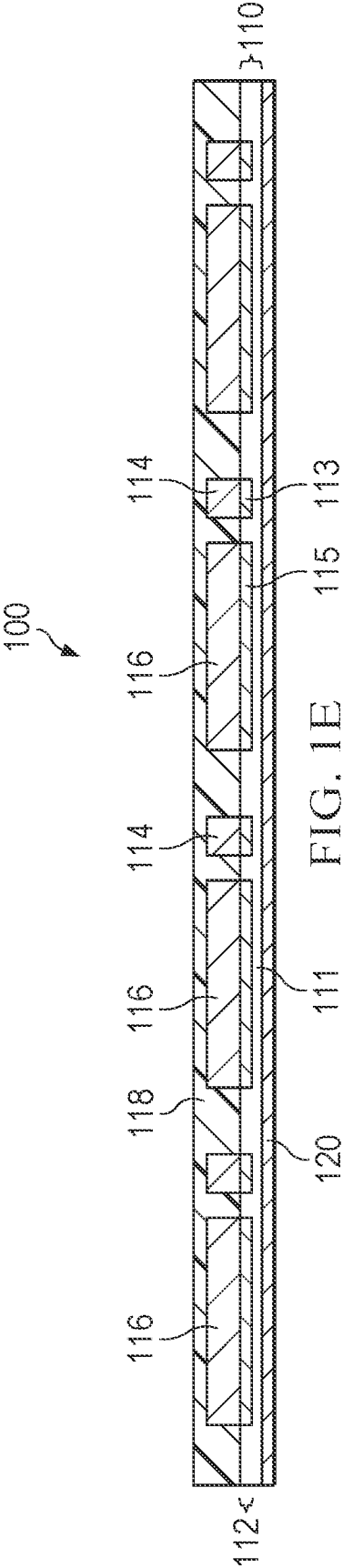
 wherein the field effect transistor has an RDS(on) value less than 10 milliohms.

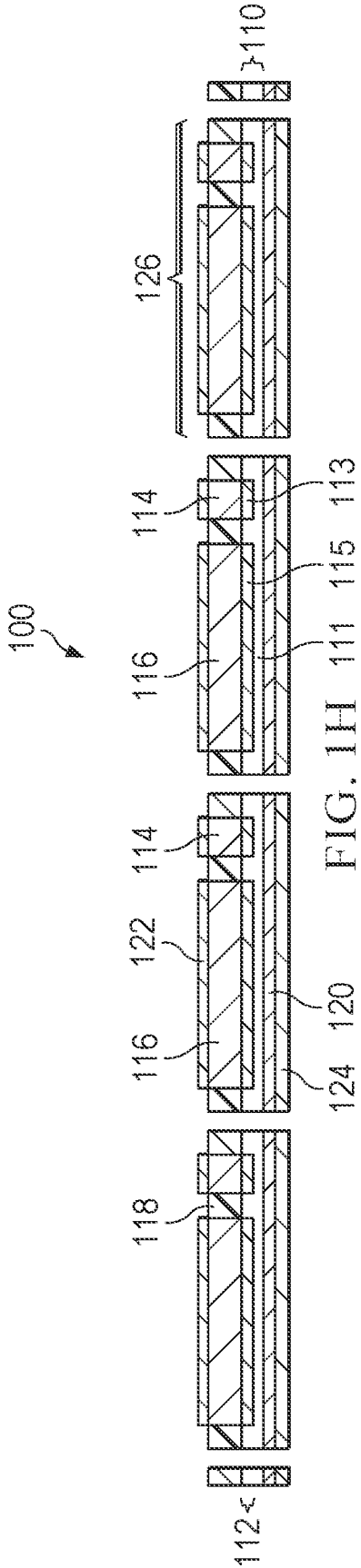
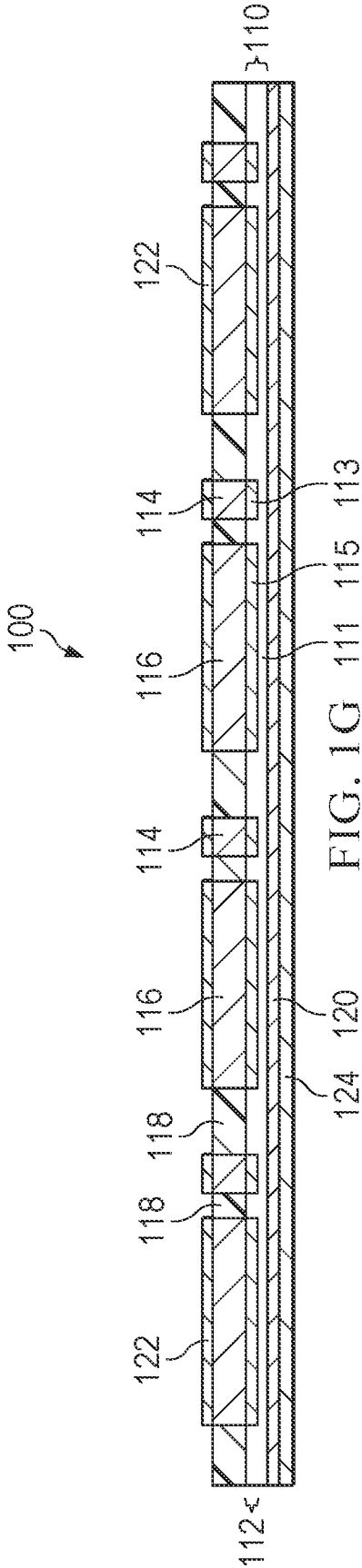
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20. The field effect transistor as in claim 19, wherein a surface of the structural support coating, a surface of the source pad, and a surface of the gate pad are coplanar.









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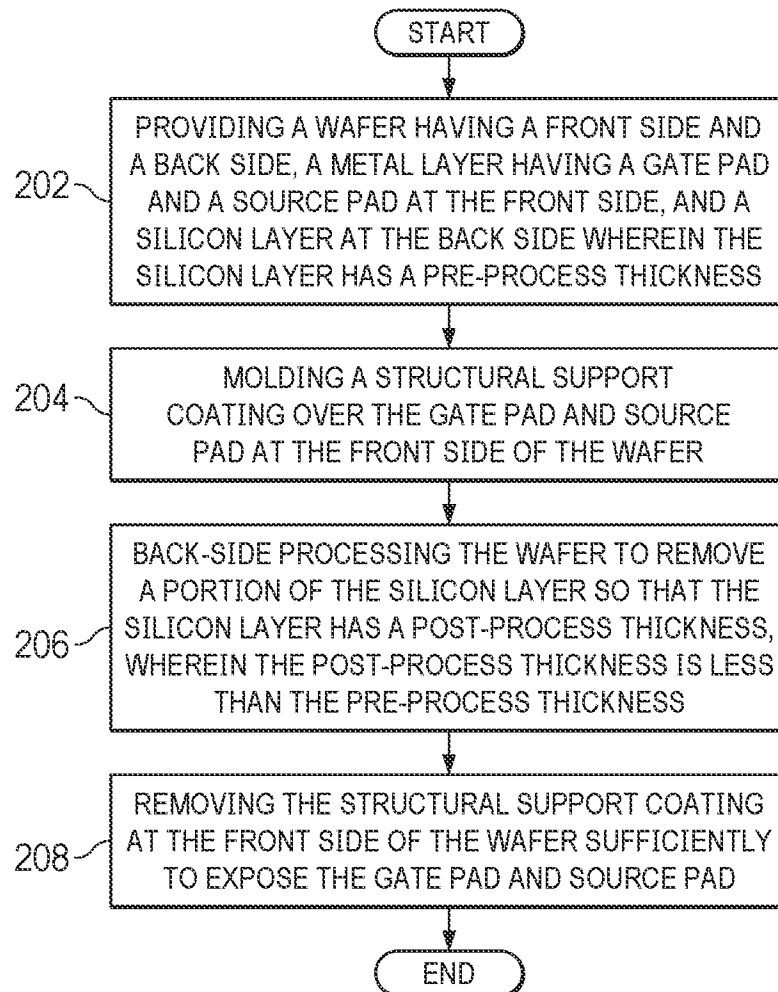


FIG. 2

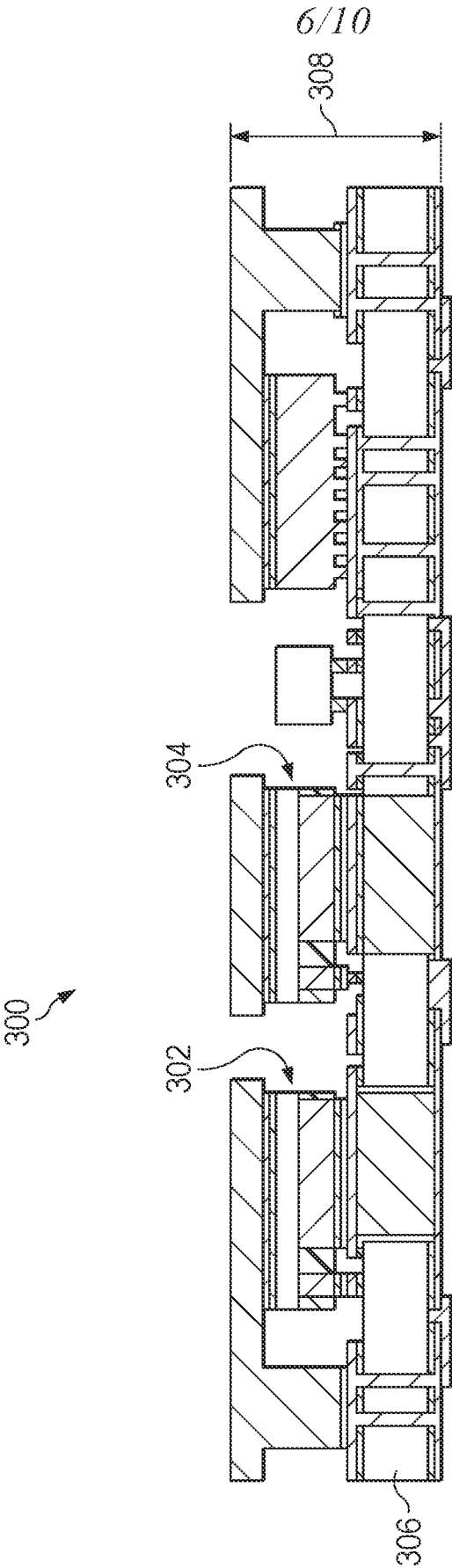


FIG. 3

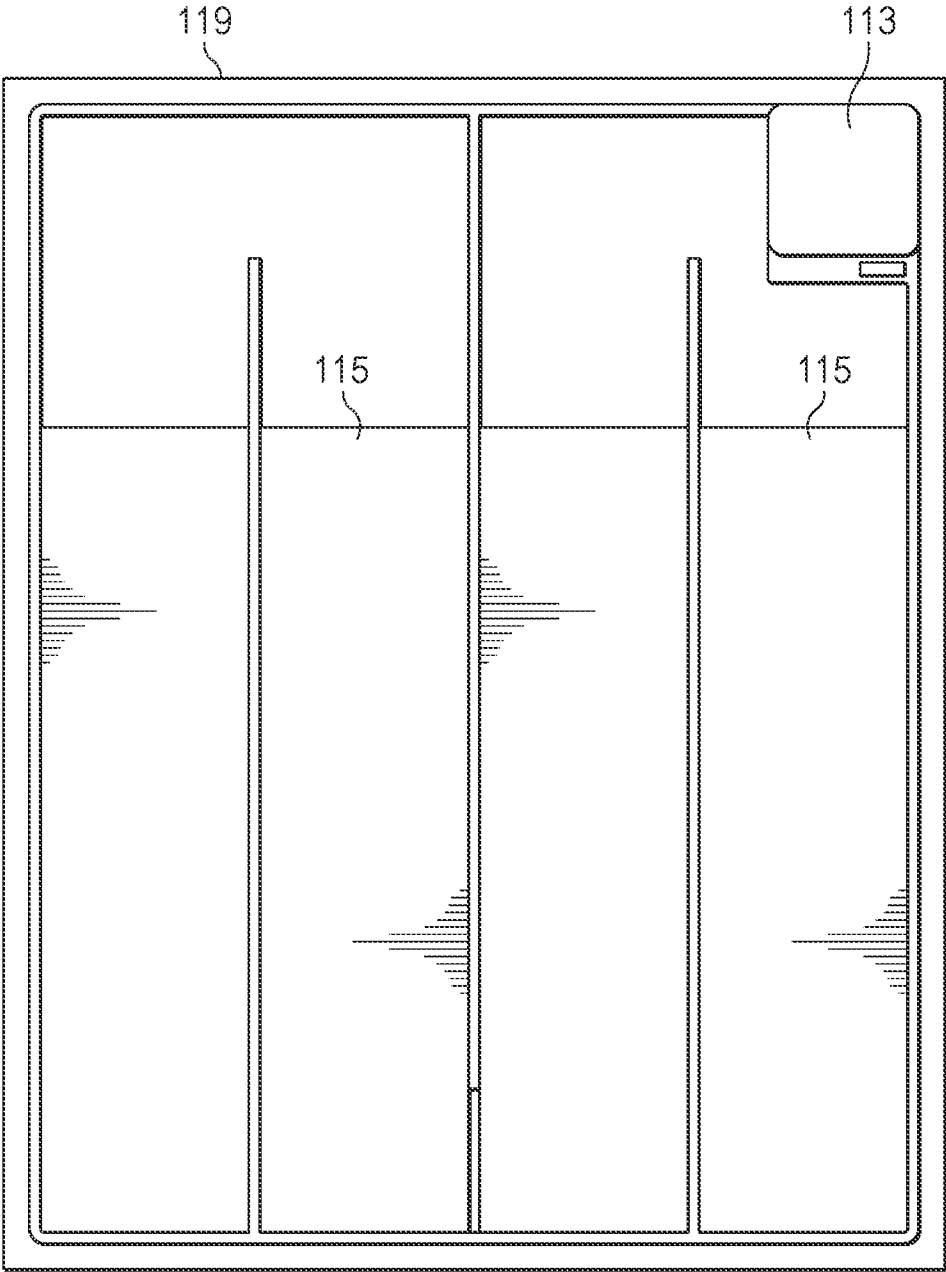


FIG. 4A

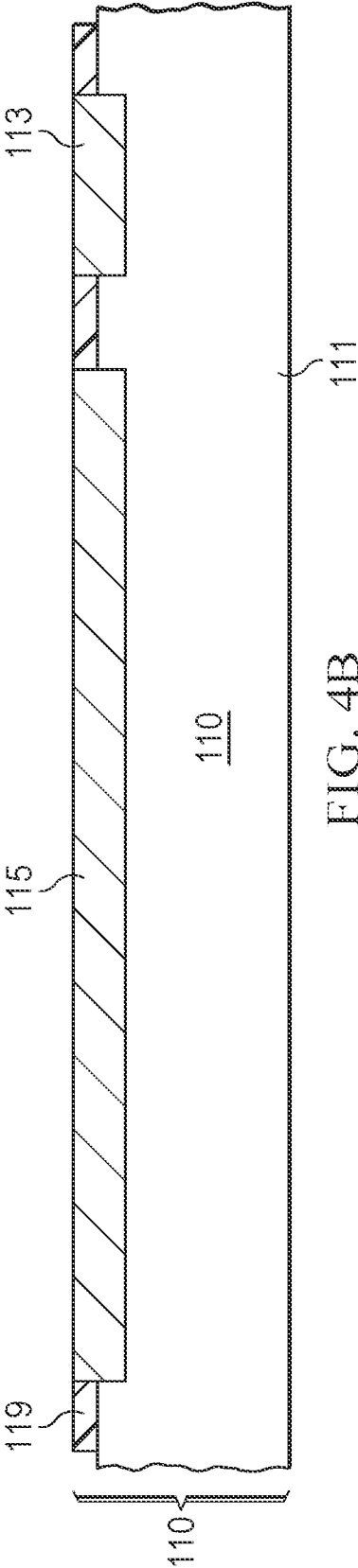


FIG. 4B

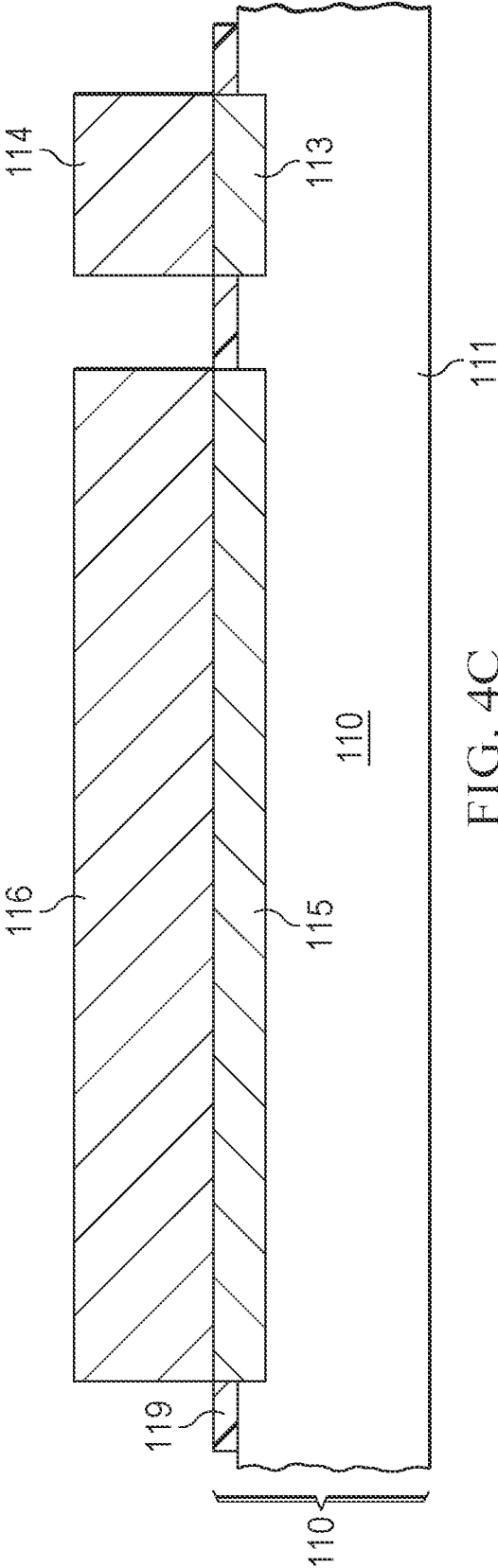
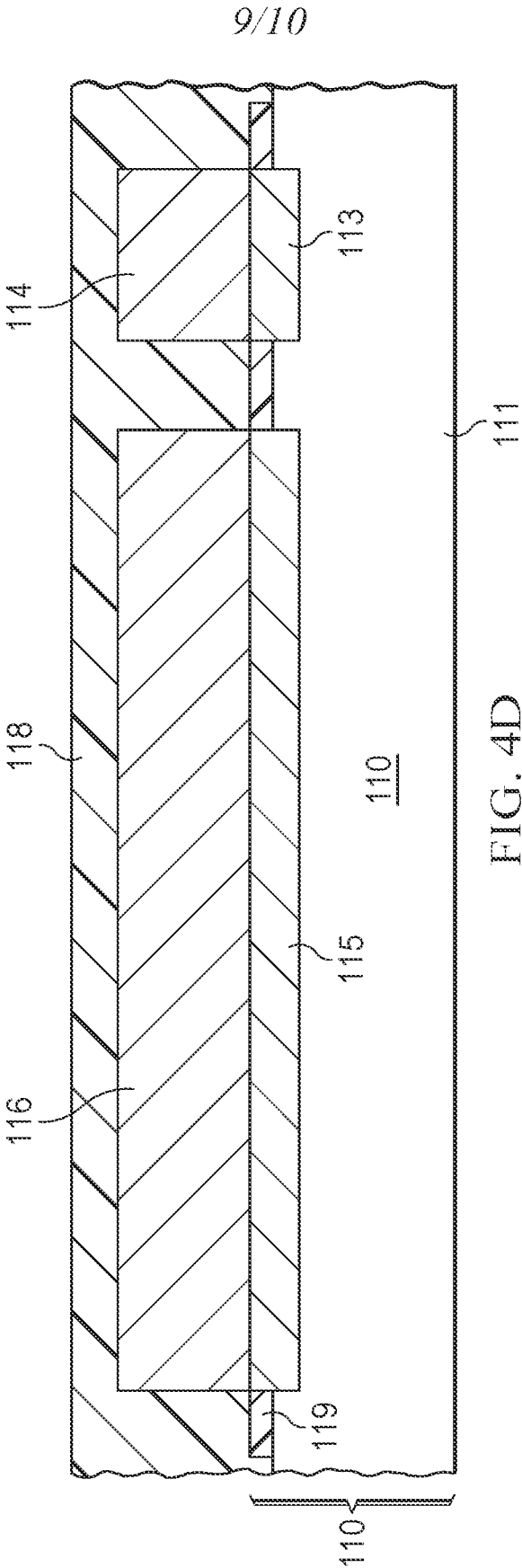
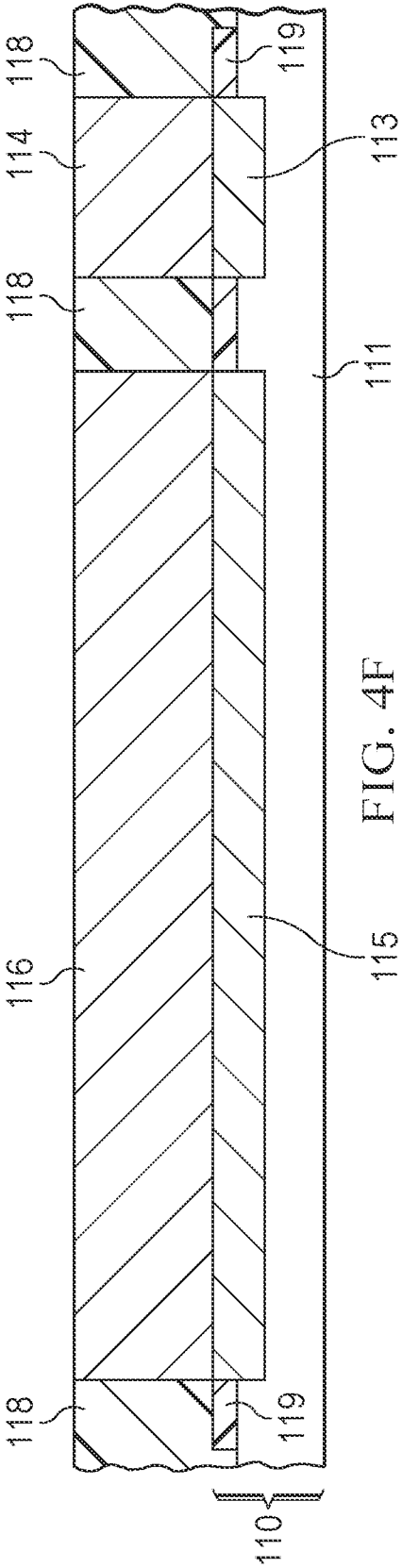
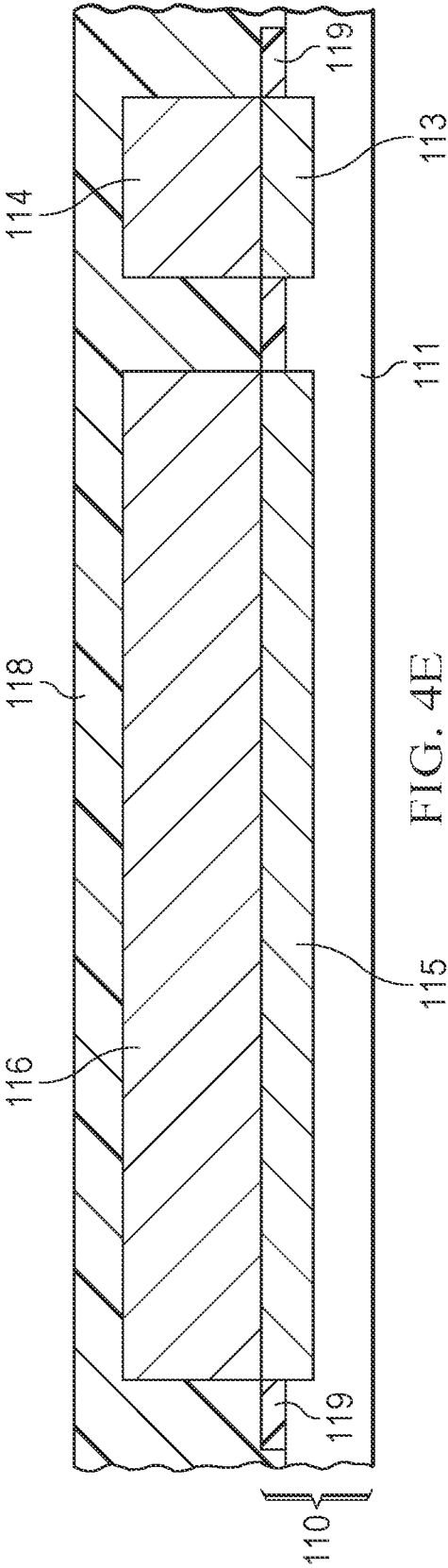


FIG. 4C





INTERNATIONAL SEARCH REPORT

International application No
PCT/US2023/083951

A. CLASSIFICATION OF SUBJECT MATTER INV. H01L23/48 H01L21/56 H01L29/78 ADD. H01L21/78		
According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED		
Minimum documentation searched (classification system followed by classification symbols) H01L		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched		
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used) EPO-Internal		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 2021/225119 A1 (ROHM CO LTD [JP]) 11 November 2021 (2021-11-11) figures 1, 2, 6, 20 & US 2023/352371 A1 (NAKANO YUKI [JP]) 2 November 2023 (2023-11-02) paragraphs [0051], [0063], [0147], [0156], [0080], [0116], [0143], [0159], [0080], [0160], [0163], [0270]; figures 1, 2, 6, 20 -----	1-14, 16-18
X	US 2023/082976 A1 (NAKANO YUKI [JP]) 16 March 2023 (2023-03-16) paragraphs [0053], [0059], [0107], [0117], [0118], [0119], [0126], [0128]; figures 1-5, 7-10, 14-17 -----	1, 3-17, 19, 20
☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.		
* Special categories of cited documents : "A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier application or patent but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance;; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance;; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art "&" document member of the same patent family		
Date of the actual completion of the international search 8 May 2024		Date of mailing of the international search report 27/05/2024
Name and mailing address of the ISA/ European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016		Authorized officer Gélébart, Jacques

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/US2023/083951

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US 2023082976 A1	16-03-2023	CN 115516644 A DE 112021000398 T5 DE 212021000199 U1 JP WO2021225125 A1 US 2023082976 A1 WO 2021225125 A1	23-12-2022 13-10-2022 07-02-2022 11-11-2021 16-03-2023 11-11-2021