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(54) Cell exchanging apparatus.

(57) An exchanging apparatus for cells each comprising a data portion and a header portion including destination information. The cells input through incoming lines are stored in respective buffer memoires selected by an incoming line spatial switch. Addresses of the stored cells in the buffer memories are managed for eachof the destinations of the cells. In accordance with the addresses under management for each destination, the cells stored in the buffer memories are read out and output to desired outgoing lines connected to the buffer memories through an outgoing line spatial switch.

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CELL EXCHANGING APPARATUS

This invention relates relates to a cell exchanging apparatus for exchanging cells at a high speed which are obtained from various information for multimedia, such as voices, data and images, in blocks.

Fig. 1 is a block diagram showing a conventional cell exchanging apparatus disclosed in Japanese Patent disclosure No. 117241/90, for example. In Fig. 1, the reference numerals 1_1 - 1_n designate n ($n \geqq 2$) incoming lines through which packets are input. Each packet has a fixed length and has a header portion including encoded destination information. 2_1 - 2_m designate m ($m \geqq 2$) outgoing lines through which the packets are output dependent on the destinations specified by the header portions. 3_1 - 3_ℓ designate ℓ ($\ell \geqq n$) buffer memories in which the input packets are temporarily stored. 4 designates an empty buffer selection switch for connecting each of the incoming lines 1_1 -1_n, through which a packet is input, to an empty one of the buffer memories 3_1 - 3_ℓ.

Denoted by 5_1 - 5_ℓ are header memory circuits provided in correspondence to the buffer memories 3_1 - 3_ℓ for extracting and storing only the header portions of those packets which are stored in the corresponding buffer memories. 6_1 - 6_ℓ denote outgoing line selection circuits provided in correspondence to the header memory circuits 5_1 - 5_ℓ for making the outputs thereof significant, i.e., "1", from which the stored contents of the corresponding header memory circuits are sent to output lines.

Denoted by 7_1 - 7_m are encoders provided in correspondence to the outgoing lines 2_1 - 2_m for receiving outputs from the outgoing selection circuits 6_1 - 6_ℓ to encode the outputs as buffer numbers of the buffer memories 3_1 - 3_ℓ. 8_1 - 8_m, are first-in, first-out type (hereinafter referred to FIFO) memories provided in correspondence to the encoders 7_1 - 7_m such that the buffer numbers encoded by the encoders 7_1 - 7_m are written into the FIFO memories and then read out therefrom in the same order that the buffer numbers are input. 9_1 - 9_m are buffer connection switches controlled in accordance with the buffer numbers delivered from the corresponding FIFO memories for outputting the packets stored in the buffer memories to the outgoing lines specified by the header portions of the packets.

Although the packet is used here instead of a cell to describe a transmitted unit of information, both the terms "cell" and "packet" mean the same thing in that multimedia information is divided into blocks and a header including destination information is added to each block. Generally, however, the two terms are different in that the packet is handled as having blocks of variable length, while the cell is handled as having a fixed length prescribed by the International Standard.

An operation of the conventional cell exchanging apparatus will now be described. Fig. 2 is a time chart showing a timing relation between signals at the various points. This figure illustrates a flow of control in the case of receiving, at the same time, packets sent from the incoming lines 1_1 and 1_n to the outgoing line 2_1 when the buffer memories 3_1 and 3_ℓ are empty. It is also assumed that the packets handled here have a fixed length as mentioned above and the header portions include, as destination information, encoded outgoing line numbers.

When a packet arrives through any one of the incoming lines 1_1 - 1_n, the empty buffer selection switch 4 selects an empty one of the buffer memories 3_1 - 3_ℓ and connects it to the incoming line along which the packet has arrived. Here, if two packets having the same outgoing line number "1" designating the outgoing line 2_1 arrive through the incoming lines 1_1 and 1_n at the same time, as shown in Figs. 2(a) and 2(b), the empty buffer selection switch 4 selects the incoming lines 1_1 - 1_n and the buffer memories 3_1 - 3_ℓ one by one in the ascending order, for example, and interconnects a selected pair of the incoming line and the buffer memory. In this case, therefore, the empty buffer selection switch 4 connects the incoming line 1_1 to the buffer memory 3_1 and the incoming line 1_n to the buffer memory 3_ℓ, whereby a packet A having arrived along the incoming line 1_1 is stored in the buffer memory 3_1 and a packet B having arrived along the incoming line 1_n is stored in the buffer memory 3_ℓ, respectively.

With the switching operation of the empty buffer selection switch 4, the packet A is also supplied to the header memory circuit 5_1 corresponding to the buffer memory 3_1 and the packet B is also supplied to the header memory circuit 5_ℓ corresponding to the buffer memory 3_ℓ. The header memory circuits 5_1 - 5_ℓ serve to extract only the header portions of the received packets and to store the contents of the header portions, i.e., the outgoing line numbers. Accordingly, the outgoing line number "1" designating the outgoing line 2_1 is stored in the header memory circuits 5_1 and 5_ℓ. The contents of the header memory circuits 5_1 and 5_ℓ are sent to the corresponding outgoing line selection circuits 6_1 and 6_ℓ, respectively. Among the outputs of the outgoing line selection circuit 6_1 - 6_ℓ, those outputs which identify the output lines corresponding to the outgoing line numbers speci-

fied by the contents of the header memory circuits turn to a significant level, that is, "1", and outputs which identify other output lines remain insignificant, i.e., "0".

Accordingly, the outgoing line selection circuit 6_1 sets the output to the encoder 7_1 to "1" as shown in Fig. 2(c), and the outgoing line selection circuit 6_ℓ also sets the output to the encoder 7_1 to "1" as shown in Fig. 2(d). When any one of the outputs of the outgoing line selection circuits 6_1 - 6_ℓ is turned to "1", a corresponding one of the encoders 7_1 - 7_m encodes the buffer number of the buffer memory which corresponds to one of the outgoing line selection circuits 6_1 - 6_ℓ, and causes the encoded buffer number to be stored in corresponding one of the FIFO memories 8_1 - 8_m. In the case the output of the two outgoing line selection circuits 6_1 and 6_ℓ turn to "1" at the same time as shown in Figs. 2(c) and 2(d), the encoder 7_1 causes the buffer numbers to be stored in the FIFO memory 8_1 in the ascending order, for example.

Therefore, the FIFO memory 8_1 first stores the buffer number ① of the buffer memory 3_1 and then stores the buffer number ⓛ of the buffer memory 3_ℓ. Each of the buffer connection switches 9_1 - 9_m reads out the buffer numbers, stored in the FIFO memories 8_1 - 8_m, in the order of the buffer numbers stored, and connects the buffer memories designated by the read-out buffer numbers to the outgoing line connected to the buffer connection switch.

Specifically, as shown in Fig. 2(e), the buffer connection switch 9_1 first reads the buffer number ① out of the FIFO memory 8_1 and, after the completion of the necessary connection process, reads the next buffer number ⓛ therefrom. When the buffer number ① is read out, the buffer memory 3_1 is connected to the outgoing line 2_1 and the packet A stored in the buffer memory 3_1 is output to the outgoing line 2_1 as shown in Fig. 2(f). After the completion of outputting the packet A to the outgoing line 2_1, the buffer number ⓛ is read out as mentioned above, whereupon the buffer memory 3_ℓ is connected to the outgoing line 2_1 and the packet B stored in the buffer memory 3_ℓ is output to the outgoing line 2_1, as shown in Fig. 2-(g). As a result, the packets A and B are output to the outgoing line 2_1 successively as shown in Fig. 2(h).

Whenever a packet is delivered to one of the outgoing lines 2_1- 2_m, the buffer connection switches 9_1 - 9_m resease a corresponding one of the buffer memories 3_1 - 3_ℓ and inform the empty buffer selection switch 4 of the fact so as to make it ready for receiving further packets.

In the conventional cell exchanging apparatus, only one cell can be stored in each of the buffer memories 3_1 -3_ℓ thus avoiding any collision between cells (packets) when the cells are read out of the buffer memories. If the number of cells to be written exceeds the number of buffer memories 3_1 - 3_ℓ, the excessive cells are discarded. To reduce the number of discarded cells, it is required to prepare a large quantity of buffer memories. This necessarily increases the size of the empty buffer selection switch 4 for connecting the incoming lines to the buffer memories and the buffer connection switches for connecting the buffer memories to the outgoing lines 2_1 - 2_m.

This invention has been made to solve the problems as explained above, and has for its object to provide a cell exchanging apparatus which can reduce the number of cells discarded due to collisions using a small number of buffer memories, and which can also reduce the size of switching devices for connecting the buffer memories to incoming lines and outgoing lines.

To achieve the above object, a cell exchanging apparatus of the present invention comprises header processing circuits provided in correspondence to incoming lines for detecting destinations from header portions of received cells, and a plurality of buffer memories capable of storing the cells in accordance with specified addresses and reading out the stored cells in accordance with the specified addresses independently of the order of the cells stored. According to one aspect of the present invention, the header processing circuits are connected to the buffer memories through an incoming line spatial switch, and the buffer memories are connected to the outgoing lines through an outgoing line spatial switch. A buffer control circuit controls the incoming line spatial switch to select the buffer memories for writing the cells in the selected buffer memories, and manages the addresses of the written cells in the buffer memories for each of the destinations of the cells. The buffer control circuit also controls the outgoing line spatial switch in accordance with those addresses under management so that the cells are output to the specified outgoing lines in a predetermined order.

Thus, the cells input through the incoming lines are stored in the buffer memories selected by the incoming line spatial switch after detection of the cell destinations. The addresses of the stored cells in the buffer memories are managed for each of the destinations of the cells. In accordance with the addresses under management for each destination, the buffer memories are accessed to cause the cells stored therein to be read out and output to the outgoing lines connected to the buffer memories through the outgoing line spatial switch. Consequently, when reading the cells out of the buffer memories, a plurality of cells can be led to the outgoing lines through the spatial switch while avoiding collision between cells. Also, a processing

speed (rate) is the same throughout the circuits, whereby the cells can be exchanged without any necessity to increase such a speed. Furthermore, the number of buffer memories can be reduced, which enables a lowering in the number of cells discarded when the number of written cells exceeds the capacity of the buffer memories, without any necessity to increase the size of the spatial switches for connecting the buffer memories to the incoming lines and the outgoing lines.

According to another aspect to the present invention, the cells input through the incoming lines are held in the header processing circuits for a period of one time slot. The buffer memories are provided in number equal to or greater than (number of incoming lines + number of outgoing lines - 1). The buffer control circuit controls the incoming line spatial switch such that the cells held in the header processing circuits are written in the buffer memories which are selected so as to avoid the overlapping of the cells, i.e., to prevent a plurality of cells from being written in one buffer memory at the same time within one time slot. The outgoing line spatial switch is controlled such that, when the cells have already been written in the buffer memories and are managed using the addresses in the buffer memories for each of the destinations and for each of the reading time slots so as to avoid the overlapping of the destinations within the same time slot, the cells are output to the outgoing lines specified by the cell header portions in a predetermined order.

Thus, by setting one time slot as the operation cycle unit, the cells held in the header processing circuits are written in the buffer memories selected so as to avoid the overlapping of the cells within one time slot. The cells which are managed using the addresses in the buffer memories for each of the destinations and reading time slots so as to avoid the overlapping of the destinations within the same time slot are read out to the outgoing lines specified by the header portions. Consequently, it is possible to reduce the number of cells discarded due to collision therebetween or delay of the cells during the writing and reading operations.

According to still another aspect of the present invention, outgoing line speed adjusting buffers connected to the buffer memories through the outgoing line spatial switch for storing the cells to adjust an outgoing line speed are additionally provided in correspondence to the outgoing lines. The buffer control circuit functions to control the incoming line spatial switch to select the buffer memories in which the cells are to be written, to manage the addresses of the cells written in the buffer memories for each destination, to read the cells out of the buffer memories in accordance with those addresses under management in a predetermined order at a speed r ($2 \leq r <$ number of outgoing lines) times the outgoing line speed, to control the outgoing line spatial switch to write the read-out cells in the specified outgoing line speed adjusting buffers in a predetermined order, and to read out those written cells in accordance with the outgoing line speed to output the cells to the outgoing lines.

Thus, the cells the destinations of which have been detected are stored in the selected buffer memories. The addresses of the cells stored in the buffer memories are managed for each destination, and the buffer memories are accessed in accordance with those addresses for reading out the stored cells at a speed r ($2 \leq r <$ number of outgoing lines) times the outgoing line speed. Consequently, when reading the cells out of the buffer memories, a plurality of cells can be led to the outgoing lines through the spatial switch so as to avoid any collision between cells, while allowing the cells up to a number of r to be read out of the same buffer memory in overlapped relation. The reading speed is raised as high as r times the outgoing line speed at its maximum and, therefore, the cells can be exchanged without any necessity to increase the speed. Because the opportunities of reading the cells out of the same buffer memory is increased, it is possible to further reduce the number of cells discarded by collision during the reading operation.

According to still another aspect of the present invention, incoming line speed adjusting buffers for storing the cells to adjust an incoming speed are additionally provided in correspondence to the incoming lines. The buffer control circuit functions to control the outgoing line spatial switch to control the connection between the buffer memories and the outgoing lines, to control the incoming line spatial switch to select the buffer memories in which the cells are to be written, to write the cells read out of the incoming line speed adjusting buffers to the selected buffer memories at a speed w ($2 \leq w <$ number of incoming lines) times the incoming line speed, to manage the addresses of the cells written in the buffer memories for each destination, and to control the outgoing line spatial switch in accordance with those addresses under management to output the cells to the specified outgoing lines in a predetermined order.

Thus, the cells for which destinations have been detected are written in the buffer memories selected by the incoming line spatial switch as a speed w ($2 \leq w <$ number of incoming lines) times the incoming line speed. The addresses of the cells stored in the buffer memories are managed for each destination, and the buffer memories are accessed in accordance with those addresses for reading out the stored cells. Consequently, even in a condition that the buffer memories become al-

most full with cells and a plurality of cells must be written in one buffer memory in one time slot, it is possible to write up to w cells in one buffer memory. Also, when reading the cells out of the buffer memories, a plurality of cells can be led to the outgoing lines through the spatial switch, while avoiding collisions between cells. The writing speed is raised as high as w times the incoming line speed at its maximum and, therefore, the cells can be exchanged without any necessity to increase the speed. As a result, it is possible to further reduce the number of cells discarded due to collision during the writing operation.

The above and other objects and advantages of the present invention will be become clearer from reading the following description with reference to the accompanying drawings which illustrate several preferred embodiments by way of example.

Fig. 1 is a block diagram showing a conventional cell exchanging apparatus;

Fig. 2 is a time chart showing a timing relation between signals at various points in the cell exchanging apparatus of Fig. 1;

Fig. 3 is a block diagram showing a cell exchanging apparatus according to a first embodiment of the present invention;

Fig. 4 is a time chart showing a timing relation between signals at various points in the cell exchanging apparatus of Fig. 3;

Fig. 5 is a block diagram showing a cell exchanging apparatus according to a second embodiment of the present invention;

Fig. 6 is a time chart showing a timing relation between signals at various points in the cell exchanging apparatus of Fig. 5;

Fig. 7 is a block diagram showing a cell exchanging apparatus according to a third embodiment of the present invention;

Fig. 8 is a time chart showing a timing relation between signals at various points in the cell exchanging apparatus of Fig. 7;

Fig. 9 is an enlarged time chart showing an main part of the time chart of Fig. 8;

Fig. 10 is a block diagram showing a cell exchanging apparatus according to a forth embodiment of the present invention; and

Fig. 11 is a time chart showing a timing relation between signals at various points in the cell exchanging apparatus of Fig. 10.

Hereinafter, several preferred embodiments of the present invention will be described by referring to the drawings. Fig. 3 is a block diagram showing the structure of a cell exchanging apparatus according to a first embodiment of the present invention. In Fig. 3, denoted by 1_1 -1_n are n ($n \geqq 2$) incoming lines through which cells are input, each cell comprising a data portion and a header portion including an outgoing line number as destination information. 2_1 - 2_m designates m ($m \geqq 2$) outgoing lines through which the cells are output dependent on the designations specified by their header portions. The above arrangement is identical to that shown in Fig. 1.

Denoted by $10a_1$ - $10a_n$ are header processing circuits provided in correspondence to the incoming lines 1_1 - 1_n for detecting the outgoing lines designated by the header portions of the cells received through the incoming lines. 11_1 - 11_p designate p ($p \geqq 2$) buffer memories, each buffer memory being capable of storing cells at specified addresses and reading out the stored cells by specifying the addresses regardless of the order in which the cells are stored or written. These buffer memories 11_1 - 11_p are different from the conventional buffer memories 3_1 - 3_ℓ shown in Fig. 1 in that a plurality of cells can be stored in each buffer memory. 12_1 - 12_p designate storage control circuits provided in correspondence to the buffer memories 11_1 - 11_p, each storage control circuit supervising empty addresses using, for example, an FIFO-type memory to give an associated one of the buffer memories 11_1 - 11_p READ and WRITE addresses.

Denoted by 13 is an incoming line spatial switch for selectively connecting the header processing circuits $10a_1$ - $10a_n$ to predetermined buffer memories 11_1 - 11_p, and 14 designates an outgoing line spatial switch for selectively connecting the buffer memories 11_1 - 11_p to predetermined outgoing lines 2_1 - 2_m.

Denoted by 15a is a buffer control circuit which functions to (i) control a switching operation of the incoming line spatial switch 13 to select the buffer memories in which cells are to be stored, (ii) manage the addresses of the stored cells in the buffer memories on the basis of the respective destinations of the cells, and (iii) control a switching operation of the outgoing line spatial switch 14 in accordance with the addresses under management for the respective destinations, thereby outputting the cells, in a predetermined order, to the outgoing lines specified by the cell headers.

The buffer control circuit 15a comprises a first buffer selection circuit 16 which, when a cell arrives along one of the incoming lines 1_1 - 1_n, receives the outgoing line number of the cell detected by the header processing circuits $10a_1$ - $10a_n$ associated with that incoming line, selects one of the buffer memories 11_1 - 11_p in which the cell is to be stored, and controls a switching operation of the incoming line spatial switch 13 so that the selected buffer memory is connected to the cell-detecting header processing circuit. 17 designates an address exchanging circuit which functions to sort out the arriving cells on the basis of the destinations, i.e., the outgoing lines, by referring to the outgoing

line numbers detected by the buffer selection circuit 16, and obtain, from the storage control circuits associated with the buffer memories, the WRITE addresses in the buffer memories in which the cells are written to write the obtained WRITE addresses in address queues (described later).

Denoted by 18_1 - 18_m are address queues each constituted by an FIFO-type memory and provided in corresponding to the outgoing lines 2_1 - 2_m. The address exchanging circuit 17 writes, in the address queues, the WRITE addresses in the buffer memories in which the cells destined for the outgoing lines are stored, in the order in which the addresses arrive, for every outgoing lines 2_1 - 2_m corresponding to the address queues. 19 designates a second buffer selection circuit which functions to determine the cells to be read out of the buffer memories by referring to the address queues 18_1 - 18_m, send the address read out of the address queues, as READ addresses, to the storage control circuits associated with the corresponding buffer memories, and control a switching operation of the outgoing line spatial switch 14 to cause the buffer memories to the corresponding outgoing lines.

An operation of this cell exchanging apparatus will be described below. Fig. 4 is a time chart showing a timing relation between signals at various points in the cell exchanging apparatus. The time chart illustrates a control flow in which the number n of the incoming lines 1_1 - 1_n and the number m of the outgoing lines 2_1 - 2_m are respectively four (4) and the number p of the buffer memories 11_1 - 11_p is ten (10). It is also assumed that the cells handled here are input at random and have a fixed length, and that the phases of the respective cells are adjusted prior to being input to the incoming lines 1_1 - 1_n in such a manner that the cells are supplied at the same phase through all the incoming lines.

Figs. 4(a) - 4(d) show examples of the cells input to the incoming lines 1_1 - 1_4, Figs. 4(e) - 4(n) show examples of the cells stored in the buffer memories 11_1 - 11_{10} in that case, the Figs. 4(o) - 4(r) show examples of the cells output to the outgoing lines 2_1 - 2_4. It is assumed that all the circuits are synchronized with each other, and one cell per one time slot can be input and output.

When the cells are input to the incoming lines, the header processing circuits $10a_1$ - $10a_4$ provided in correspondence to the incoming lines 1_1 - 1_4 detect the outgoing line numbers from the header portions of the input cells. While referring to the header processing circuits $10a_1$ -$10a_4$, the first buffer selection circuit 16 of the buffer control circuit 15a instructs the incoming line spatial switch 13 to respectively connect the incoming lines along which the cells have arrived to the buffer memories which are selected for storing the cells.

The manner in which the incoming line spatial switch 13 connects between the incoming lines and the buffer memories can be described in various ways. It is undesirable that two or more cells to be read exist in the same buffer memory at the time the cells are stored and then read out of the buffer memories. To avoid this, the cells are preferably distributed to a number of buffer memories. To accomplish this the same number of buffer memories as that of the incoming lines is not sufficient. Control is facilitated by using as many buffer memories as possible. As a simpler example of control, it can also be envisaged to select a buffer memory which holds the least number of cells therein, and to write cells in the buffer memory. In other words, when x cells arrive simultaneously, x buffer memories which hold the least number of cells therein are selected, and the incoming lines receiving the x cells are spatially connected to the selected buffer memories.

Fig. 4 shows, as a further simpler example of control, a manner in which the buffer memories 11_1 - 11_{10} are sequentially selected and arriving cells are written in the buffer memories. In other words, the buffer memories 11_1, 11_2, 11_3, ..., 11_{10} are written therein successively. In a time slot 1, the first cell of a signal f (referred to as an "F1 cell" herein; the remaining cells are similarly referred to) is input from the incoming line 1_1, a G1 cell of a signal g from the incoming line 1_2, and an I1 cell of a signal i from the incoming line 1_4. The header portion of the respective cells include outgoing line numbers; that is, the F1 cell has the number O_1 specifying the outgoing line 2_1, the G1 cell has O_4 specifying the outgoing line 2_4, and the I1 cell has O_3 specifying the outgoing line 2_3, respectively. In a time slot 2, the incoming line spatial switch 13 connects the incoming line 1_1 to the buffer memory 11_1, the incoming line 1_2 to the buffer memory 11_2, and the incoming line 1_4 to the buffer memory 11_3, respectively. Therefore, these cells are stored, in the time slot 2, in the buffer memories 11_1 - 11_4 at the addresses specified by the storage control circuits 12_1 - 12_3. At this time, the storage control circuits 12_1 - 12_3 send the WRITE addresses of the buffer memories to the address exchanging circuit 17. The WRITE addresses are selected from among those addresses which are managed by the storage control circuits 12_1 - 12_3 as empty addresses. The address exchanging circuit 17 sorts out the input cells for each destination outgoing line in reference to the first buffer selection circuit 16, and writes the WRITE address of the buffer memory 11_1 in the tail end of the address queue 18_1, the WRITE address of the buffer memory 11_2 in the tail end of the address queue 18_4, and the WRITE address of the buffer memory 11_3 in the

tail end of the address queue 18_3, respectively.

Then, in a time slot 3, the second buffer selection circuit 19 takes out the addresses stored in the address queues 18_1 - 18_3, sends the addresses to the storage control circuits 12_1 - 12_3 associated with the buffer memories 11_1 -11_3, and instructs the outgoing line spatial switch 14 to connect the buffer memories 11_1 - 11_3 to the outgoing lines 2_1, 2_3 and 2_4, respectively. The outgoing line spatial switch 14 connects the buffer memory 11_1 to the outgoing line 2_1, the buffer memory 11_2 to the outgoing line 2_4 and the buffer memory 11_3 to the outgoing line 2_3, respectively, in the time slot 3. The storage control circuits 12_1 -12_3 send the received addresses to the associated buffer memories 11_1 - 11_3 as READ addresses and, thereafter, manage those addresses as empty ones. The cells read out of the respective buffer memories 11_1 - 11_3 are output to the destination outgong lines 2_1, 2_4 and 2_3 specified by their headers, respectively.

While the outgoing lines specified by the input cells are different from one another in the above example, the cells input in the time slot 2 have the header portions specifying the same destination outgoing lines. An F2 cell, a G2 cell and an H1 cell input in the time slot 2 are respectively written in the buffer memories 11_4, 11_5 and 11_6 in a like manner, but the header portions of these three cells include the outgoing line number O_4 specifying the same outgoing line 2_4. In the example of Fig. 4, higher priority is given for an incoming line of a smaller number, thereby to causing cells to be delayed. The F2, G2 and H1 cells are read out of the buffer memories 11_4, 11_5 and 11_6 in this order in time slots 4, 5 and 6, respectively, and output to the outgoing line 2_4. Subsequently, such cell exchange will be executed in the manner described above.

In a time slot 8, an I2 cell and an H6 cell are stored in the buffer memory 11_3. Although these I2 and H6 cells have different destinations, i.e., the outgoing line 2_2 and the outgoing line 2_3, respectively, they are stored in the same buffer memory 11_3 and hence cannot be taken out simultaneously. In such a case, a collision of the two cells can be avoided by giving the outgoing lines 2_1 - 2_4 fixed preferential orders or variable preferential orders to be changed on the basis of a random number and by taking out only one cell, e.g., the I2 cell while delaying the other H6 cell. A similar event also occurs in other time slots 9, 10 and 15, but not cell is lost due to collision.

In the cell exchanging apparatus according to the first embodiment, as described above, the cells input through the incoming lines are stored in the respective buffer memories selected by the incoming line spatial switch, after the detection of the cell destinations. The addresses of the stored cells in the buffer memories are managed for each of the destinations of the cells. In accordance with the addresses under management for each destination, the buffer memories are accessed for reading out the cells stored therein and outputting those cells to desired outgoing lines connected to the buffer memories through the outgoing line spatial switch. As a result, it is possible to achieve a cell exchanging apparatus which can lower the number of discarded cells due to collision by using a relatively small number of buffer memories, and can reduce the size of swtich devices for connecting the buffer memories to incoming and outgoing lines.

Fig. 5 is a block diagram showing the construction of a cell exchanging apparatus according to a second embodiment of the present invention. In Fig. 5, the same or corresponding elements are denoted by the same reference numerals as in the cell exchanging apparatus according to the first embodiment and not explained here.

Referring to Fig. 5, denoted by $10b_1$ - $10b_n$ are header processing circuits provided in correspondence to the incoming lines 1_1 - 1_n for detecting the outgoing lines from the header portions of the cells input through the incoming lines and for holding the cells therein for a period of one tme slot. The buffer memories 11_1 - 11_p are provided in a number corresponding to p = (n + m - 1). 15b designates a buffer control circuit which (i), for a period of one time slot, controls a switching operation of the incoming line spatial switch 13 to select the buffer memories in which the cells are to be written (i.e., the writing of cells), (ii) manages, for each of the destination of the cells and for each time slot for reading out the cells, the addresses of the stored cells in the buffer memories and (iii) outputs the cells in each reading time slot to the outgoing lines specified by their headers in a predetermined order.

The buffer control circuit 15b comprises an address table 21 provided in correspondence to the outgoing lines 2_1 - 2_m. When the cells arrive through the incoming lines, the address table 21 receives the outgoing line numbers of the arriving cells which are detected by the header processing circuits associated with the incoming lines, and selects the buffer memories in which the cells are to be stored, and then stores the buffer memory numbers and the corresponding WRITE addresses in the table for each of the destination outgoing lines. 20 designates an incoming line connection instructing circuit which receives the number of the buffer memories storing the cells determined by the address table 21 and the WRITE addresses and controls a switching operation of the incoming line spatial swtich 13 to connect between the header processing circuits $10b_1$ - $10b_n$ and the buffer memories 11_1 - 11_p. 22 designates an outgoing line

connection instructing circuit which determines the cells to be read out of the buffer memories in reference to the address table 21, sends the addresses read out of the address table 21, as READ addresses, to the storage control circuits associated with the buffer memories, and controls a switching operation of the outgoing line spatial switch 14 to connect the buffer memories to the corresponding outgoing lines respectively.

An operation of this cell exchanging apparatus will be described below. Fig. 6 is a time chart showing a timing relation between signals at various points in the cell exchanging apparatus. The time chart illustrates a control flow in which the number n of the incoming lines 1_1 - 1_n and the number m of the outgoing lines 2_1 - 2_m are each four (4) and the number p of the buffer memories 11_1 - 11_p is equal to (n + m - 1); i.e., seven (7). It is also assumed that the cells handled here have a fixed length, and that the input phases of the respective cells are adjusted prior to being input to the incoming lines 1_1 - 1_n in such a manner that input cells are supplied at the same phase through all the incoming lines. For convenience of explanation, those incoming lines 1_1 - 1_4 are indicated by I_0, I_1, I_2 and I_3, and those outgoing lines 2_1 - 2_4 are indicated by O_0, O_1, O_2 and O_3, respectively. Further, the buffer memories 11_1 -11_7 are indicated by buffer #0, buffer #1, ..., buffer #6, respectively.

Fig. 6(a) shows time slot numbers, Fig. 6(b) shows examples of the cells input to the incoming lines I_0 - I_3, Fig. 6(c) shows the internal state of the address table 21, Figs. 6(d) and (e) show the internal states of the incoming line connection instructing circuit 20 and the outgoing line connection instruction circuit 22, respectively, Fig. 6(f) shows the state of the buffer memories 11_1 - 11_7 storing cells, and Fig. 6(g) shows the cells output through the outgoing lines O_1 - O_3. It is assumed that all the circuits are synchronized with each other, and only on cell can be input and output per one time slot.

When the cells are input to the incoming lines, the header processing circuits $10b_1$ - $10b_4$ provided in correspondence to the incoming lines I_0 - I_3 detect the outgoing line numbers from the header portions of the input cells, and hold the cells for a period of one time slot. In reference to the header processing circuit $10b_1$ - $10b_4$, the address table 21 in the buffer control circuit 15b determines in which buffer memory the cells input through the incoming lines are to be written. When the determined result is instructed to the incoming line connection instructing circuit 20, the incoming line spatial switch 13 connects the incoming lines at which the cells have arrived to the buffer memories which have been selected for storing the cells. Because only one cell can be written in and read out of one buffer memory within the same one time slot, the buffer memories 11_1 - 11_7 must be so selected that the writing and reading of a plurality of cells do not occur in the same time slot.

The address table 21 includes a table rows of which represent destination outgong lines and columns of which represent reading time slots. Each of the boxes in the table contains the buffer memory number and the address in the buffer memory in which the cell to be read out in that time slot is written. Null signals are put in those boxes corresponding to the outgoing lines through which no cells are to be output in any time slots. Upon arrival of the cells, the incoming line spatial switch 13 can be considered to connect the cells to the buffer memories 11_1 - 11_7 in various ways. It is, however, undesirable for two or more cells to exist in the same one buffer memory in the case where the cells are stored and then read out of the buffer memories. To prevent this situation, the cells are preferably distributed to a number of buffer memories. To do this, employing the same number of buffer memories as that of the incoming lines is not sufficient. Also, when the cells are written, different buffer memories must be selected. Therefore, the number p of the buffer memories should be at least (number n of incoming lines) + (number m of outgoing lines) - 1. (In this second embodiment, the number p of the buffer memories is 7.)

In Fig. 6, the matrix-like table in the address table 21 is partitioned for each of the reading time slots. Because the capacity is finite, the table is cyclically reused in various time slots. To this end, a READ pointer rp is employed to point a READ position in the next time slot, and is cyclically updated. The table is arranged to prepare queues for the arriving cells in the order of arrival for each of the destination outgoing lines. Fig. 6 shows an example of WRITE pointers wp_0 - wp_3 employed for the respective destination outgoing lines to point the next writing positions next to the tail ends of the respective queues.

In order to determine the buffer memories in which the cells are to be written, when the cells arrive at the incoming lines, the buffer memories 11_1 - 11_7 are checked sequentially from the incoming lines I_1 - I_3 to confirm that the writing of a plurality of cells in the same buffer memory will not be effected in the same time slot and that the reading of a plurality of cells out of the same buffer memory will not be effected in the same time slot, and then buffer memories in which the cells to be written are determined. In this case, those buffer memories which are not filled with cells are selected in a cyclic manner.

In Fig. 6, it is assumed that no cell arrives before a time slot 1, and that three cells arrive through the incoming lines I_0, I_1 and I_3 in the time

slot 1. each cell is identified using the incoming line number, the outgoing line number and the time slot in which the cell arrived. For instance, a cell 312 indicates that his cell arrives through the incoming line I_3 in the time slot 2 and is destined for the outgoing line O_1. The READ pointer rp is positioned at the column No. 2 in the table in the time slot 1, and, it is assumed that, though not shown in Fig. 6, the WRITE pointer wp_0 - wp_3 are all positioned at the column No. 3 in the table at the beginning of the time slot 1. A cell 011 arriving through the incoming line I_0 is stored in, for example, the buffer #0 because no other cell exists the table at this time slot. This buffer memory 11_1 is associated with the storage control circuit 12_1 for managing the WRITE addresses. The WRITE address of the cell 011 is assumed to be 0. As shown in Fig. 6(c), in each box the upper side represents a buffer memory number and the lower side represents an address in the buffer memory. A cell 121 arriving through the incoming line I_1 is destined for the outgoing line O_2 and, therefore, a buffer memory other than the buffer #0, for example, the buffer #1, used for storing the cell 011 is selected as a candidate. In reading the cell 121, it is required to check the column No. 3 in the table. Because only the buffer #0 is used in addition to the buffer #1, the buffer #1 meets the requirements. Accordingly, the cell 121 is stored at an address 0 in the buffer #1. A cell 311 arriving through incoming line I_3 is destined for the outgoing line O_1 and, therefore, stored at an address 0 in a buffer other than the buffer #0 and #1 used for storing the cells 011 and 121, that is, in the buffer #2, for example. When the writing and reading of the cells in the next time slot are determined, as explained above, the address table 21 sends constructions to the incoming line connection instructing circuit 20 and the outgoing line connection instruction circuit 22 to cause the incoming line spatial switch 13 and the outgoing line spatial switch 14 to perform necessary exchanging operations. Thus, the incoming line spatial swtich 13 connects the incoming line I_0 to the buffer #0, the incoming line I_1 to the buffer #1 and the incoming line I_3 to the buffer #2, respectively and the cells are written in these buffers in the time slot 2. The column No. 2 of the table pointed by the READ pointer rp is fully occupied by null signals and, therefore, the outgoing line connection instructing circuit 22 is instructed to cause the outgoing line spatial switch 14 to perform no exchanging operation.

In the time slot 2, cells arrive through all the incoming lines I_0 - I_3. Similar to the operation in the time slot 1, some of the buffer memories 11_1 - 11_7 are selected so that a plurality of cells will not be written in or read out of the same buffer memory in the same time slot. In the time slot 2, the READ pointer rp is updated by one as compared with the time slot 1 and positioned in the column No. 3 of the table. The cell information in the column No. 3 of the table is sent to the outgoing line connection instructing circuit 22. The outgoing line spatial switch 14 then connects the buffer #0 to the outgoing line O_1 and the buffer #1 to the outgoing line O_2 in a time slot 3, respectively, and the reading of the cells is effected in the time slot 3.

As can be understood from the above description, when a cell arrives through the incoming lines, the buffer memories 11_1 - 11_7 are checked in turn to confirm that a plurality of cells will not be written in the same buffer memory in the same single time slot, and a plurality of cells will not be read out of the same buffer memory in the same single time slot. Then, a buffer memory in which the cell is to be written is determined as a candidate. At this time, those buffer memories which are not filled with the cells are selected as candidates in a cyclic manner. In a time slot 4, a cell 134 being destined for an outgoing line O_3, the buffer #5 was first selected as a candidate. However, because the cell in the buffer #5 is read out in the same time slot, the buffer #6 is determined as a candidate. Likewise, the buffer #3 is finally selected for a cell 304. These two examples are indicated by o in Fig. 6.

As described above, in the cell exchanging apparatus according to the second embodiment, one time slot is set as the unit of an operation cycle, and cells are written in buffer memories selected so as to avoid overlapping of the cells within each time slot. Cells are written in buffer memories, and are managed, in addresses in the buffer memories, for each destination and for each reading time slot in such a manner as to avoid overlapping of destinations within the same time slot. Those cells are then output to predetermined outgong lines. Consequently, as compared with the case of merely allocating the buffer memories 11_1 - 11_7 in a cyclic manner, it is possible to avoid any collision between cells, and hence discarding of cells due to collision and delayed reading of the cells during the writing and reading operations can be avoided.

The third embodiment of the present invention will be described below with reference to Figs. 7 - 9.

Fig. 7 is a block diagram showing the construction of a cell exchanging apparatus according to the third embodiment of the present invention. In Fig. 7, the same or corresponding elements are denoted by the same reference numerals as those in the cell exchanging apparatus according to the first embodiment and are not explained here.

Referring to Fig. 7, outgoing line speed adjusting buffers 231 - 23_m are provided in correspondence to the outgoing lines 2_1 - 2_m to be con-

nected to predetermined buffer memories through the outgoing line spatial switch 14. The speed adjusting buffers store the cells read out of the buffer memories at a speed r ($2 \leqq r <$ number of outgoing lines) times the outgoing line speed, and then output the cells of the corresponding outgong lines in accordance with the outgoing line speed.

A buffer control circuit 15c comprises a first buffer selection circuit 16, an address exchanging circuit 17, address queues 181 - 18_m and a second buffer selection circuit 19. The buffer control circuit 15c functions to (i) control a switching operation of the incoming line spatial switch 13 to select the buffer memories in which cells are to be written, (ii) manage the addresses of the written cells in the buffer memories for each of the destinations of the cells, (iii) cause the cells to be read out of the buffer memories in accordance with the managed addresses in a predetermined order at a speed r ($2 \leqq r <$ number of outgoing lines) times the outgoing lines speed, (iv) control the outgoing line spatial switch 14 to cause the read-out cells to be output to the outgoing lines specified by the header portions, (v) write the cells in the corresponding outgoing line speed adjusting buffers, and (vi) read out the stored cells in accordance with the outgoing line speed for outputting them to the corresponding outgoing lines.

An operation of this cell exchanging apparatus will be described below. Fig. 8 is a time chart showing a timing relation between signals at various points in the cell exchanging apparatus. Similar to the first embodiment, the time chart illustrates a control flow in which the number n of the incoming lines 1_1 - 1_n and the number m of the outgoing lines 2_1 - 2_m are each four (4) and that the number p of the buffer memoires 11_1 - 11_p is ten (10). Figs. 8(a) -8(r) show the same states as those in Figs. 4(a) - 4(r), respectively. It is also assumed that cells handled here are input at random and have a fixed length, and that the phases of respective cells are adjusted prior to being input to the incoming lines 1_1 - 1_n in such a manner that the cells are supplied at the same phase through all the incoming lines.

The basic sequence of exchanging cells proceeds in a manner similar to the first embodiment. It is noted that an I2 cell and an H6 cell are both stored in the buffer memory 11_3 in a time slot 8 as illustrated. Although the I2 and H6 cells have destinations different from each other; that is, the I2 cell is destined for the outgoing line 2_2 and the H6 cell is destined for the outgoing cell 2_3, because these cells are stored in the same buffer memory 11_3, they cannot be taken out simultaneously at a speed equal to the outgoing line speed in the outgoing lines 2_1 - 2_4.

Fig. 9 is a time chart partially showing the time slots 6 - 13 in Fig. 8 on a larger scale. Fig. 9 shows the case where the cells are read out of the buffer memories 11_1 - 11_{10} at a speed 3 times the outgoing line speed in the outgoing lines 2_1 - 2_m. In Figs. 9(e) - 9(n) show examples of the cells stored in the buffer memories 11_1 - 11_{10}, Figs. 9(s) - 9(v) show states of the cells written in the outgoing line speed adjusting buffers 23_1 - 23_4, and Figs. 9(o) - 9(r) show examples of the cells output to the outgoing lines 2_1 - 2_4, respectively.

In Fig. 9, the I2 cell and the H6 cell in the buffer memory 11_3 are destined for different destinations in the same time slot 8. However, both the I2 and H6 cells would be simultaneously output to the corresponding outgoing lines 2_2 and 2_3 by reading these cells out of the buffer memory 11_3 at a speed 3 times the outgoing lines speed. Generally, by reading cells out of the buffer memory 11_1 - 11_{10} at a speed 3 times the outgoing line speed, it becomes possible to write in each of the buffer memories 11_1 - 11_{10} up to 3 cells which are to be read out in the same time slot.

Similar events occur in other time slots 9, 10 and 15 as well, but the cells are not in any case required to delay the reading of a cell in order to avoid any collision.

The speed of reading cells out of the buffer memories 11_1 - 11_{10} is not limited to 3 times the outgoing line speed, and may be generally set at r ($2 \leqq r <$ number of outgoing lines) times the outgoing line speed. While it is assumed that the buffer memories 11_1 - 11_{10} are of the type of a dual-port memory, this embodiment is also made feasible by using single-port memories which can operate at a speed double or more the outgoing line speed.

Even in the case that the number of cells read out of the same buffer memory in one time slot exceeds r, a collision between the cells can be avoided by setting the outgoing lines 2_1 - 2_m in a fixed preferential order or variable preferential order changeable at random and by taking out r cells while delaying the reading of the remaining cells.

In the cell exchanging apparatus according to the third embodiment, as described above, since the cells stored in the buffer memories are read out at a speed r ($2 \leqq r <$ number of outgoing lines) times the outgoing line speed, opportunities of reading the cells out of the same buffer memory increase, which enables a reduction in the rate of cells discarded by collision during the reading operation.

Fig. 10 is a block diagram showing the construction of a cell exchanging apparatus according to a fourth embodiment of the present invention. In Fig. 10, the same or corresponding elements are denoted by the same reference numerals as those in the cell exchanging apparatus according to the

third embodiment and are therefore not explained here.

Referring to Fig. 10, incoming line speed adjusting buffers 24_1 - 24_n are provided in correspondence to the incoming lines 1_1 - 1_n for storing the cells output from the corresponding header processing circuits $10a_1$ - $10a_n$ and for then reading the stored cells at a speed w ($2 \leqq w <$ number of incoming lines) times the incoming line speed to deliver the cells to predetermined buffer memories 11_1 - 11_p through the incoming line spatial switch 13.

A buffer control circuit 15d comprises a first buffer selection circuit 16, an address exchanging circuit 17, address queues 18_1 - 18_m and a second buffer selection circuit 19. The buffer control circuit 15d functions to (i) cause the cells stored in the incoming line speed adjusting buffers to be read out at a speed w ($2 \leqq w <$ number of incoming lines) times the incoming line speed, (ii) control the incoming line spatial switch 13 to select the buffer memories in which the cells are to be written, (iii) cause the read-out cells to be written the selected buffer memories at a speed w times the incoming line speed, (iv) manage the addresses of the cells written in the buffer memories for each of the destinations of the cells, and (v) control the outgoing line spatial switch 14 in accordance with those addresses under management for outputting the cells in a predetermined order to the outgoing lines specified by the header portions.

An operation of this cell exchanging apparatus will be described below. Fig. 11 is a time chart showing a timing relation between signals at various points in the cell exchanging apparatus of Fig. 10. Similar to the first embodiment shown in Fig. 4, the time chart illustrates a control flow in which the number n of the incoming lines 1_1 - 1_n and the number m of the outgoing lines 2_1 - 2_m are each four (4) and that the number p of the buffer memories 11_1 -11_p is ten (10). Figs. 11(a) - 11(r) show the same states as those in Figs. 4(a) - 4(r), respectively. It is assumed that the buffer memories 11_1 - 11_p each have capacities equal to two cells, that cells handled in this embodiment are input at random and have a fixed length, and that the phases of respective cells input are adjusted prior to being input to the incoming lines 1_1 - 1_n in such a manner that the input cells are supplied at the same phase through all the incoming lines.

When cells are input through the incoming lines, the header processing circuits associated with the incoming lines detect outgoing line numbers from the cell headers and cause the cells to write in the corresponding incoming line speed adjusting buffers. In reference to the header processing circuits, the first buffer selection circuit 16 in the buffer control circuit 15d instructs the incoming line spatial switch 13 to interconnect the incoming line speed adjusting buffers in which the cells have been written and the buffer memories selected for storing the cells, respectively.

A speed of reading cells out of the incoming line speed adjusting buffers 24_1 - 24_4, i.e., a speed of writing cells in the buffer memories 11_1 - 11_{10} is assumed to be set 2 times the incoming line speed in the incoming lines 1_1 -1_4, thereby allowing two cells to be written in the same buffer memory in one time slot.

Assuming that the buffer memories 11_1, 11_2, 11_3, ..., 11_{10} are selected in this order to cause the arriving cells to be written in the buffer memories in the order of arrival, if some of the buffer memories in which cells are to be written in any time slot are already filled with the cells, the filled buffer memoires are skipped over, and a cell is written in the next buffer memory. In order to make sure that the cells are written in different buffer memories, the cells are preferably distributed by being written in the buffer memories. In this embodiment, because the speed of writing cells in the buffer memories 11_1 - 11_{10} is set at 2 times the incoming line speed, it is possible to write a plurality (two) of cells in which of the buffer memoires 11_1 - 11_{10} in one time slot if any cells are unavoidably discarded, thereby reducing the number of cells discarded.

In Fig. 11, because the buffer memory 11_6 is empty to be able to receive two cells and the buffer memory 11_7 is empty to be able to receive one cell in a time slot 11, three cells, i.e., F10, H10 and I8 cells input in the time slot 11 cannot be written in different buffer memories. By utilizing the fact that the speed of writing cells in the buffer memories 11_1 - 11_{10} is twice the incoming line speed, therefore, the both F10 and H10 cells are written in the buffer memory 11_6 in order to prevent the cells from being discarded. The state after those three cells have been written in the buffer memories is indicated in Figs. 11(i) and 11(j) by putting the symbols F10, H10 and I8 is circles.

The basic sequence of exchanging cells proceeds in a manner similar to the first embodiment.

Although the speed of writing cells in the buffer memories 11_1 - 11_{10} is set at 2 times the incoming line speed in the above case, that speed may generally be set to w ($2 \leqq w <$ number of incoming lines) times the incoming line speed. While it is assumed that the buffer memories 11_1 - 11_{10} are each constituted by dual-port memories, this embodiment is also made feasible by using single-port memories which can operate at a double speed or more.

In the cell exchanging apparatus according to the fourth embodiment, as described above, destinations of cells are detected and the cells are

then written, at a speed w ($2 \leq w <$ number of incoming lines) times the incoming line speed, in the buffer memories selected by the incoming line spatial switch. It is therefore possible to write no more than w cells in the same buffer memory and hence to reduce the number of cells discarded due to collision during the writing operation.

The present invention has been described in detail with particular reference to several preferred embodiments thereof, but variations and modifications of the invention can be effected without departing from the spirit and scope of the invention. For example:

(i) Although the first to fourth embodiments show a single unit cell exchanging apparatus, a plurality of cell exchanging apparatuses may be linked to form a multi-stage configuration;

(ii) Instead of directly designating, as destination (address) information in the header portions, the outgoing line numbers corresponding to the outgoing lines of the cell exchanging apparatus, some conversion process may be allowed; for example, encoded numbers may be provided as destination information in the header portions;

(iii) In Figs. 4, 6, 8 and 11, for simplicity of explanation, when the cells arrive through the incoming lines, the cell exchanging apparatus selects buffer memoires are candidates from one end thereof to the other (in the order of the buffers #0, #1, ... in Fig. 6) for writing the cells in the selected memories. But, it may be possible when there is a difference in the arrival time of the cells to further reduce the number of discarded cells by selecting the buffer memories which hold the least number of cells, as memory candidates, to write the cells in the selected memories, so that the individual buffer memories operate as if as a whole they substantially have capacity equivalent to that of one large-sized buffer memory shared by all the incoming lines;

(iv) Although one cell is output to one outgoing line in the above first to fourth embodiments, it may be possible that the cell selection circuits in the output stage can be arranged to cause one single cell to be output to a plurality of outgoing lines by means of a proper determination of addresses. This permits the addition of a broadcasting function to the cell exchanging apparatus;

(v) It may be possible that, as an alternative structure of the cell, a data portion and a header portion of a cell are separated and transmitted through separate circuits having different speeds, the data and the header portions being respectively allocated to a plurality of signal lines arranged in parallel;

(vi) Although a link speed of the incoming lines is constant in any of the above first to fourth embodiments, traffic convergence can be made possible by setting the reading speed at the buffer memories higher than the link speed of the incoming lines. Conversely, it is also possible to make the link speed of the incoming lines higher than the outgoing line speed. When a plurality of cell exchanging apparatuses are linked with each other as mentioned above, the number of discarded cells between the adjacent stages of the cell exchanging apparatuses can be further lowered by setting a transfer speed between the stages higher than the incoming line speed;

(vi) In any of the above first to fourth embodiments, the address queues are provided in correspondence to the outgoing lines of the cell exchanging apparatus. But, it is also possible to allocate to each outgoing line a plurality of address queues having different priorities and read the cells out of the buffer memories in the order of priority based on symbols placed in addition to the outgoing line numbers in the cell headers for indicating the priority; and

(viii) If it is required to restrict the operation speed, a serial/parallel converter and a parallel/serial converter may be added before and after the cell exchanging apparatus, respectively, thereby carrying out a parallel signal processing.

Claims

1. A cell exchanging apparatus comprising: a plurality of incoming lines to which cells each including a data portion and a header portion including destination information are input; a plurality of outgoing lines to which the cells are output in accordance with the destinations specified by the header portions; header processing circuit means provided in correspondence to said incoming lines for detecting the destination outgoing lines from the header portions of the cells input through said incoming lines; a plurality of buffer memory means in which the cells are written at specified addresses and from which the cells are read out at the specified addresses independently of the order of the cells written; an incoming line spatial switch means for selectively connecting said header processing circuit means to predetermined said buffer memory means; an outgoing line spatial switch means for selectively connecting said buffer memory means to predetermined said outgoing lines; and a buffer control circuit means for controlling said incoming line spatial switch means to select the buffer memory means in which the cells are to be written, said control circuit means managing the addresses of

the cells written in the buffer memory means for each of the destinations of the cells, to control said outgoing line spatial switch means in accordance with the addresses under management so that the cells are output in a predetermined order to the outgoing lines specified by the header portions of the cells.

2. A cell exchanging apparatus comprising; a plurality of incoming lines to which cells each including a data portion and a header portion including destination information are input; a plurality of outgoing lines to which the cells are output in accordance with the destinations specified by the cell header portions; header processing circuit means provided in correspondence to said incoming lines for holding the cells input through said incoming lines for a period of one time slot and for detecting the destination outgoing lines from the header portions; a plurality number of buffer memory means, said number being equal to or greater than (number of incoming lines + number of outgoing lines - 1), the cells being written in said buffer memory means at specified addresses and being read at the specified addresses independently of the order of the cells written; an incoming line spatial switch means for selectively connecting said header processing circuit means to predetermined said buffer memory means; an outgoing line spatial switch means for selectively connecting said buffer memory means to predetermined said outgoing lines; and a buffer control circuit means for controlling said incoming line spatial switch means to cause the cells held in said header processing circuit means to be written, in one time slot, in the buffer memory means which are selected so as to avoid the overlapping of cells, said control circuit means controlling said outgoing line spatial switch means to cause the cells which have already been written in said buffer memory means and are managed under the addresses in said buffer memory means for each destination and for each reading time slot to be output in a predetermined order to the outgoing lines specified by the header portions of the cells.

3. A cell exchanging apparatus comprising: a plurality of incoming lines through which cells each including a data portion and a header portion including destination information are input; a plurality of outgoing lines to which the cells are output in accordance with the destination specified by the header portions; header processing circuit means provided in correspondence to said incoming lines for detecting the destination outgoing lines from the header portions of the cells input through said incoming lines; a plurality of buffer memory means in which the cells are written at specified addresses and from which the cells are read at the specified addresses independently of the order of the cells written; an incoming line spatial switch means for selectively connecting said header processing circuit means to predetermined said buffer memory means; outgoing line speed adjusting buffer means provided in correspondence to said outgoing lines for storing the cells and for adjusting an outgoing line speed; and outgoing line spatial switch means for selectively connecting said buffer memory means to predetermined said outgoing line speed adjusting buffer means; and a buffer control circuit means for controlling said incoming line spatial switch means to select the buffer memory means in which the cells are to be written, said control circuit means managing the addresses of the written cells in said buffer memory means for each of the destinations of the cels so as to cause the cells to be read out of said buffer memory means in a predetermined order in accordance with the addresses under management at a speed arrived at by multiplying the outgoing speed by a number equal to or greater than 2 but smaller than the number of said outgoing lines, said control circuit means further controlling said outgoing line spatial switch means to cause the cells to be output to the outgoing lines specified by the header portions of the cells, whereby the cells are written in said outgoing line speed adjusting buffer means and read out of said outgoing line speed adjusting buffer means in accordance with the outgoing line speed.

4. A cell exchanging apparatus comprising: a plurality of incoming lines through which cells each including a data portion and a header portion including destination information are input; a plurality of outgoing lines to which the cells are output in accordance with destinations specified by the header portions; header processing circuit means provided in correspondence to said incoming lines for detecting the destination outgoing lines from the header portions of the cells input through said incoming lines; incoming line speed adjusting buffer means provided in correspondence to said incoming lines for storing the cells to adjust an incoming line speed; a plurality of buffer memory means in which the cells are written at specified addresses and from which the cells are read independently of the order of the cells written at the specified addresses; an incoming line spatial switch means for selectively connecting said incoming line speed adjusting buffer means to predetermined said buffer memory means; an outgoing line spatial switch means for selectively connecting said buffer memory means to predetermined said outgoing lines; and a buffer control circuit means for causing the cells to be read out of said incoming line speed adjusting buffer means to control said incoming line spatial switch means to select said buffer memory means in which the cells

are to be written, the cells being written in said buffer memory means at a speed arrived at by multiplying the incoming line speed by a number equal to or greater than 2 but smaller than the number of said incoming lines, said control circuit means managing the addresses of the cells written in said buffer memory means for each of the destinations of the cells to control said outgoing line spatial switch means in accordance with the addresses under management so that the cells are output in a predetermined order to the outgoing lines specified by the header portions of the cell.

Fig.1

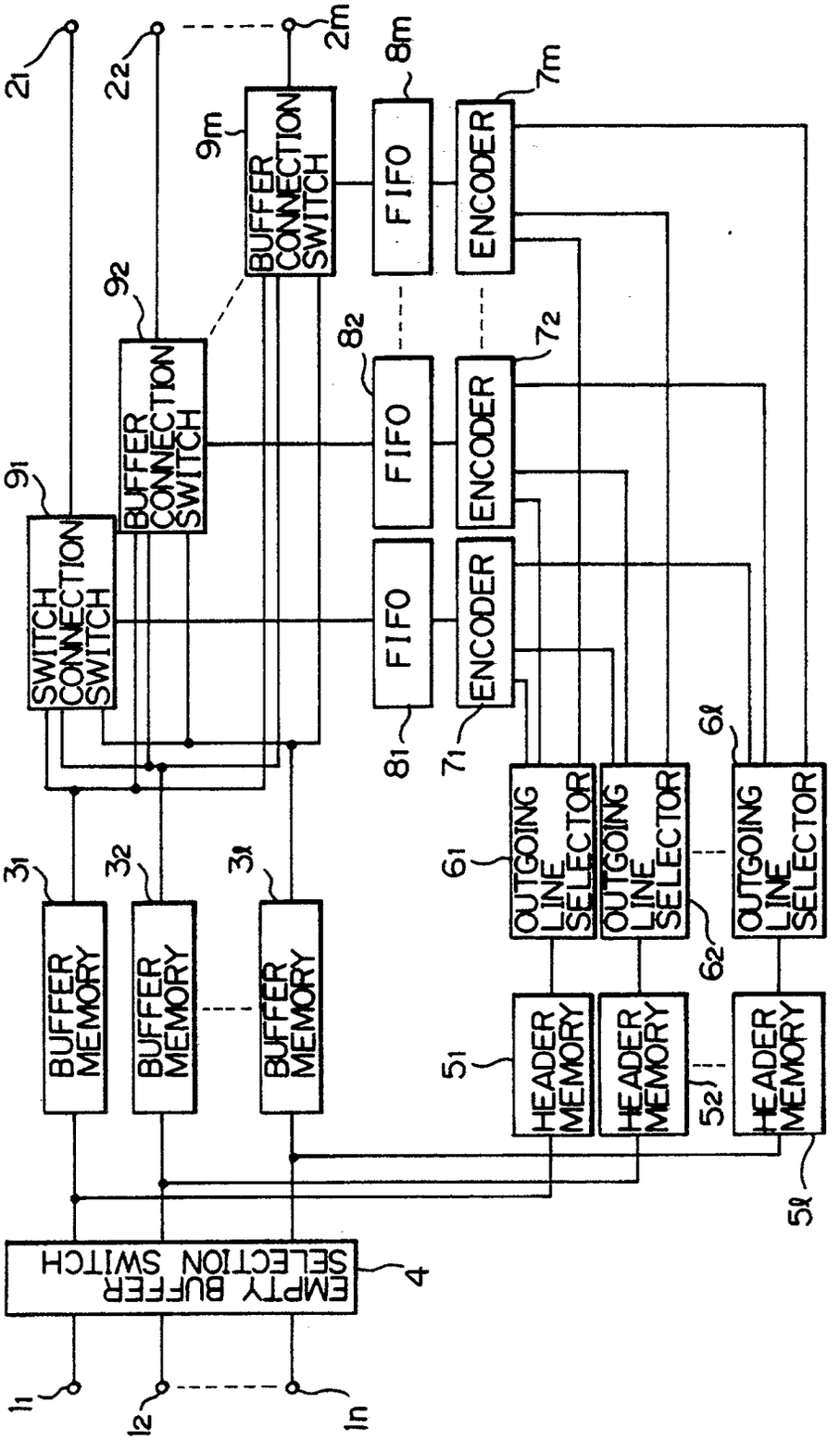

21
22
2m
8m
7m
9m
BUFFER CONNECTION SWITCH
FIFO
ENCODER
92
82
72
BUFFER CONNECTION SWITCH
FIFO
ENCODER
91
SWITCH CONNECTION SWITCH
FIFO
ENCODER
81
71
61
6ℓ
OUTGOING LINE SELECTOR
OUTGOING LINE SELECTOR
OUTGOING LINE SELECTOR
62
31
32
3ℓ
BUFFER MEMORY
BUFFER MEMORY
BUFFER MEMORY
51
HEADER MEMORY
HEADER MEMORY
52
HEADER MEMORY
5ℓ
EMPTY BUFFER SELECTION SWITCH
4
11
12
1n

Fig.2

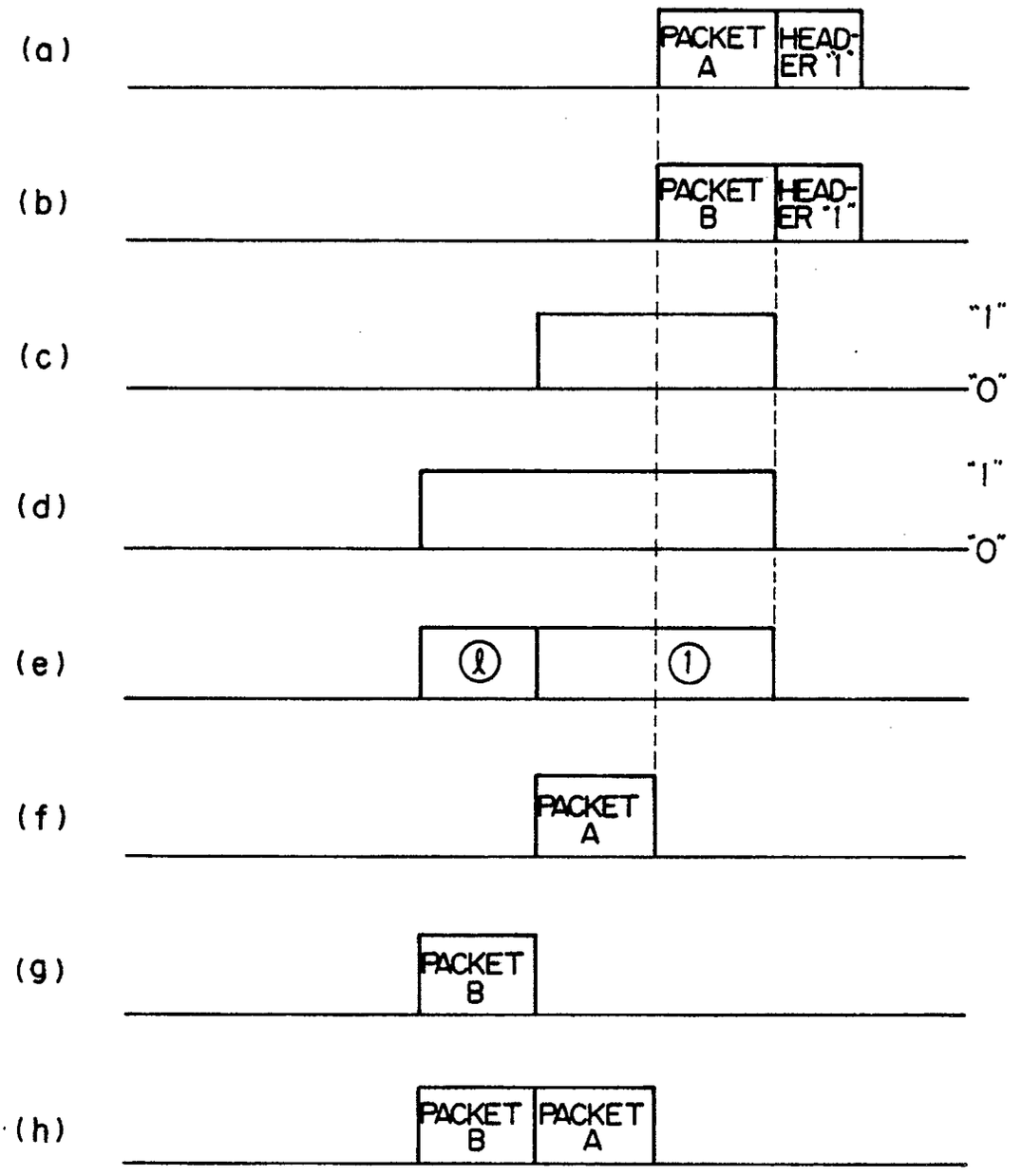
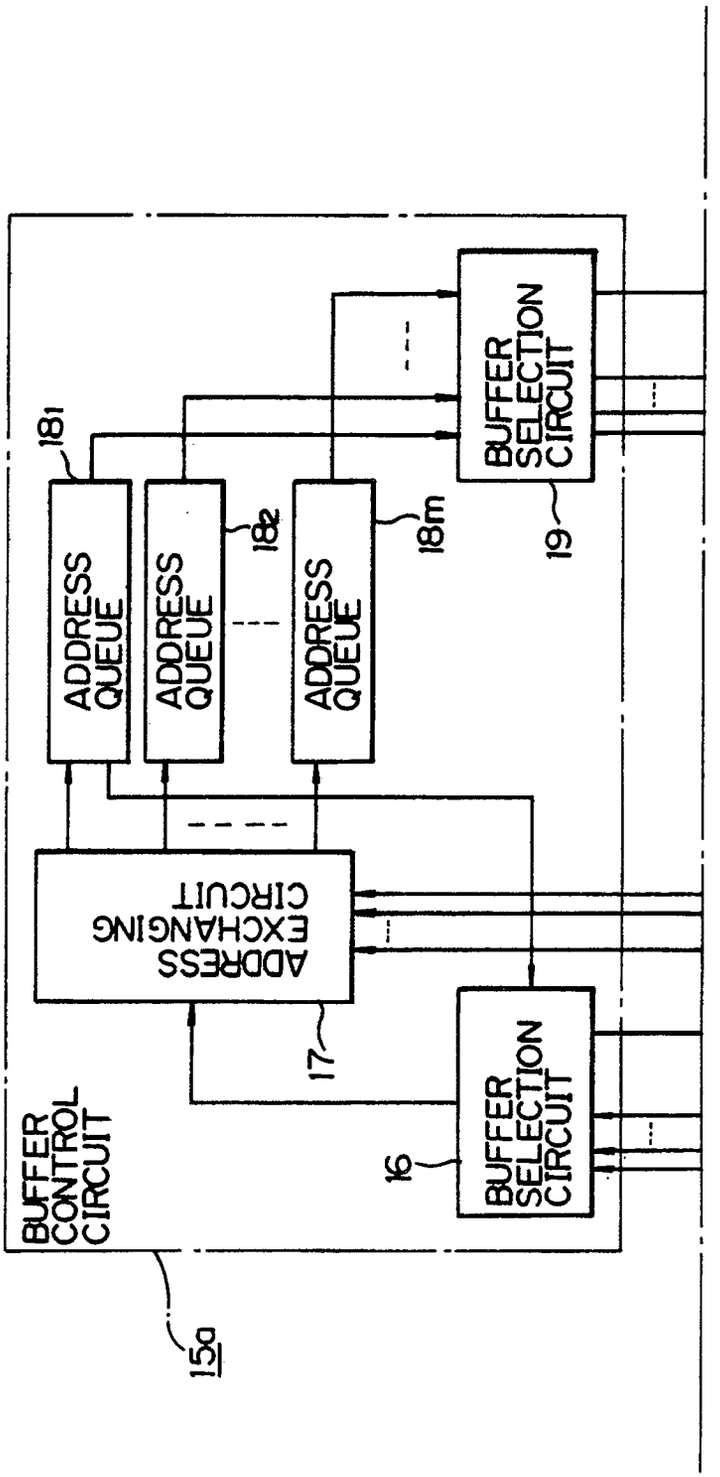

(a)
PACKET A
HEAD-ER "1"
(b)
PACKET B
HEAD-ER "1"
(c)
"1"
"0"
(d)
"1"
"0"
(e)
ℓ
1
(f)
PACKET A
(g)
PACKET B
(h)
PACKET B
PACKET A

Fig.3

Fig.3A
Fig.3B

Fig.3A



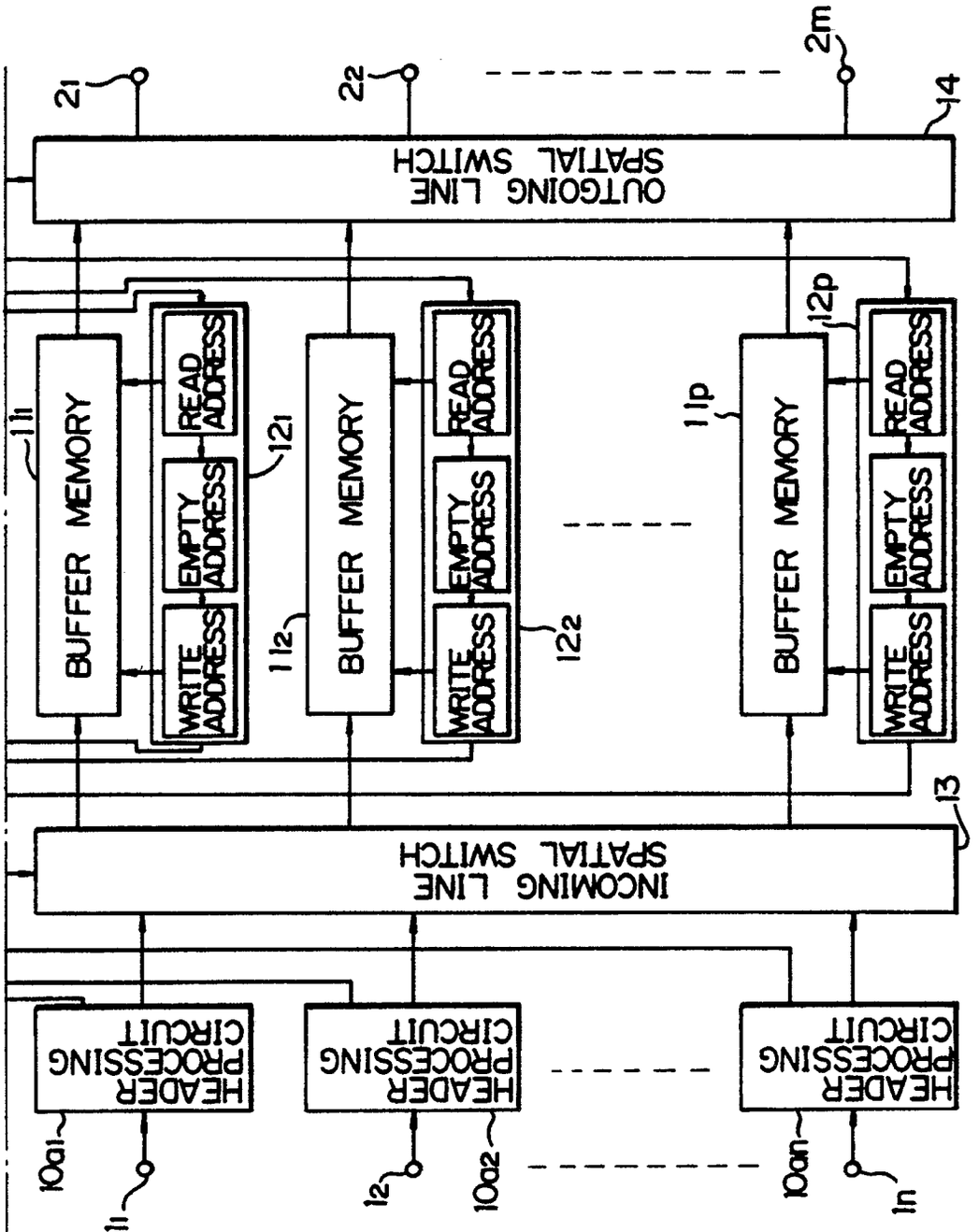

OUTGOING LINE SPATIAL SWITCH
INCOMING LINE SPATIAL SWITCH
BUFFER MEMORY
READ ADDRESS
EMPTY ADDRESS
WRITE ADDRESS
HEADER PROCESSING CIRCUIT
11
12
12p
121
122
13
14
21
22
2m
1p
1n
10a1
10a2
10an

Fig.3B

Fig.4A

Fig.4

Fig.4A | Fig.4B

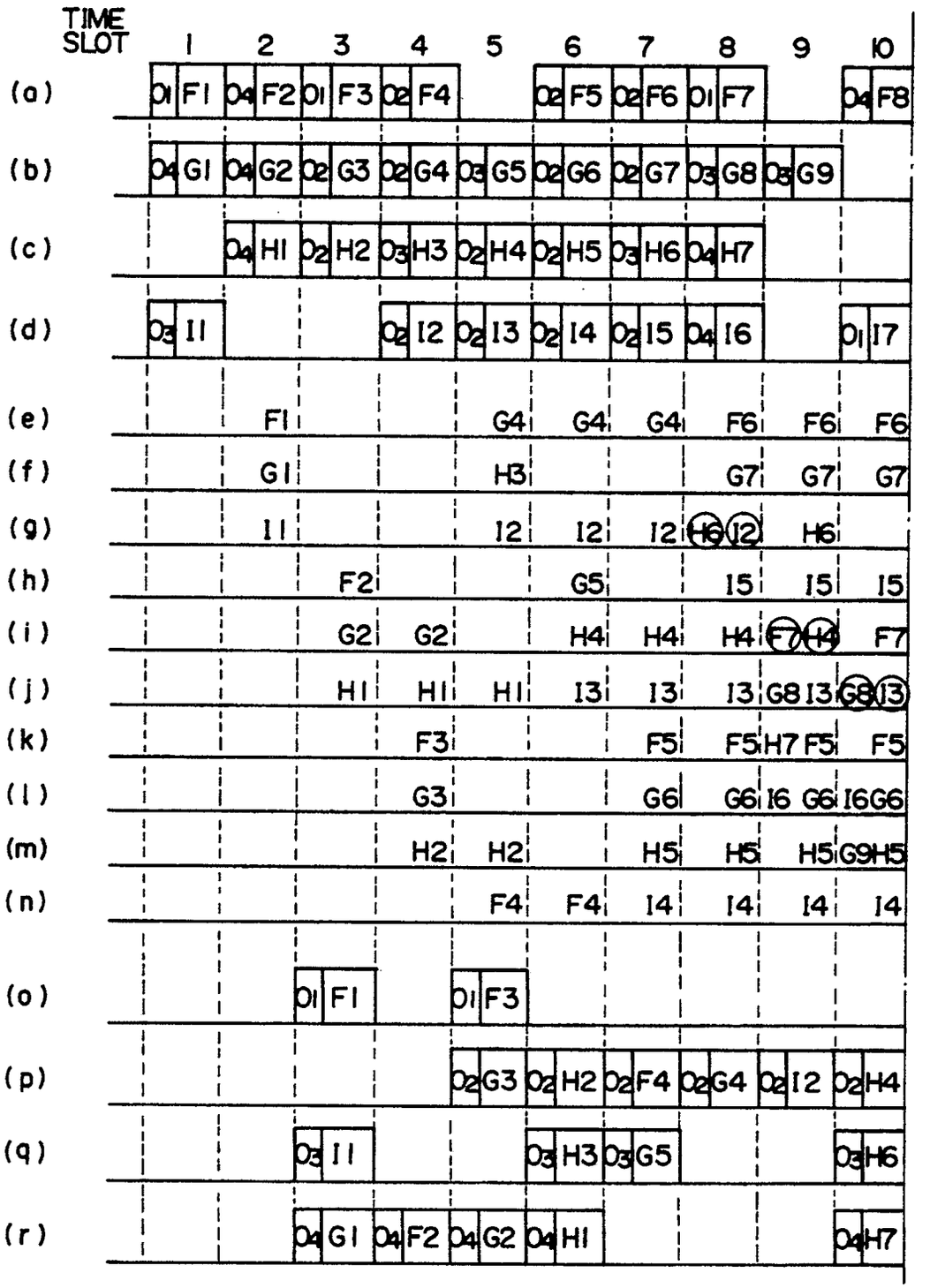


Fig.4B

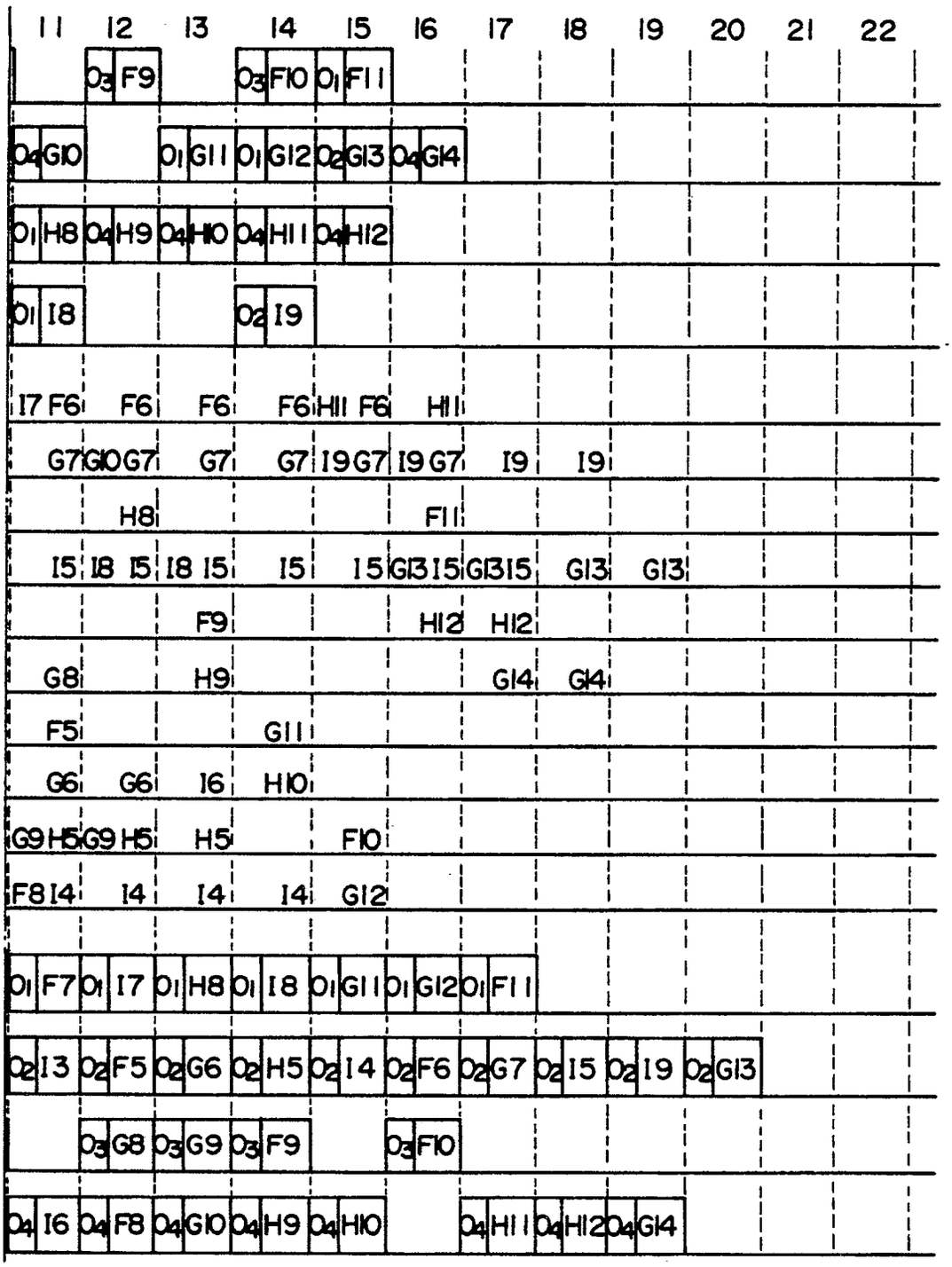

11 12 13 14 15 16 17 18 19 20 21 22
O3 F9 O3 F10 O1 F11
O4 G10 O1 G11 O1 G12 O2 G13 O4 G14
O1 H8 O4 H9 O4 H10 O4 H11 O4 H12
O1 I8 O2 I9
I7 F6 F6 F6 F6 H11 F6 H11
G7 G10 G7 G7 G7 I9 G7 I9 G7 I9 I9
H8 F11
I5 I8 I5 I8 I5 I5 I5 G13 I5 G13 I5 G13 G13
F9 H12 H12
G8 H9 G14 G14
F5 G11
G6 G6 I6 H10
G9 H5 G9 H5 H5 F10
F8 I4 I4 I4 I4 G12
O1 F7 O1 I7 O1 H8 O1 I8 O1 G11 O1 G12 O1 F11
O2 I3 O2 F5 O2 G6 O2 H5 O2 I4 O2 F6 O2 G7 O2 I5 O2 I9 O2 G13
O3 G8 O3 G9 O3 F9 O3 F10
O4 I6 O4 F8 O4 G10 O4 H9 O4 H10 O4 H11 O4 H12 O4 G14

Fig.5

Fig.5A
Fig.5B

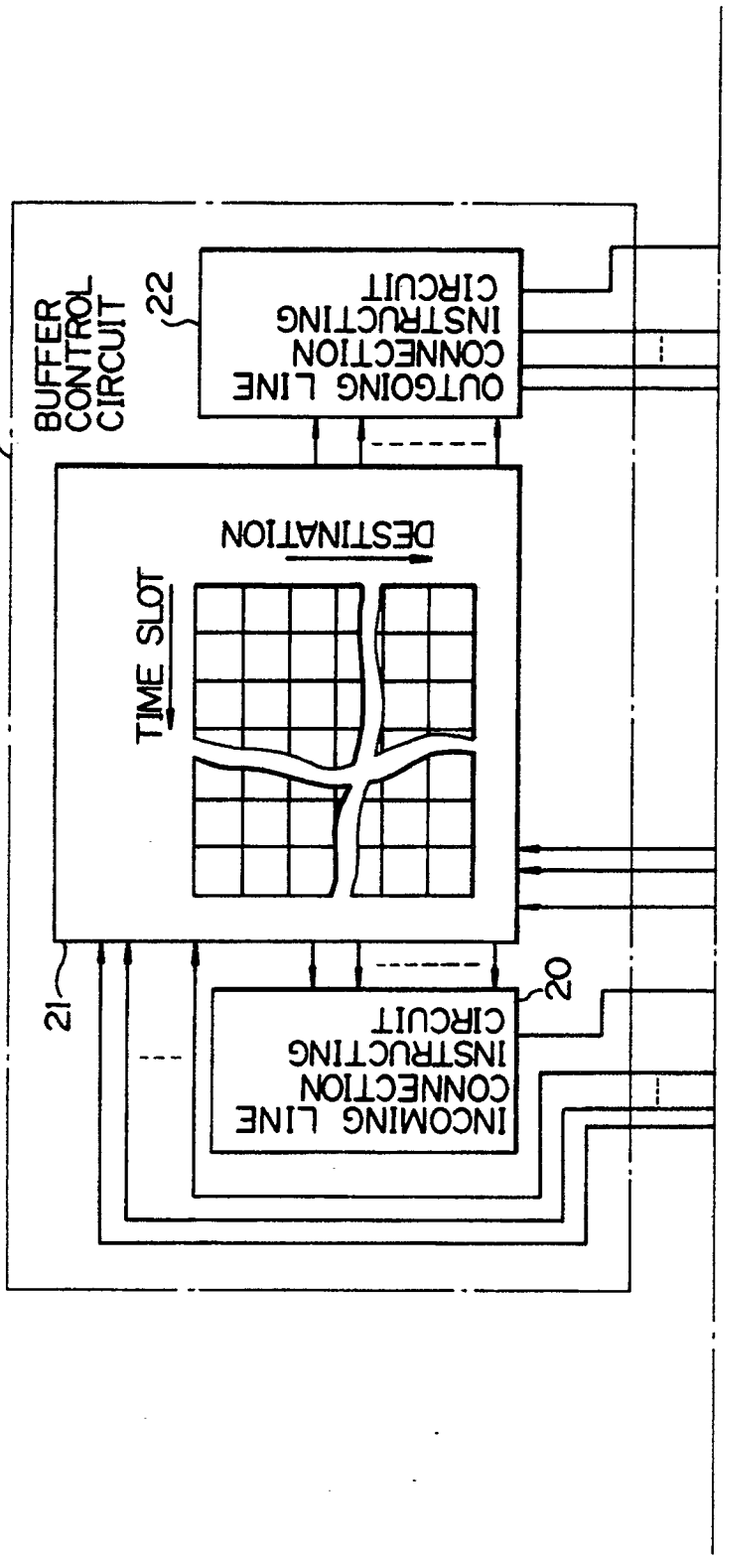


Fig.5A

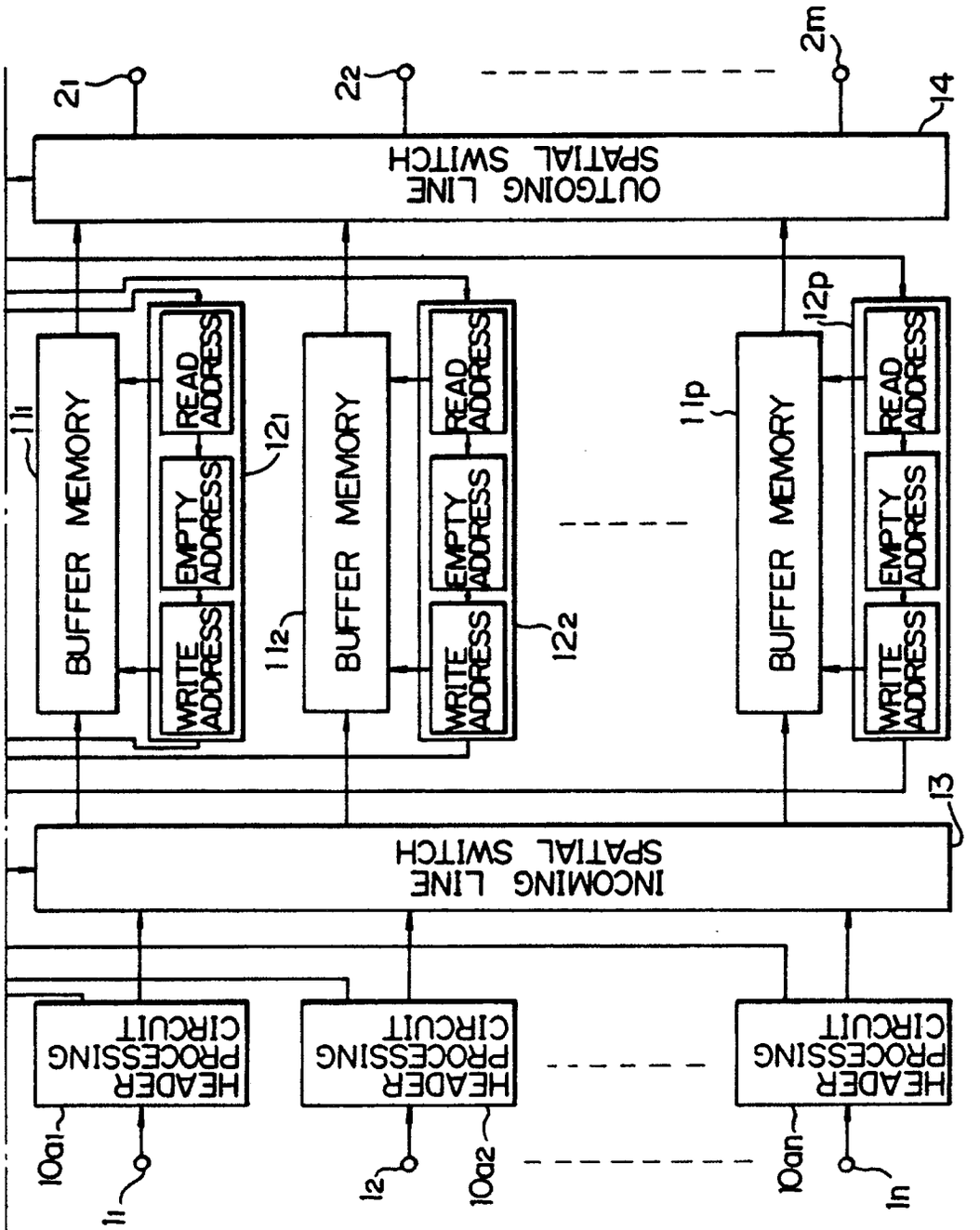

21
22
2m
14
OUTGOING LINE SPATIAL SWITCH
12p
11i
BUFFER MEMORY
READ ADDRESS
EMPTY ADDRESS
WRITE ADDRESS
121
112
11p
122
13
INCOMING LINE SPATIAL SWITCH
HEADER PROCESSING CIRCUIT
10a1
10a2
10an
1i
12
1n

Fig.5B

Fig.6

Fig.6A	Fig.6B
Fig.6C	Fig.6D

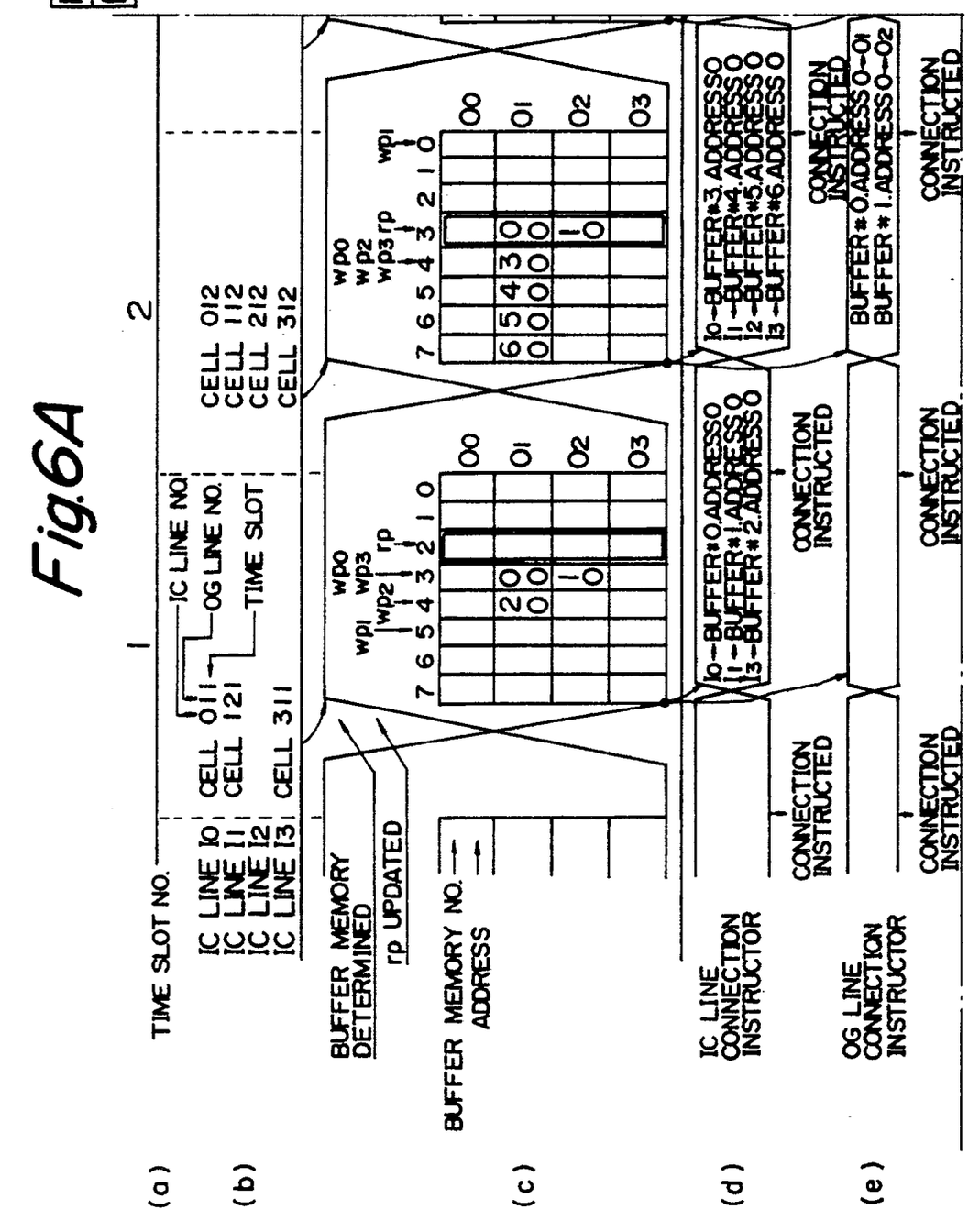


Fig.6B

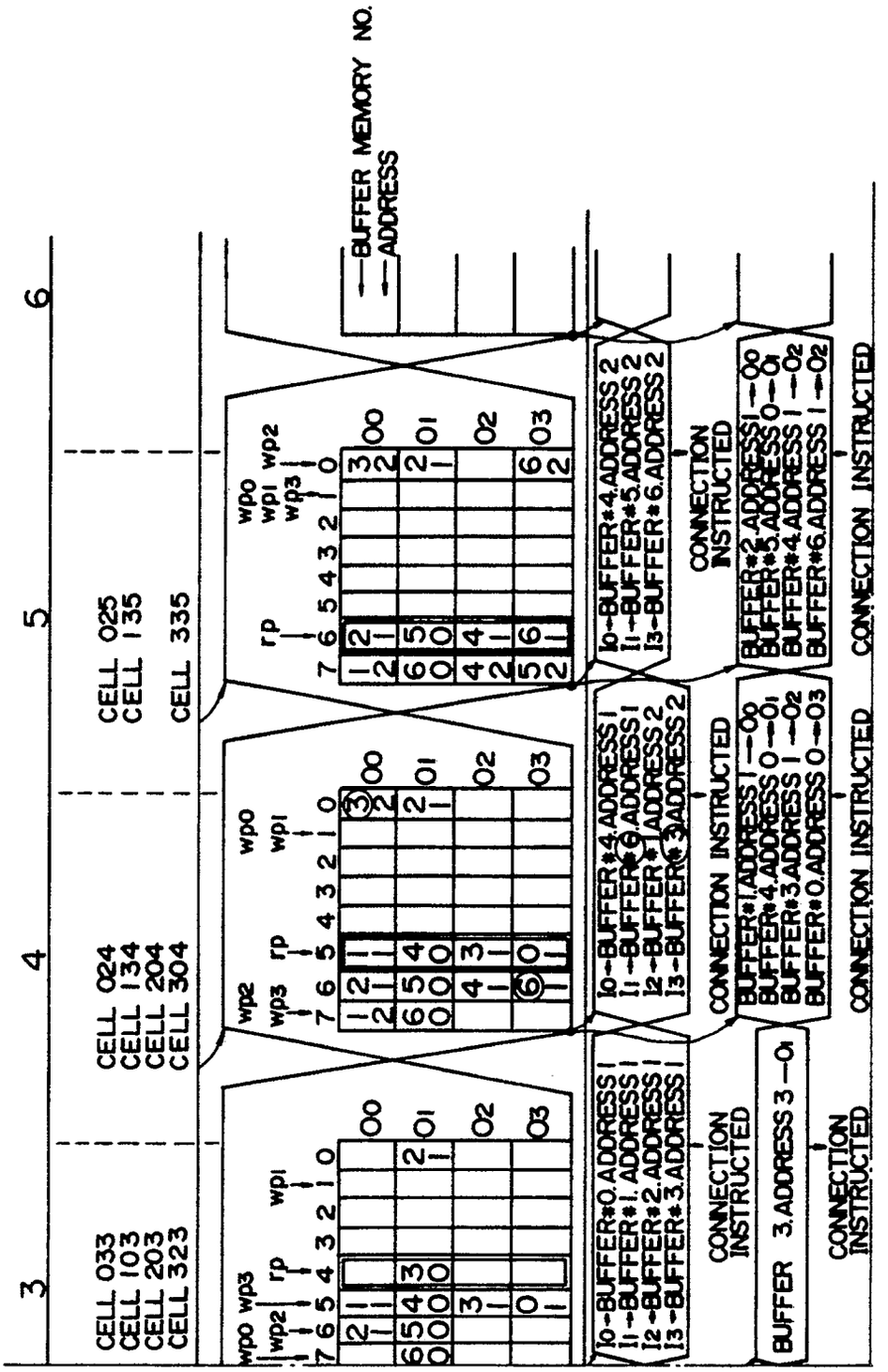

3
4
5
6
CELL 033
CELL 103
CELL 203
CELL 323
CELL 024
CELL 134
CELL 204
CELL 304
CELL 025
CELL 135
CELL 335
BUFFER MEMORY NO.
ADDRESS
wp0 wp3 wp2 rp wp1
wp2 wp3 rp wp0 wp1
rp wp0 wp1 wp2 wp3
BUFFER 3.ADDRESS 3 → O1
CONNECTION INSTRUCTED
I0→BUFFER#0.ADDRESS 1
I1→BUFFER#1.ADDRESS 1
I2→BUFFER#2.ADDRESS 1
I3→BUFFER#3.ADDRESS 1
I0→BUFFER#4.ADDRESS 1
I1→BUFFER#5.ADDRESS 1
I2→BUFFER#1.ADDRESS 2
I3→BUFFER#3.ADDRESS 2
I0→BUFFER#4.ADDRESS 2
I1→BUFFER#5.ADDRESS 2
I3→BUFFER#6.ADDRESS 2
BUFFER#1.ADDRESS 1 → O0
BUFFER#4.ADDRESS 0 → O1
BUFFER#3.ADDRESS 1 → O2
BUFFER#0.ADDRESS 0 → O3
BUFFER#2.ADDRESS 1 → O0
BUFFER#5.ADDRESS 0 → O1
BUFFER#4.ADDRESS 1 → O2
BUFFER#6.ADDRESS 1 → O2

Fig6C

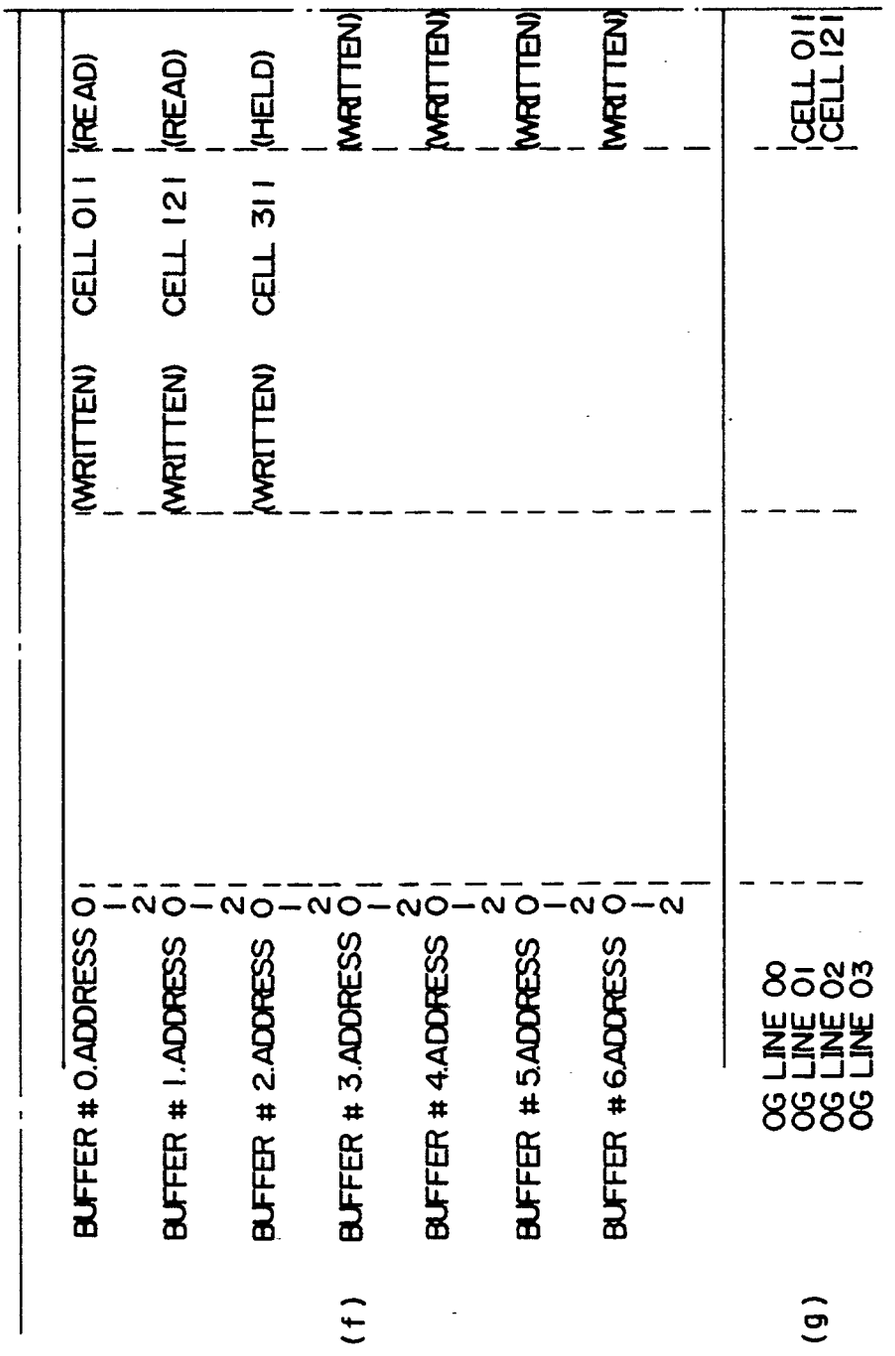

BUFFER # 0.ADDRESS 0
2
BUFFER # 1.ADDRESS 0
2
BUFFER # 2.ADDRESS 0
2
BUFFER # 3.ADDRESS 0
2
BUFFER # 4.ADDRESS 0
2
BUFFER # 5.ADDRESS 0
2
BUFFER # 6.ADDRESS 0
2
(WRITTEN)
CELL 011
(READ)
(WRITTEN)
CELL 121
(READ)
(WRITTEN)
CELL 311
(HELD)
(WRITTEN)
(WRITTEN)
(WRITTEN)
(WRITTEN)
(f)
OG LINE 00
OG LINE 01
OG LINE 02
OG LINE 03
CELL 011
CELL 121
(g)

Fig.6D

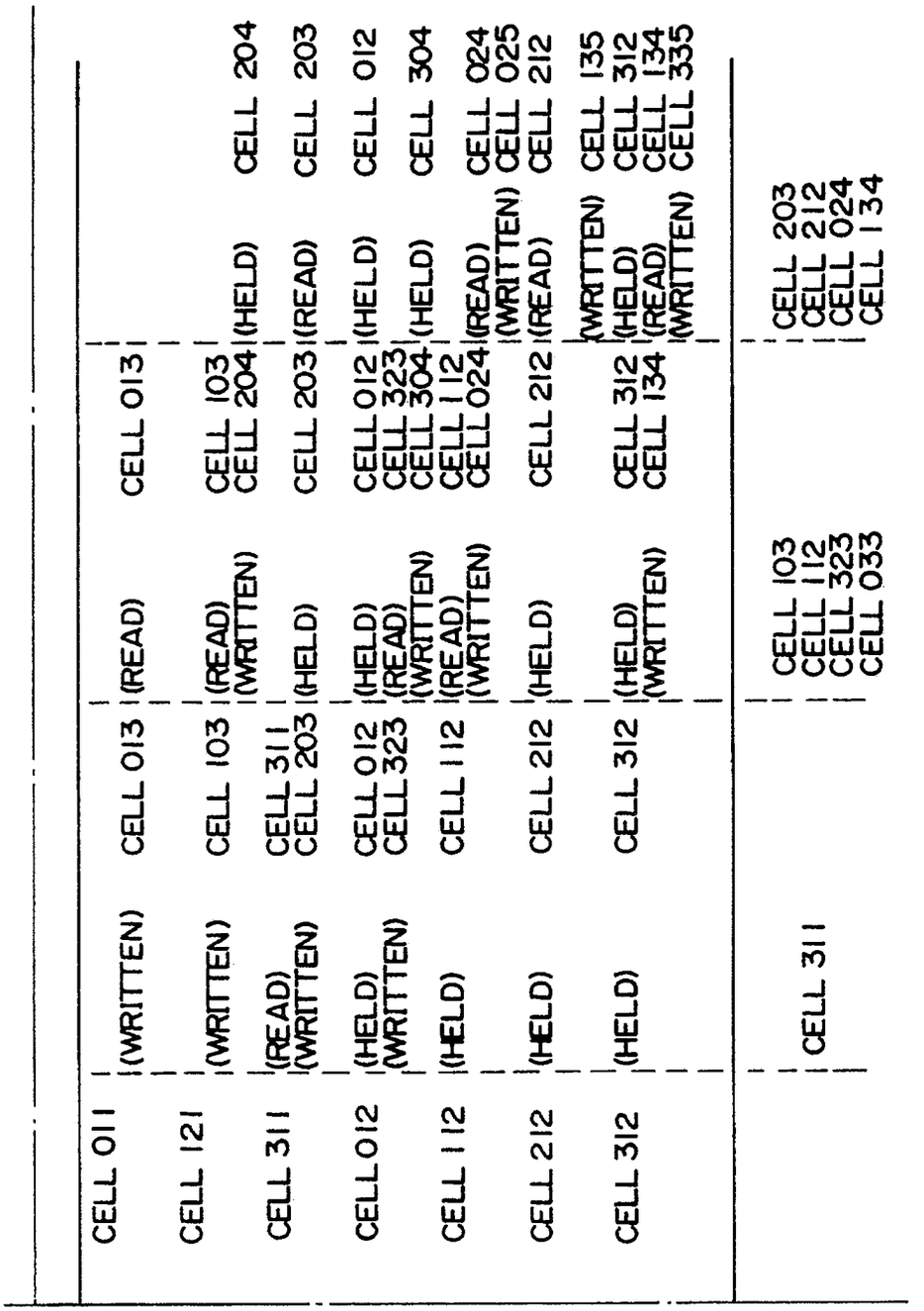
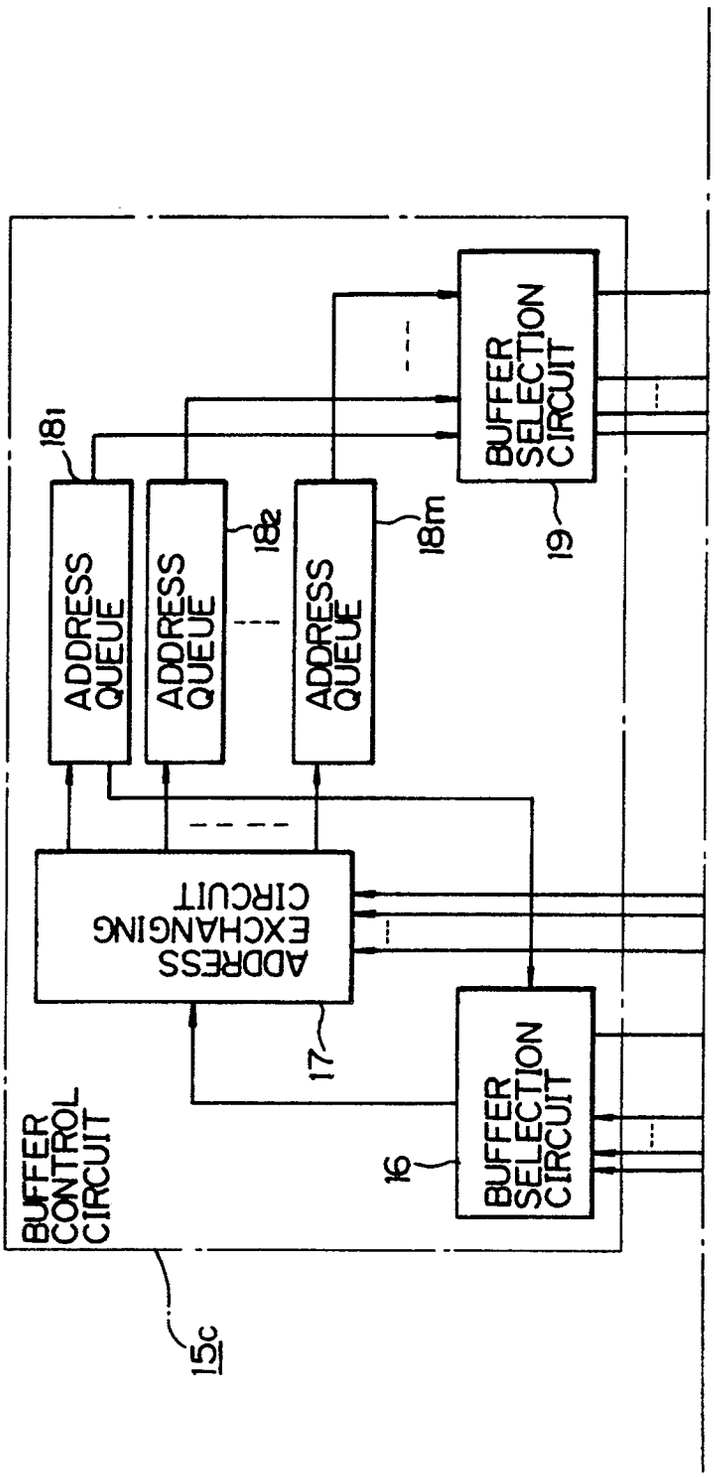

CELL 011
CELL 121
CELL 311
CELL 012
CELL 112
CELL 212
CELL 312
(WRITTEN)
(WRITTEN)
(READ)
(WRITTEN)
(HELD)
(HELD)
(WRITTEN)
(HELD)
(HELD)
(HELD)
CELL 311
CELL 013
CELL 103
CELL 203
CELL 012
CELL 323
CELL 112
CELL 212
CELL 312
(READ)
(READ)
(WRITTEN)
(HELD)
(HELD)
(READ)
(WRITTEN)
(HELD)
(HELD)
(WRITTEN)
CELL 103
CELL 112
CELL 323
CELL 033
CELL 013
CELL 103
CELL 204
CELL 203
CELL 012
CELL 323
CELL 304
CELL 112
CELL 024
CELL 212
CELL 312
CELL 134
(READ)
(HELD)
(READ)
(HELD)
(HELD)
(READ)
(WRITTEN)
(READ)
(HELD)
(READ)
(WRITTEN)
CELL 204
CELL 203
CELL 012
CELL 304
CELL 024
CELL 025
CELL 212
CELL 135
CELL 312
CELL 134
CELL 335
CELL 203
CELL 212
CELL 024
CELL 134

Fig.7

Fig.7A
Fig.7B

Fig.7A



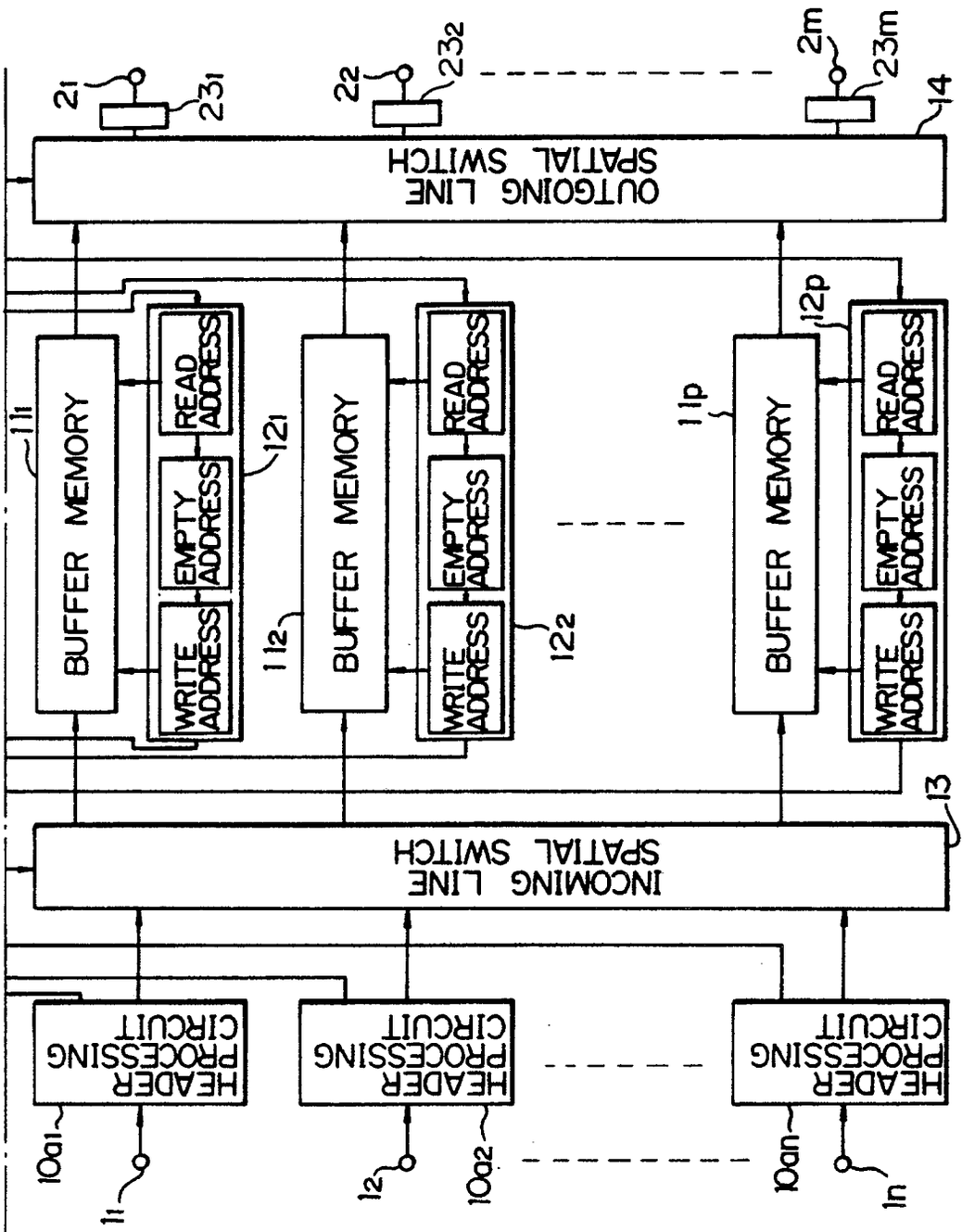

OUTGOING LINE SPATIAL SWITCH
INCOMING LINE SPATIAL SWITCH
BUFFER MEMORY
READ ADDRESS
EMPTY ADDRESS
WRITE ADDRESS
HEADER PROCESSING CIRCUIT
21
22
23₂
2m
23m
14
13
111
112
11p
121
122
12p
10a1
10a2
10an
11
12
1n

Fig.7B

Fig. 8A

Fig. 8

Fig. 8A	Fig. 8B

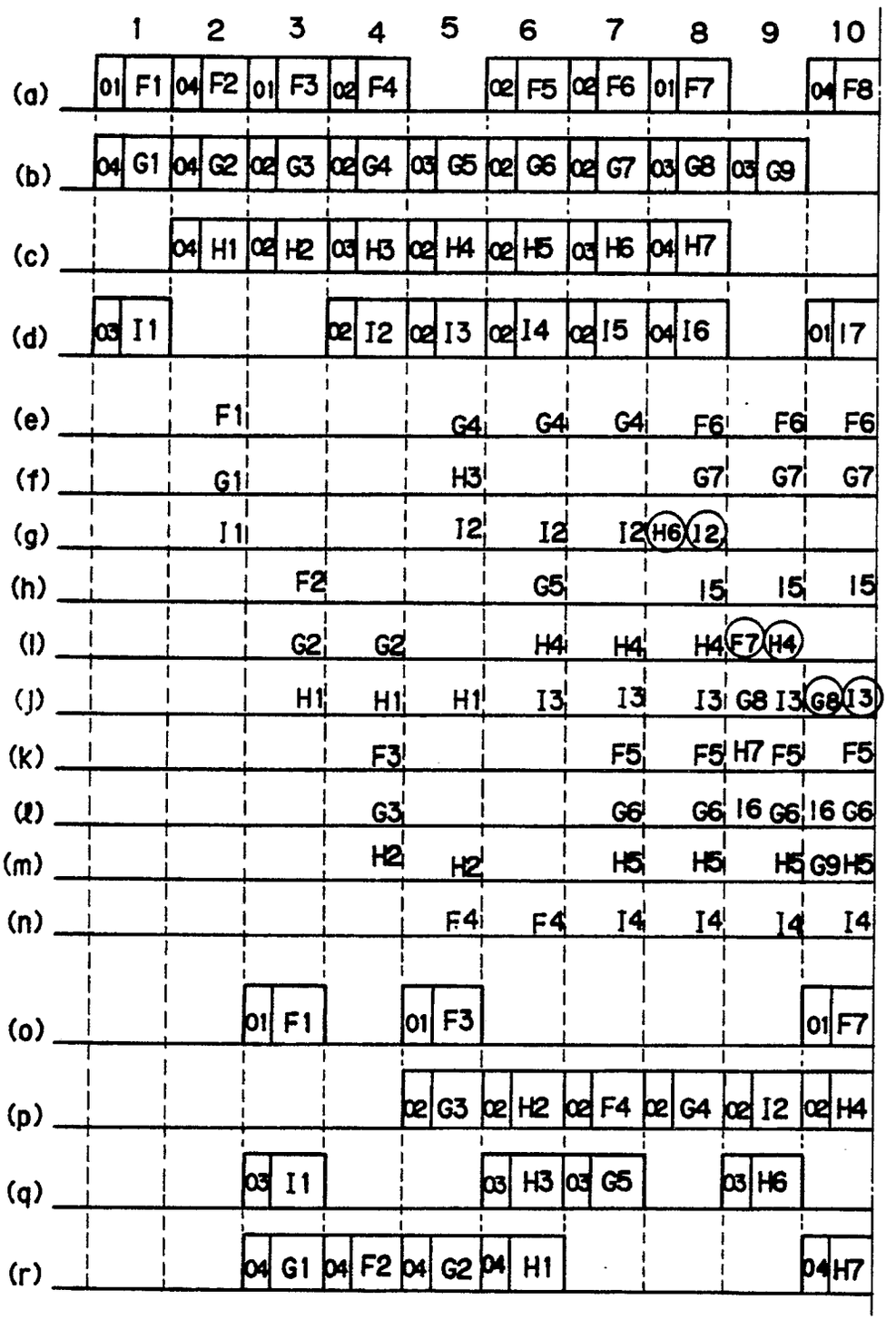


Fig.8B

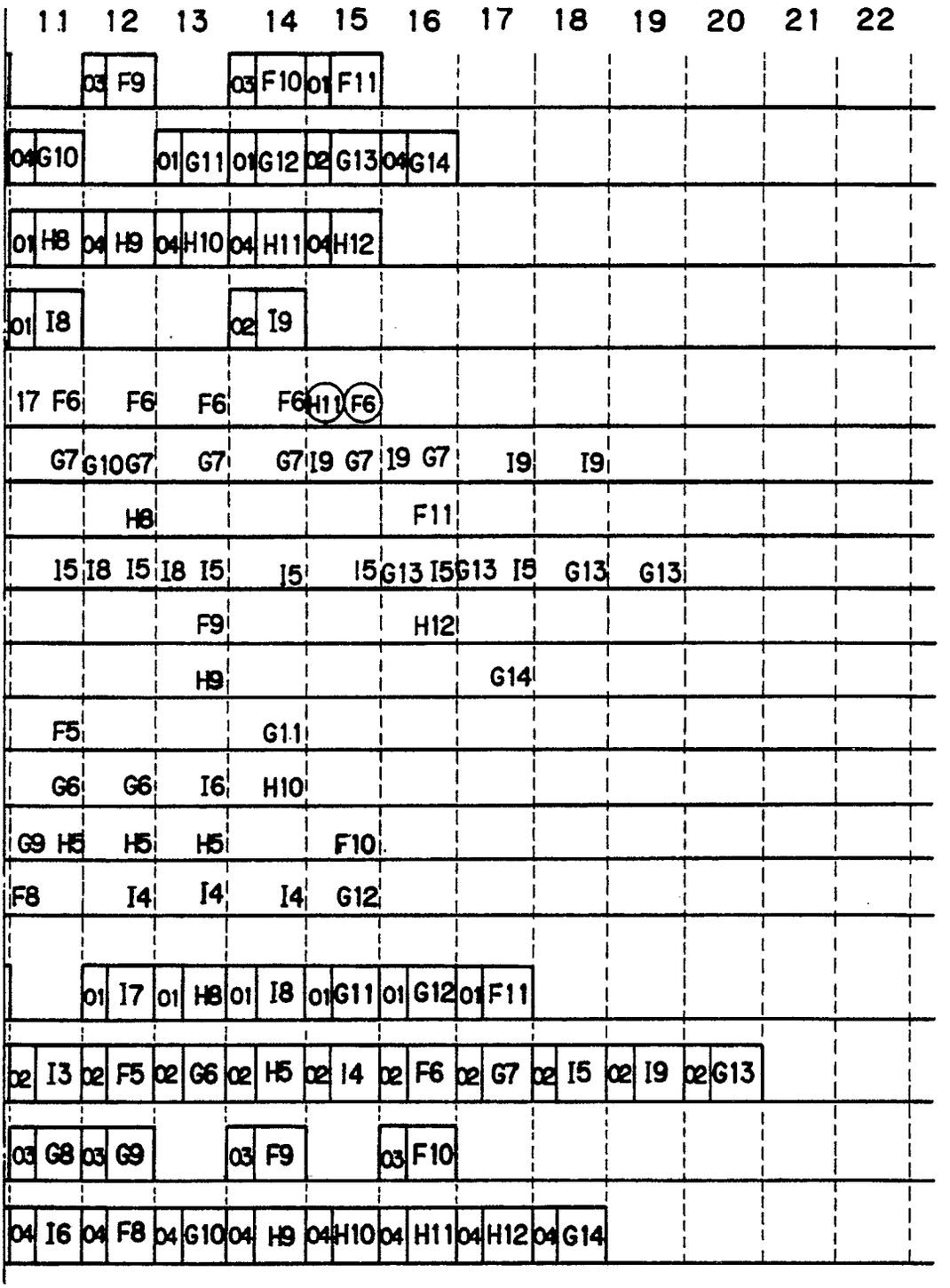

11 12 13 14 15 16 17 18 19 20 21 22
03 F9 03 F10 01 F11
04 G10 01 G11 01 G12 02 G13 04 G14
01 H8 04 H9 04 H10 04 H11 04 H12
01 I8 02 I9
17 F6 F6 F6 F6 H11 F6
G7 G10 G7 G7 G7 I9 G7 I9 G7 I9 I9
H8 F11
I5 I8 I5 I8 I5 I5 I5 G13 I5 G13 I5 G13 G13
F9 H12
H9 G14
F5 G11
G6 G6 I6 H10
G9 H5 H5 H5 F10
F8 I4 I4 I4 G12
01 I7 01 H8 01 I8 01 G11 01 G12 01 F11
02 I3 02 F5 02 G6 02 H5 02 I4 02 F6 02 G7 02 I5 02 I9 02 G13
03 G8 03 G9 03 F9 03 F10
04 I6 04 F8 04 G10 04 H9 04 H10 04 H11 04 H12 04 G14

Fig.9A

Fig.9

Fig.9A
Fig.9B

CELLS HELD IN BUFFER MEMORIES

TIME SLOT	6	7	8	9	10	11	12	13
(e)	G4	G4	F6	F6	F6	I7 F6	F6	F6
(f)			G7	G7	G7	G7	G10 G7	G7
(g)	I2	I2	H6 I2				H8	
(h)	G5		I5	I5	I5	I5	I8 I5	I8 I5
(i)	H4	H4	H4	F7 H4				F9
(j)	I3	I3	I3	G8 I3	G8 I3			H9
(k)		F5	F5	H7 F5	F5	F5		
(ℓ)		G6	G6	I6 G6	I6 G6	G6	G6	I6
(m)		H5	H5	H5	G9 H5	G9 H5	H5	H5

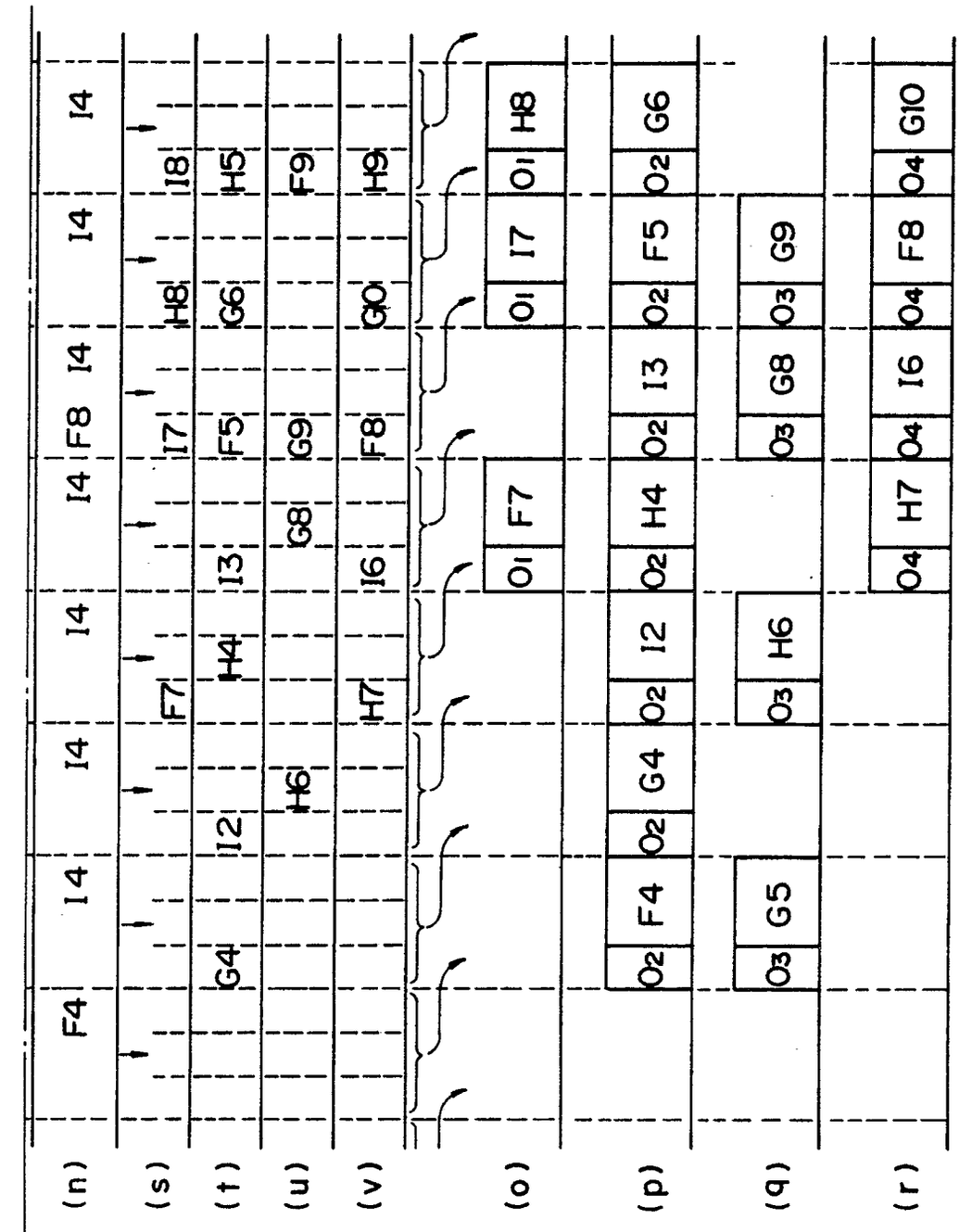
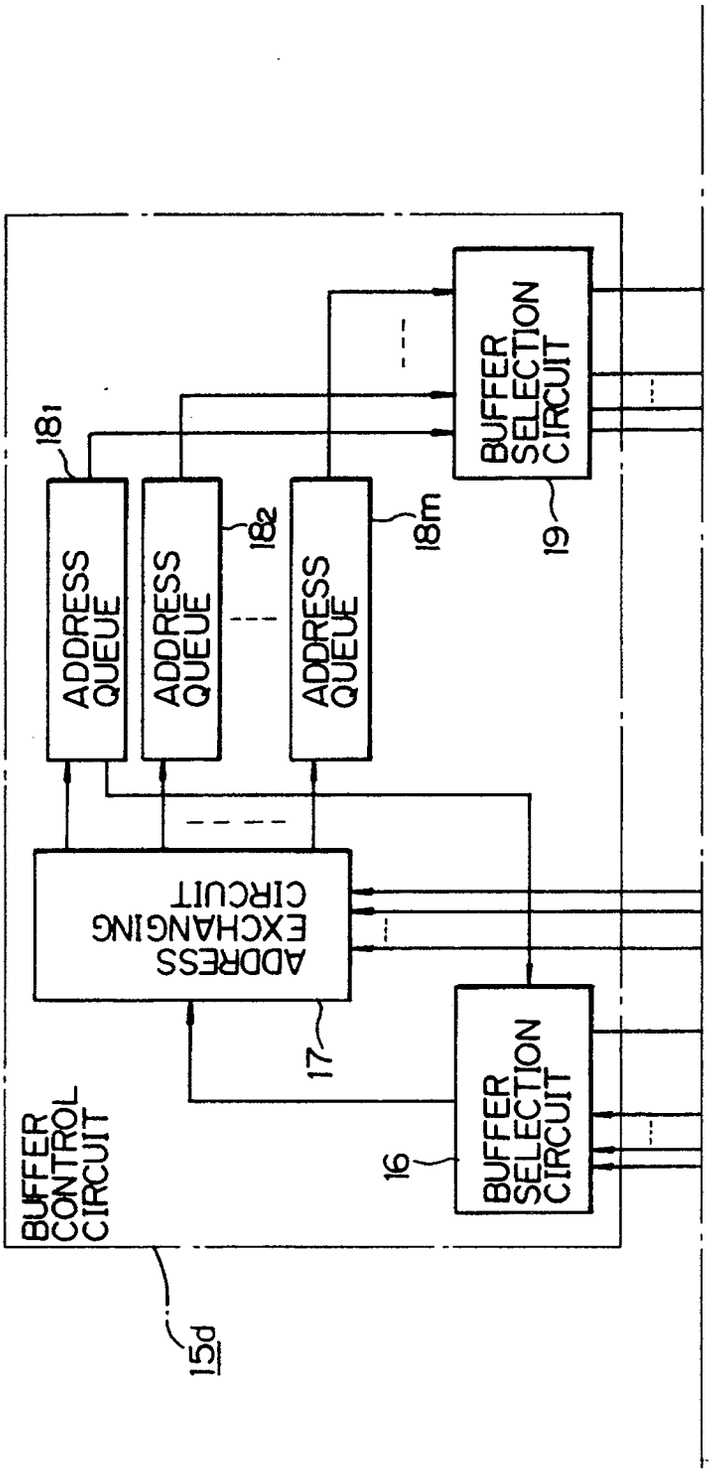

(n)
(s)
(t)
(u)
(v)
(o)
(p)
(q)
(r)
CELLS WRITTEN IN OG SPEED ADJUST BUFFERS
OUTGOING CELLS

Fig.9B

Fig.10

Fig.10A
Fig.10B

Fig.10A



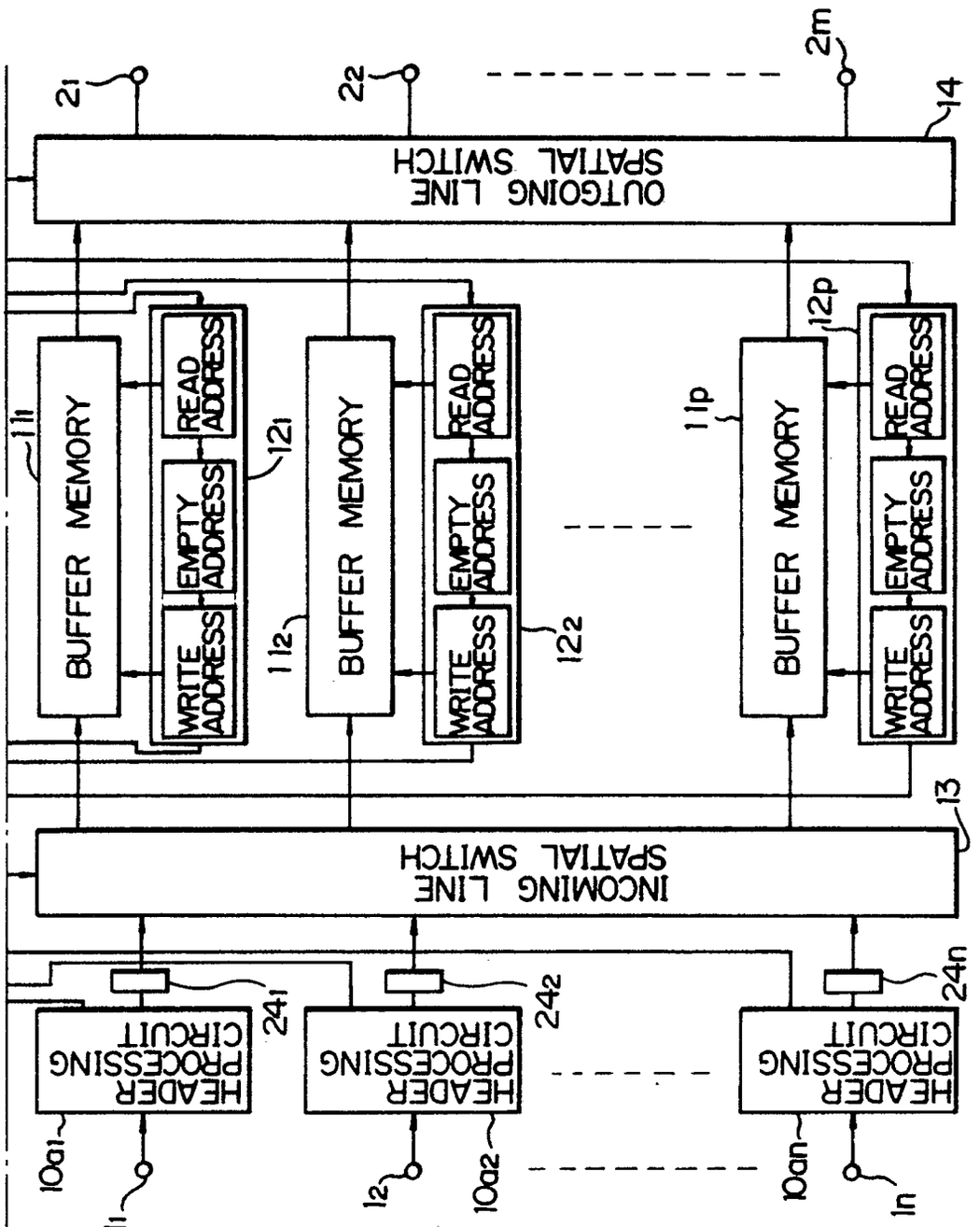

OUTGOING LINE SPATIAL SWITCH
INCOMING LINE SPATIAL SWITCH
BUFFER MEMORY
READ ADDRESS
EMPTY ADDRESS
WRITE ADDRESS
HEADER PROCESSING CIRCUIT
2m
2₂
2₁
14
12p
12₂
12₁
11p
11₂
11₁
13
24n
24₂
24₁
10aₙ
10a₂
10a₁
1ₙ
1₂
1₁

Fig.10B

Fig.11A

Fig.11

Fig.11A | Fig.11B

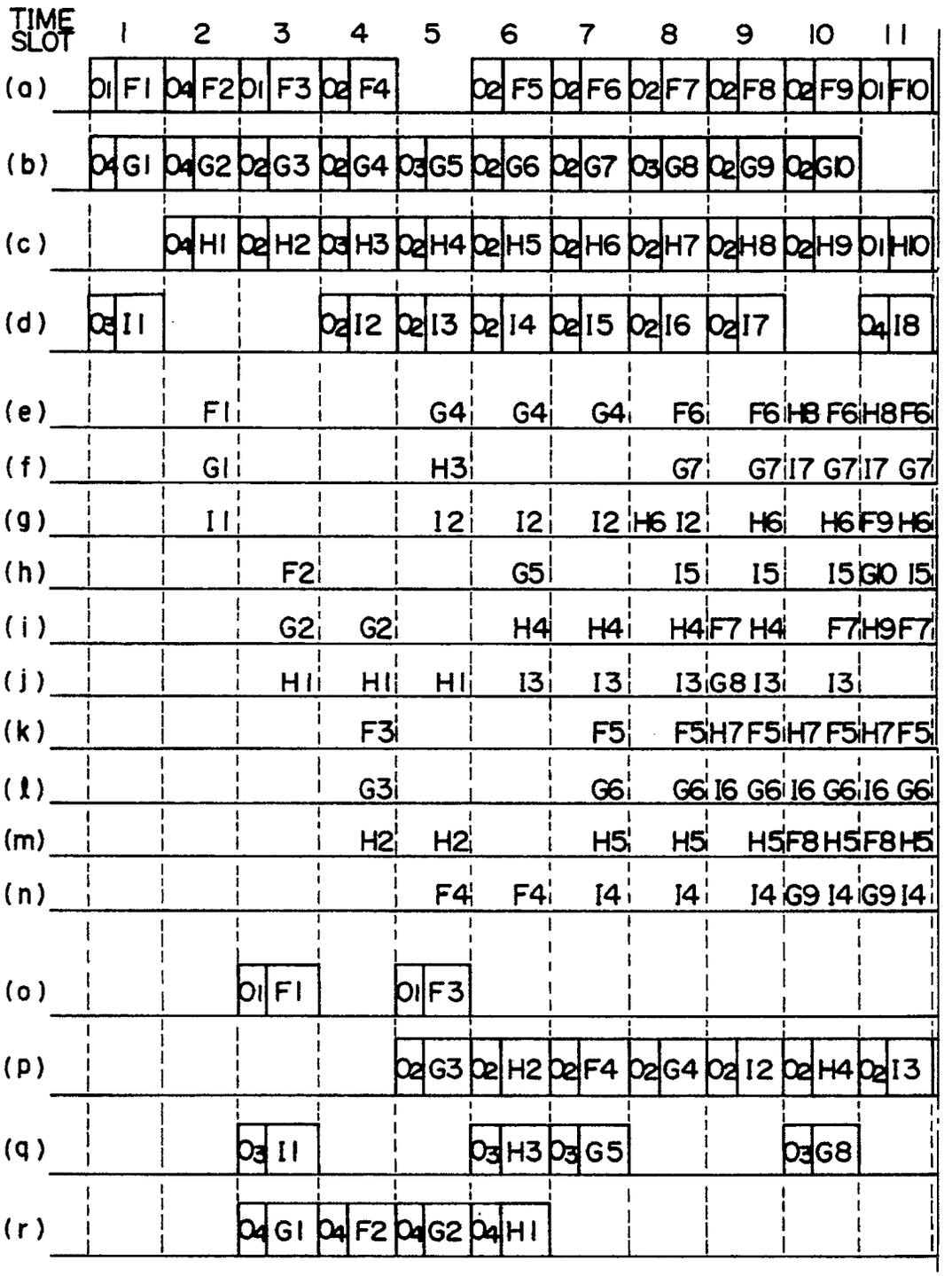
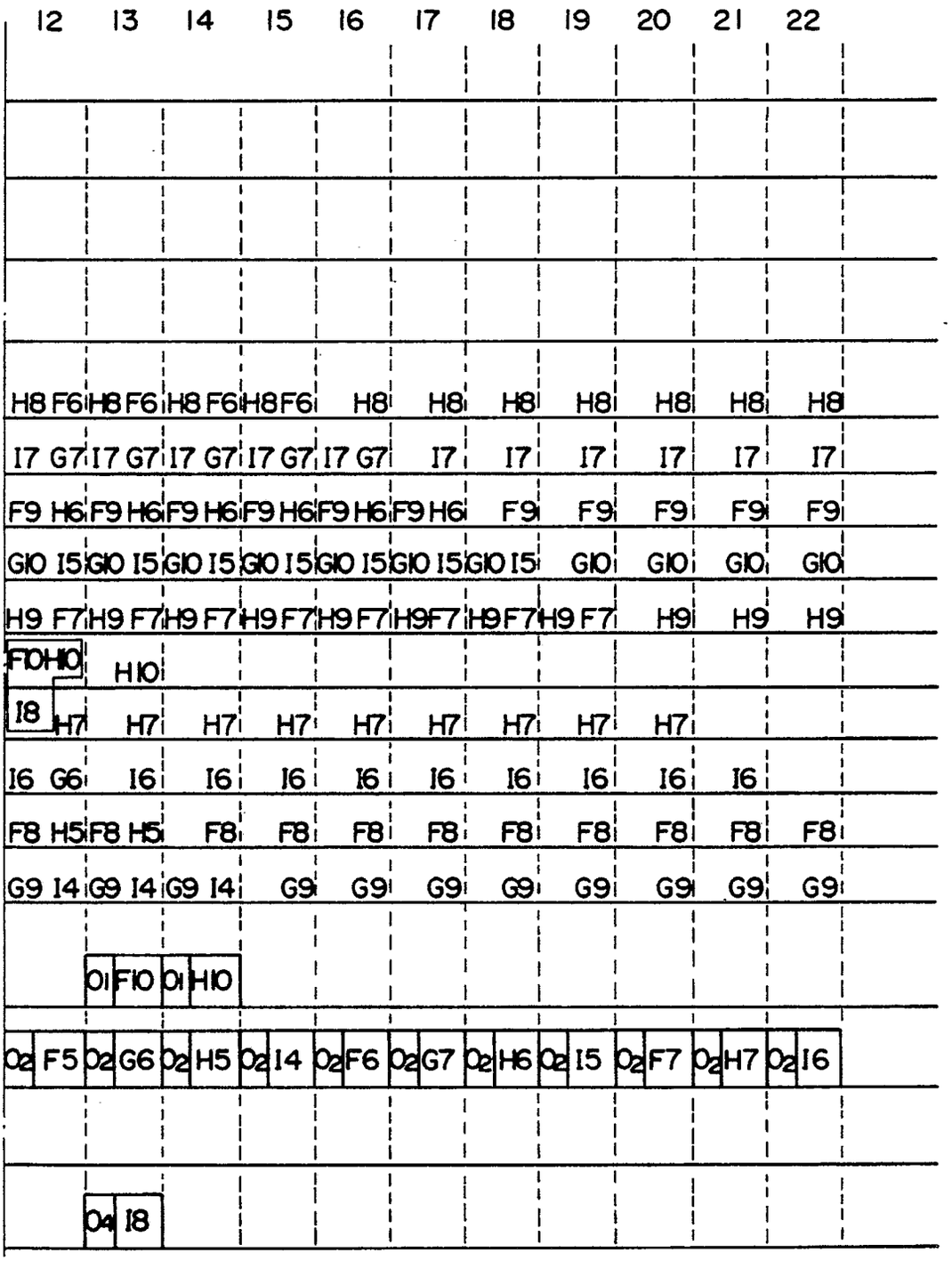


Fig.11B


12 13 14 15 16 17 18 19 20 21 22
H8 F6 H8 F6 H8 F6 H8 F6 H8 H8 H8 H8 H8 H8 H8
I7 G7 I7 G7 I7 G7 I7 G7 I7 G7 I7 I7 I7 I7 I7 I7
F9 H6 F9 H6 F9 H6 F9 H6 F9 H6 F9 H6 F9 F9 F9 F9 F9
G10 I5 G10 I5 G10 I5 G10 I5 G10 I5 G10 I5 G10 I5 G10 G10 G10 G10
H9 F7 H9 F7 H9 F7 H9 F7 H9 F7 H9 F7 H9 F7 H9 F7 H9 H9 H9
F10 H10 H10
I8 H7 H7 H7 H7 H7 H7 H7 H7 H7
I6 G6 I6 I6 I6 I6 I6 I6 I6 I6 I6
F8 H5 F8 H5 F8 F8 F8 F8 F8 F8 F8 F8 F8
G9 I4 G9 I4 G9 I4 G9 G9 G9 G9 G9 G9 G9 G9
O1 F10 O1 H10
O2 F5 O2 G6 O2 H5 O2 I4 O2 F6 O2 G7 O2 H6 O2 I5 O2 F7 O2 H7 O2 I6
O4 I8