



- (51) International Patent Classification:
H02M 3/335 (2006.01)
- (21) International Application Number:
PCT/US2013/039069
- (22) International Filing Date:
1 May 2013 (01.05.2013)
- (25) Filing Language: English
- (26) Publication Language: English
- (30) Priority Data:
13/462,388 2 May 2012 (02.05.2012) US
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- (81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY,

BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

- (84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

- with international search report (Art. 21(3))
- before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments (Rule 48.2(h))

(54) Title: DRIVER CIRCUITS FOR DIMMABLE SOLID STATE LIGHTING APPARATUS

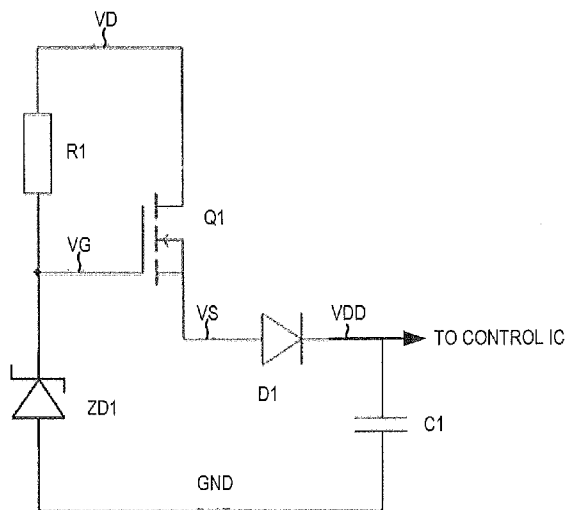


FIGURE 1

(57) Abstract: A voltage regulator for generating a house-keeping voltage in a high voltage power supply circuit includes a charging switch coupled to a high voltage node and to a storage device at an output node, and a control voltage regulation circuit coupled to the charging switch and configured to cause the charging switch to generate a current pulse for charging the storage device.

WO 2013/166152 A1

DRIVER CIRCUITS FOR DIMMABLE SOLID STATE LIGHTING APPARATUS

FIELD

[0001] The present inventive concept relates to driver circuits for solid state lighting apparatus.

BACKGROUND

[0002] Solid-state lighting arrays are used for a number of lighting applications. For example, solid-state lighting panels including arrays of solid-state light emitting devices have been used as direct illumination sources, for example, in architectural and/or accent lighting. A solid-state light emitting device may include, for example, a packaged light emitting device including one or more light emitting diodes (LEDs), which may include inorganic LEDs, which may include semiconductor layers forming p-n junctions and/or organic LEDs (OLEDs), which may include organic light emission layers. Typically, a solid-state light emitting device generates light through the recombination of electronic carriers, i.e. electrons and holes, in a light emitting layer or region. A solid-state light emitting device may include, for example, a packaged light emitting device including one or more light emitting diodes (LEDs).

[0003] Cree, Inc. produces a variety of recessed downlights, such as the LR-6 and CR-6, which use LEDs for illumination. Solid-state lighting panels are also commonly used as backlights for small liquid crystal display (LCD) screens, such as LCD display screens used in portable electronic devices, and for larger displays, such as LCD television displays.

[0004] Solid state lighting devices are typically powered with a DC signal. However, power is conventionally delivered in AC form. It is therefore generally desirable for a solid state light fixture to include an AC/DC converter to convert AC line voltage to a DC voltage.

[0005] Boost converters can be used to generate DC voltage from an AC line voltage with high power factor and low total harmonic distortion. The voltage of an LED-based load may be higher than the peak of the input (line) AC voltage. In that case, a single-stage boost converter can be employed as the driver, achieving high power efficiency and low cost. For example, a power factor corrected (PFC) boost converter which converts 120V ac, 60 Hz, to 200-250V dc output could be used to drive an array of high-voltage (HV) LEDs at a power level of 10-15W.

[0006] For general lighting applications, it is desirable for a solid state lighting apparatus to be compatible with a phase-cut dimming signal. Phase-cut dimmers are commonly used to reduce input power to conventional incandescent lighting fixtures, which causes the fixtures to dim. Phase-cut dimmers only pass a portion of the input voltage waveform in each cycle. Thus, during a portion of a phase-cut AC input signal, no voltage is provided to the fixture.

[0007] Compatibility with phase cut dimming signals is also feasible for LED drivers based on boost converters. One low cost approach is to use open-loop control, which means a driver will not respond to the LED current decrease due to phase cut dimming, but rather keep the preset input current during dimmer conduction time. In this way, a 'natural' dimming performance is achieved, and input power, and thus LED current will reduce as the dimmer conduction time decreases. One other approach is for drivers to use closed-loop control. As control loops are complete and in effect, these drivers will try to compensate the input power decrease due to dimmer phase cut. In order to dim LEDs in these cases, the control loops should be saturated so that the input current cannot increase. The control loop saturation can be realized by clamping the output of an error amplifier, for example.

[0008] Another challenge due to phase cut dimming is for the boost converter to generate the bias voltage that is used to power the control circuits of the boost converter (so-called "housekeeping power") during deep dimming. Conventional LED driver circuits draw housekeeping power from the auxiliary winding of a boost circuit inductor. Depending on how much of the input waveform is cut by the dimmer, during the dimmer off period, the control circuits can lose power. This can cause the entire driver circuit to cut off, which can result in visible flicker of the solid state lighting apparatus or other issues.

SUMMARY

[0009] A voltage regulator according to some embodiments includes a charging switch including a first terminal coupled to a high voltage node, a second terminal, and a control terminal, a rectifier coupled to the second terminal of the charging switch, an output capacitor coupled to the rectifier, a control switch coupled to the second terminal, and a control voltage regulation circuit coupled to the control terminal of the charging switch. The control switch and the charging switch are configured so that when the control switch is turned off, a rise in voltage on the control switch causes an increase in voltage on the

control terminal of the charging switch sufficient to allow a charging current to flow through the rectifier and into the output capacitor. The control voltage regulation circuit is configured to dissipate the increased voltage on the control switch so that the charging current only flows for a limited period of time in response to the control switch being turned off.

[0010] The control voltage regulation circuit may include a clamping diode coupled to the control terminal of the charging switch.

[0011] The voltage regulator may further include a resistor in parallel with the clamping diode and configured to allow a voltage clamped by the clamping diode to dissipate. A resistance of the resistor is selected to provide a desired pulse width of the charging current.

[0012] The control switch has a parasitic capacitance that is charged when the control switch is turned off thereby causing the rise in voltage on the control switch.

[0013] In some embodiments, the control voltage regulation circuit may include a Zener diode coupled to a voltage node, a first resistor coupled between the voltage node and a voltage source, a clamping diode coupled to the control terminal of the charging switch, a second resistor coupled in parallel with the clamping diode, a third resistor coupled between the clamping diode and the voltage node, and a capacitor coupled to the voltage node. The second and third resistors and the capacitor may be configured to dissipate the increased voltage on the control terminal of the charging switch. The charging switch is configured to turn off in response to dissipation of the increased voltage on the control terminal of the charging switch.

[0014] In some embodiments, the voltage regulator may further include a main inductor, a zero crossing detection (ZCD) circuit configured to generate a zero cross detection signal in response to current through the main inductor falling to zero, and a control circuit configured to selectively activate the control switch in response to the zero cross detection signal. The zero crossing detection signal is configured to generate the zero cross detection signal to have a sufficient voltage swing to trigger a zero cross detection by the control circuit.

[0015] In some embodiments, the zero crossing detection circuit may include a capacitor coupled to the high voltage node and to a first node, a first resistor coupled to the capacitor and to a ZCD output node, a second resistor coupled to the ZCD output node, a

first diode including an anode coupled to the first node and including a cathode, a second resistor coupled to the cathode of the diode, and a second diode including a cathode coupled to the second resistor.

[0016] In other embodiments, the zero crossing detection circuit may include a first resistor coupled to the high voltage node, a first Zener diode having a cathode coupled to the first resistor and having an anode coupled to a ZCD output node, a second Zener diode having a cathode coupled to the ZCD output node, a second resistor coupled to the ZCD output node, and a capacitor coupled to the ZCD output node.

[0017] Some embodiments provide a voltage regulator for generating a housekeeping voltage in a power supply circuit. The voltage regulator includes a charging switch coupled to a high voltage node and to an output capacitor, and a control voltage regulation circuit coupled to a control terminal of the charging switch. The control switch and the charging switch are configured so that when the control switch is turned off, a rise in voltage on the control switch causes an increase in voltage on the control terminal of the charging switch sufficient to allow a charging current to flow into the output capacitor. The control voltage regulation circuit is configured to dissipate the increased voltage on the control switch so that the charging current only flows for a limited period of time in response to a state transition of the control switch.

[0018] A voltage regulator for generating a housekeeping voltage in a power supply circuit according to further embodiments includes a charging switch coupled to a high voltage node and to an output capacitor, and a control voltage regulation circuit coupled to the charging switch and configured to cause the charging switch to generate a current pulse for charging the output capacitor in response to a control signal.

[0019] In accordance with further embodiments of the invention, a method of generating a low voltage in a high voltage power supply includes generating a high voltage at a voltage node, and in response to a change in a voltage level at the voltage node, generating a pulse of current for charging an output capacitor to a level that is lower than the high voltage.

BRIEF DESCRIPTION OF THE DRAWINGS

[0020] The accompanying drawings, which are included to provide a further understanding of the inventive subject matter and are incorporated in and constitute a part

of this application, illustrate certain embodiment(s) of the inventive subject matter. In the drawings:

[0021] Figure 1 is a circuit diagram of a linear voltage regulator that can be used to generate a control circuit voltage.

[0022] Figure 2 is a circuit diagram of a voltage regulator circuit according to embodiments of the inventive concepts that can be used to generate a control circuit voltage.

[0023] Figure 3 is a graph of waveforms associated with the voltage regulator circuit shown in Figure 2.

[0024] Figure 4 is a block diagram of a zero cross detection circuit.

[0025] Figures 5-7 are circuit diagrams of zero cross detection circuits according to embodiments of the inventive concepts.

DETAILED DESCRIPTION OF EMBODIMENTS

[0026] Embodiments of the present inventive subject matter now will be described more fully hereinafter with reference to the accompanying drawings, in which embodiments of the inventive subject matter are shown. This inventive subject matter may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the inventive subject matter to those skilled in the art. Like numbers refer to like elements throughout.

[0027] It will be understood that, although the terms first, second, etc. may be used herein to describe various elements, these elements should not be limited by these terms. These terms are only used to distinguish one element from another. For example, a first element could be termed a second element, and, similarly, a second element could be termed a first element, without departing from the scope of the present inventive subject matter. As used herein, the term "and/or" includes any and all combinations of one or more of the associated listed items.

[0028] It will be understood that when an element is referred to as being "connected" or "coupled" to another element, it can be directly connected or coupled to the other element or intervening elements may be present. In contrast, when an element is

referred to as being "directly connected" or "directly coupled" to another element, there are no intervening elements present.

[0029] It will be understood that when an element or layer is referred to as being "on" another element or layer, the element or layer can be directly on another element or layer or intervening elements or layers may also be present. In contrast, when an element is referred to as being "directly on" another element or layer, there are no intervening elements or layers present. Throughout the specification, like reference numerals in the drawings denote like elements.

[0030] The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting of the present inventive subject matter. As used herein, the singular forms "a", "an" and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms "comprises" "comprising," "includes" and/or "including" when used herein, specify the presence of stated features, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components, and/or groups thereof.

[0031] Unless otherwise defined, all terms (including technical and scientific terms) used herein have the same meaning as commonly understood by one of ordinary skill in the art to which this present inventive subject matter belongs. It will be further understood that terms used herein should be interpreted as having a meaning that is consistent with their meaning in the context of this specification and the relevant art and will not be interpreted in an idealized or overly formal sense unless expressly so defined herein. The term "plurality" is used herein to refer to two or more of the referenced item.

[0032] The expression "lighting apparatus", as used herein, is not limited, except that it indicates that the device is capable of emitting light. That is, a lighting apparatus can be a device which illuminates an area or volume, e.g., a structure, a swimming pool or spa, a room, a warehouse, an indicator, a road, a parking lot, a vehicle, signage, e.g., road signs, a billboard, a ship, a toy, a mirror, a vessel, an electronic device, a boat, an aircraft, a stadium, a computer, a remote audio device, a remote video device, a cell phone, a tree, a window, an LCD display, a cave, a tunnel, a yard, a lamppost, or a device or array of devices that illuminate an enclosure, or a device that is used for edge or back-lighting (e.g., back light poster, signage, LCD displays), bulb replacements (e.g., for replacing AC incandescent lights,

low voltage lights, fluorescent lights, etc.), lights used for outdoor lighting, lights used for security lighting, lights used for exterior residential lighting (wall mounts, post/column mounts), ceiling fixtures/wall sconces, under cabinet lighting, lamps (floor and/or table and/or desk), landscape lighting, track lighting, task lighting, specialty lighting, ceiling fan lighting, archival/art display lighting, high vibration/impact lighting, work lights, etc., mirrors/vanity lighting, or any other light emitting device.

[0033] Some embodiments of the invention provide electronic circuits that address various needs in a dimmable LED driver circuit and/or that enable a wide range of dimming (e.g., down to 1%) with low-cost components. Embodiments of the invention are described herein in connection with a boost (step-up) converter. However, the invention is not limited to boost converters and may be used in connection with other types of circuits, such as, for example, buck (step-down), buck-boost, SEPIC, and/or other switch-mode power supply topologies and/or other voltage converter topologies.

[0034] Instead of drawing the control circuit voltage from the auxiliary winding of a boost converter inductor, some embodiments generate a DC housekeeping voltage from a high voltage level found in the boost converter, such as a rectified line voltage. However, the rectified line voltage may be substantially higher than the voltage level needed to power the driver circuitry (e.g., 150 V vs 15 V). This difference in voltage may result in undesirable losses in the control voltage generation circuit.

[0035] For example, a linear voltage regulator having a cascoded switch topology that can be used to generate a relatively low control circuit voltage is illustrated in Fig. 1. The function of the circuit is to generate a relatively low bias "housekeeping" voltage VDD (typically about 15 V) from a high-voltage source VD (e.g., 150 V), which can be a rectified line voltage, as noted above.

[0036] The linear voltage regulator circuit shown in Fig. 1 includes a Zener diode ZD1, a resistor R1, a charging switch Q1, a diode D1 and an output capacitor C1. The Zener diode ZD1 and the resistor R1 form a gate voltage regulation circuit that supplies a gate voltage equal to the Zener voltage of the Zener diode to the gate of the charging switch Q1. The charging switch Q1 is illustrated as a MOSFET transistor switch in Fig. 1. However, it will be appreciated that other types of transistor switches, such as bipolar junction transistors, can be used instead.

[0037] After power up, a DC voltage V_G is generated through the resistor R_1 and the Zener diode ZD_1 (e.g., 18V). The charging switch Q_1 conducts when its gate-to-source voltage ($V_G - V_S$) is larger than a threshold value V_{th} (e.g., 2 V). The diode D_1 conducts as long as $V_S - V_{DD}$ is larger than the forward voltage V_d of the diode D_1 (e.g., 1 V). Consequently, the output capacitor C_1 charges through charging switch Q_1 and diode D_1 as long as $V_G - V_{DD}$ is larger than $V_{th} + V_d$, and the final value of V_{DD} equals to $V_G - V_{th} - V_d$. If V_{DD} rises to a level greater than $V_G - V_{th} - V_d$, the charging switch Q_1 ceases to conduct, and the capacitor is no longer charged by the voltage V_D . The capacitor can then supply the bias voltage V_{DD} until the charge on the capacitor drops to the point that V_{DD} is less than $V_G - V_{th} - V_d$, at which point the voltage V_D begins to charge the output capacitor C_1 again.

[0038] This linear regulation structure is able to provide very fast start-up and a constant dc bias voltage V_{DD} . However, it may suffer the disadvantage of a large power loss, especially when V_D is much higher than V_{DD} . The large power loss is due to the operation of the MOSFET charging switch Q_1 in saturation mode (or linear operation mode if the charging switch Q_1 is a bipolar transistor) and the large voltage drop $V_D - V_{DD}$ across the charging switch Q_1 . For instance, if V_D is ten times V_{DD} , the power loss on Q_1 is nine times the power delivered to the output capacitor C_1 .

[0039] In order to provide a linear regulation structure that has reduced power loss, embodiments of the present inventive concept enable the charging of the output capacitor for limited intervals every switching period. This approach can be realized by manipulating the gate voltage of the charging switch. For example, referring to Fig. 2, an example is shown based on a boost converter 100. The boost converter 100 is configured to supply two different DC output voltages, namely, a high voltage V_{out} that can be used to drive a load, such as a solid state lighting apparatus, and a lower voltage V_{DD} that can be used as "housekeeping power," for example, to power a control circuit 20.

[0040] The basic structure of the boost converter 100 includes a main inductor L_1 , a switch structure including a charging switch Q_2 and a control switch Q_3 , a primary rectifying diode D_3 and a primary output capacitor C_4 that provides an output voltage to a load 26, which may, for example, be a solid state lighting device including a plurality of light emitting diodes. In particular embodiments, the load 26 may include high voltage LEDs, including LEDs having forward voltages in excess of 4 Volts. High voltage LEDs are disclosed, for example, in U.S. patent application Ser. No. 12/814,241 to Ibbetson et al., entitled "High

Voltage Low Current Surface Emitting LED, the disclosure of which is incorporated by reference herein in its entirety. Other high voltage LEDs, such as XB-D LEDs manufactured by the assignee of the present invention, may be used in the load. At least some of the light emitting diodes of the load may be connected in series, so that the forward voltage required to drive the light emitting diodes may be relatively high, e.g., greater than 100 V.

[0041] In some embodiments, the DC output voltages provided to the load 26 could be between about 180V and about 500V +/-10%, respectively with the boost. With a buck-boost converter, the output voltages could be between about 50V and about 250V. The power levels of the converter could vary considerably from 2W to 200W. Typical line (AC) voltage ranges are 100Vac, 120Vac, 230Vac, 277Vac with +/- 10% variation at a frequency of 50/60Hz.

[0042] The charging switch Q2 may be rated for high voltage (e.g., 250V or more) while the control switch Q3 is a low-voltage switch (e.g., ~20V) and can be internal to the controller (such as, for example, a model TPS92210 power factor correcting LED lighting driver controller manufactured by Texas Instruments Incorporated).

[0043] Referring still to Fig. 2, a control voltage regulation circuit 25 is provided to regulate the gate voltage on the charging switch Q2. The control voltage regulation circuit 25 includes resistors R2, R3, R4, Zener diodes ZD2, ZD3 and a capacitor C3. The resistors R3 and R4 and Zener diode ZD3 are connected between the cathode of the Zener diode ZD2 and the gate of the charging switch Q2. The Zener diode ZD3 may have a Zener voltage of, e.g., 4.7 V. A charging circuit 27 is formed by the charging switch Q2, a secondary rectifying diode D2 and a secondary output capacitor C2.

[0044] In the boost converter of Fig. 2, the charging switch Q2 and the control switch Q3 are MOSFET transistor devices; however, other types of transistor devices could be used to implement the switches. The drain of the charging transistor Q2 is coupled to the main inductor L1 and the anode of the primary rectifying diode D3 at a node VD. The gate of the charging transistor Q2 is coupled to the control voltage regulation circuit 25 at a node VG, and the source of the charging transistor is coupled to the anode of the secondary rectifying diode D2 at a node VS. A number of parasitic capacitances are associated with the charging switch Q2, including a gate-to-drain capacitance Cgd, a drain-to-source capacitance Cds, and a gate-to-source capacitance Cgs.

[0045] The control switch Q3 is coupled to the node VS and has an associated parasitic capacitance Cd3.

[0046] The primary output capacitor C4 is coupled to the cathode of the primary rectifying diode D3 at a node Vout, and the secondary output capacitor C2 is coupled to the cathode of the secondary rectifying diode D2 at a node VDD.

[0047] A control circuit 20 receives power from the secondary output capacitor C2 at node VDD. The control circuit 20 has an output coupled to the gate of the control switch Q3, and controls the operation of the control switch Q3 in response to a timing signal provided by a timing reference circuit 29. As discussed in more detail below, the timing reference circuit 29 may include a zero crossing detection (ZCD) circuit that detects when a current through the main inductor L1 falls to zero.

[0048] Fig. 3 is a waveform diagram illustrating operation of the circuit of Fig. 2. In Fig. 3, curve 42 represents the voltage VD at the drain of the charging switch Q2, curve 44 represents the voltage VG at the gate of the charging switch Q2, and curve 46 represents the current i_{D2} through the secondary rectifying diode D2.

[0049] Referring again to Fig. 2, the secondary output capacitor C2 is charged only for a brief period after the on-to-off transitions of switches Q3-Q2 as discussed below. When the control and charging switches Q3 and Q2 are on, the main inductor L1 is charged by the input voltage source and reaches a certain current. In an embodiment with transition mode control with a controller such as a model L6562A driver controller manufactured by STMicroelectronics, Inc., the inductor current ramps up in a linear fashion from zero to a peak value i_{peak} . When control switch Q3 is switched off, the inductor current (i_{peak}) through the main inductor L1 charges the parasitic capacitance Cd3 of the control switch Q3 and brings its drain voltage at node VS up from zero. During this transition, VG, the gate voltage of the charging switch Q2, is temporarily boosted up due to parasitic capacitance of the charging switch Q2, Zener diode D3 and resistor R3. This voltage is clamped by the Zener diode ZD3.

[0050] Referring to Fig. 2 and Fig. 3, at time t0, VD (curve 42) is high. VG (curve 44) is clamped at about 18V. At time t1, the control circuit 20 turns on the transistor Q3. At this point, voltage VD drops to zero, causing current through the inductor L1 to increase up to a peak value. At time t2, the transistor switch Q3 is turned off by the control circuit 20. This causes the voltages at nodes VS and VD to rise as the parasitic capacitances are charged by

inductor current. In addition, the voltage at node VG increases sharply when the transistor switch Q3 is turned off as the gate-source capacitance of the charging switch Q2 holds charge. The voltage at node VG is clamped by the Zener diode ZD3. This voltage holds for a short period (t_2-t_3) due to the current charging the gate-drain capacitance of Q2 until the voltage at node VD settles at the primary output voltage. During this period, the charging channel through the secondary rectifying diode D2 is open, resulting in a charging current (curve 46) flowing into the secondary output capacitor C2. As the parasitic capacitance at the gate of the charging switch Q2 discharges, the voltage at node VG decreases, which turns off the charging switch Q1 when its gate-source voltage is below the threshold, causing the charging current flowing through the secondary rectifying diode D2 to drop off to zero at time t_3 .

[0051] The resistor R3 has a resistance value that is selected to slow down the discharge of the gate-source capacitance of the charging switch Q2 but at the same time defines the width of the charging pulse. During this time, as seen in the waveforms of Fig. 3 (namely, the bump in the voltage VG at time t_2), the charging switch Q2 is on and the inductor current is charging the secondary output capacitor C2. As the gate-source voltage of the charging switch Q2 decays and the charging switch Q2 starts going into saturation, the voltage at node VD rises until the primary rectifying diode D3 conducts and clamps it to V_{out} . As long as the voltage at node VD reaches the output voltage, the charging of the parasitic capacitances stops and the voltage at node VG returns to the voltage set by the Zener diode ZD2.

[0052] With proper component values, the charging of the secondary output capacitor C2 occurs only when the voltage at node VG is boosted up during the on-to-off-transition of the control transistor Q3, which may reduce the power loss normally associated with charging the secondary output capacitor C2 when the voltage at node VD is high.

[0053] One major cost item in a switch mode power supply or a driver (for LEDs) is the main inductor that has an auxiliary winding. The auxiliary winding is needed to generate auxiliary power or bias power (housekeeping power) at around 12-15V to power the control circuitry. Having the auxiliary winding makes the inductor a custom part where the ratio of primary to auxiliary turns has to be managed and an inductor core such as a toroid or EE core with bobbin has to be used. This increases the cost of the inductor. Being able to

generate an auxiliary power supply without the use of auxiliary winding may allow the use of a less expensive inductor. The inductor on a toroid or EE core could be 10-30% less expensive than one with an auxiliary winding. However, embodiments of the invention may allow the use of a standard off-the-shelf drum core inductor which could be less than half the cost of a custom inductor with auxiliary winding.

[0054] Once the energy in the main inductor L1 is completely delivered to the output, the inductor current falls to zero and the primary rectifying diode D3 reverse biases. A resonance between the main inductor L1 and the capacitance at node VD drives the voltage VD down. This voltage needs to be detected in order to initiate a new switching period. When the auxiliary winding on the boost circuit inductor is used for housekeeping power, it is easy to sense the voltage on the winding and make the decision to start a new switching period. Without an auxiliary winding, a typical approach is to use RC coupling to convey the VD node signal to the controller. With a boost converter and with dimming, there are certain limitations to this 'zero cross detection' (ZCD) method. Embodiments of the invention provide additional circuitry for determining when to start a new switching period as discussed in more detail below.

[0055] For voltage converters operating in critical conduction mode (CRM, boundary mode, or transition mode), it is desirable to provide a zero cross detection (ZCD) signal to the control circuit 20 to trigger a new switch on period. The ZCD signal indicates that the current through the main inductor has reached zero, and is commonly generated with a secondary winding of the main inductor L1. If the secondary winding is unavailable, the ZCD signal can also be generated with an RC network. As shown in Fig. 4, a zero cross detector 30 may be coupled between the voltage VD and ground and may generate a zero cross detection signal ZCD that is provided to the control circuit 20 when the current through the main inductor L1 has reached zero.

[0056] A ZCD detection circuit 30A according to some embodiments based on a boost converter topology is shown in Fig. 5.

[0057] The ZCD detection circuit 30A in Fig. 5 includes a capacitor C5 and resistors R5, R6 coupled between the output of the inductor L1 (i.e. the location of the voltage VD) and ground. The voltage at the node between the resistor R5 and the capacitor C5 is denoted VC. A transistor switch Q4 which is controlled by a control circuit 20 is also coupled between VD and ground along with an associated parasitic capacitance Cp1.

[0058] During the time when the switch Q4 is off and diode D3 is conducting, the output voltage V_{out} is approximately equal to V_D , and the ZCD detection capacitor C5 is charged through the resistors R5 and R6. When the inductor current i_{L1} decreases to zero, the diode D3 turns off and V_D decreases due to the resonance between inductor L1 and parasitic capacitance C_{p1} . As the capacitor C5 is able to hold its voltage, the voltage at node VC follows the variation of voltage at node V_D . By choosing an appropriate ratio between R5 and R6, a ZCD signal can be generated and fed to the control circuit 20.

[0059] The voltage level on the capacitor C5 and the speed required to get to that level may be selected so that a correct ZCD signal is provided, especially when the circuit has to be compatible with phase-cut dimmers. The threshold voltages for the ZCD signal in typical control circuits are normally low voltages (close to zero). A high-to-low transition of the ZCD signal triggers a new switching-on interval.

[0060] In a boost converter, when the peak input voltage (e.g. 180V) is close to the output voltage (e.g. 190V) the resonant swing of the voltage V_D may be small (e.g. 20V - twice the difference) at the peak. If the DC voltage on the capacitor C5 is low, then the voltage signal ZCD may not be able to swing low enough to trigger a zero crossing detection by the control circuit 20. To better ensure correct ZCD triggering, the voltage on capacitor C5 may be large enough to allow correct ZCD triggering, but lower than the output voltage V_{out} . Furthermore, this large value may be reached within one switching period.

[0061] When the switch Q4 is conducting, the voltage at V_D is close to zero, and the capacitor C5 is discharged through R5, R6 and Q4. Similarly, the voltage on the capacitor C5 can decrease to zero during a long off period due to dimming. However, as soon as the voltage level V_D goes high, the capacitor C5 should be charged to a high voltage as quickly as possible. These requirements can be met by manipulating the voltage on the capacitor C5 and charging/discharging C5 with different speeds. One circuit to realize these functions is shown in Fig. 6.

[0062] Referring to Figure 6, a ZCD detection circuit 30B includes capacitors C5 and C6, a diode D5, a Zener diode ZD4 and resistors R5, R6 and R7 connected as shown between the output of the inductor L1 and ground.

[0063] With the circuit shown in Fig. 6, the capacitor C5 is mostly charged through the diode D5, resistor R7 and Zener diode ZD4 when V_D is high. The small resistance of R7 leads to fast charging, while the Zener diode ZD4 defines the maximum voltage on C5, which

is roughly the output voltage V_{out} minus the Zener voltage of ZD4. The Zener diode ZD4 is provided so that the voltage at ZCD is able to go higher than the trigger threshold when VD is high. When VD is low, C5 is discharged through R5 and R6, while the R7 branch is blocked by diode D5. Thus, the discharging can be slowed by using high-resistance values for R5 and R6. The capacitor C6 is used to introduce a little delay to ZCD signal. With this configuration, the voltage on C5 can be close to, but less than the output voltage; thus, a correct ZCD signal can be generated.

[0064] Another zero cross detection circuit 30C that can generate a suitable zero current detection signal is illustrated in Fig. 7. The ZCD circuit 30C includes resistors R7 and R8, Zener diodes ZD5 and ZD6, and a capacitor C7.

[0065] In the circuit 30C, the Zener diode ZD5 is a high voltage Zener diode (e.g., 180V). When VD drops below the Zener voltage of the Zener diode ZD5, the voltage at node ZCD will collapse to zero as R7 discharges the capacitor C7. This triggers the zero crossing detection threshold (e.g., 0.7V). When the voltage VD rises above the voltage on the Zener diode ZD5, the voltage at node ZCD rises above another threshold required for resetting the control circuit (e.g., 1.4V) which readies the control circuit for the next zero crossing event. The Zener diode ZD6 clamps the voltage level of the ZCD signal if necessary (e.g., at 4.7V).

[0066] Many different embodiments have been disclosed herein, in connection with the above description and the drawings. It will be understood that it would be unduly repetitious and obfuscating to literally describe and illustrate every combination and subcombination of these embodiments. Accordingly, all embodiments can be combined in any way and/or combination, and the present specification, including the drawings, shall be construed to constitute a complete written description of all combinations and subcombinations of the embodiments described herein, and of the manner and process of making and using them, and shall support claims to any such combination or subcombination.

[0067] In the drawings and specification, there have been disclosed typical embodiments of the invention and, although specific terms are employed, they are used in a generic and descriptive sense only and not for purposes of limitation, the scope of the invention being set forth in the following claims.

What is claimed is:

1. A voltage regulator, comprising:
a charging switch including a first terminal coupled to a high voltage node, a second terminal, and a control terminal;
a rectifier coupled to the second terminal of the charging switch;
an output capacitor coupled to the rectifier;
a control switch coupled to the second terminal; and
a control voltage regulation circuit coupled to the control terminal of the charging switch;

wherein the control switch and the charging switch are configured so that when the control switch is turned off, a rise in voltage on the control switch causes an increase in voltage on the control terminal of the charging switch sufficient to allow a charging current to flow through the rectifier and into the output capacitor; and

wherein the control voltage regulation circuit is configured to dissipate the increased voltage on the control switch so that the charging current only flows for a limited period of time in response to the control switch being turned off.

2. The voltage regulator of Claim 1, wherein the control voltage regulation circuit comprises a clamping diode coupled to the control terminal of the charging switch.

3. The voltage regulator of Claim 2, further comprising:
a resistor in parallel with the clamping diode and configured to allow a voltage clamped by the clamping diode to dissipate.

4. The voltage regulator of Claim 3, wherein a resistance of the resistor is selected to provide a desired pulse width of the charging current.

5. The voltage regulator of Claim 1, wherein the control switch has a parasitic capacitance that is charged when the control switch is turned off thereby causing the rise in voltage on the control switch.

6. The voltage regulator of Claim 5, wherein the control voltage regulation circuit comprises:

- a Zener diode coupled to a voltage node;
- a first resistor coupled between the voltage node and a voltage source;
- a clamping diode coupled to the control terminal of the charging switch;
- a second resistor coupled in parallel with the clamping diode;
- a third resistor coupled between the clamping diode and the voltage node; and
- a capacitor coupled to the voltage node.

7. The voltage regulator of Claim 6, wherein the second and third resistors and the capacitor are configured to dissipate the increased voltage on the control terminal of the charging switch.

8. The voltage regulator of Claim 7, wherein the charging switch is configured to turn off in response to dissipation of the increased voltage on the control terminal of the charging switch.

9. The voltage regulator of Claim 1, further comprising:
a main inductor;
a zero crossing detection (ZCD) circuit configured to generate a zero cross detection signal in response to current through the main inductor falling to zero; and
a control circuit configured to selectively activate the control switch in response to the zero cross detection signal;

wherein the zero crossing detection signal is configured to generate the zero cross detection signal to have a sufficient voltage swing to trigger a zero cross detection by the control circuit.

10. The voltage regulator of Claim 9, wherein the zero crossing detection circuit comprises:

- a capacitor coupled to the high voltage node and to a first node;
- a first resistor coupled to the capacitor and to a ZCD output node;
- a second resistor coupled to the ZCD output node;
- a first diode including an anode coupled to the first node and including a cathode;
- a second resistor coupled to the cathode of the diode; and
- a second diode including a cathode coupled to the second resistor, wherein the second diode comprises a Zener diode.

11. The voltage regulator of Claim 9, wherein the zero crossing detection circuit comprises:

- a first resistor coupled to the high voltage node;
- a first Zener diode having a cathode coupled to the first resistor and having an anode coupled to a ZCD output node;
- a second Zener diode having a cathode coupled to the ZCD output node;
- a second resistor coupled to the ZCD output node; and
- a capacitor coupled to the ZCD output node.

12. A voltage regulator for generating a secondary voltage in a power supply circuit, the voltage regulator comprising:

- a charging switch coupled to a high voltage node and to an output capacitor; and
- a control voltage regulation circuit coupled to a control terminal of the charging switch;

wherein the control switch and the charging switch are configured so that when the control switch is turned off, a rise in voltage on the control switch causes an increase in voltage on the control terminal of the charging switch sufficient to allow a charging current to flow into the output capacitor; and

wherein the control voltage regulation circuit is configured to dissipate the increased voltage on the control switch so that the charging current only flows for a limited period of time in response to a state transition of the control switch.

13. A voltage regulator for generating a secondary voltage in a power supply circuit, the voltage regulator comprising:
a charging circuit coupled to a switching node and to an output node;
a storage element coupled to the output node; and
a control voltage regulation circuit coupled to the charging circuit and configured to cause the charging circuit to generate a current pulse for charging the storage element.

14. A method of generating a low voltage in a high voltage power supply, the method comprising:
generating a high voltage at a voltage node; and
in response to a change in a voltage level at the voltage node, generating a pulse of current for charging an output capacitor to a level that is lower than the high voltage.

15. A solid state lighting device, comprising:
a solid state load comprising a plurality of solid state light emitting devices; and
a power supply circuit that generates a primary voltage and supplies the primary voltage to the solid state load;
wherein the power supply circuit comprises a voltage regulator that generates a secondary voltage, the voltage regulator comprising:
a charging circuit coupled to a switching node and to an output node;
a storage element coupled to the output node; and
a control voltage regulation circuit coupled to the charging circuit and configured to cause the charging circuit to generate a current pulse for charging the storage element.

16. A zero crossing detection (ZCD) circuit that generate a zero crossing detection signal in response to current through an inductor falling to zero, comprising:
a capacitor coupled to the inductor and to a first node;
a first resistor coupled to the capacitor and to a ZCD output node;
a second resistor coupled to the ZCD output node;
a first diode including an anode coupled to the first node and including a cathode;
a second resistor coupled to the cathode of the diode; and

a second diode including a cathode coupled to the second resistor, wherein the second diode comprises a Zener diode.

17. A zero crossing detection (ZCD) circuit that generate a zero crossing detection signal in response to current through an inductor falling to zero, comprising:

- a first resistor coupled to the inductor;
- a first Zener diode having a cathode coupled to the first resistor and having an anode coupled to a ZCD output node;
- a second Zener diode having a cathode coupled to the ZCD output node;
- a second resistor coupled to the ZCD output node; and
- a capacitor coupled to the ZCD output node.

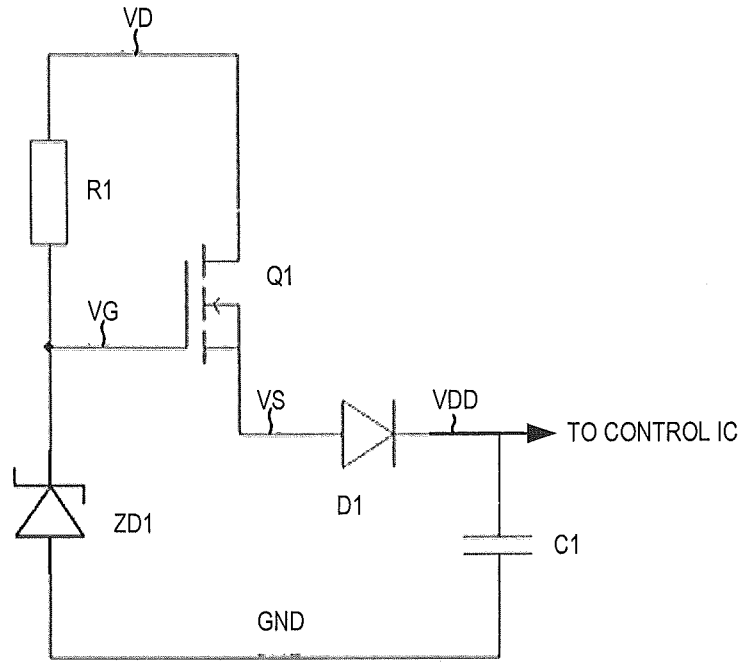


FIGURE 1

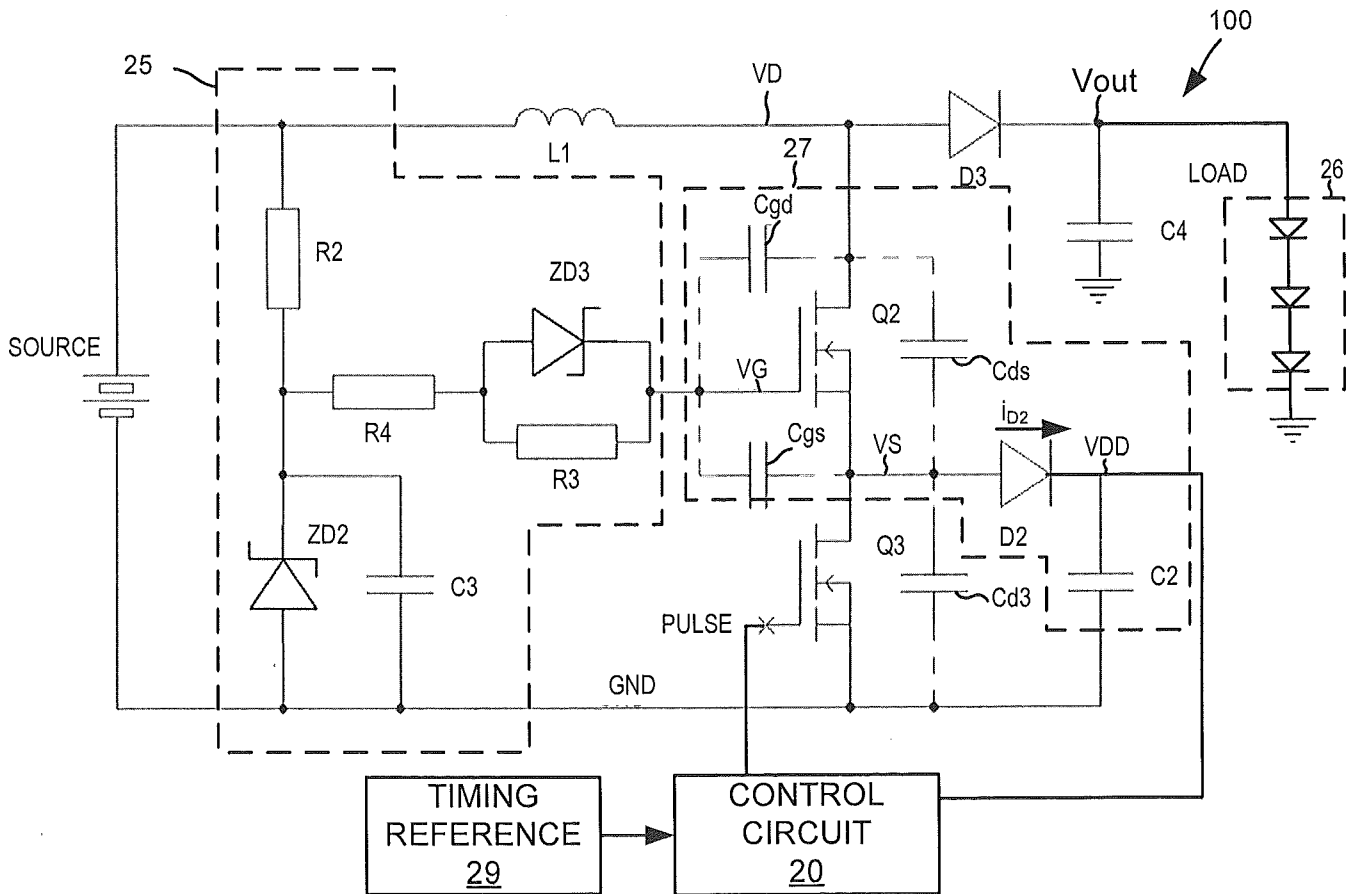


FIGURE 2

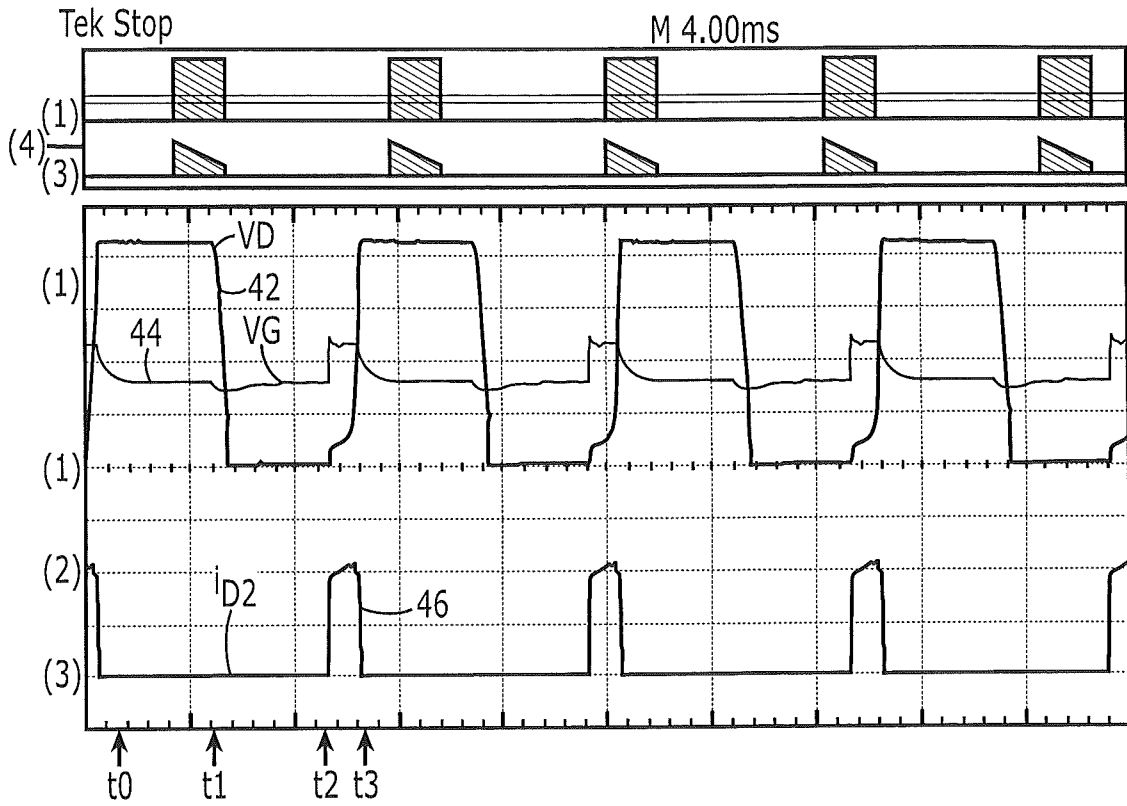


FIGURE 3

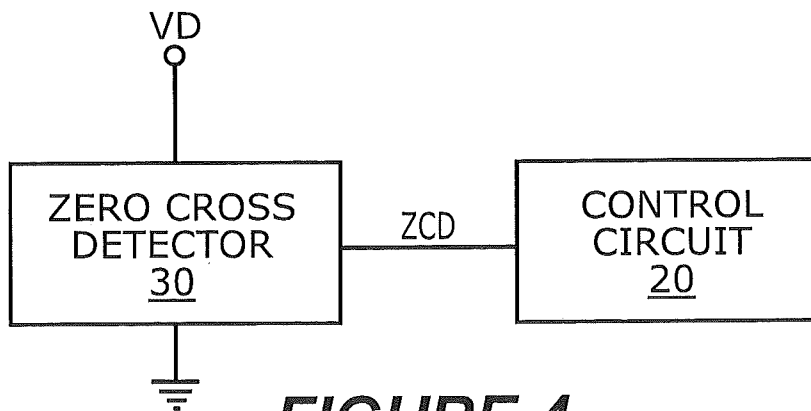


FIGURE 4

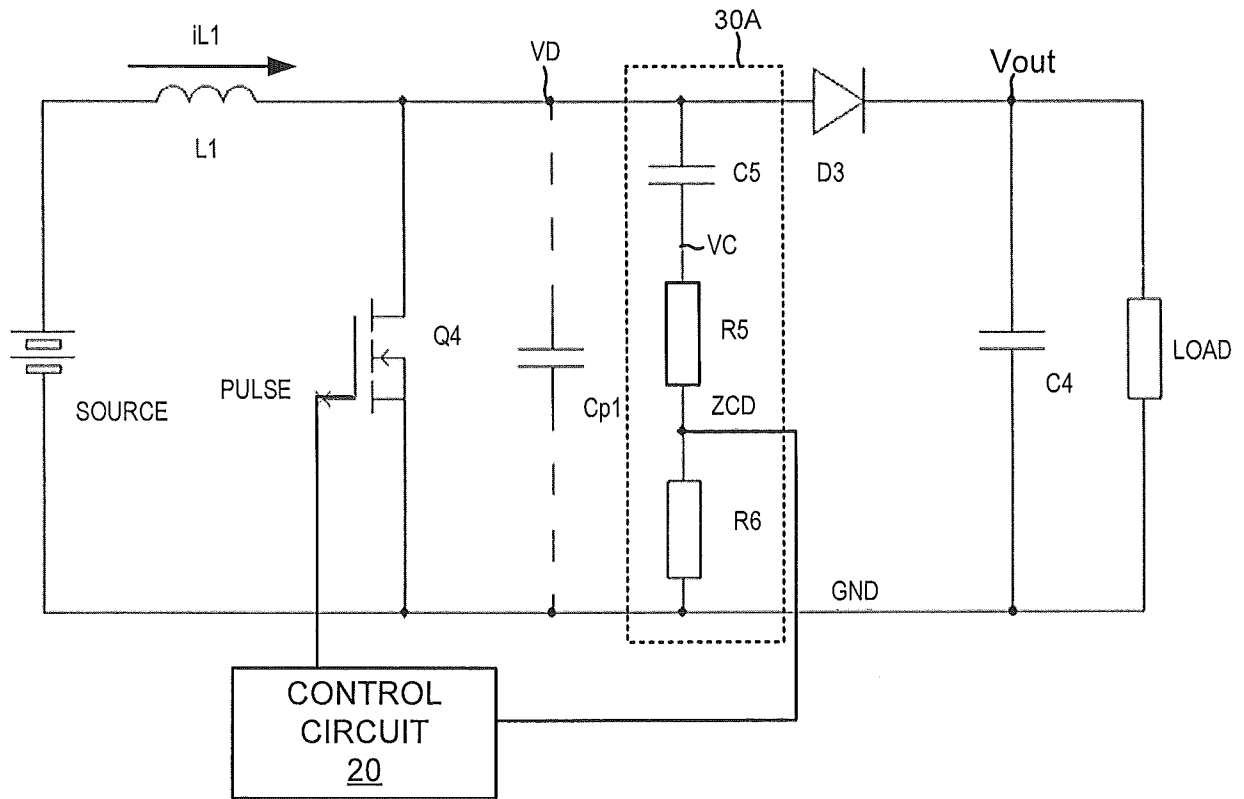


FIGURE 5

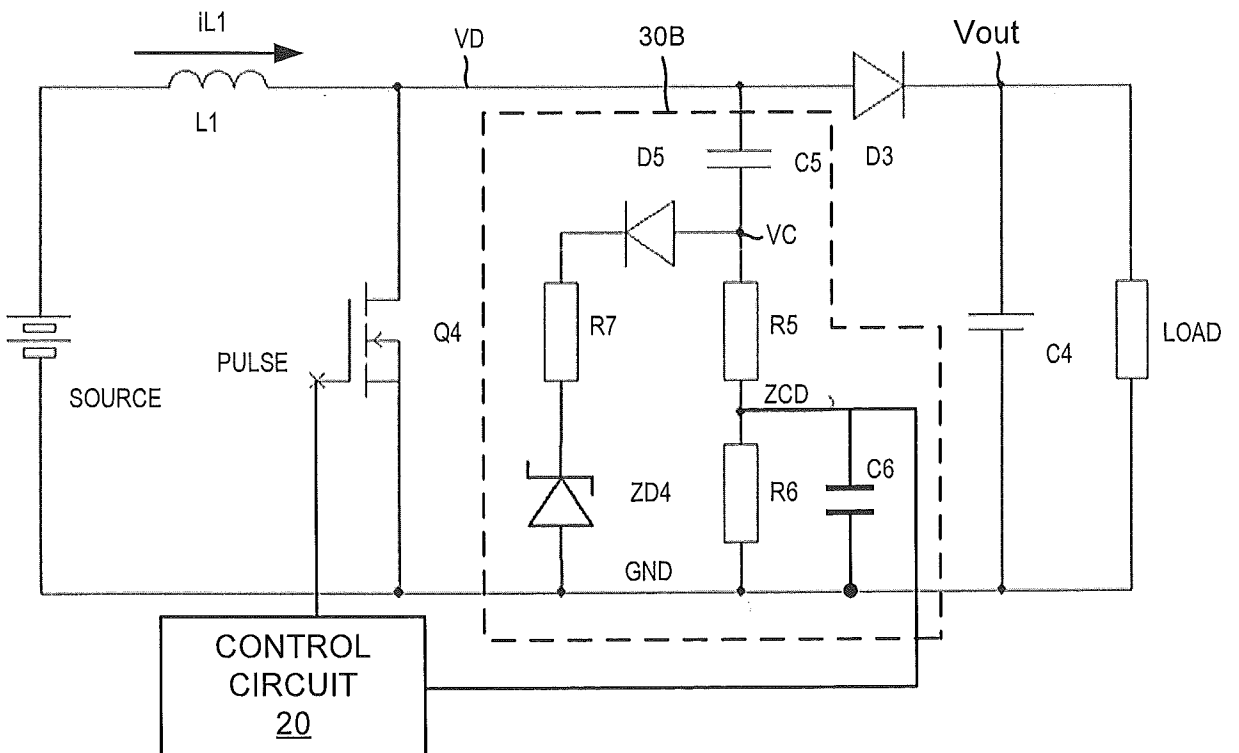


FIGURE 6

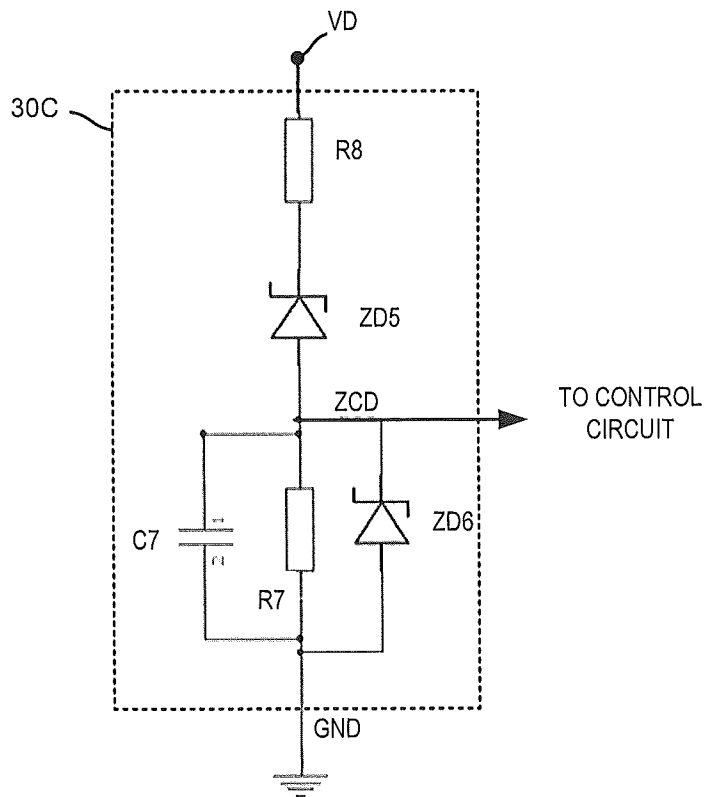


FIGURE 7

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2013/039069

A. CLASSIFICATION OF SUBJECT MATTER
 IPC(8) - H02M 3/335 (2013.01)
 USPC - 363/44
 According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
 IPC(8) - H02H 3/08; H02M 1/12, 3/335, 5/00; H05B 37/02; G05F 1/40 (2013.01)
 USPC - 315/294; 323/285, 328; 361/93.7; 363/21.01, 21.12, 44

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
 CPC - H02M 3/156, 3/33507; H03K 17/0822; H05B 37/029; Y02B 70/126 (2013.01)

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
 Orbit, Google Patents, Google Scholar

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2010/0148697 A1 (BAYAT et al) 17 June 2010 (17.06.2010) entire document	13, 15
X	US 5,886,512 A (BECERRA) 23 March 1999 (23.03.1999) entire document	14
Y	US 2011/0127925 A1 (HUANG et al) 02 June 2011 (02.06.2011) entire document	17
Y	US 8,018,694 B1 (WU) 13 September 2011 (13.09.2011) entire document	17
A	US 2012/0091816 A1 (LIU et al) 19 April 2012 (19.04.2012) entire document	1-17
A	US 2011/0194312 A1 (GAKNOKI et al) 11 August 2011 (11.08.2011) entire document	1-17
A	US 2007/0222485 A1 (UEDA) 27 September 2007 (27.09.2007) entire document	1-17
A	US 2012/0056552 A1 (YU et al) 08 March 2012 (08.03.2012) entire document	1-17
A	US 2011/0096577 A1 (YAMADA) 28 April 2011 (28.04.2011) entire document	1-17
A	US 2006/0098464 A1 (OSAKA et al) 11 May 2006 (11.05.2006) entire document	1-17

Further documents are listed in the continuation of Box C.

* Special categories of cited documents:	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A" document defining the general state of the art which is not considered to be of particular relevance	"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E" earlier application or patent but published on or after the international filing date	"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&" document member of the same patent family
"O" document referring to an oral disclosure, use, exhibition or other means	
"P" document published prior to the international filing date but later than the priority date claimed	

Date of the actual completion of the international search 21 August 2013	Date of mailing of the international search report 06 SEP 2013
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Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Authorized officer: Blaine R. Copenheaver PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774
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