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(54) **Title:** SEQUENTIAL CIRCUIT WITH CURRENT MODE ERROR DETECTION

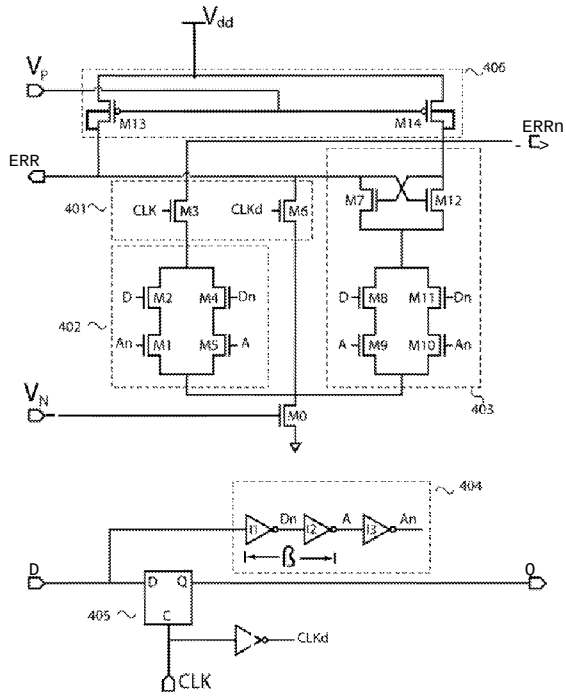

Fig 4 a

(57) **Abstract:** A sequential circuit with transition error detector comprising: a sequential element (405) with an input that is asserted to the output during the second clock phase of a two phase clock signal, a transition error detector (401, 402, 403, 404) coupled to the sequential element input to assert an error signal if a transition occurs at the sequential element input during the second clock phase but not to assert during the first clock phase, wherein transition error detection circuit comprises a current mode circuit (401, 402, 403) as detection circuit for transition timing error detection from signals derived from the sequential element clock signal and input signals.

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Sequential Circuit with Current Mode Error Detection

The invention relates to combinatory logic timing error detection and especially to improvements to subtreshold CMOS devices by a use of a type of new timing error detection circuit.

Background

In conventional digital design flow, combinational logic delay constraints are static in the sense that the resulting circuit from synthesis must meet the worst case operation condition delays in order to guarantee the circuit operation. If the run-time delay is longer than analyzed during the design time, correct circuit operation cannot be secured. In a conventional design, meeting timing requirements introduces overdesign leading to both area and power - dynamic and static - consumption increase in the system. On the other hand, a timing error detection (TED) system equipped with Error-Detection Sequential (EDS) latches (Bowman, K.A.; et. al. "Energy-Efficient and Metastability-Immune Resilient Circuits for Dynamic Variation Tolerance" IEEE Journal of Solid-State Circuits, Volume: 44 , Issue: 1, Page(s): 49 - 63, 2009) can tolerate late arriving signals from combinational logic. The EDS latch detects late arriving data and reacts to recover from the error. EDS operation is conceptually shown in Fig. 1, where in Fig la a logic stage (102) between two sequential elements (101, 103) is shown. In Fig. lb, where the signals of the second sequential element (103) are shown, the first transition in D arrives early and does not trigger a conceptual Error signal, whereas the second transition in D arrives late and triggers the Error signal. The Error signal can then be used, for example, to trigger an instruction replay in modern processors. Fig. 2 shows a conventional circuit for error detection, where the data (D) and clock (CLK) inputs of a conventional latch (201) are connected to a transition detector (202) which generates the Error signal when the data transitions within the clock high period (for a positive edge triggered latch).

The minimum energy point for static CMOS logic is in the subthreshold region, where the operating voltage is below the threshold voltage of the CMOS transistors. Although minimum energy operation is achieved, the effect of the variations in

modern deep submicron CMOS processes is greatly increased. Subthreshold current is due to diffusion charge transport mechanism and it can be observed that the drain current is exponentially related to the gate-source voltage, drain-source voltage, and thermal voltage. From this exponential relationship it can be seen that, when compared to nominal operating conditions (strong inversion), effects of process variation, supply voltage, and temperature are greatly amplified in the subthreshold operating region.

Combining subthreshold design with TED mitigates the subthreshold design hindrances. Although adding TED circuitry introduces extra energy consumption, the timing error information provided by the TED circuitry can be used to control the circuit operation for better energy efficiency. With TED, circuits can be designed with relaxed timing margin overhead, and dynamic voltage (DVS) or frequency (DFS) scaling can be used alongside error recovery. This works not only from process variance and operating conditions point of view, but a TED system also takes into account data related delay variance issues. However, if the circuits designed for the nominal voltage range are used in the subthreshold range, the size, and thus the energy consumption, of the circuits grows unfeasibly large (Turnquist, M.J.; et. al. "Adaptive Sub-Threshold Test Circuit" NASA/ESA Conference on Adaptive Hardware and Systems, 2009. Page(s): 197 - 203, 2009).

Subthreshold source-coupled logic (STSCL) can be used to provide both robustness to process, supply voltage and temperature (PVT) variations and reduced power consumption in subthreshold. STSCL has been shown to consume less power than static CMOS for low operation frequencies. Since the delay of an STSCL gate is independent of the threshold voltage (VT), STSCL is more robust to PVT than static CMOS. In addition, STSCL allows for accurate control of gate current consumption and operation frequency. These advantages are all beneficial for TED systems operating in subthreshold where less power overhead, robustness, and ease in adaptability are considered key parameters. As shown in Fig. 3, an STSCL circuit is constructed by a network of differential NMOS pairs comprised of transistors M1,M2 (301), an adjustable PMOS load, transistors M3, M4, (302) with have an output resistance RP, and an adjustable tail current ISS. The NMOS pairs are used to construct logic gates and thus steer ISS between the two PMOS loads. The voltage

swing VSW=RP · ISS in STSCL is maintained by balancing the size of RP and magnitude of ISS. Since ISS can be reduced to the pA range in subthreshold, RP needs to be in the low GΩ range to achieve proper VSW. By connecting the bulk of the PMOS load devices to the drain, a large RP is achieved without excessively large transistor lengths. The size of RP and the magnitude of ISS are both adjusted by the Voltage Swing Control (VSC) block (303). The VSC decreases the dependence on global process variations, supply noise, and temperature fluctuations. It is important to recognize that one VSC generates VP and VN for a large number of STSCL gates. The VSC typically consists of an operational amplifier connected to a dummy STSCL circuit.

Error detection principle and error decovery is described in US2010079184 (Al) and in WO2004084072. The general ideas timing error detection and recovery is not described here in detail. Current mode logic circuits are described in US2009219054 (Al).

One object of the invention is to minimize the effects of sensitivity to PVT variations of the device and timing error detection. The invention allows use of for example subtreshold CMOS circuits, and it allows also larger voltage and temperature tolerances.

Modern digital design flow CAD tools do not support STSCL, which forces STSCL to be designed by hand. Accordingly, a new approach is required. This approach should integrate the robustness of STSCL but can be placed within the conventional digital design flow. The purpose of our invention is also to overcome the aforementioned problems.

The object is achieved by a circuit according to the claim 1.

Brief Description of the Drawings

Fig.l (a) is a conceptual diagram showing a logic stage between two sequential elements.

Fig.l (b) is a timing diagram showing the concept of timing error detection.

Fig. 2 is a schematic diagram of a previous nominal voltage sequential circuit with error detection

Fig. 3 is a conceptual schematic diagram of a STSCL inverter.

Fig. 4 (a) is a schematic diagram of a sequential logic element with current mode error detection in accordance with some embodiments.

Fig. 4 (b) is a timing diagram for the circuit of Fig. 4(a) in accordance with some embodiments.

Detailed Description

An embodiment of our invention, a Sequential Circuit with Current Mode Error Detection (SCCMED), is shown in Figure 4a. This circuit, described in more detail below, may be used, for example, to replace traditional master slave flip flop circuits in the critical paths of pipelined logic. The error detection feature can then be further used to attain gain in performance, power, and/or yield. The use of current-mode avoids the power and performance penalty of using conventional circuits designed for nominal operating voltage ranges. As only the error detection is designed with current mode logic, it is simple to integrate the circuit into a static CMOS logic pipeline which has been designed with conventional CAD digital design flow.

The block diagram of the Current Mode Sequential Circuit with Error Detection is shown in Fig. 4(a). It generally consists of a current mode transition detector (401, 402, 403), a delay line (404), a sequential element such as a latch (405), a load (406), and a delayed clock signal (CLKd).

Although the latch 405 of the figure is a positive edge triggered latch, it should be appreciated that any type of latch (for example negative edge triggered) can be used without any loss of generality. The latch input is connected to the critical path of the logic (D) of which the timing errors are to be detected. The error detection

according to invention may be used with any sequential element with suitable timing requirements for the TED-device.

The delay line (404) consists of three delay stages, which can be, but are not limited to, conventional static CMOS inverters or SCSTL inverters. The function of the delay line is to pass on the critical path signal D to the transition detector in three delayed stages. The delay line may be made of alike gates as the element 404, resulting to alike delays temperature and voltage dependencies as in the element 404. The delays may also controllable, for example by controlling the current.

The transition detector includes a timing error reset switch (401), consisting of transistors M3 and M6, a pulldown network switch (402) (transistors Ml, M2, M4, M5), and a latching switch (403) (transistors M7, M8, M9, M10, Mil, M12). The function of the combination of the load line 406 and transition detector 401, 402, 403 is to recognize a transition of D during the time CLK is high. A transition of D during CLK high generates a differential timing error (i.e. ERR goes high and ERRn low). This is the result of (402) pulling ERRn low and 403 being OFF. After a transition of D is complete, 403 is ON and keeps ERR high and ERRn low until a negative CLK edge. The functionality of Error Detection can be further explained with the help of Fig. 4(b). As CLK goes low to high, D stays high and Dn=An=low and A=high. In other words, 403 is ON and 402 is OFF. Transistors M7 and M12 ensure that ERR is latched low during this time. After D transitions from high to low, a number of events happen during the delay β. First, 403 shuts OFF since D=An=low. This cuts off the path to ground for M7 and M12 thus helping to drive the ERR signal high. Secondly, after a small delay through II, both 402 and M3 turn ON since Dn=A=high and CLK=high. This event drives ERRn low through 402. 402 stays ON for the delay of β. At the end of β, 402 turns OFF and 403 ON. The ERR stays high until an error reset (ERR-reset) is performed using 401. At the negative edge of CLK, M3 shuts OFF thus driving the ERRn node high. At the same time, M6 turns ON and pulls the ERR node low. The ERR-reset condition continues for the entire time CLK is low since detecting a transition of D during this time is insignificant for a TED pipeline.

The term "transistor" here encompasses both N-type and P-type metal oxide field effect (MOS) transistors. Further encompassed are MOS transistors, where different parameters such as VT, material type, gate size and configuration, insulator thickness, etc. are varied. The term "transistor" can also include other FET-type and bipolar-junction transistors and other types of transistors not yet known or developed.

CLAIMS

1. A sequential circuit with transition error detector comprising:
a sequential element (405) with an input that is asserted to the output during the second clock phase of a two phase clock signal, a transition error detector (401, 402, 403, 404) coupled to the sequential element input to assert an error signal if a transition occurs at the sequential element input during the second clock phase but not to assert during the first clock phase, **characterized** by transition error detection circuit comprising a current mode circuit (401, 402, 403) as detection circuit for transition timing error detection from signals derived from the sequential element clock signal and input signals.

2. The sequential circuit of claim 1 comprising further delay line (404) for generating delayed versions (Dn, A, An) of the sequential element input signal (D) for the detection circuit and delay for generating delayed clock (CLKd) for the detection circuit (401, 402, 403).

3. The sequential circuit of claim 1 or 2, in which the current mode transition detection circuit (401, 402, 403) comprises differential transistor circuit.

4. The circuit of claim 3, in which the transition detection circuit (401, 402, 403) comprises a source coupled current mode logic.

5. The sequential circuit of claim 4, in which the transition detection circuit (401, 402, 403) comprises a subthreshold source coupled current mode logic.

6. The sequential circuit according any of claims 1 to 5, in which the sequential element (405) input and output are part of a digital pipelined logic stage.

7. The sequential circuit of any preceding claim, in which the sequential element (405) comprises logic functioning in subthreshold voltage mode.

8. The circuit of any preceding claim, in which one path of the differential operation (401, 402) in the detection circuit is activated during the second phase of the clock signal when there is a transition in the latch input signal.

9. The circuit of any preceding claim, in which one path of the differential operation (403) in the detection circuit is activated during the first phase of the clock signal or during the second phase of the clock signal if there is no transition in the latch input signal.

10. Method for detecting transition error in sequential circuit, method comprising step of providing signals derived from clock and input signals of the sequential circuit to a transition detection circuit that works in current mode.

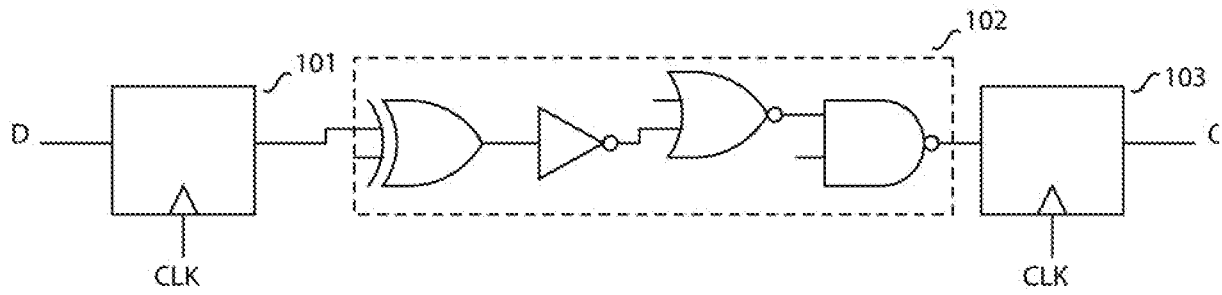

Fig 1a (Prior art)

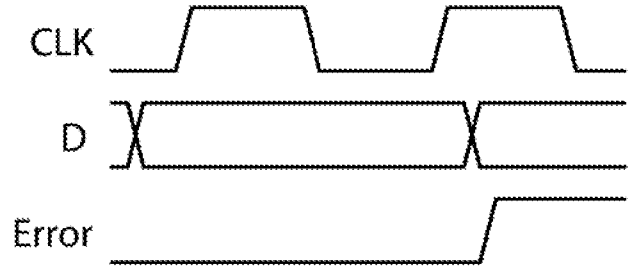

Fig 1 b (Prior art)

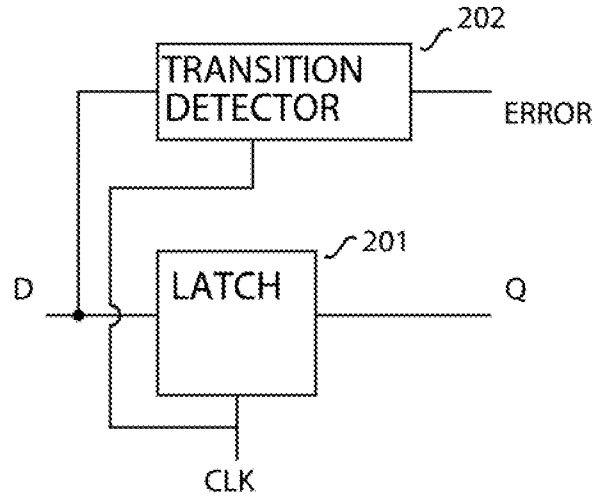

Fig 2 (Prior art)

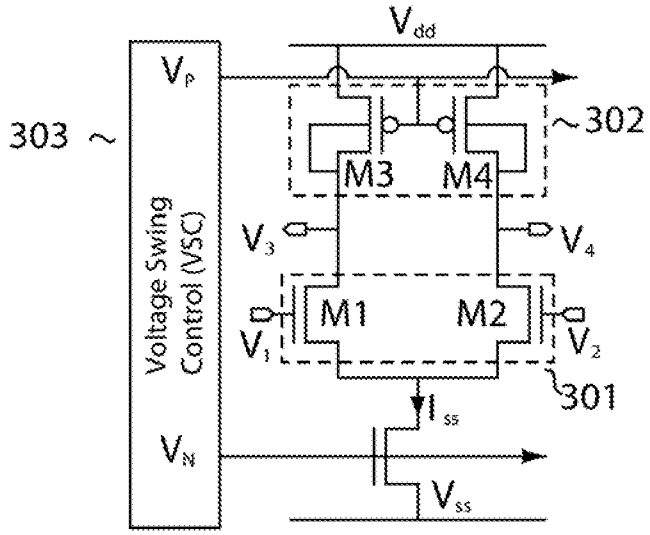

Fig 3 (Prior art)

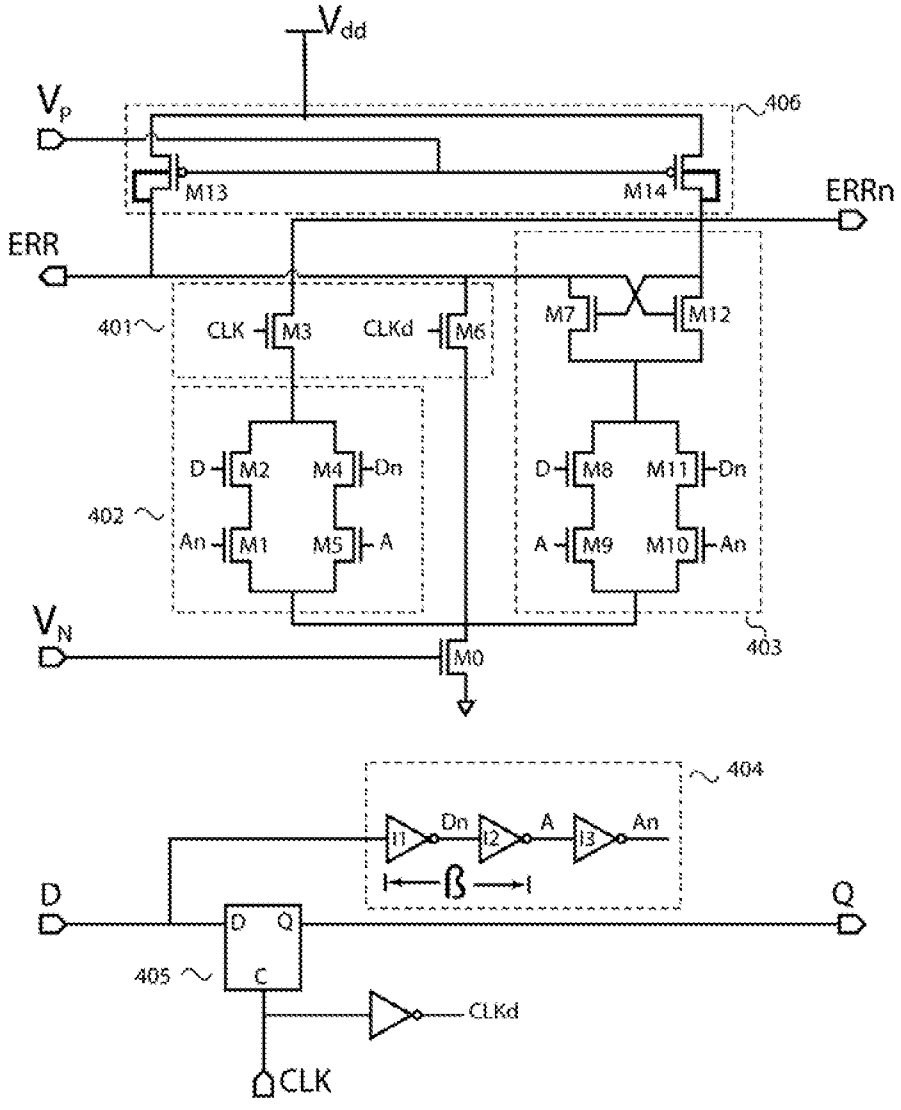

Fig 4 a

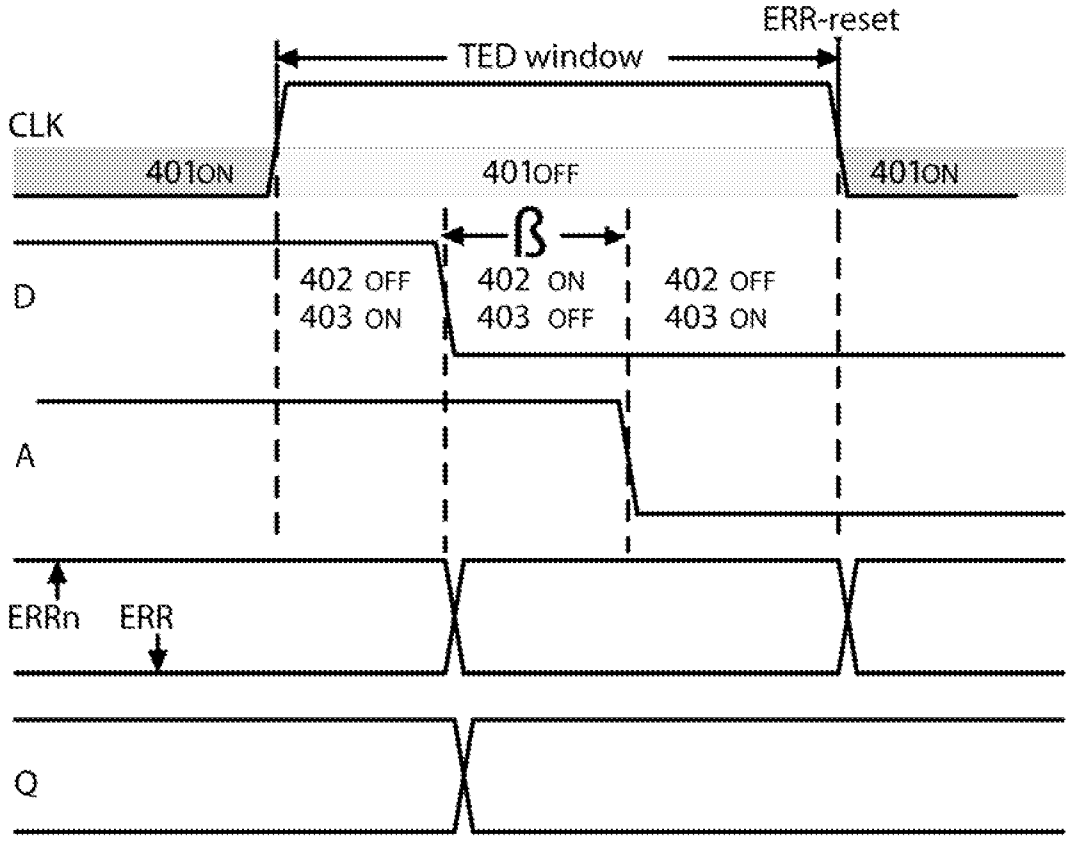
ERR-reset
TED window
CLK
401ON
401OFF
401ON
β
D
402 OFF
403 ON
402 ON
403 OFF
402 OFF
403 ON
A
ERRn
ERR
Q

Fig 4 b

INTERNATIONAL SEARCH REPORT

International application No.
PCT/FI201 1/050653

A. CLASSIFICATION OF SUBJECT MATTER

See extra sheet

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H03K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

FI, SE, NO, DK

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI, IEEE Xplore

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 201 00791 84 A 1 (BOWMAN, K et al.) 0 1 April 201 0 (01 .04.201 0) Abstract; paragraphs [001 5]-[001 9]; claim 1; figs. 2 and 3	1-10
A	TAJALLI, A.: "Subthreshold source-coupled logic circuits for ultra-low-power applications", IEEE J. of Solid-State Circuits, Vol. 43, No. 7, July 2008, pp. 1699-1 7 10 the whole document	1-10
A	VALADIMAS, S.: "Timing error tolerance in nanometer ICs", IEEE 16th International On-Line testing Symposium, 5-7 July 201 0, pp. 283-288 the whole document	1-10
A	CHOUDHURY, M.: "TIMBER: Time borrowing and error relaying for online timing error resilience", Design, Automation & Test in Europe Conference & Exhibition (DATE), 8-1 2 March 20 10, 6 pages the whole document	1-10

☒ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
18 October 201 1 (18.10.201 1)	25 October 201 1 (25. 10.201 1)

Name and mailing address of the ISA/FI	Authorized officer
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INTERNATIONAL SEARCH REPORT

International application No.
PCT/FI201 1/050653

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category'*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	DAS, S.: "Razorl I: In situ error detection and correction for PVT and SER tolerance", IEEE J. of Sol id-State Circuits, Vol. 44, No. 1, Jan. 2009, pp. 32-48 the whole document	1-10
A	BLAAUW, D.: "Statistical timing analysis: from basic principles to state of the art", IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems, Vol. 27, No. 4, April 2008, pp. 589-607 the whole document	1-10
T	TURNQUIST, M.:" A timing error detection latch using subthreshold source-coupled logic", 201 0 Conference on Ph.D. Research in Microelectronics and Electronics (PRIME), 18-21 July 2010, 4 pages the whole document	1-10

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/FI201 1/050653

Patent document cited in search report	Publication date	Patent family members(s)	Publication date
US 201 00791 84 A 1	01/04/201 0	None	

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CLASSIFICATION OF SUBJECT MATTER

Int.Cl.
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