(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
29 December 2016 (29.12.2016)

WIPO | PCT

(10) International Publication Number
WO 2016/209529 A1

(51) **International Patent Classification**:
H01R 13/648 (2006.01) *H01R 13/22* (2006.01)
H01R 13/652 (2006.01)

(21) **International Application Number**:
PCT/US2016/034343

(22) **International Filing Date**:
26 May 2016 (26.05.2016)

(25) **Filing Language**: English

(26) **Publication Language**: English

(30) **Priority Data**:
14/750,846 25 June 2015 (25.06.2015) US

(71) **Applicant**: **INTEL CORPORATION** [US/US]; 2200 Mission College Boulevard, Santa Clara, California 95054 (US).

(72) **Inventors**: **KONG, Jackson Chung Peng**; 12A, Denai Bayu 12, Seri Tanjung Pinang, Tanjung Tokong, 10470 (MY). **CHEN, Kuan-Yu**; 1828 NE Ashberry Drive, Hillsboro, Oregon 97124 (US). **CHEAH, Bok Eng**; 1, Tingkat Pasir Belanda 4, Teluk Kumbar, Bayan Lepas, 11920 (MY). **KOH, Boon Ping**; 22, Lorong Sutera Prima 2, Taman Sutera Prima, Seberang Jaya, 13700 (MY). **TANG, Min Keen**; 7-9-3, Lavinia Apartment, Jalan Bukit Kecil 1, Taman Sri Nibong, 11900 (MY). **HECK, Howard L.**; 2969 NE 1st Ct., Hillsboro, Oregon 97124 (US). **OOI, Kooi Chi**; 96, Jalan Bunga Raya, Bukit Glugor, Glugor, 11700 (MY).

(74) **Agent**: **CAVEN, Jed W.**; Alpine Technology Law Group LLC, c/o CPA Global, 900 Second Avenue South, Suite 600, Minneapolis, Minnesota 55402 (US).

(81) **Designated States** *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) **Designated States** *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU,

[Continued on next page]

(54) **Title**: ELECTROSTATIC DISCHARGE FOR ELECTRONIC DEVICE COUPLING

(57) **Abstract**: In one example an electronic device comprises a housing, a receptacle in the housing comprising an opening at a distal end to receive a plug, a data connector positioned in the receptacle to provide a communication connection, and an electrostatic conductor assembly positioned proximate the opening in the receptacle, wherein the electrostatic conductor assembly comprises a dedicated discharge path and a conductive pin mounted on a retention latch and moveable between a first position in which the conductive pin is in electrical contact with the data connector and a second position in which the conductive pin is not in electrical contact with the data connector. Other examples may be described.

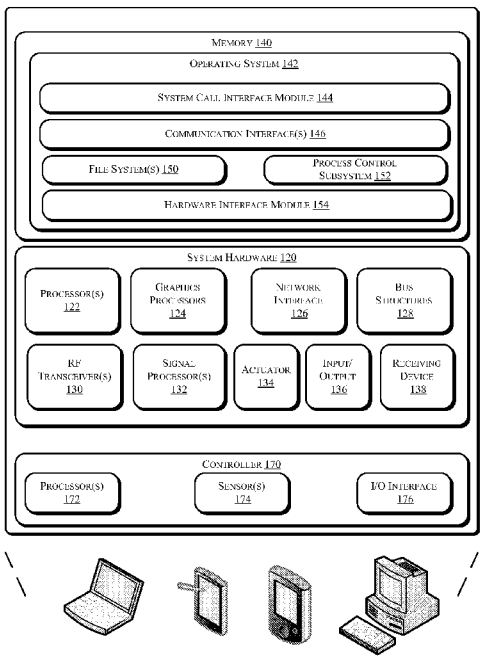

FIG. 1

ELECTRONIC DEVICE 100

WO 2016/209529 A1

TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

Published:

— *with international search report (Art. 21(3))*

ELECTROSTATIC DISCHARGE FOR ELECTRONIC DEVICE COUPLING

BACKGROUND

The subject matter described herein relates generally to the field of electronic devices and more particularly to an electrostatic discharge for electronic device coupling.

Electronic devices may be coupled to remote devices by a data connectors such as a universal serial bus (USB) connector, audiovisual (AV) connectors or Ethernet connectors. Static electricity may build up on the connector plug and, if discharged through a data connector, may present a risk to the electronic circuitry in the devices. Accordingly, electrostatic discharge techniques for electronic device couplings may find utility.

BRIEF DESCRIPTION OF THE DRAWINGS

The detailed description is described with reference to the accompanying figures.

Fig. 1 is a schematic illustration of an electronic device which may be adapted to implement electrostatic discharge in accordance with some examples.

Fig. 2 is a side view of a schematic illustration of a connector for an electronic device adapted to implement electrostatic discharge in accordance with some examples.

Fig. 3 is a perspective view of a schematic illustration of a connector for an electronic device adapted to implement electrostatic discharge in accordance with some examples.

Figs. 4A-4C are side views of a schematic illustration of a connector for an electronic device adapted to implement electrostatic discharge in accordance with some examples.

Fig. 5 is a side view schematic illustrations of examples of a connector for an electronic device adapted to implement electrostatic discharge in accordance with some examples.

Figs. 6-10 are schematic illustrations of electronic devices which may be adapted to implement electrostatic discharge in accordance with some examples.

DETAILED DESCRIPTION

Described herein are exemplary systems and methods to implement electrostatic discharge in electronic devices. In the following description, numerous specific details are set forth to provide a thorough understanding of various examples. However, it will be understood by those skilled in the art that the various examples may be practiced without the specific details. In other instances, well-known methods, procedures, components, and circuits have not been illustrated or described in detail so as not to obscure the particular examples.

As described above, it may be useful to provide techniques for electrostatic discharge in electrical connectors which may be used to couple components of an electronic device to an external device. For example, it may be useful to provide for electrostatic discharge in data connectors such as universal serial bus (USB) connectors, audiovisual (AV) connectors or Ethernet connectors such that electrostatic charges may be dissipated through an electrical discharge path that is removed from data pins on the connectors.

To address this issue, in some examples an electrical connector is provided with a receptacle comprising an opening at a distal end to receive a plug and an electrostatic conductor assembly positioned proximate the opening in the receptacle, wherein the electrostatic conductor assembly is coupled to a dedicated electrical discharge path. In further examples the electrical connector may be coupled to an input/output (I/O) interface of a component, which may be incorporated into an electronic device.

Additional features and operating characteristics of the electronic device and associated system are described below with reference to Figs. 1-10.

Fig. 1 is a schematic illustration of an electronic device which may be adapted to implement electrostatic discharge in accordance with some examples. In various examples, electronic device 100 may include or be coupled to one or more accompanying input/output devices including a display, one or more speakers, a keyboard, one or more other I/O device(s), a mouse, a camera, or the like. Other exemplary I/O device(s) may include a touch screen, a voice-activated input device, a track ball, a geolocation device, an accelerometer/gyroscope, biometric feature input devices, and any other device that allows the electronic device 100 to receive input from a user.

The electronic device 100 includes system hardware 120 and memory 140, which may be implemented as random access memory and/or read-only memory. A file store may be communicatively coupled to electronic device 100. The file store may be internal to electronic device 100 such as, *e.g.*, eMMC, SSD, one or more hard drives, or other types of storage devices. Alternatively, the file store may also be external to electronic device 100 such as, *e.g.*, one or more external hard drives, network attached storage, or a separate storage network.

System hardware 120 may include one or more processors 122, graphics processors 124, network interfaces 126, and bus structures 128. In one embodiment, processor 122 may be embodied as an Intel® Atom™ processors, Intel® Atom™ based System-on-a-Chip (SOC) or Intel ® Core2 Duo® or i3/i5/i7 series processor available from Intel Corporation, Santa Clara, California, USA. As used herein, the term "processor" means any type of computational element, such as but not limited to, a microprocessor, a microcontroller, a complex instruction set computing (CISC) microprocessor, a reduced instruction set (RISC) microprocessor, a very

long instruction word (VLIW) microprocessor, or any other type of processor or processing circuit.

Graphics processor(s) 124 may function as adjunct processor that manages graphics and/or video operations. Graphics processor(s) 124 may be integrated onto the motherboard of electronic device 100 or may be coupled via an expansion slot on the motherboard or may be located on the same die or same package as the Processing Unit.

In one embodiment, network interface 126 could be a wired interface such as an Ethernet interface (see, e.g., Institute of Electrical and Electronics Engineers/IEEE 802.3-2002) or a wireless interface such as an IEEE 802.11a, b or g-compliant interface (see, e.g., IEEE Standard for IT-Telecommunications and information exchange between systems LAN/MAN--Part II: Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) specifications Amendment 4: Further Higher Data Rate Extension in the 2.4 GHz Band, 802.11G-2003). Another example of a wireless interface would be a general packet radio service (GPRS) interface (see, e.g., Guidelines on GPRS Handset Requirements, Global System for Mobile Communications/GSM Association, Ver. 3.0.1, December 2002).

Bus structures 128 connect various components of system hardware 120. In one embodiment, bus structures 128 may be one or more of several types of bus structure(s) including a memory bus, a peripheral bus or external bus, and/or a local bus using any variety of available bus architectures including, but not limited to, 11-bit bus, Industrial Standard Architecture (ISA), Micro-Channel Architecture (MCA), Extended ISA (EISA), Intelligent Drive Electronics (IDE), VESA Local Bus (VLB), Peripheral Component Interconnect (PCI), Universal Serial Bus (USB), Advanced Graphics Port (AGP), Personal Computer Memory Card International Association bus (PCMCIA), and Small Computer Systems Interface (SCSI), a High Speed Synchronous Serial Interface (HSI), a Serial Low-power Inter-chip Media Bus (SLIMbus®), or the like.

Electronic device 100 may include an RF transceiver 130 to transceive RF signals, and a signal processing module 132 to process signals received by RF transceiver 130. RF transceiver may implement a local wireless connection via a protocol such as, e.g., Bluetooth or 802.11X. IEEE 802.11a, b or g-compliant interface (see, e.g., IEEE Standard for IT-Telecommunications and information exchange between systems LAN/MAN--Part II: Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) specifications Amendment 4: Further Higher Data Rate Extension in the 2.4 GHz Band, 802.11G-2003). Another example of a wireless interface would be a WCDMA, LTE, general packet radio service (GPRS) interface (see, e.g., Guidelines on GPRS Handset Requirements, Global System for Mobile Communications/GSM Association, Ver. 3.0.1, December 2002).

Electronic device 100 may further include one or more actuators 134 and one or more input/output interfaces 136 such as, e.g., a keypad and/or a display. In some examples electronic device 100 may not have a keypad and use the touch panel for input.

Electronic device 100 may further include at least one wireless power receiving device 138 to receive power via an electromagnetic coupling with a driven coil in a charging device. The wireless power receiving device 138 may comprise one or more coil(s) to receive power through an inductive coupling with a driven coil or coupling charge plate(s) to receive power through a capacitive coupling with a driven capacitor in the charging device.

Memory 140 may include an operating system 142 for managing operations of electronic device 100. In one embodiment, operating system 142 includes a hardware interface module 154 that provides an interface to system hardware 120. In addition, operating system 142 may include a file system 150 that manages files used in the operation of electronic device 100 and a process control subsystem 152 that manages processes executing on electronic device 100.

Operating system 142 may include (or manage) one or more communication interfaces 146 that may operate in conjunction with system hardware 120 to transceive data packets and/or data streams from a remote source. Operating system 142 may further include a system call interface module 144 that provides an interface between the operating system 142 and one or more application modules resident in memory 140. Operating system 142 may be embodied as a UNIX operating system or any derivative thereof (*e.g.*, Linux, Android, *etc.*) or as a Windows® brand operating system, or other operating systems.

In some examples an electronic device may include a controller 170, which may comprise one or more controllers that are separate from the primary execution environment. The separation may be physical in the sense that the controller may be implemented in controllers which are physically separate from the main processors. Alternatively, the trusted execution environment may logical in the sense that the controller may be hosted on same chip or chipset that hosts the main processors.

By way of example, in some examples the controller 170 may be implemented as an independent integrated circuit located on the motherboard of the electronic device 100, e.g., as a dedicated processor block on the same SOC die. In other examples the trusted execution engine may be implemented on a portion of the processor(s) 122 that is segregated from the rest of the processor(s) using hardware enforced mechanisms. In the embodiment depicted in Fig. 1 the controller 170 comprises a processor 172, a sensor 174, and an I/O interface 176.

One example of an electrical connector for an electronic device adapted to implement electrostatic discharge will be described with reference to Figs. 2-3, 4A-4C, and 5. While the connector depicted in Figs. 2-3, 4A-4C, and 5 is a USB connector, one skilled in the art will

recognized that the principles described herein are not limited to USB connectors, but are equally applicable to other connectors, e.g., audiovisual (AV) connectors or Ethernet connectors.

Referring to Figs. 2-3, 4A-4C, and 5, in one example an electrical connector 200 for an electronic device 100 comprises a receptacle 210 comprising an opening 220 at a distal end to receive a plug 260 (Figs. 4A-4C), a data connector 250 positioned in the receptacle 210 to provide a communication connection, and an electrostatic conductor assembly 230 comprising a dedicated discharge path 240 and a conductive pin 232 mounted on a retention latch 234 and moveable between a first position in which the conductive pin 232 is in electrical contact with the data connector 250 and a second position in which the conductive pin 232 is not in electrical contact with the data connector 250.

In the case of a USB connector as depicted in Figs. 2-3, 4A-4C, and 5, the receptacle 210 comprises a housing 212 which includes multiple interior surfaces 214 and which defines an opening 220 adapted to receive a plug 260 (Figs. 4A-4C). Similarly, plug 260 comprises a housing 262 which includes multiple exterior surfaces which define an opening 276 (Figs. 4A-4C).

The housing 212 encloses at least one data connector 250/252, and in the case of a USB connector comprises a plurality of data connectors 250/252. Similarly, the plug 260 includes at least one data connector 290/292, and in the case of a USB connector a plurality of data connectors 290/292. Further the opening 276 of the plug 260 is configured to receive the plurality of data connectors 250/252 in the receptacle 210 when the plug 260 in inserted into the receptacle 210, such that the plurality of data connectors 250/252 in the receptacle establish a data connection with the plurality of data connectors 290/292 in the plug 260 (Figs. 4A-4C).

The housing 212 further comprises a plurality of retention latches 234 formed on surfaces of the housing. In accordance with examples described herein, the receptacle 210 is provided with an electrostatic conductor assembly 230. In the example depicted in Figs. 2-3, 4A-4C, and 5 the electrostatic conductor assembly 230 comprises an array of conductive pins 232 positioned at least some of the retention latches 234. The conductive pins 232 are coupled to a dedicated discharge path 240 which is configured to conduct electrical charges away from the data connectors 250. In some examples the retention latch 234 is biased in a first direction such that the conductive pin 232 is in a first position in which the conductive pin 232 is in electrical contact with the data connector 250.

In some examples the conductive pins 232 are formed in the shape of at least one of a cone, a frustocone, or a dome to provide a shape which facilitate electrostatic discharge. However in other examples the respective electrostatic conductor assemblies 230 may be formed as a continuous line of conductive material (e.g., a metallic strip or the like).

Operation of the connector 200 will be explained with reference to Figs. 4A-4C. In the example depicted in Fig. 4A the plug 260 is disengaged from the receptacle 210. In use, a human hand or other mechanism inserts the plug 260 into the receptacle 210. In this position the retention latch 234 is biased in a first direction such that the conductive pin 232 is in a first position in which the conductive pin 232 is in electrical contact with the data connector 250. Referring to Fig. 4B, at the inception of the engagement between receptacle 210 and plug 260 the conductive pins 232 remain in the first position. Thus, any static electricity which may have accumulated on the plug 260 may be discharged via the dedicated discharge path(s) 240 rather than via the respective data connectors 250. Fig. 4C depicts the plug 260 inserted completely into receptacle 210. Note that the retention latch 234 is positioned such that inserting the plug 260 into the receptacle 210 moves the retention latch 234 from the first position to the second position, such that the conductive pin 232 is no longer in contact with the data connector 250.

Fig. 5 is a schematic illustration of an alternate connector 200 in accordance with examples described herein. Referring briefly to Fig. 5, one advantage of a connector constructed in accordance with principles described herein is that receptacle 210 maintains a dedicated discharge path even when the receptacle 210 is not connected to a plug 260. Thus, as illustrated in Fig. 5, in the event that an electrical charge is applied to the receptacle 210, e.g., via a electrostatic discharge from a user's hand or the like, the electrical charge may be discharged via the conductive pin 232 and discharge path 240, thereby preventing the electrical charge from damaging any circuitry 500 to which the data connector 250 is coupled.

As described above, in some examples the electronic device may be embodied as a computer system. Fig. 6 illustrates a block diagram of a computing system 600 in accordance with an example. The computing system 600 may include one or more central processing unit(s) 602 or processors that communicate via an interconnection network (or bus) 604. The processors 602 may include a general purpose processor, a network processor (that processes data communicated over a computer network 603), or other types of a processor (including a reduced instruction set computer (RISC) processor or a complex instruction set computer (CISC)). Moreover, the processors 602 may have a single or multiple core design. The processors 602 with a multiple core design may integrate different types of processor cores on the same integrated circuit (IC) die. Also, the processors 602 with a multiple core design may be implemented as symmetrical or asymmetrical multiprocessors. In an example, one or more of the processors 602 may be the same or similar to the processors 122 of Fig. 1.

A chipset 606 may also communicate with the interconnection network 604. The chipset 606 may include a memory control hub (MCH) 608. The MCH 608 may include a memory controller 610 that communicates with a memory 612 (which may be the same or similar to the

memory 140 of Fig. 1). The memory 612 may store data, including sequences of instructions, that may be executed by the processor 602, or any other device included in the computing system 600. In one example, the memory 612 may include one or more volatile storage (or memory) devices such as random access memory (RAM), dynamic RAM (DRAM), synchronous DRAM (SDRAM), static RAM (SRAM), or other types of storage devices. Nonvolatile memory may also be utilized such as a hard disk. Additional devices may communicate via the interconnection network 604, such as multiple processor(s) and/or multiple system memories.

The MCH 608 may also include a graphics interface 614 that communicates with a display device 616. In one example, the graphics interface 614 may communicate with the display device 616 via an accelerated graphics port (AGP). In an example, the display 616 (such as a flat panel display) may communicate with the graphics interface 614 through, for example, a signal converter that translates a digital representation of an image stored in a storage device such as video memory or system memory into display signals that are interpreted and displayed by the display 616. The display signals produced by the display device may pass through various control devices before being interpreted by and subsequently displayed on the display 616.

A hub interface 618 may allow the MCH 608 and an input/output control hub (ICH) 620 to communicate. The ICH 620 may provide an interface to I/O device(s) that communicate with the computing system 600. The ICH 620 may communicate with a bus 622 through a peripheral bridge (or controller) 624, such as a peripheral component interconnect (PCI) bridge, a universal serial bus (USB) controller, or other types of peripheral bridges or controllers. The bridge 624 may provide a data path between the processor 602 and peripheral devices. Other types of topologies may be utilized. Also, multiple buses may communicate with the ICH 620, e.g., through multiple bridges or controllers. Moreover, other peripherals in communication with the ICH 620 may include, in various examples, integrated drive electronics (IDE) or small computer system interface (SCSI) hard drive(s), USB port(s), a keyboard, a mouse, parallel port(s), serial port(s), floppy disk drive(s), digital output support (e.g., digital video interface (DVI)), or other devices.

The bus 622 may communicate with an audio device 626, one or more disk drive(s) 628, and a network interface device 630 (which is in communication with the computer network 603). Other devices may communicate via the bus 622. Also, various components (such as the network interface device 630) may communicate with the MCH 608 in some examples. In addition, the processor 602 and one or more other components discussed herein may be combined to form a single chip (e.g., to provide a System on Chip (SOC)). Furthermore, the graphics accelerator 616 may be included within the MCH 608 in other examples.

Furthermore, the computing system 600 may include volatile and/or nonvolatile memory (or storage). For example, nonvolatile memory may include one or more of the following: read-only memory (ROM), programmable ROM (PROM), erasable PROM (EPROM), electrically EPROM (EEPROM), a disk drive (e.g., 628), a floppy disk, a compact disk ROM (CD-ROM), a digital versatile disk (DVD), flash memory, a magneto-optical disk, or other types of nonvolatile machine-readable media that are capable of storing electronic data (e.g., including instructions).

Fig. 7 illustrates a block diagram of a computing system 700, according to an example. The system 700 may include one or more processors 702-1 through 702-N (generally referred to herein as "processors 702" or "processor 702"). The processors 702 may communicate via an interconnection network or bus 704. Each processor may include various components some of which are only discussed with reference to processor 702-1 for clarity. Accordingly, each of the remaining processors 702-2 through 702-N may include the same or similar components discussed with reference to the processor 702-1.

In an example, the processor 702-1 may include one or more processor cores 706-1 through 706-M (referred to herein as "cores 706" or more generally as "core 706"), a shared cache 708, a router 710, and/or a processor control logic or unit 720. The processor cores 706 may be implemented on a single integrated circuit (IC) chip. Moreover, the chip may include one or more shared and/or private caches (such as cache 708), buses or interconnections (such as a bus or interconnection network 712), memory controllers, or other components.

In one example, the router 710 may be used to communicate between various components of the processor 702-1 and/or system 700. Moreover, the processor 702-1 may include more than one router 710. Furthermore, the multitude of routers 710 may be in communication to enable data routing between various components inside or outside of the processor 702-1.

The shared cache 708 may store data (e.g., including instructions) that are utilized by one or more components of the processor 702-1, such as the cores 706. For example, the shared cache 708 may locally cache data stored in a memory 714 for faster access by components of the processor 702. In an example, the cache 708 may include a mid-level cache (such as a level 2 (L2), a level 3 (L3), a level 4 (L4), or other levels of cache), a last level cache (LLC), and/or combinations thereof. Moreover, various components of the processor 702-1 may communicate with the shared cache 708 directly, through a bus (e.g., the bus 712), and/or a memory controller or hub. As shown in Fig. 7, in some examples, one or more of the cores 706 may include a level 1 (L1) cache 716-1 (generally referred to herein as "L1 cache 716").

Fig. 8 illustrates a block diagram of portions of a processor core 706 and other components of a computing system, according to an example. In one example, the arrows shown in Fig. 8 illustrate the flow direction of instructions through the core 706. One or more processor cores

(such as the processor core 706) may be implemented on a single integrated circuit chip (or die) such as discussed with reference to Fig. 7. Moreover, the chip may include one or more shared and/or private caches (e.g., cache 708 of Fig. 7), interconnections (e.g., interconnections 704 and/or 712 of Fig. 7), control units, memory controllers, or other components.

As illustrated in Fig. 8, the processor core 706 may include a fetch unit 802 to fetch instructions (including instructions with conditional branches) for execution by the core 706. The instructions may be fetched from any storage devices such as the memory 714. The core 706 may also include a decode unit 804 to decode the fetched instruction. For instance, the decode unit 804 may decode the fetched instruction into a plurality of uops (micro-operations).

Additionally, the core 706 may include a schedule unit 806. The schedule unit 806 may perform various operations associated with storing decoded instructions (e.g., received from the decode unit 804) until the instructions are ready for dispatch, e.g., until all source values of a decoded instruction become available. In one example, the schedule unit 806 may schedule and/or issue (or dispatch) decoded instructions to an execution unit 808 for execution. The execution unit 808 may execute the dispatched instructions after they are decoded (e.g., by the decode unit 804) and dispatched (e.g., by the schedule unit 806). In an example, the execution unit 808 may include more than one execution unit. The execution unit 808 may also perform various arithmetic operations such as addition, subtraction, multiplication, and/or division, and may include one or more an arithmetic logic units (ALUs). In an example, a co-processor (not shown) may perform various arithmetic operations in conjunction with the execution unit 808.

Further, the execution unit 808 may execute instructions out-of-order. Hence, the processor core 706 may be an out-of-order processor core in one example. The core 706 may also include a retirement unit 810. The retirement unit 810 may retire executed instructions after they are committed. In an example, retirement of the executed instructions may result in processor state being committed from the execution of the instructions, physical registers used by the instructions being de-allocated, etc.

The core 706 may also include a bus unit 814 to enable communication between components of the processor core 706 and other components (such as the components discussed with reference to Fig. 8) via one or more buses (e.g., buses 704 and/or 712). The core 706 may also include one or more registers 816 to store data accessed by various components of the core 706 (such as values related to power consumption state settings).

Furthermore, even though Fig. 7 illustrates the control unit 720 to be coupled to the core 706 via interconnect 712, in various examples the control unit 720 may be located elsewhere such as inside the core 706, coupled to the core via bus 704, etc.

In some examples, one or more of the components discussed herein can be embodied as a System On Chip (SOC) device. Fig. 9 illustrates a block diagram of an SOC package in accordance with an example. As illustrated in Fig. 9, SOC 902 includes one or more processor cores 920, one or more graphics processor cores 930, an Input/Output (I/O) interface 940, and a memory controller 942. Various components of the SOC package 902 may be coupled to an interconnect or bus such as discussed herein with reference to the other figures. Also, the SOC package 902 may include more or less components, such as those discussed herein with reference to the other figures. Further, each component of the SOC package 902 may include one or more other components, e.g., as discussed with reference to the other figures herein. In one example, SOC package 902 (and its components) is provided on one or more Integrated Circuit (IC) die, e.g., which are packaged into a single semiconductor device.

As illustrated in Fig. 9, SOC package 902 is coupled to a memory 960 (which may be similar to or the same as memory discussed herein with reference to the other figures) via the memory controller 942. In an example, the memory 960 (or a portion of it) can be integrated on the SOC package 902.

The I/O interface 940 may be coupled to one or more I/O devices 970, e.g., via an interconnect and/or bus such as discussed herein with reference to other figures. I/O device(s) 970 may include one or more of a keyboard, a mouse, a touchpad, a display, an image/video capture device (such as a camera or camcorder/video recorder), a touch surface, a speaker, or the like.

Fig. 10 illustrates a computing system 1000 that is arranged in a point-to-point (PtP) configuration, according to an example. In particular, Fig. 10 shows a system where processors, memory, and input/output devices are interconnected by a number of point-to-point interfaces. The operations discussed with reference to Fig. 2 may be performed by one or more components of the system 1000.

As illustrated in Fig. 10, the system 1000 may include several processors, of which only two, processors 1002 and 1004 are shown for clarity. The processors 1002 and 1004 may each include a local memory controller hub (MCH) 1006 and 1008 to enable communication with memories 1010 and 1012.

In an example, the processors 1002 and 1004 may be one of the processors 702 discussed with reference to Fig. 7. The processors 1002 and 1004 may exchange data via a point-to-point (PtP) interface 1014 using PtP interface circuits 1016 and 1018, respectively. Also, the processors 1002 and 1004 may each exchange data with a chipset 1020 via individual PtP interfaces 1022 and 1024 using point-to-point interface circuits 1026, 1028, 1030, and 1032. The

chipset 1020 may further exchange data with a high-performance graphics circuit 1034 via a high-performance graphics interface 1036, e.g., using a PtP interface circuit 1037.

As shown in Fig. 10, one or more of the cores 106 and/or cache 108 may be located within the processors 1004. Other examples, however, may exist in other circuits, logic units, or devices within the system 1000 of Fig. 10. Furthermore, other examples may be distributed throughout several circuits, logic units, or devices illustrated in Fig. 10.

The chipset 1020 may communicate with a bus 1040 using a PtP interface circuit 1041. The bus 1040 may have one or more devices that communicate with it, such as a bus bridge 1042 and I/O devices 1043. Via a bus 1044, the bus bridge 1042 may communicate with other devices such as a keyboard/mouse 1045, communication devices 1046 (such as modems, network interface devices, or other communication devices that may communicate with the computer network 1003), audio I/O device, and/or a data storage device 1048. The data storage device 1048 (which may be a hard disk drive or a NAND flash based solid state drive) may store code 1049 that may be executed by the processors 1004.

The following pertain to further examples.

Example 1 is an electronic device comprising a receptacle comprising an opening at a distal end to receive a plug, a data connector positioned in the receptacle to provide a communication connection, and an electrostatic conductor assembly comprising a dedicated discharge path and a conductive pin mounted on a retention latch and moveable between a first position in which the conductive pin is in electrical contact with the data connector and a second position in which the conductive pin is not in electrical contact with the data connector.

In Example 2, the subject matter of Example 1 can optionally include an arrangement in which the receptacle comprises at least one of a power receptacle, a universal serial bus (USB) receptacle, an audio/visual (AV) receptacle, or an Ethernet receptacle.

In Example 3, the subject matter of any one of Examples 1–2 can optionally include an arrangement in which the electrostatic conductor assembly comprises an array of conductive pins mounted on an array of retention latches and moveable between a first position in which the conductive pins are in electrical contact with data connectors and a second position in which the conductive pins are not in electrical contact with data connectors.

In Example 4, the subject matter of any one of Examples 1–3 can optionally include an arrangement in which the retention latch is biased in a first direction such that the conductive pin is in the first position.

In Example 5, the subject matter of any one of Examples 1–4 can optionally include an arrangement in which the retention latch is positioned such that inserting the plug into the receptacle moves the retention latch from the first position to the second position.

In Example 6, the subject matter of any one of Examples 1–5 can optionally include an arrangement in which the conductive pins are formed in the shape of at least one of a cone, a frustocone, or a dome.

In Example 7, the subject matter of any one of Examples 1-6 can optionally include an arrangement in which the dedicated discharge path is configured to conduct electrical charges away from the data connector.

Example 8 is a component for an electronic device comprising an input/output interface, a receptacle comprising an opening at a distal end to receive a plug, a data connector positioned in the receptacle to provide a communication connection, and an electrostatic conductor assembly comprising a dedicated discharge path and a conductive pin mounted on a retention latch and moveable between a first position in which the conductive pin is in electrical contact with the data connector and a second position in which the conductive pin is not in electrical contact with the data connector.

In Example 9, the subject matter of Example 8 can optionally include an arrangement in which the receptacle comprises at least one of a power receptacle, a universal serial bus (USB) receptacle, an audio/visual (AV) receptacle, or an Ethernet receptacle.

In Example 10, the subject matter of any one of Examples 8-9 can optionally include an arrangement in which the electrostatic conductor assembly comprises an array of conductive pins mounted on an array of retention latches and moveable between a first position in which the conductive pins are in electrical contact with data connectors and a second position in which the conductive pins are not in electrical contact with data connectors

In Example 11, the subject matter of any one of Examples 8-10 can optionally include an arrangement in which the retention latch is biased in a first direction such that the conductive pin is in the first position.

In Example 12, the subject matter of any one of Examples 8-11 can optionally include an arrangement in which the retention latch is positioned such that inserting the plug into the receptacle moves the retention latch from the first position to the second position.

In Example 13, the subject matter of any one of Examples 8-11 can optionally include an arrangement in which the conductive pins are formed in the shape of at least one of a cone, a frustocone, or a dome.

In Example 14, the subject matter of any one of Examples 8-13 can optionally include an arrangement in which the dedicated discharge path is configured to conduct electrical charges away from the data connector.

Example 15 is an electrical connector, comprising a receptacle comprising an opening at a distal end to receive a plug, a data connector positioned in the receptacle to provide a

communication connection, and an electrostatic conductor assembly comprising a dedicated discharge path and a conductive pin mounted on a retention latch and moveable between a first position in which the conductive pin is in electrical contact with the data connector and a second position in which the conductive pin is not in electrical contact with the data connector.

In Example 16, the subject matter of Example 15 can optionally include an arrangement in which the receptacle comprises at least one of a power receptacle, a universal serial bus (USB) receptacle, an audio/visual (AV) receptacle, or an Ethernet receptacle.

In Example 17, the subject matter of any one of Examples 15-16 can optionally include an arrangement in which the electrostatic conductor assembly comprises an array of conductive pins mounted on an array of retention latches and moveable between a first position in which the conductive pins are in electrical contact with data connectors and a second position in which the conductive pins are not in electrical contact with data connectors.

In Example 18, the subject matter of any one of Examples 15-17 can optionally include an arrangement in which the retention latch is biased in a first direction such that the conductive pin is in the first position.

In Example 19, the subject matter of any one of Examples 15-18 can optionally include an arrangement in which the retention latch is positioned such that inserting the plug into the receptacle moves the retention latch from the first position to the second position.

In Example 20, the subject matter of any one of Examples 15-19 can optionally include an arrangement in which the conductive pins are formed in the shape of at least one of a cone, a frustocone, or a dome.

In Example 21, the subject matter of any one of Examples 15-20 can optionally include an arrangement in which the dedicated discharge path is configured to conduct electrical charges away from the data connector.

The terms “logic instructions” as referred to herein relates to expressions which may be understood by one or more machines for performing one or more logical operations. For example, logic instructions may comprise instructions which are interpretable by a processor compiler for executing one or more operations on one or more data objects. However, this is merely an example of machine-readable instructions and examples are not limited in this respect.

The terms "computer readable medium" as referred to herein relates to media capable of maintaining expressions which are perceivable by one or more machines. For example, a computer readable medium may comprise one or more storage devices for storing computer readable instructions or data. Such storage devices may comprise storage media such as, for example, optical, magnetic or semiconductor storage media. However, this is merely an example of a computer readable medium and examples are not limited in this respect.

The term "logic" as referred to herein relates to structure for performing one or more logical operations. For example, logic may comprise circuitry which provides one or more output signals based upon one or more input signals. Such circuitry may comprise a finite state machine which receives a digital input and provides a digital output, or circuitry which provides one or more analog output signals in response to one or more analog input signals. Such circuitry may be provided in an application specific integrated circuit (ASIC) or field programmable gate array (FPGA). Also, logic may comprise machine-readable instructions stored in a memory in combination with processing circuitry to execute such machine-readable instructions. However, these are merely examples of structures which may provide logic and examples are not limited in this respect.

Some of the methods described herein may be embodied as logic instructions on a computer-readable medium. When executed on a processor, the logic instructions cause a processor to be programmed as a special-purpose machine that implements the described methods. The processor, when configured by the logic instructions to execute the methods described herein, constitutes structure for performing the described methods. Alternatively, the methods described herein may be reduced to logic on, e.g., a field programmable gate array (FPGA), an application specific integrated circuit (ASIC) or the like.

In the description and claims, the terms coupled and connected, along with their derivatives, may be used. In particular examples, connected may be used to indicate that two or more elements are in direct physical or electrical contact with each other. Coupled may mean that two or more elements are in direct physical or electrical contact. However, coupled may also mean that two or more elements may not be in direct contact with each other, but yet may still cooperate or interact with each other.

Reference in the specification to "one example" or "some examples" means that a particular feature, structure, or characteristic described in connection with the example is included in at least an implementation. The appearances of the phrase "in one example" in various places in the specification may or may not be all referring to the same example.

Although examples have been described in language specific to structural features and/or methodological acts, it is to be understood that claimed subject matter may not be limited to the specific features or acts described. Rather, the specific features and acts are disclosed as sample forms of implementing the claimed subject matter.

CLAIMS

What is claimed is:

1. An electronic device, comprising:

a receptacle comprising an opening at a distal end to receive a plug;

a data connector positioned in the receptacle to provide a communication connection; and

an electrostatic conductor assembly comprising a dedicated discharge path and a conductive pin mounted on a retention latch and moveable between:

a first position in which the conductive pin is in electrical contact with the data connector; and

a second position in which the conductive pin is not in electrical contact with the data connector.

2. The electronic device of claim 1, wherein the receptacle comprises at least one of a power receptacle, a universal serial bus (USB) receptacle, an audio/visual (AV) receptacle, or an Ethernet receptacle .

3. The electronic device of claim 1, wherein the electrostatic conductor assembly comprises an array of conductive pins mounted on an array of retention latches and moveable between:

a first position in which the conductive pins are in electrical contact with data connectors; and

a second position in which the conductive pins are not in electrical contact with data connectors.

4. The electronic device of claim 1, wherein the retention latch is biased in a first direction such that the conductive pin is in the first position.

5. The electronic device of claim 4, wherein the retention latch is positioned such that inserting the plug into the receptacle moves the retention latch from the first position to the second position.

6. The electronic device of claim 1, wherein the conductive pin is formed in the shape of at least one of:

a cone;

a frustocone; or

a dome.

7. The electronic device of claim 1, wherein:

the dedicated discharge path is configured to conduct electrical charges away from the data connector.

8. A component for an electronic device, comprising:

an input/output interface;

a receptacle in the housing comprising an opening at a distal end to receive a plug;

a data connector positioned in the receptacle to provide a communication connection; and

an electrostatic conductor assembly positioned proximate the opening in the receptacle, wherein the electrostatic conductor assembly comprises a dedicated discharge path and a conductive pin mounted on a retention latch and moveable between:

a first position in which the conductive pin is in electrical contact with the data connector; and

a second position in which the conductive pin is not in electrical contact with the data connector.

9. The component of claim 8, wherein the receptacle comprises at least one of a power receptacle, a universal serial bus (USB) receptacle, an audio/visual (AV) receptacle, or an Ethernet receptacle .

10. The component of claim 8, wherein the electrostatic conductor assembly comprises an array of electrostatic conductor assemblies, each of which comprises a conductive pin mounted on a retention latch and moveable between:

a first position in which the conductive pin is in electrical contact with the data connector; and

a second position in which the conductive pin is not in electrical contact with the data connector.

11. The component of claim 8, wherein the retention latch is biased in a first direction such that the conductive pin is in the first position.

12. The component of claim 11, wherein the retention latch is positioned such that inserting the plug into the receptacle moves the retention latch from the first position to the second position.

13. The component of claim 8, wherein the conductive pin are formed in the shape of at least one of:

a cone;

a frustocone; or

a dome.

14. The component of claim 8, wherein:

the dedicated discharge path is configured to conduct electrical charges away from the data connector.

15. An electrical connector, comprising:

a receptacle in the housing comprising an opening at a distal end to receive a plug;

a data connector positioned in the receptacle to provide a communication connection; and

an electrostatic conductor assembly positioned proximate the opening in the receptacle, wherein the electrostatic conductor assembly comprises a dedicated discharge path and a conductive pin mounted on a retention latch and moveable between:

a first position in which the conductive pin is in electrical contact with the data connector; and

a second position in which the conductive pin is not in electrical contact with the data connector.

16. The electrical connector of claim 15, wherein the receptacle comprises at least one of a power receptacle, a universal serial bus (USB) receptacle, an audio/visual (AV) receptacle, or an Ethernet receptacle .

17. The electrical connector of claim 15, wherein the electrostatic conductor assembly comprises an array of electrostatic conductor assemblies, each of which comprises a conductive pin mounted on a retention latch and moveable between:

a first position in which the conductive pin is in electrical contact with the data connector; and

a second position in which the conductive pin is not in electrical contact with the data connector.

18. The electrical connector of claim 15, wherein the retention latch is biased in a first direction such that the conductive pin is in the first position.

19. The electrical connector of claim 18, wherein the retention latch is positioned such that inserting the plug into the receptacle moves the retention latch from the first position to the second position.

20. The electrical connector of claim 15, wherein the conductive pin are formed in the shape of at least one of:

a cone;

a frustocone; or

a dome.

21. The electrical connector of claim 15, wherein:

the dedicated discharge path is configured to conduct electrical charges away from the data connector.

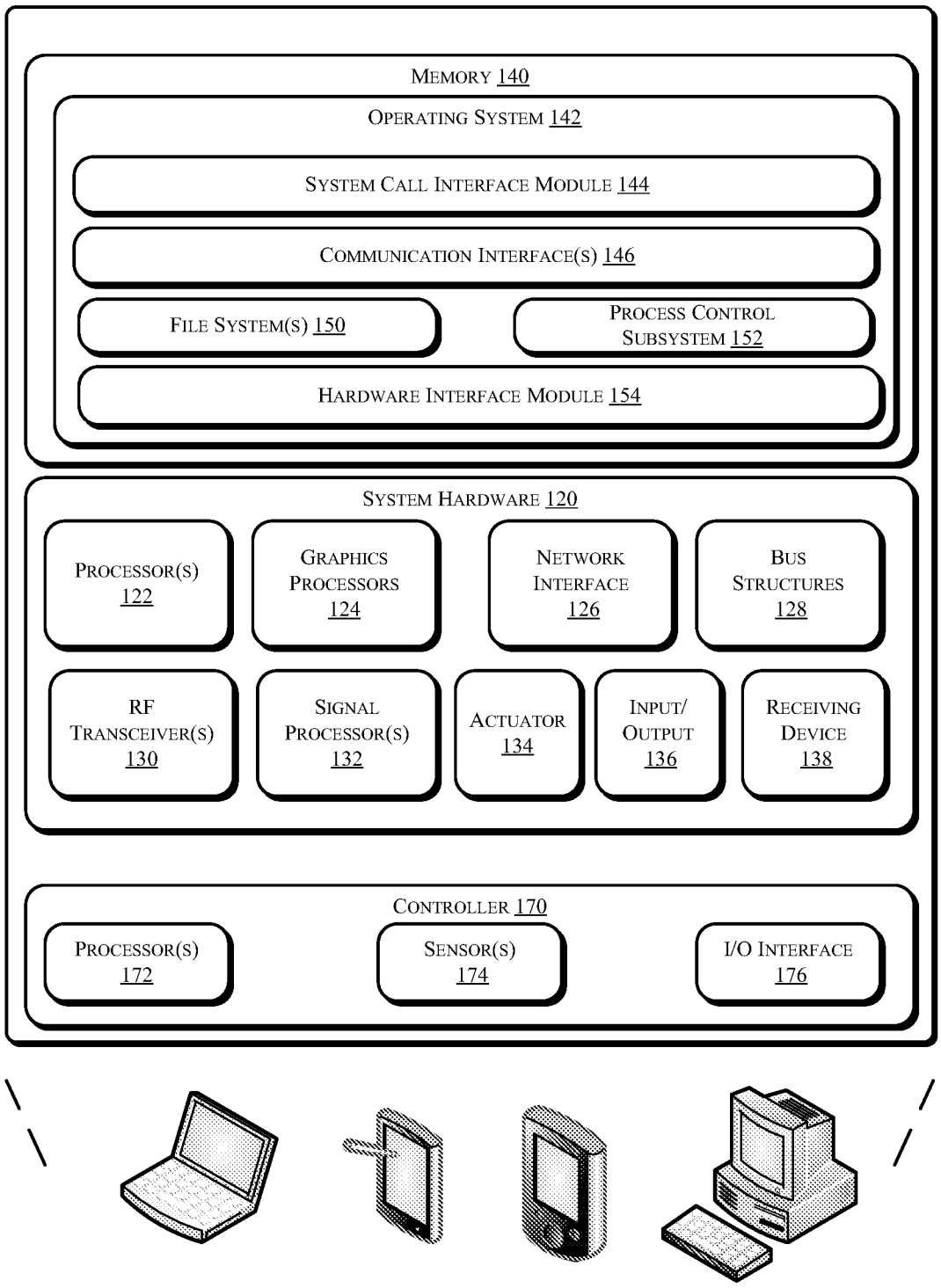

FIG. 1 ELECTRONIC DEVICE 100

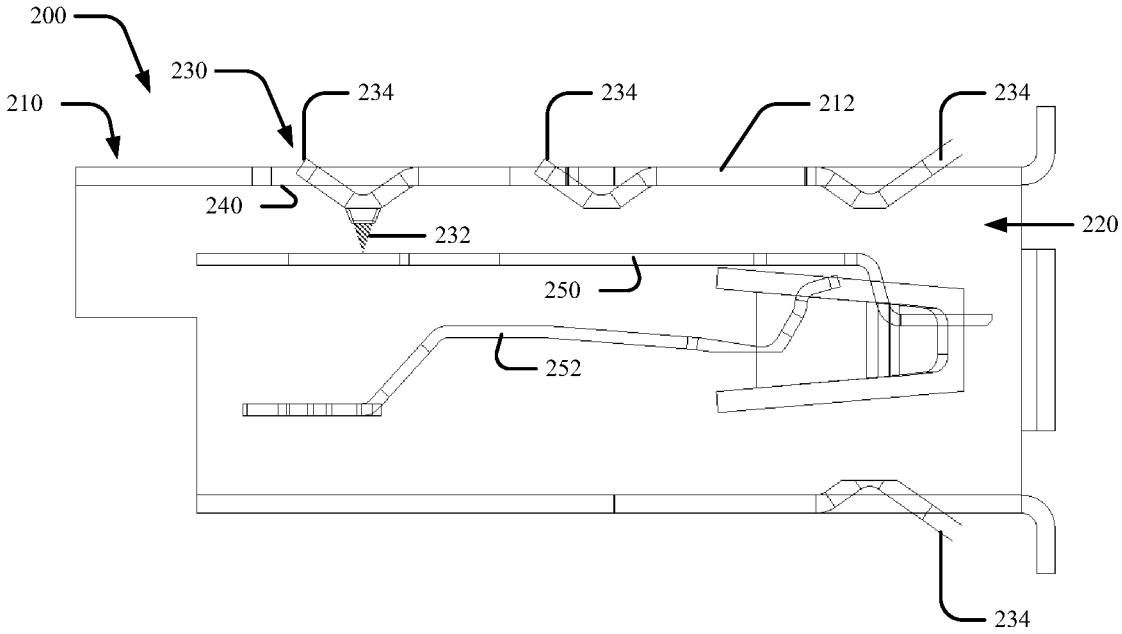
200
230
210
234
234
212
234
240
232
220
250
252
234

FIG. 2

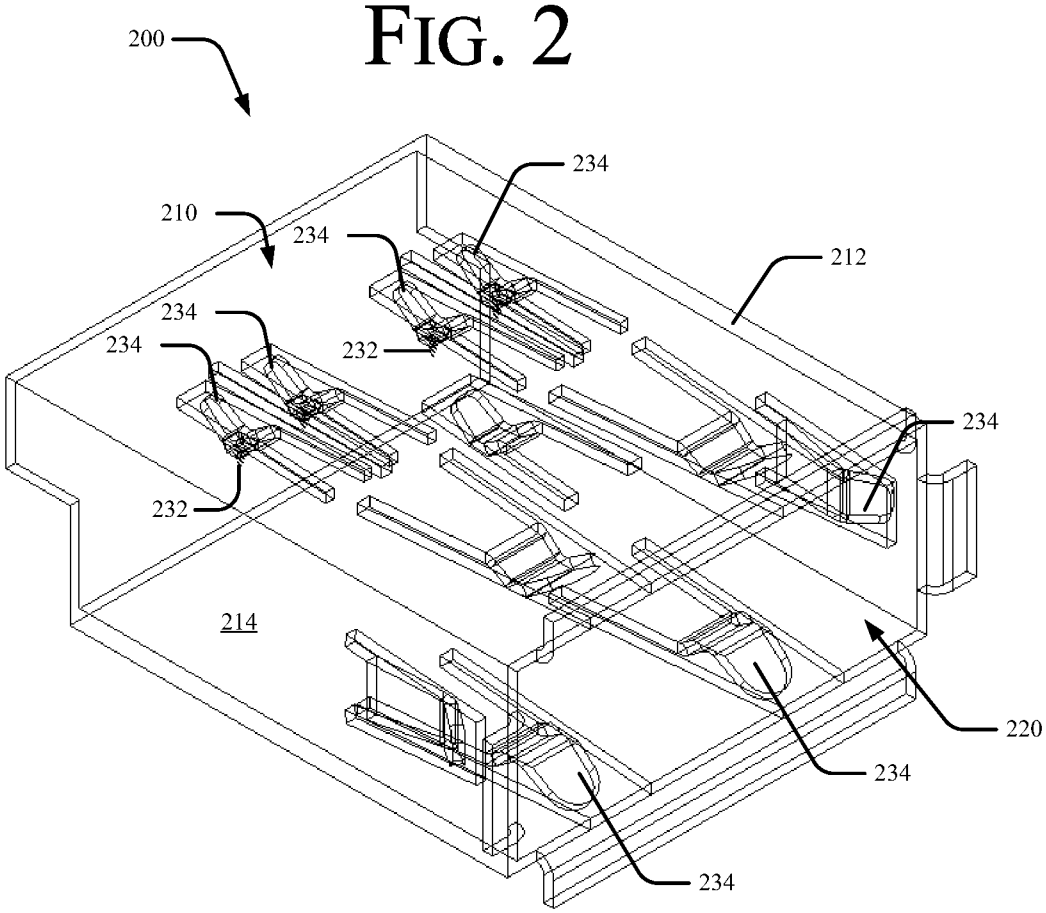
200
234
210
234
212
234
234
232
234
232
214
220
234
234

FIG. 3

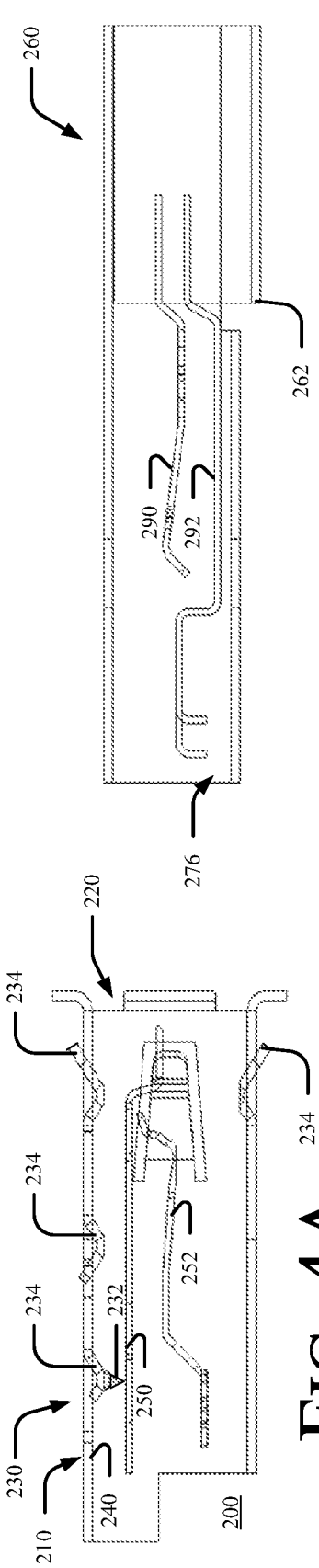

FIG. 4A

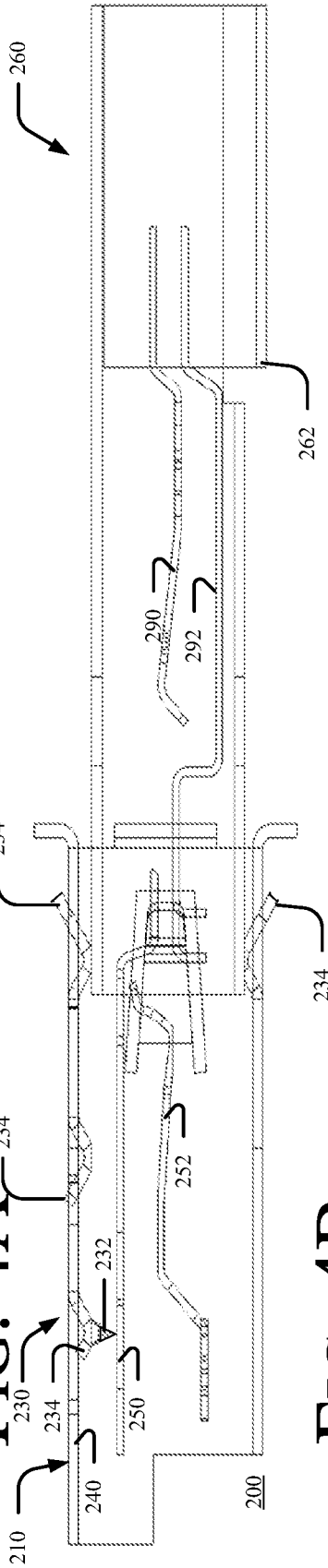

FIG. 4B

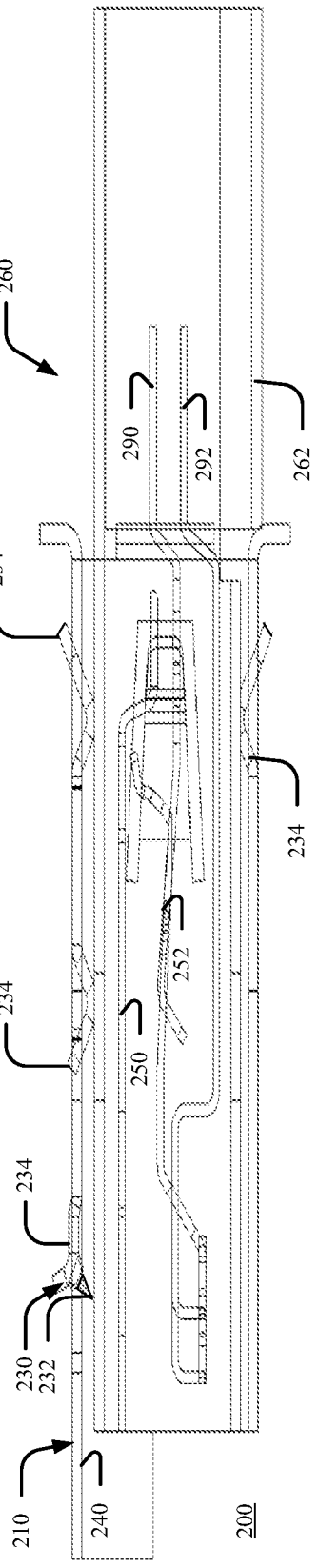

FIG. 4C

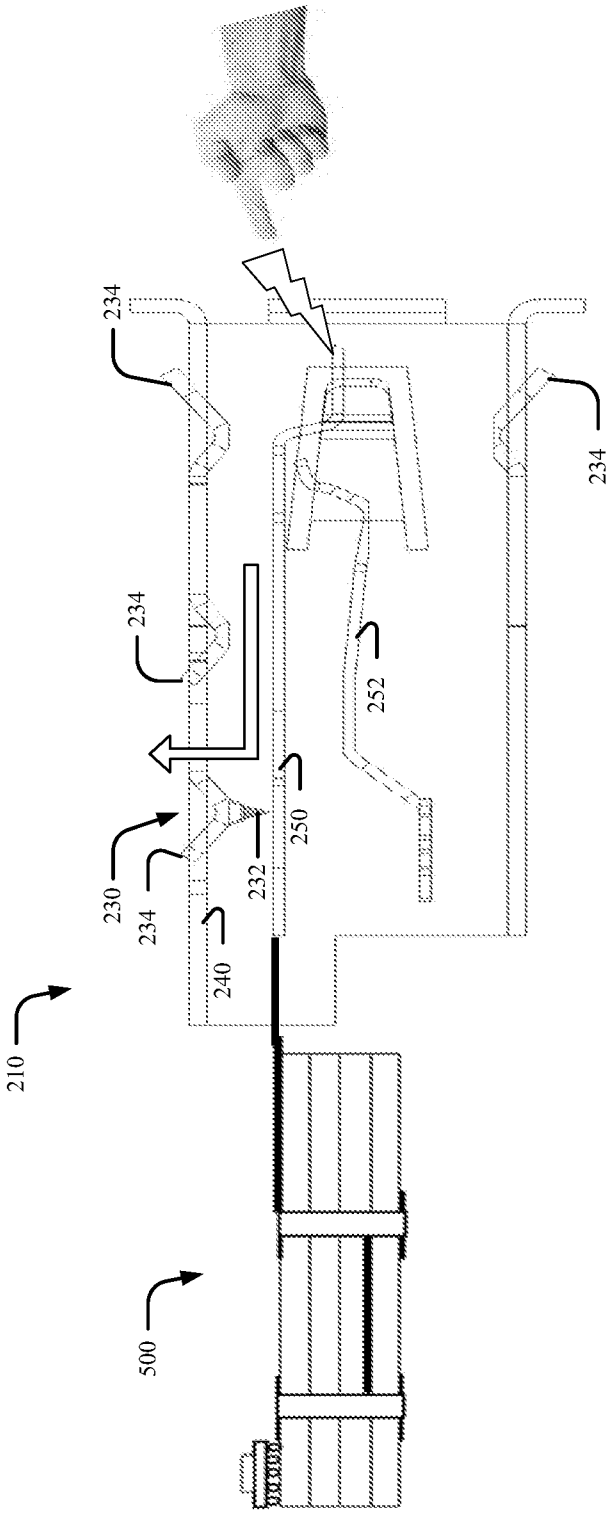

FIG. 5

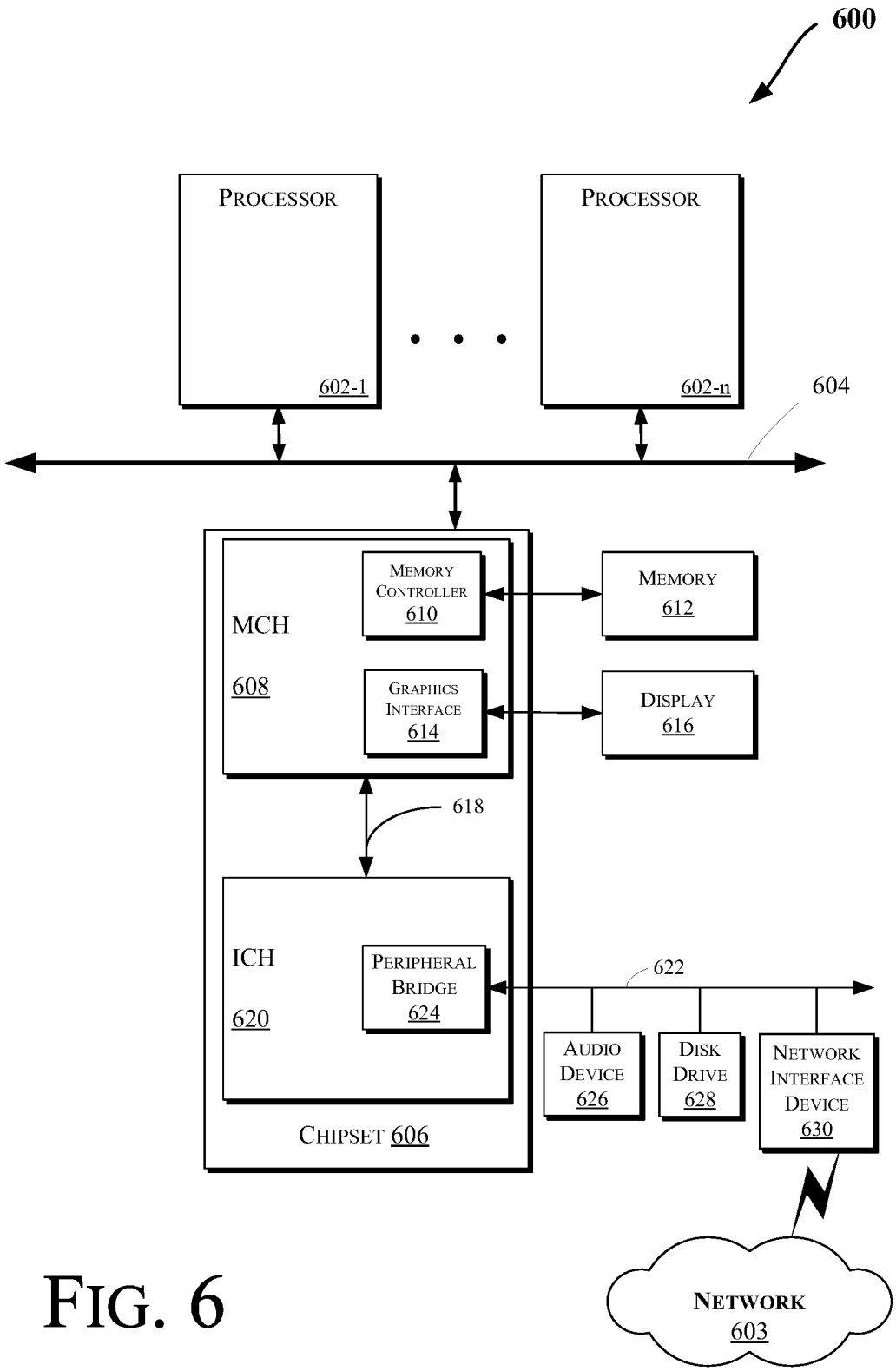
600
PROCESSOR
602-1
PROCESSOR
602-n
604
MCH
608
MEMORY CONTROLLER
610
GRAPHICS INTERFACE
614
MEMORY
612
DISPLAY
616
618
ICH
620
PERIPHERAL BRIDGE
624
622
AUDIO DEVICE
626
DISK DRIVE
628
NETWORK INTERFACE DEVICE
630
CHIPSET 606
NETWORK
603

FIG. 6

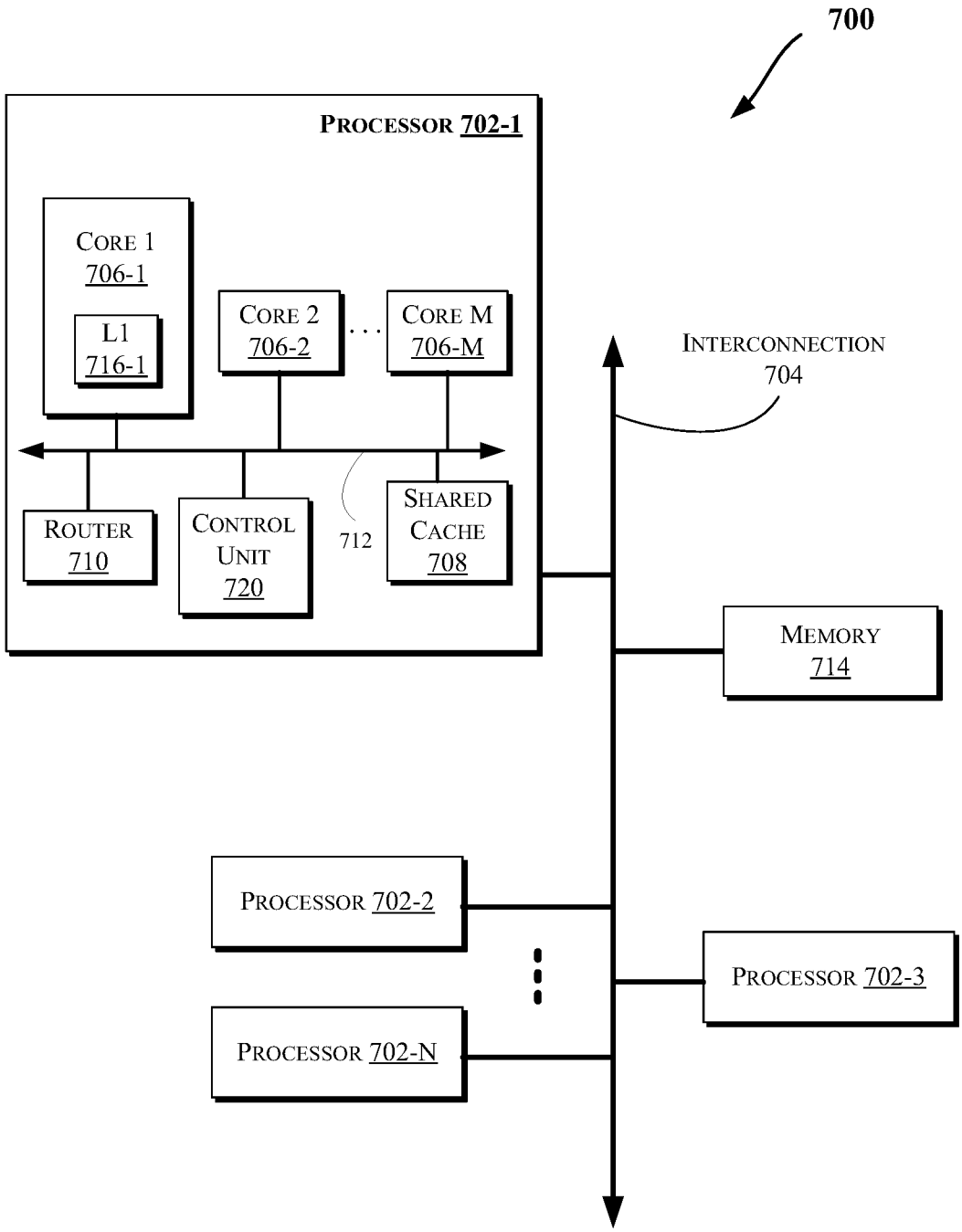
700
PROCESSOR 702-1
CORE 1
706-1
L1
716-1
CORE 2
706-2
CORE M
706-M
INTERCONNECTION
704
ROUTER
710
CONTROL
UNIT
720
712
SHARED
CACHE
708
MEMORY
714
PROCESSOR 702-2
PROCESSOR 702-3
PROCESSOR 702-N

FIG. 7

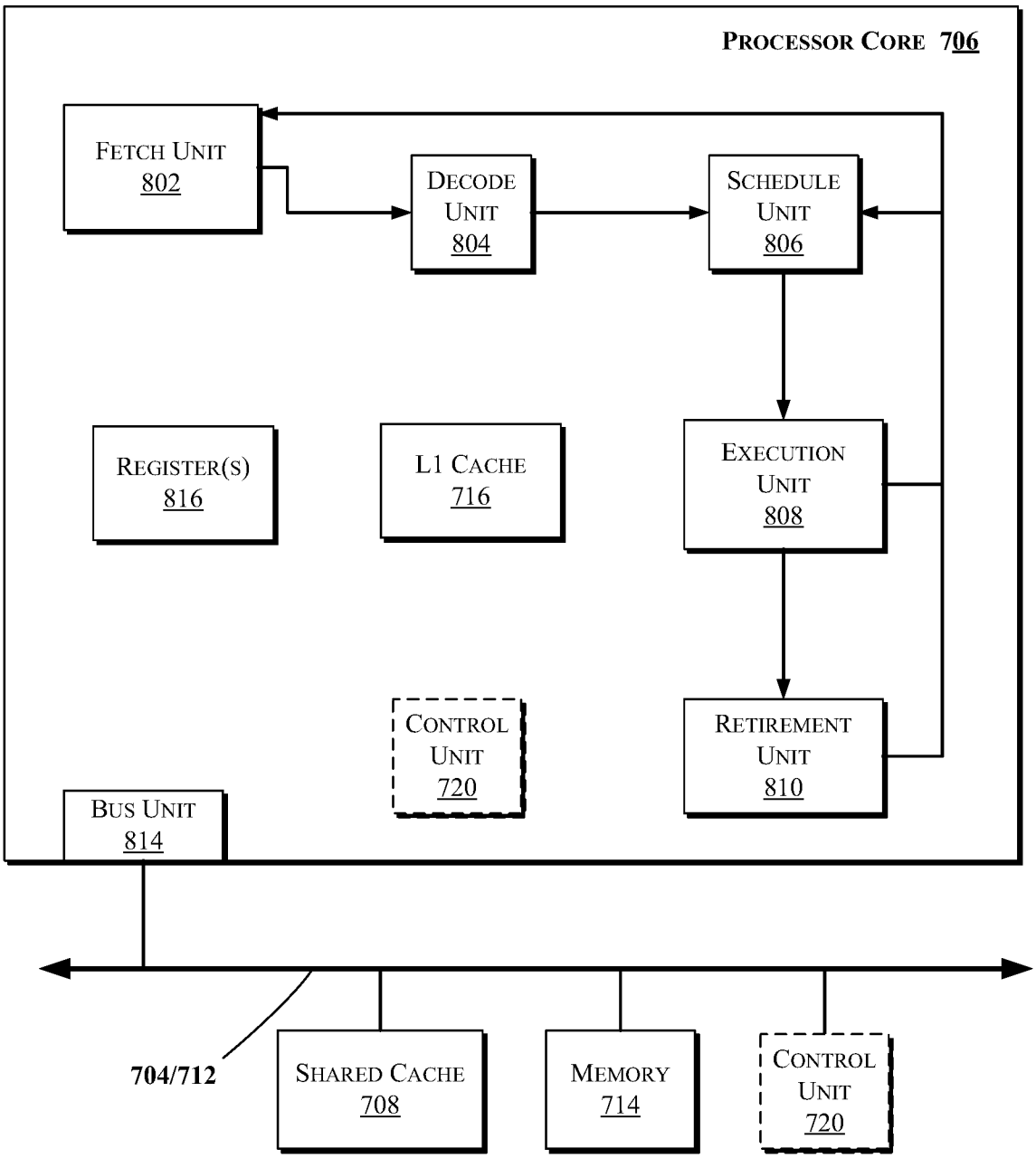
PROCESSOR CORE 706
FETCH UNIT 802
DECODE UNIT 804
SCHEDULE UNIT 806
REGISTER(S) 816
L1 CACHE 716
EXECUTION UNIT 808
CONTROL UNIT 720
RETIREMENT UNIT 810
BUS UNIT 814
704/712
SHARED CACHE 708
MEMORY 714
CONTROL UNIT 720

FIG. 8

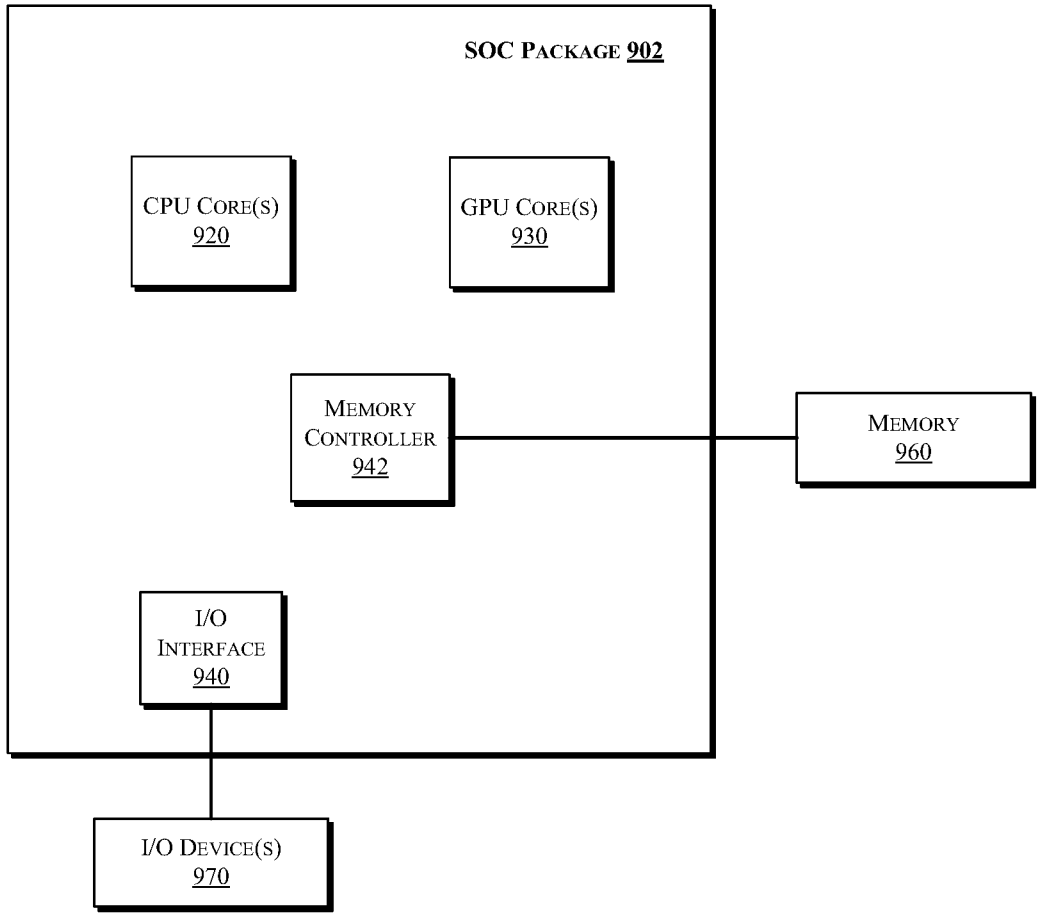
SOC PACKAGE 902
CPU CORE(S) 920
GPU CORE(S) 930
MEMORY CONTROLLER 942
MEMORY 960
I/O INTERFACE 940
I/O DEVICE(S) 970

FIG. 9

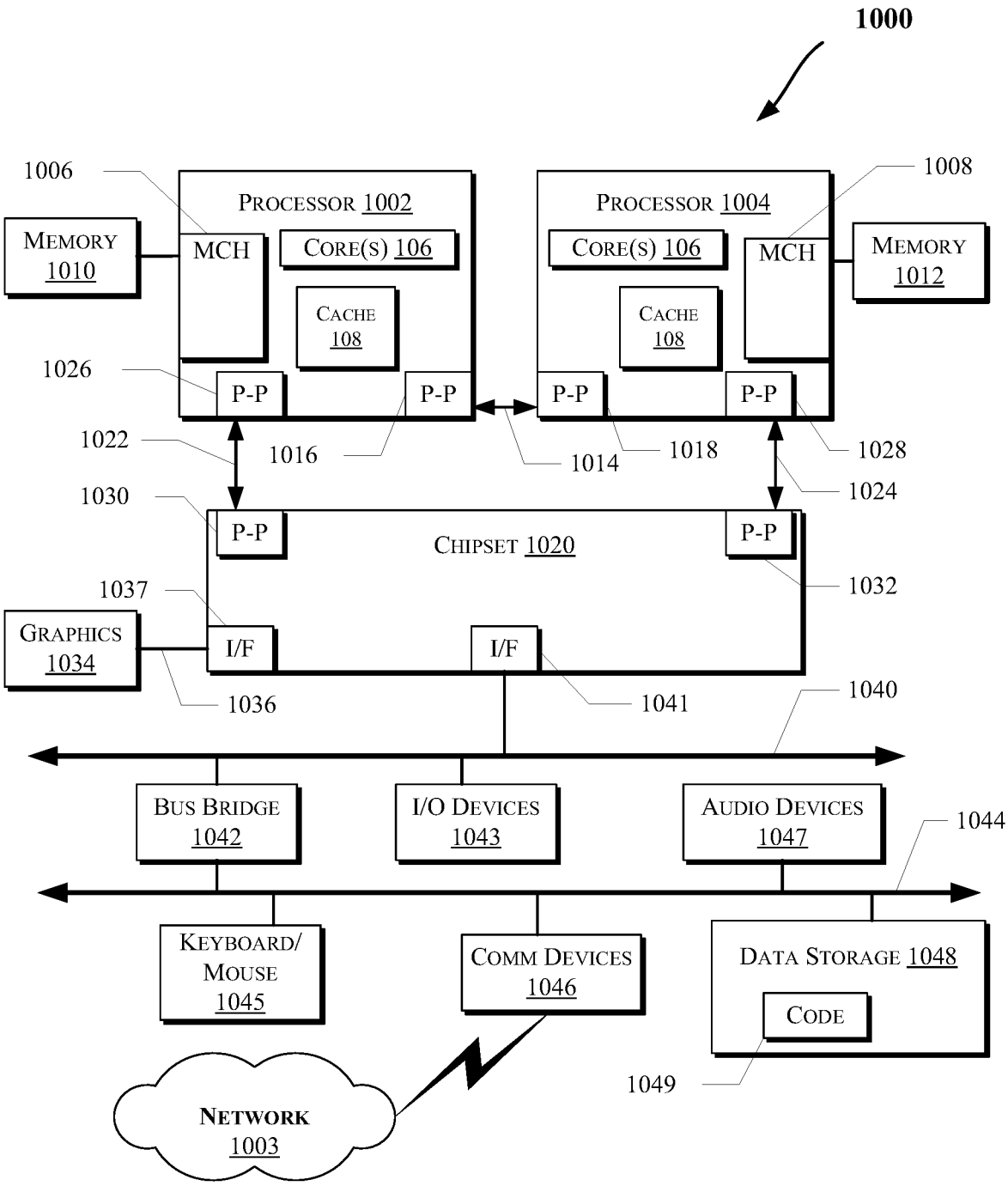
1000
1006
1008
PROCESSOR 1002
PROCESSOR 1004
MEMORY 1010
MCH
CORE(S) 106
CACHE 108
CORE(S) 106
MCH
MEMORY 1012
CACHE 108
1026
P-P
P-P
P-P
P-P
1022
1016
1014
1018
1028
1024
1030
P-P
CHIPSET 1020
P-P
1032
1037
GRAPHICS 1034
I/F
I/F
1036
1041
1040
BUS BRIDGE 1042
I/O DEVICES 1043
AUDIO DEVICES 1047
1044
KEYBOARD/ MOUSE 1045
COMM DEVICES 1046
DATA STORAGE 1048
CODE
1049
NETWORK 1003

FIG. 10

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2016/034343

A. CLASSIFICATION OF SUBJECT MATTER

H01R 13/648(2006.01)I, H01R 13/652(2006.01)I, H01R 13/22(2006.01)I

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01R 13/648; H03F 99/00; H01R 13/53; H01R 24/00; H01R 13/652; H01R 13/22

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords:receptacle, plug, data connector, electrostatic discharge, conductive pin

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2013-0225007 A1 (J. SCOTT SYLVESTER et al.) 29 August 2013 See paragraphs [0012]-[0034], claims 1, 17 and figures 1-2, 7.	1-21
A	JP 2009-110956 A (HON HAI PRECISION INDUSTRY CO., LTD.) 21 May 2009 See paragraphs [0008]-[0012], claim 1 and figures 1, 9.	1-21
A	US 2012-0099742 A1 (WOLFGANG EDELER) 26 April 2012 See paragraphs [0033]-[0043], claim 1 and figure 1.	1-21
A	US 2002-0151201 A1 (MICHEL BOHBOT) 17 October 2002 See paragraphs [0031]-[0032], claim 1 and figure 1.	1-21
A	US 2008-0081513 A1 (CORY A. CHAPMAN et al.) 03 April 2008 See paragraphs [0037]-[0039] and figure 9.	1-21

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
07 September 2016 (07.09.2016)	**12 September 2016 (12.09.2016)**

Name and mailing address of the ISA/KR
International Application Division
Korean Intellectual Property Office
189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea
Facsimile No. +82-42-481-8578

Authorized officer
KIM, Sung Gon
Telephone No. +82-42-481-8746

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2016/034343

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2013-0225007 A1	29/08/2013	US 8602801 B2	10/12/2013
JP 2009-110956 A	21/05/2009	CN 101499575 A	05/08/2009
		CN 101499575 B	03/10/2012
		CN 102790306 A	21/11/2012
		CN 102790306 B	03/12/2014
		JP 4943404 B2	30/05/2012
		TW 200919861 A	01/05/2009
		TW 201244294 A	01/11/2012
		TW I397220 B	21/05/2013
		TW I397221 B	21/05/2013
		US 7445505 B1	04/11/2008
US 2012-0099742 A1	26/04/2012	US 2014-0045354 A1	13/02/2014
		US 8771021 B2	08/07/2014
		US 8801443 B2	12/08/2014
US 2002-0151201 A1	17/10/2002	CA 2440817 A1	19/09/2002
		CA 2440817 C	22/09/2009
		EP 1371115 A2	17/12/2003
		US 6780035 B2	24/08/2004
		WO 02-073741 A2	19/09/2002
		WO 02-073741 A3	03/01/2003
US 2008-0081513 A1	03/04/2008	US 7597572 B2	06/10/2009