



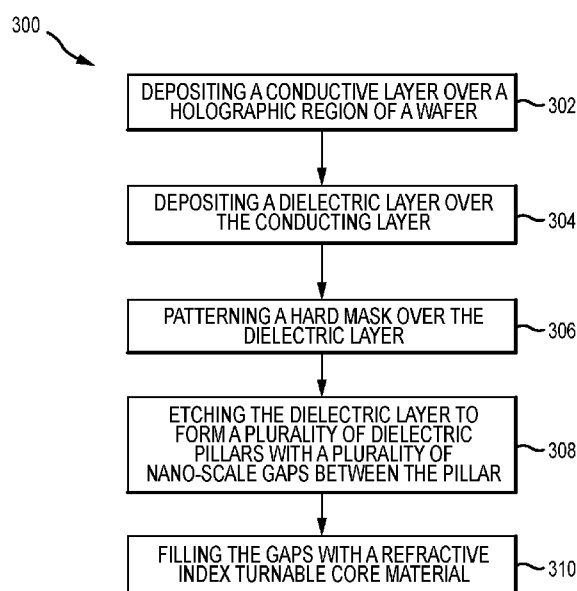
- (51) International Patent Classification:
G03F 7/20 (2006.01) *H01L 21/8238* (2006.01)
H01L 21/768 (2006.01)
- (21) International Application Number:
PCT/US2018/019269
- (22) International Filing Date:
22 February 2018 (22.02.2018)
- (25) Filing Language: English
- (26) Publication Language: English
- (30) Priority Data:
62/462,105 22 February 2017 (22.02.2017) US
15/799,654 31 October 2017 (31.10.2017) US
15/824,189 28 November 2017 (28.11.2017) US
15/824,893 28 November 2017 (28.11.2017) US
- (71) Applicant: **ELWHA LLC** [US/US]; 3150 139th Ave SE, Bldg 4, Bellevue, WA 98005 (US).
- (72) Inventors: **AKSELROD, Gleb, M.**; 10710 NE 10th St, Apt 304, Bellevue, WA 98004 (US). **JOSBERGER, Erik, Edward**; 2901 NE Blakeley St #328, Seattle, WA 98105 (US). **WEIDMAN, Mark, C.**; 11011 NE 9th St., Apt. 306, Bellevue, WA 98004 (US).

(74) Agent: **CHRISTENSEN, Kory**; Polsinelli LLP, Three Embarcadero Center, Suite 2400, San Francisco, CA 94111 (US).

(81) Designated States (*unless otherwise indicated, for every kind of national protection available*): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (*unless otherwise indicated, for every kind of regional protection available*): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

(54) Title: CONTROL CIRCUITRY AND FABRICATION TECHNIQUES OF OPTICAL METASURFACES



(57) Abstract: The method is provided for fabricating an optical metasurface. The method may include depositing a conductive layer over a holographic region of a wafer and depositing a dielectric layer over the conducting layer. The method may also include patterning a hard mask on the dielectric layer. The method may further include etching the dielectric layer to form a plurality of dielectric pillars with a plurality of nano-scale gaps between the pillars.

FIG.3

Published:

— *with international search report (Art. 21(3))*

CONTROL CIRCUITRY AND FABRICATION TECHNIQUES OF OPTICAL METASURFACES

CROSS-REFERENCE TO RELATED PATENT APPLICATION

[0001] The present application claims the benefit of the earliest available effective filing date(s) from the following listed application(s) (the “Priority Applications”), if any, listed below (e.g., claims earliest available priority dates for other than provisional patent applications, or claims benefits under 35 U.S.C. § 119(e) for provisional patent applications, for any and all parent, grandparent, great-grandparent, etc. applications of the Priority Application(s)).

Priority Applications:

[0002] The present application claims benefit of priority of United States Provisional Patent Application No. 62/462,105, entitled “Optical Surface Scattering Antennas,” filed on February 22, 2017, which was filed within the twelve months preceding the filing date of the present application or is an application of which a currently co-pending priority application is entitled to the benefit of the filing date.

[0003] The present application also claims benefit of priority of U.S. Patent Application No. 15/799,654, entitled “Fabrication of Optical Metasurfaces,” filed on October 31, 2017, which was filed within the twelve months preceding the filing date of the present application or is an application of which a currently co-pending priority application is entitled to the benefit of the filing date.

[0004] The present application also claims benefit of priority of U.S. Patent Application No. 15/824,189, entitled “Control Circuitry for 1D Optical Metasurfaces,” filed on November 28, 2017, was filed within the twelve months preceding the filing date of the present application or is an application of which a currently co-pending priority application is entitled to the benefit of the filing date.

[0005] The present application further claims benefit of priority of U.S. Patent Application No. 15/824,893, entitled “Control Circuitry for 2D Optical Metasurfaces,” filed on November 28, 2017, was filed within the twelve months preceding the filing date of the present application or is an application of which a currently co-pending priority application is entitled to the benefit of the filing date.

FIELD

[0006] The disclosure is directed to methods for fabrication of metasurfaces. In particular, the disclosure is directed to a combination of high resolution and low resolution processes for fabrication of metasurfaces including arrays of dielectric pillars with nano-scale gaps between the dielectric pillars. The fabrication process also includes filling the nano-scale gaps with a refractive index tunable core material.

BACKGROUND

[0007] Autonomous systems, such as vehicles, drones, robotics, security, mapping, among others, need to view the world in 3D. Scanning Light Detection and Ranging (Lidar) is the 3D sensor for self-driving cars. The current Lidar is unreliable, bulky and high cost. Lidar can also be used to make high-resolution maps and provides dynamic field of view.

[0008] Solid state Lidar uses chips and does not include moving parts and thus has high reliability. The solid state Lidar also uses low power, and small packages, and is able to use low cost CMOS fabrication technique. The solid state Lidar can have mass production. However, there still remains a need to develop techniques to produce solid-state Lidar.

BRIEF SUMMARY

[0009] In a first embodiment, a method is provided for fabricating an optical metasurface. The method may include depositing a conductive layer over a holographic region of a wafer and depositing a dielectric layer over the conducting layer. The method may also include patterning a hard mask on the dielectric layer. The method may further include etching the dielectric layer to form a plurality of dielectric pillars with a plurality of nano-scale gaps between the pillars.

[0010] In some embodiments, the patterning is performed by e-beam lithography.

[0011] In some embodiments, the patterning is performed by deep UV immersion lithography.

[0012] In some embodiments, the method may also include filling the plurality of nano-scale gaps with a refractive index tunable core material.

[0013] In some embodiments, the refractive index tunable core material comprises a liquid crystal or EO polymers.

[0014] In some embodiments, the step of filling the plurality of nano-scale gaps comprising preparing the surface to be hydrophobic or hydrophilic, spin coating the liquid crystal over the

plurality of pillars, filling the liquid crystal into the nano-scale gap by a capillary action, and encapsulating the liquid crystal with a clear coating.

[0015] In some embodiments, the step of filling the plurality of nano-scale gaps comprising applying a coating to a first portion of the plurality of nano-scale gaps, spin coating the liquid crystal onto the plurality of dielectric pillars, filling the liquid crystal into a second portion of the plurality of nano-scale gaps by a capillary action, and encapsulating the liquid crystal with a clear coating.

[0016] In some embodiments, the plurality of dielectric pillars comprises a constant gap between each of the pillars.

[0017] In some embodiments, the plurality of dielectric pillars comprises a plurality of pairs of dielectric pillars.

[0018] In some embodiments, the gap between each pair of pillars is smaller than the gap between two adjacent pairs of pillars.

[0019] In some embodiments, the plurality of dielectric pillars comprises amorphous silicon.

[0020] In some embodiments, the refractive index tunable core material comprises chalcogenide glass.

[0021] In some embodiments, the step of filling the plurality of nano-scale gaps comprising depositing the chalcogenide glass over the dielectric pillars by sputtering and removing the chalcogenide glass from all areas except inside the plurality of nano-scale gaps.

[0022] In some embodiments, the step of depositing a dielectric layer over a conducting layer comprising depositing an etch-stop dielectric layer over the conducting layer and depositing the dielectric layer over the etch-stop dielectric layer.

[0023] In some embodiments, the etch-stop dielectric layer comprises Al_2O_3 .

[0024] In some embodiments, the aspect ratio of height to width of the nano-scale gap is at least 5.

[0025] In some embodiments, the step of patterning a hard mask on the dielectric layer comprising depositing a hard mask over the dielectric layer, patterning the hard mask to remove a first portion of the hard mask near an interconnect region, patterning the hard mask by a high resolution process to form the nano-scale gap, and plasma etching the hard mask to remove a second portion of the hard mask in the nano-scale gap to expose the dielectric layer.

[0026] In some embodiments, the hard mask comprises Al_2O_3 .

[0027] In some embodiments, patterning the hard mask to remove a first portion of the hard mask near an interconnect region is performed by a low resolution process.

[0028] In some embodiments, the method may also include forming a plurality of conductive contacts over an interconnect region of the wafer for wire bonding to a CMOS. The plurality of conductive contacts is configured to apply voltage to the plurality of dielectric pillars.

[0029] In some embodiments, an optical metasurface is fabricated by any of the above methods of the first embodiment and its variations.

[0030] In a second embodiment, a method is provided for fabricating dielectric pillars having a nano-scale gap inbetween. The method may include depositing a dielectric layer over a conducting layer. The method may also include patterning a hard mask on the dielectric layer by a high resolution process. The method may further include applying a plasma to etch a portion of a dielectric layer at a temperature below room temperature in a chamber to form dielectric pillars with the nano-scale gap.

[0031] In some embodiments, the nano-scale gap has an aspect ratio of at least 5.

[0032] In some embodiments, the plasma comprises a mixture of gases.

[0033] In some embodiments, the mixture of gases comprises SF₆ gas for anisotropic etching.

[0034] In some embodiments, the mixture of gases comprises C₄F₈ gas for reducing the etching rate isotropically.

[0035] In some embodiments, the method may also include increasing the concentration of the C₄F₈ gas to reduce the undercut of the dielectric pillars.

[0036] In some embodiments, the method may also include decreasing the concentration of the C₄F₈ gas to reduce the sidewall angle of the dielectric pillars from the conducting layer.

[0037] In some embodiments, the sidewall angle ranges between 80° and 100°.

[0038] In some embodiments, the method may also include adjusting the pressure of the chamber to reduce the undercut of the dielectric pillars.

[0039] In some embodiments, the method may also include adjusting the power of the plasma to reduce the undercut of the dielectric pillars.

[0040] In some embodiments, the dielectric layer comprises amorphous silicon.

[0041] In some embodiments, the step of patterning a hard mask on the dielectric layer by a high resolution process comprising depositing a hard mask over the dielectric layer, patterning the hard mask by a low resolution process to remove a first portion of the mask near a wire contact region, patterning the hard mask to form the nano-scale gap by a high resolution process, and applying a plasma to etch the hard mask to remove a second portion of the hard mask in the nano-scale gap to expose the dielectric layer.

[0042] In some embodiments, the hard mask comprises Al₂O₃.

[0043] In some embodiments, the high resolution process comprises e-beam lithography.

[0044] In some embodiments, the high resolution process comprises deep UV immersion lithography.

[0045] In some embodiments, a plurality of dielectric pillars is fabricated by any of the methods of the second embodiment and its variations.

[0046] The disclosure is also directed to control circuitry for one dimensional metasurface array. In particular, the disclosure is directed to a hologram system including one or more hologram chip(s) and one or more control circuit chip(s). The disclosure also includes methods for forming the hologram chip(s) and methods for assembling the hologram chip(s) and the control circuit chip(s).

[0047] In an embodiment, a hologram system may include a hologram chip comprising a wafer substrate having a first plurality of conductive pads on a hologram surface region connected to a second plurality of conductive pads on an interconnect surface region. The hologram chip may also include an array of sub-wavelength hologram elements integrated with a refractive index tunable core material on the hologram region of the wafer substrate. The hologram system may also include a control circuit chip having a third plurality of conductive pads connected to the second plurality of conductive pads on the interconnect region of the wafer substrate. The interconnect region is on the same side of the wafer substrate as the hologram region. The first plurality of conductive pads is directly connected to the array of sub-wavelength hologram elements.

[0048] In some embodiments, the array of sub-wavelength hologram elements is a plurality of nano-walls arranged in a one-dimensional array, and the plurality of nano-walls is respectively coupled to the first plurality of conductive pads.

[0049] In some embodiments, the first plurality of conductive pads is connected to the second plurality of conductive pads by an interconnecting wire bus.

[0050] In some embodiments, the second plurality of conductive pads is connected to the third plurality of conductive pads via solder bumps.

[0051] In some embodiments, the chip is a CMOS chip.

[0052] In some embodiments, the wafer substrate includes silicon.

[0053] In some embodiments, each of the first, second, and third plurality of conductive pads includes a respective first, second, and third plurality of sub-group of conductive pads.

[0054] In some embodiments, the first plurality of sub-group of conductive pads is electrically connected to the second plurality of sub-group of conductive pads.

[0055] In some embodiments, the second plurality of sub-group of conductive pads is electrically connected to the third plurality of sub-group of conductive pads.

[0056] In an embodiment, a hologram system may include one or more hologram chips, each of the one or more hologram chips comprising an array of sub-wavelength hologram elements integrated with a refractive index tunable core material on a wafer substrate and a plurality of through-vias in the respective wafer substrates. The hologram system may also include an interposer positioned under the one or more hologram chips and electrically coupled to the one or more hologram chips. The hologram system may further include a control circuit chip disposed on the top of the interposer. The control circuit chip is electrically connected to the one or more arrays of sub-wavelength hologram elements through the respective plurality of through-vias in each of the one or more respective wafer substrates for the one or more hologram chips. Each of the one or more respective wafer substrates are positioned between the interposer and the one or more arrays of sub-wavelength holograph elements.

[0057] In some embodiments, the one or more respective wafer substrates include silicon.

[0058] In some embodiments, the one or more arrays of sub-wavelength hologram elements are aligned with each other.

[0059] In some embodiments, the one or more respective wafer substrates are in a square shape or a rectangular shape.

[0060] In some embodiments, the control circuit chip is a CMOS chip.

[0061] In some embodiments, the interposer includes a first plurality of conductive pads in a hologram region and a second plurality of conductive pads in an interconnect region. The first plurality of conductive pads is connected to the second plurality of pads in the interposer. The first plurality of conductive pads includes one or more subsets of conductive pads.

[0062] In some embodiments, each of the one or more hologram chips having a third plurality of conductive pads connected between the plurality of silicon through vias and the respective subset of the first plurality of conductive pads in the hologram region, such that one or more arrays of sub-wavelength hologram elements are electrically coupled to the plurality of conductive pads on the hologram region of the interposer.

[0063] In some embodiments, the second plurality of conductive pads on the interposer is connected to a fourth plurality of pads of the control circuit chip.

[0064] In some embodiments, the first plurality of conductive pads and second plurality of conductive pads are near the edge of the respective region of the interposer.

[0065] In some embodiments, the one or more arrays of sub-wavelength hologram elements include a plurality of nano-walls arranged in a one-dimensional array, and the plurality of nano-walls is respectively coupled to the first plurality of conductive pads.

[0066] In some embodiments, the first plurality of conductive pads is connected to the second plurality of conductive pads by an interconnecting wire bus.

[0067] In some embodiments, the second plurality of conductive pads is connected to the fourth plurality of conductive pads via solder bumps. The one or more subsets of first plurality of conductive pads are connected to the respective third plurality of conductive pads via solder bumps.

[0068] In an embodiment, a method is provided for fabricating a hologram chip suitable for bonding to a control circuit chip. The method may include fabricating a first plurality of conductive pads in a hologram region of a wafer substrate. The method may also include forming a second plurality of conductive pads in an interconnect region of the wafer substrate. The method may further include fabricating an interconnecting wire bus on the wafer substrate to connect the first plurality of conductive pads to the second plurality of conductive pads. The method may also include forming an array of sub-wavelength hologram elements over the wafer substrate in the hologram region such that the array of sub-wavelength hologram elements is respectively directly coupled to the first plurality of conductive pads. The sub-wavelength hologram elements are integrated with a refractive index tunable core material.

[0069] In some embodiments, the method may also include bonding a third plurality of conductive pads on the control circuit chip to the second plurality of conductive pads via solder bumps such that the control circuit chip connects to the hologram chip.

[0070] In an embodiment, a method is provided for assembling a hologram chip and a control circuit chip. The method may include providing a hologram chip having a wafer substrate having a first plurality of conductive pads in a hologram region and a second plurality of conductive pads in an interconnect region and an array of sub-wavelength hologram elements in the hologram region on the wafer substrate. The first plurality of conductive pads is electrically connected to the hologram elements. The method may also include flipping a control circuit chip having a third plurality of conductive pads such that the third plurality of conductive pads faces down. The method may further include bonding the second plurality of conductive pads in the interconnect region to the third plurality of conductive pads such that the control circuit chip is electrically connected to the hologram chip.

[0071] In some embodiments, the second plurality of conductive pads is electrically connected to the first plurality of conductive pads on the wafer substrate by an interconnecting wire bus on the wafer substrate.

[0072] In some embodiments, bonding the second plurality of conductive pads in the interconnect region to the third plurality of conductive pads includes bonding via solder bumps.

[0073] In some embodiments, the array of sub-wavelength hologram elements includes a plurality of nano-walls arranged in a one-dimensional array, and the plurality of nano-walls is respectively coupled to the first plurality of conductive pads.

[0074] In an embodiment, a method is provided for fabricating a hologram chip suitable for bonding to a control circuit chip. The method may include fabricating an array of sub-wavelength hologram elements on a first side of a wafer substrate. The method may also include forming through-silicon vias on the wafer substrate. The method may further include forming a first plurality of conductive pads on a second side of the wafer substrate. The sub-wavelength hologram elements are respectively coupled to the first plurality of conductive pads via the through-silicon vias. The sub-wavelength hologram elements are integrated with a refractive index tunable core material.

[0075] In some embodiments, the method may also include fabricating an interposer having a second plurality of conductive pads in a hologram region and a third plurality of conductive pads in an interconnect region. The second plurality of conductive pads is electrically connected to the third plurality of conductive pads via an interconnecting wire bus.

[0076] In some embodiments, the method may also include bonding the first plurality of conductive pads of each of the one or more hologram chips to the second plurality of conductive pads in the hologram region of the interposer via solder bumps such that the one or more hologram chips connect to the interposer.

[0077] In some embodiments, the method may also include bonding a fourth plurality of conductive pads of the control circuit chip to the third plurality of conductive pads in the interconnect region of the interposer via solder bumps such that the control circuit chip connects to the interposer.

[0078] In an embodiment, a method is provided for assembling a hologram system. The method may include providing one or more hologram chips, each of the one or more hologram chips comprising a wafer substrate having a plurality of through-silicon vias, an array of sub-wavelength hologram elements on a first side of the wafer substrate, and the plurality of

through-silicon vias connecting the sub-wavelength hologram elements to a first plurality of conductive pads on a second side of the wafer substrate. The method may also include providing an interposer having a second plurality of conductive pads in a hologram region and a third plurality of conductive pads in an interconnect region. The method may further include flipping a control circuit chip having a fourth plurality of conductive pads such that the fourth plurality of conductive pads faces down toward the third plurality of conductive pads. The method may also include connecting the arrays of hologram elements to the control circuit chip. The one or more arrays of sub-wavelength hologram elements are integrated with a refractive index tunable core material on the one or more substrates.

[0079] In some embodiments, connecting the arrays of hologram elements to the control circuit chip may include bonding the second plurality of conductive pads to the respective first plurality of conductive pads of the one or more hologram chips; and bonding the fourth plurality of conductive pads to the third plurality of conductive pads.

[0080] In some embodiments, bonding the first plurality of conductive pads to a respective subset of the second plurality of conductive pads in the hologram region may include bonding via solder bumps.

[0081] In some embodiments, bonding the fourth plurality of conductive pads to the third plurality of conductive pads in the interconnect region may include bonding via solder bumps.

[0082] In some embodiments, the one or more arrays of sub-wavelength hologram elements may include a plurality of nano-walls arranged in a one-dimensional array. The plurality of nano-walls is respectively coupled to the first plurality of conductive pads.

[0083] In some embodiments, the second plurality of conductive pads is electrically connected to the first plurality of conductive pads on the interposer by an interconnecting wire bus.

[0084] In an embodiment, a method is provided for fabricating a hologram system. The method may include (a) fabricating an array of sub-wavelength hologram elements on a first side of a wafer substrate. The method may also include (b) forming through-silicon vias on the wafer substrate. The method may further include (c) fabricating a first plurality of conductive pads on a second opposite side of the wafer substrate to form a first hologram chip and (d) bonding a second plurality of conductive pads on a first region of the control circuit chip to the first plurality of conductive pads of the first hologram chip such that the control circuit chip connects to the hologram elements of the first hologram chip. The sub-wavelength hologram elements are integrated with a refractive index tunable core material.

[0085] In some embodiments, bonding a second plurality of conductive pads on a first region of the control circuit chip to the first plurality of conductive pads of the first hologram chip is via solder bumps.

[0086] In some embodiments, the method may also include forming a second hologram chip by repeating steps (a) to (c). The method may further include bonding the second plurality of conductive pads on a second region of the control circuit chip to the first plurality of conductive pads of the second hologram chip such that the control circuit chip connects to the hologram elements of the second hologram chip. The sub-wavelength hologram elements are integrated with a refractive index tunable core material.

[0087] In some embodiments, bonding a second plurality of conductive pads on a second region of the control circuit chip to the first plurality of conductive pads of the second hologram chip is via solder bumps.

[0088] The disclosure is also directed to control circuitry or addressing schemes for 2D optical metasurfaces including a 2D array of hologram elements. In particular, the disclosure is directed to a hologram system including an active matrix addressing scheme or a passive matrix addressing scheme, depending upon the type of tunable core material used in the 2D optical metasurfaces. The disclosure also provides methods for operating the hologram systems. The disclosure also includes methods for fabricating the hologram system including a matrix control circuitry.

[0089] In an embodiment, a 2D hologram system with a matrix addressing scheme is provided. The system may include a 2D array of sub-wavelength hologram elements integrated with a refractive index tunable core material on a wafer substrate. The system may also include a matrix addressing scheme coupled to the 2D array of sub-wavelength hologram elements and configured to independently control each of the sub-wavelength hologram elements by applying a voltage.

[0090] In some embodiments, the system may also include an active matrix addressing scheme for controlling the 2D array of sub-wavelength hologram elements.

[0091] In some embodiments, the refractive index tunable core material includes EP polymer.

[0092] In some embodiments, the wafer substrate includes a matrix control circuitry having a 2D array of CMOS transistors.

[0093] In some embodiments, the 2D array of CMOS transistors includes metal-oxide-semiconductor field-effect transistors (MOSFETs).

[0094] In some embodiments, each of the 2D arrays of CMOS transistors has a Drain connected to each of the hologram elements.

[0095] In some embodiments, all Gates of each row of the 2D array of CMOS transistors are coupled together to a respective ROW line and all Sources of each column of CMOS transistors are coupled together to a respective COLUMN line.

[0096] In some embodiments, each ROW line is configured to digitally control each Gate of the CMOS transistors in the respective row to be “on” and “off”.

[0097] In some embodiments, each COLUMN line is configured to apply an analog voltage through each Source of the CMOS transistors in the column to each of the hologram elements when the Gate of the CMOS transistors is in an “on” state.

[0098] In some embodiments, the analog voltage ranges from -5 v to 5 v.

[0099] In some embodiments, each of the hologram elements includes two dielectric pillars and acts as a capacitor, at least one of the two dielectric pillars being grounded.

[00100] In some embodiments, the 2D array of sub-wavelength hologram elements is aligned with each other.

[00101] In some embodiments, the matrix addressing scheme includes a passive matrix addressing scheme for controlling the 2D array of sub-wavelength hologram elements.

[00102] In some embodiments, the wafer substrate includes silicon.

[00103] In some embodiments, the refractive index tunable core material includes liquid crystals or chalcogenide glasses.

[00104] In some embodiments, each of the hologram elements includes a first dielectric pillar and a second dielectric pillar. The tunable core material is positioned between the first and second dielectric pillars. Each hologram element acts as a capacitor.

[00105] In some embodiments, the first dielectric pillars of each row of the hologram elements are all connected to a ROW line applied with a first analog voltage, and the second dielectric pillars of each column of the hologram elements are all connected to a COLUMN line applied with a second analog voltage.

[00106] In some embodiments, a total analog voltage applied to each of the hologram elements is the sum of the first analog voltage and the second analog voltage.

[00107] In some embodiments, the total analog voltage has a refresh rate of at least 1 k Hz.

[00108] In some embodiments, each of the first analog voltage and the second analog voltage has a refresh rate of at least 1000 times higher than the relaxation rate of the refractive index tunable core material.

[00109] In some embodiments, the refractive index tunable core material in the hologram element has a long term memory such that the hologram element remains stable until a refreshed total analog voltage exceeds a previous value.

[00110] In some embodiments, each of the hologram elements is configured to switch to a different state by refreshing the first analog voltage and/or the second analog voltage.

[00111] In an embodiment, a method is provided for operating a 2D hologram system having a 2D array of hologram elements with a matrix addressing scheme. The method may include adjusting a binary voltage on a first row to change the first row from an “off” state to an “on” state. The method may also include applying a first analog voltage to a first column such that the first analog voltage is stored in a first hologram element in the first column and the first row. The method may further include changing the first row to an “off” state and adjusting a second row from an “off” state to an “on” state. The method may also include applying a second analog voltage to a second column such that the second analog voltage is stored in a second hologram element in the second column and the second row. Each of the 2D array of sub-wavelength hologram elements is integrated with a refractive index tunable core material on a wafer substrate comprising a matrix control circuitry having a 2D array of CMOS transistors.

[00112] In some embodiments, the refractive index tunable core material includes EP polymer.

[00113] In an embodiment, a method is provided for operating a hologram system having a 2D array of sub-wavelength hologram elements, with a passive matrix addressing scheme. The method may include applying a first analog voltage to a first ROW line. A first row of a 2D array of sub-wavelength hologram elements is coupled to the first ROW line. The method may also include applying a second analog voltage to a first COLUMN line. A first column of the 2D array of sub-wavelength hologram elements is coupled to the first COLUMN line. The method may further include applying a third analog voltage to the first ROW line or to the first COLUMN line in a refreshing time shorter than a relaxation time of a refractive index tunable core material integrated with a pair of dielectric pillars of each of the 2D array of sub-wavelength hologram elements. A first hologram element in the first row and the first column has a first total analog voltage equal to a sum of the first analog voltage and the second

analog voltage. A second total analog voltage is equal to the sum of the third analog voltage and the first or second analog voltage. If the second total analog voltage is smaller than the first total analog voltage, the state of the refractive index tunable core material of the first hologram element remains substantially constant, or if the second total analog voltage is greater than the first total analog voltage, the state of the refractive index tunable core material of the first hologram element is changed according to the second total analog voltage.

[00114] In some embodiments, the method may also include applying a fourth analog voltage to a second ROW line. A second row of the 2D array of sub-wavelength hologram elements is coupled to the second ROW line. The method may further include applying a fifth analog voltage to a second COLUMN line. A second column of the 2D array of sub-wavelength hologram elements is coupled to the second COLUMN line.

[00115] In some embodiments, the second hologram element has a total analog voltage equal to the sum of the fourth analog voltage and the fifth analog voltage, such that the second hologram element is independently controlled from the first hologram element.

[00116] In some embodiments, the refractive index tunable core material includes liquid crystals or chalcogenide glasses.

[00117] In an embodiment, a method is provided for fabricating a hologram system having a 2D array of hologram elements with a matrix addressing scheme. The method may include fabricating a matrix control circuitry having a 2D array of CMOS transistors over a wafer and forming metallic interconnects to the matrix control circuitry. The method may also include depositing an oxide layer over the metallic interconnects and planarizing the oxide layer. The method may further include disposing a reflector layer over planarized oxide layer and fabricating a 2D array of sub-wavelength hologram elements over the reflector layer. Each of the 2D array of sub-wavelength hologram elements includes a pair of dielectric pillars integrated with a refractive index tunable core material.

[00118] In some embodiments, the wafer includes silicon.

[00119] In some embodiments, the metallic interconnects include metal vias connecting between the sub-wavelength hologram elements and the respective CMOS transistors.

[00120] In some embodiments, the step of fabricating the 2D array of sub-wavelength hologram elements includes a high resolution nano-scale process.

[00121] In some embodiments, the step of fabricating the 2D array of sub-wavelength hologram elements includes filling a gap between the dielectric pillars with the refractive index tunable core material.

[00122] In some embodiments, the reflector layer is under the gap between the dielectric pillars and has a pitch smaller than a pitch of the hologram element.

[00123] In some embodiments, the step of planarizing the oxide layer includes chemical mechanical polishing.

[00124] In some embodiments, the step of depositing an oxide layer includes chemical vapor deposition.

[00125] Additional embodiments and features are set forth, in part, in the description that follows, and will become apparent to those skilled in the art upon examination of the specification or may be learned by the practice of the disclosed subject matter. A further understanding of the nature and advantages of the present disclosure may be realized by reference to the remaining portions of the specification and the drawings, which form a part of this disclosure.

BRIEF DESCRIPTION OF THE DRAWINGS

[00126] The description will be more fully understood with references to the following figures and data graphs, which are presented as various embodiments of the disclosure and should not be construed as a complete recitation of the scope of the disclosure, wherein:

[00127] FIG. 1A shows a top overview of a holographic metasurface device in accordance with embodiments of the disclosure.

[00128] FIG. 1B is a perspective view of a 1D holographic metasurface device in accordance with embodiments of the disclosure.

[00129] FIG. 1C is a perspective view of a 2D holographic metasurface device in accordance with embodiments of the disclosure.

[00130] FIG. 2A shows a side view of one sub-wavelength holographic element including a pair of a-Si pillars in the array of FIG. 1B or 1C in accordance with embodiments of the disclosure.

[00131] FIG. 2B shows a schematic of the 2D holographic metasurface including metal vias in accordance with embodiments of the disclosure.

[00132] FIG. 3 is a flow chart illustrating the steps of forming the 1D holographic metasurface in accordance with embodiments of the disclosure.

[00133] FIG. 4A shows the 1D metasurface before the integration of liquid crystals in accordance with embodiments of the disclosure.

[00134] FIG. 4B shows the 1D metasurface after the integration of liquid crystals in accordance with embodiments of the disclosure.

[00135] FIG. 5 shows a cross-sectional view of deposition of a conductive layer for wirebond on a first portion of a wafer in accordance with embodiments of the disclosure.

[00136] FIG. 6 shows a cross-sectional view of deposition of a conductive layer as a metallic reflector on a second portion of the wafer in accordance with embodiments of the disclosure.

[00137] FIG. 7 shows a cross-sectional view of plasma enhanced chemical vapor deposition (PECVD) of dielectric layer (e.g. SiO_2) over the conductive layers and etching the dielectric layer in accordance with embodiments of the disclosure.

[00138] FIG. 8 shows a cross-sectional view of PECVD and etching of the dielectric layer (e.g. SiO_2) after the step of FIG. 7 in accordance with embodiments of the disclosure.

[00139] FIG. 9 shows a cross-sectional view of PECVD of amorphous silicon after the step of FIG. 8 in accordance with embodiments of the disclosure.

[00140] FIG. 10 shows a cross-sectional view of deposition of a hard mask (e.g. Al_2O_3) after the step of FIG. 9 in accordance with embodiments of the disclosure.

[00141] FIG. 11 shows a cross-sectional view of e-beam lithography of resist (e.g. PMMA) after the step of FIG. 10 in accordance with embodiments of the disclosure.

[00142] FIG. 12 shows a cross-sectional view of etching of the hard mask (e.g. Al_2O_3) with a patterned resist (e.g. PMMA) to form a nano-scale gap in the hard mask after the step of FIG. 11 in accordance with embodiments of the disclosure.

[00143] FIG. 13 shows a cross-sectional view of stripping the patterned resist (e.g. PMMA) after the step of FIG. 12 in accordance with embodiments of the disclosure.

[00144] FIG. 14 shows a cross-sectional view of etching the a-Si layer with the patterned hard mask (e.g. Al_2O_3) to form a nano-scale gap of a high aspect ratio between the a-Si pillars in the a-Si layer and to expose the titanium layer after the step of FIG. 13 in accordance with embodiments of the disclosure.

[00145] FIG. 15 shows a cross-sectional view of wet etching the titanium adhesion layer to expose the conductive layer after the step of FIG. 14 in accordance with embodiments of the disclosure.

[00146] FIG. 16 shows a cross-sectional view of wire bonding to the conductive layer after the step of FIG. 15 in accordance with embodiments of the disclosure.

[00147] FIG. 17 shows a cross-sectional view of applying liquid crystal to fill the nano-scale gap between the a-Si pillars in the a-Si layer after the step of FIG. 16 in accordance with embodiments of the disclosure.

[00148] FIG. 18 shows the processing issues near an amorphous silicon pillar in accordance with embodiments of the disclosure.

[00149] FIG. 19 shows a cross-sectional view of a bus connection to a-Si pillars in accordance with embodiments of the disclosure.

[00150] FIG. 20A is a side view of a hologram system including a hologram chip and a control circuit chip (e.g. CMOS chip) on the same side of the hologram chip in accordance with embodiments of the disclosure.

[00151] FIG. 20B is a top view of the hologram system of FIG. 4A.

[00152] FIG. 21A is a side view of a hologram system including two or more hologram chips and two or more control circuit chips on the same side of the hologram chips in accordance with embodiments of the disclosure.

[00153] FIG. 21B is a top view of the hologram system of FIG. 5A.

[00154] FIG. 22 shows a side view of a hologram system including a hologram chip and a control circuit chip on an opposite side of the hologram elements in accordance with embodiments of the disclosure.

[00155] FIG. 23 shows a side view of a hologram system including two or more hologram chips and two or more control circuit chips on an opposite side of the hologram elements in accordance with embodiments of the disclosure.

[00156] FIG. 24 is a flow chart illustrating steps for fabricating a hologram system with a control circuit chip and a hologram chip on the same side of a wafer in accordance with embodiments of the disclosure.

[00157] FIG. 25 is a flow chart illustrating steps for fabricating a hologram system with a control circuit chip and two or more hologram chips on the same side of an interposer in accordance with embodiments of the disclosure.

[00158] FIG. 26 is a flow chart illustrating steps for fabricating a hologram system with a control circuit chip and a hologram chip on opposite sides of a wafer in accordance with embodiments of the disclosure.

[00159] FIG. 27 is a perspective view of a 2D hologram system in accordance with embodiments of the disclosure.

[00160] FIG. 28 shows a side view of one sub-wavelength hologram element of the 2D hologram system of FIG. 1 with a matrix control circuitry in accordance with embodiments of the disclosure.

[00161] FIG. 29 shows an active matrix addressing scheme for the 2D hologram system of FIG. 27 having the matrix control circuitry of FIG. 28 in accordance with embodiments of the disclosure.

[00162] FIG. 30 is a flow chart illustrating the steps for operating the 2D hologram system of FIG. 28 with the active matrix addressing scheme of FIG. 29 in accordance with embodiments of the disclosure.

[00163] FIG. 31 shows a passive matrix addressing scheme for the 2D hologram system of FIG. 27 without any matrix control circuitry in accordance with embodiments of the disclosure.

[00164] FIG. 32 illustrates a waveform of voltage vs time applied to a hologram element using the passive matrix addressing scheme of FIG. 30 in accordance with embodiments of the disclosure.

[00165] FIG. 33 is a flow chart illustrating the steps for operating the 2D hologram system of FIG. 27 with the passive matrix addressing scheme of FIG. 31 in accordance with embodiments of the disclosure.

[00166] FIG. 34 is a flow chart illustrating the steps for fabricating the hologram system including the active matrix control circuitry of FIG. 29 in accordance with embodiments of the disclosure.

DETAILED DESCRIPTION

[00167] The disclosure may be understood by reference to the following detailed description, taken in conjunction with the drawings as described below. It is noted that, for purposes of illustrative clarity, certain elements in various drawings may not be drawn to scale.

I. Overview-Fabrication of Optical Metasurfaces

[00168] The disclosure provides methods for fabricating a holographic metasurface device, which is operable at higher frequencies, especially at infrared or visible frequencies. When operating frequencies are scaled up to optical (infrared/visible) frequencies, the sizes of individual scattering elements and the spacing between adjacent scattering elements are proportionally scaled down to preserve the subwavelength/metamaterial aspect of the

technology. The relevant length scales for operation at optical frequencies are typically on the order of microns or less, which are smaller than the typical length scales for conventional printed circuit board (PCB) processes.

[00169] The methods include micro-lithographic processes, which are referred to a low resolution process for processing features larger than 1 μm . The disclosure also includes nano-lithographic processes for features as small as 50 nm, which are also referred to a high resolution process.

[00170] The disclosure also provides methods for etching the a-Si pillars below room temperature to reduce undercut, for example, less than 10 nm.

[00171] FIG. 1A shows a top overview of a holographic metasurface device in accordance with embodiments of the disclosure. As shown in FIG. 1A, a holographic metasurface device 100 has a holographic metasurface region 102, including an array of holographic elements on a first portion of a wafer 114, which can be seen in FIG. 1B or FIG. 1C. The holographic metasurface region 102 includes an array of hologram elements. Each holographic element includes a pair of dielectric pillars and a refractive index tunable core between the pair of dielectric pillars. The dielectric pillars may be formed of amorphous silicon (a-Si) or crystalline silicon.

[00172] The holographic metasurface device 100 may also have an interconnect region 104 including CMOS transistors on a second portion of the wafer. The CMOS transistors in the interconnect region 104 can control the voltage applied to the dielectric pillars of each of the holographic elements. The CMOS transistors have low static power consumption and high noise immunity. The array of holographic elements and the electrical control circuit are decoupled.

[00173] FIG. 1B is a perspective view of 1D holographic metasurface device in accordance with embodiments of the disclosure. As shown in FIG 1B, an array 102A includes a plurality of columns of holographic elements 106 arranged linearly on a wafer.

[00174] FIG. 1C is a perspective view of 2D holographic metasurface device in accordance with embodiments of the disclosure. As shown in FIG. 1C, an array 102B may also include a plurality of holographic elements 108 arranged in rows 110 and columns 112 on a wafer 114.

[00175] FIG. 2A shows a side view of one of the sub-wavelength holographic element including a pair of a-Si pillars in the array of FIG. 1B in accordance with embodiments of the disclosure. As depicted, a holographic element 200, e.g. a sub-wavelength metasurface

holographic element, includes a refractive index tunable material 204 between two dielectric pillars 202, such as a-Si pillars over a wafer 210. The wafer 210 may be a crystalline silicon wafer, among others. A control voltage 206 is applied across the two dielectric pillars 202. The electric and magnetic energy densities are across the holographic element 200. The dielectric pillars 202 are placed over an oxide layer 208, such as Al_2O_3 , which is an etch stop layer.

[00176] A metallic reflector 210 is placed between the wafer 210 and the oxide layer 206.

[00177] In some embodiments, the metal reflector 210 under the dielectric pillars 202, such as amorphous silicon (a-Si) pillars, may be made from copper, aluminum, or a CMOS-compatible metal, without sacrificing performance. The noble metals gold and silver are not CMOS-compatible.

[00178] The grazing incidence of the incident wave excites magnetic-like Mie resonances in the a-Si pillars with a high Q factor, enabling dynamic modulation of the phase. Additionally, the a-Si pillars are deposited over a metallic reflector, which makes the structure operate as a reflect-array and thus is possible to integrate with control electronics. The resonator includes two silicon sub-pillars that are separated by a tunable core material having a tunable refractive index.

[00179] Under the grazing incidence excitation, the electric field is strongly localized in the core between the pillars, while the magnetic field is strongly localized to the entire hologram element including the pillars and the core.

[00180] The reflection phase of the dielectric pillars is sensitive to the refractive index of the core material, with phase modulation of nearly 2π possible with an index modulation of $\Delta n/n$ of about 7%. The high sensitivity to the refractive index of the core material is enabled by the high Q of the resonance, for example, a Q of 64, which can be seen in a simulated reflection spectrum (not shown). The high sensitivity of the reflection phase to the refractive index of the core enables the integration of refractive index tunable core material into the Si pillars to create dynamic metasurfaces.

[00181] Since the refractive index modulation range of the tunable dielectric materials may be small, one challenge for designing an array of tunable radiating or scattering elements is to create a high Q factor, low-loss, subwavelength resonators. The Q factor is a dimensionless parameter that characterizes a resonator's bandwidth relative to its center frequency. High Q factor indicates a lower rate of energy loss relative to the stored energy of the resonator. Resonators with high Q factors have low damping.

Tunable Core Material

Liquid Crystal

[00182] Liquid crystals (LCs) exhibit anisotropy in the refractive index, which depends on molecular orientation of the liquid crystals. The refractive index of the liquid crystal can be controlled with an AC electric field. In the widely-used nematic liquid crystals, modulation between the extraordinary and ordinary refractive index can be up 13%, exceeding the performance of EO polymers.

[00183] In some embodiments, an LC material has a relatively high switching speed. The switching time of LCs can be significantly reduced in geometries with smaller electrode spacing and low viscosity LCs, such that microsecond switching times are possible in metasurface structures. The switching time can be further reduced by employing orthogonal electrodes. The high switching speed LCs may be suitable for scanning Light Detection and Ranging (Lidar) or computational imaging based on structured illumination where MHz speeds may be desired.

Electro-Optic Polymers

[00184] Electro-optic (EO) polymer materials exhibit a refractive index change based on second order polarizability, known as the Pockels Effect, where the index modulation is proportional to the applied static or RF electric field. The index modulation is given by:

$$\Delta n = \frac{1}{2} n^3 r_{33} E$$

where n is the linear refractive index, E is the applied electric field and r_{33} is the Pockels coefficient. The electric field is limited by a dielectric breakdown. The EO polymers can potentially achieve index modulation as large as 6%.

[00185] The response time of EO polymers is extremely fast (i.e. several fs), resulting in device modulation speeds of at least 40 GHz. Due to their large nonlinear coefficients, compared with crystalline electro-optic crystalline materials, such as lithium niobate, EO polymers promise compact modulators, enabling high-density photonic integrated circuits.

[00186] In some approaches, EO polymers may be suitable for applications where switching rates of MHz and GHz may be desired, such as Lidar single beam scanning and structured illumination, or free space optical communications with holograms that simultaneously perform beam forming and data encoding, thus allowing multi-user MIMO schemes.

Chalcogenide Glasses

[00187] Chalcogenide glasses have a unique structural phase transition from the crystalline phase to the amorphous phase—which have strikingly different electrical and optical properties—with refractive index modulation in the short wave infrared spectrum of about 30%. The phase transition is thermally induced, which is typically achieved through direct electrical heating of the chalcogenide glasses. A prototypical chalcogenide glass is $\text{Ge}_2\text{Sb}_2\text{Te}_5$ (GST), which becomes crystalline at about 200°C and can be switched back to the amorphous state with a melt-quenching temperature of about 500°C.

[00188] In addition to the large index modulation between the amorphous and crystalline states of about 30%, another attractive feature of the GST is that the material state can be maintained in the absence of any additional electrical stimulus. For this reason, GST is nearing commercialization as next-generation non-volatile electronic memory and has also been demonstrated as a constituent of all-optical memory.

[00189] In some embodiments, a chalcogenide glass material may be suitable for applications where it is desired to only occasionally reconfigure metasurfaces and yet provide good thermal stability and environmental stability. For example, in free space optical links, gradual drift of the transmitter or receiver may be compensated by low duty cycle changes to the beam pointing direction. At the same time, the large index modulation in these materials allows for the use of lower Q resonators, simplifying design and easing fabrication tolerances.

[00190] Turning to FIG. 2A again, as an example, the excitation is at 80° relative to normal and transverse magnetic (TM)polarized. The reflection phase is as a function of refractive index of the tunable core material. The reflection spectrum of a metasurface element shows a peak near a laser wavelength of 1550 nm. A Q factor for resonance may be 64. The voltage may vary from -5 v to 5 v. The silicon pillar is 480 nm high and 100 nm wide. The nano-scale gap between the two pillars is 60 nm. The pitch of the element is 400 nm. The Cu reflector is about 150 nm thick, and the oxide layer between the bottom of the pillars and the Cu reflector is about 25 nm thick.

[00191] In some embodiments, the nano-scale gap may vary from 75 nm to 200 nm. In some embodiments, the gap is equal to or greater than 75 nm. In some embodiments, the gap is equal to or greater than 100 nm. In some embodiments, the gap is equal to or greater than 125 nm. In some embodiments, the gap is equal to or greater than 150 nm. In some embodiments, the gap is equal to or greater than 175 nm. In some embodiments, the gap is equal to or less

than 200 nm. In some embodiments, the gap is equal to or less than 175 nm. In some embodiments, the gap is equal to or less than 150 nm. In some embodiments, the gap is equal to or less than 125 nm. In some embodiments, the gap is equal to or less than 100 nm.

[00192] In some embodiments, the pitch of the element may vary from 200 nm to 1.6 μm . In some embodiments, the pitch is equal to or greater than 200 nm. In some embodiments, the pitch is equal to or greater than 400 nm. In some embodiments, the pitch is equal to or greater than 600 nm. In some embodiments, the pitch is equal to or greater than 800 nm. In some embodiments, the pitch is equal to or greater than 1.0 μm . In some embodiments, the pitch is equal to or greater than 1.2 μm . In some embodiments, the pitch is equal to or greater than 1.4 μm . In some embodiments, the pitch is equal to or less than 1.6 μm . In some embodiments, the pitch is equal to or less than 1.4 μm . In some embodiments, the pitch is equal to or less than 1.2 μm . In some embodiments, the pitch is equal to or less than 1.0 μm . In some embodiments, the pitch is equal to or less than 800 nm. In some embodiments, the pitch is equal to or less than 600 nm. In some embodiments, the pitch is equal to or less than 400 nm.

[00193] In some embodiments, the depth of the pillars may range from 50 nm to 50 μm . In some embodiments, the depth is equal to or greater than 50 nm. In some embodiments, the depth is equal to or greater than 100 nm. In some embodiments, the depth is equal to or greater than 150 nm. In some embodiments, the depth is equal to or greater than 200 nm. In some embodiments, the depth is equal to or greater than 400 nm. In some embodiments, the depth is equal to or greater than 600 nm. In some embodiments, the depth is equal to or greater than 800 nm. In some embodiments, the depth is equal to or greater than 1.0 μm . In some embodiments, the depth is equal to or greater than 10 μm . In some embodiments, the depth is equal to or greater than 20 μm . In some embodiments, the depth is equal to or greater than 30 μm . In some embodiments, the depth is equal to or greater than 40 μm .

[00194] In some embodiments, the depth is equal to or less than 50 μm . In some embodiments, the depth is equal to or less than 40 μm . In some embodiments, the depth is equal to or less than 30 μm . In some embodiments, the depth is equal to or less than 20 μm . In some embodiments, the depth is equal to or less than 10 μm . In some embodiments, the depth is equal to or less than 1 μm . In some embodiments, the depth is equal to or less than 800 nm. In some embodiments, the depth is equal to or less than 600 nm. In some embodiments, the depth is equal to or less than 400 nm. In some embodiments, the depth is equal to or less than 200 nm. In some embodiments, the depth is equal to or less than 150 nm. In some embodiments, the depth is equal to or less than 100 nm.

[00195] In some embodiments, the width of the pillars may range from 50 nm to 1 μ m.

[00196] FIG. 2B shows a schematic of the 2D holographic metasurface including metal vias in accordance with embodiments of the disclosure. As shown, the dielectric pillars have an extension parallel to the wafer. The extension of each sub-pillar 202 is connected to a metal via 220.

Processes

[00197] The disclosure provides a process suitable for large-scale commercial fabrication. The dielectric pillars, such as amorphous silicon (a-Si) or poly-crystalline silicon, may be deposited by using plasma-enhanced chemical vapor deposition (PECVD) or CVD.

[00198] The nano-scale gaps between the dielectric pillars may be formed by etching using either electron beam lithography, for smaller production volumes (e.g. prototyping), or with deep UV immersion lithography, for large production volumes.

[00199] The complementary metal-oxide-semiconductor (CMOS) transistors can be fabricated on a wafer, such as a crystalline silicon wafer. Then, the CMOS transistors can be connected through metal vias to the dielectric pillars for applying a voltage to each pair of pillars, which acts as a capacitor. The metal vias can be planarized with deposition of an oxide layer (e.g. SiO₂ deposition), followed by chemical mechanical polishing (CMP) to achieve sub-nanometer surface flatness over the wafer. The CMOS transistors may be metal-oxide-semiconductor field-effect transistors (MOSFETs). The fabrication processes are compatible with CMOS processes.

[00200] FIG. 3 is a flow chart illustrating the steps of forming the 1D holographic metasurface in accordance with embodiments of the disclosure. A method 300 for fabricating a holographic metasurface device may include depositing a conductive layer over a holographic region of a wafer at operation 302. The method 300 may also include depositing a dielectric layer (e.g. a-Si) over the conducting layer at operation 304.

[00201] The method 300 may further include patterning a hard mask (e.g. Al₂O₃) on the dielectric layer (e.g. a-Si) at operation 306.

[00202] In some embodiments, the patterning may be performed by e-beam lithography when volume is small. The e-beam lithography includes scanning a focused beam of electrons on a surface covered with an electron-sensitive film, e.g. a resist. The electron beam can change the solubility of the resist, enabling selective removal of either exposed or non-exposed regions of the resist by immersing the resist in a solvent, e.g. developer. The

e-beam lithography can create very small structures or patterns in the resist that can be subsequently transferred to a substrate material by etching. The e-beam lithography can create patterns with a sub-10 nm resolution.

[00203] In some embodiments, the patterning may also be performed by deep-UV immersion lithography for large volume production. In some embodiments, the gap size may be about 100 nm, and is within the limits of deep UV immersion lithography. The deep UV immersion lithography uses UV light to transfer a geometric pattern from a photomask to a light-sensitive chemical photoresist on a substrate. The pattern in the etching resist is created by exposing to UV light, either directly, without using a mask, or with an optical mask. The photoresist is exposed to a pattern of intense UV light. The exposure to UV light can cause a chemical change that allows the photoresist to be removed by a solution or a developer. The photoresist may become soluble in the developer when exposed or unexposed regions may be soluble in the developer.

[00204] In the deep UV immersion lithography, UV light travels down through a system of lenses and then through a liquid medium (e.g. water) before reaching the photoresist on the wafer. The deep UV immersion lithography replaces an air gap between the lenses and the wafer surface with the liquid medium that may have a refractive index greater than one. The resolution can be increased by a factor equal to the refractive index of the liquid. The deep UV immersion lithography uses light from lasers with wavelengths of 248 nm and 193 nm, which allow small feature sizes down to 50 nm.

[00205] The method 300 may also include etching the dielectric layer to form a plurality of dielectric pillars (e.g. a-Si pillars) with a plurality of nano-scale gaps between the pillars at operation 308.

[00206] The refractive index tunable core material can be integrated or filled into the nano-scale gaps between the dielectric pillars. For example, the tunable core material may include liquid crystals and EO polymers, which can be deposited directly via spin coating, such that the liquid crystals fill the nano-scale gaps between the dielectric pillars via capillary action. The method 300 may further include filling the plurality of nano-scale gaps with a refractive index tunable core material at operation 310.

[00207] In some embodiments, the refractive index tunable core material may include a liquid crystal or EO polymers. The filling of the liquid crystal may include preparing the surface to be hydrophobic or hydrophilic, followed by spin coating the liquid crystal over the

plurality of pillars, and continued with filling the liquid crystal into the nano-scale gap by a capillary action and encapsulating the liquid crystal with a clear coating.

[00208] In some embodiments, the filling of the liquid crystal may include applying a coating to a first portion of the plurality of nano-scale gaps, followed by spin coating the liquid crystal onto the plurality of dielectric pillars, then filling the liquid crystal into a second portion of the plurality of nano-scale gaps by a capillary action, and continues with encapsulating the liquid crystal with a clear coating.

[00209] FIG. 4A shows the 1D metasurface before the integration of liquid crystals with the dielectric pillars in accordance with embodiments of the disclosure. FIG. 4B shows the 1D metasurface before the integration of liquid crystals in accordance with embodiments of the disclosure. Liquid crystal infiltration may occur by capillary action. Each pair of pillars is individually voltage biased to create arbitrary holograms.

[00210] In some embodiments, the nano-scale gap 404 may have substantially the same width as the gap 402. In some embodiments, the gap 404 may be larger than the gap 402, as shown in FIG. 4A. In some embodiments, all the nano-scale gaps between the pillars for each holographic element 406 are filled with a refractive index tunable core material, e.g. liquid crystal, as shown in FIG. 4B, which may be simple and low cost.

[00211] In some embodiments, every other gap 404 between the pillars, i.e. between the adjacent pairs of pillars, may be covered with a surface coating. For example, a surface coating 408 may be applied to cover some nano-scale gaps, such as the larger gaps 404 between the holographic elements. With the coating, only the small gaps 402 between the pillars in each holographic element are filled with the refractive index tunable core material, such as liquid crystals. The surface of the dielectric pillars may be prepared to be either hydrophobic or hydrophilic to encourage the filling of the tunable core material or preventing the filling of the tunable core material in some nano-scale gaps, depending on the type of tunable core material.

[00212] In the case of chalcogenide glass such as GST, sputtering can be employed, followed by a wet or dry etch to remove the GST from all areas except inside the pillar cores.

Examples

[00213] FIG. 5 shows a cross-sectional view of deposition of a conductive layer for wirebond on a first portion of a wafer in accordance with embodiments of the disclosure. As shown in FIG. 5, a first conductive layer 508 is deposited over a dielectric layer 504 (e.g. SiO₂), which is deposited over a wafer 502 (e.g. crystalline silicon wafer). The deposition of SiO₂

may use CVD, thermal oxidation or PECVD, among others. The first conductive layer for wirebond may include copper (Cu), aluminum (Al), or other CMOS compatible metals, among others.

[00214] A first Ti adhesion layer 506 is deposited between the first conductive layer 508 and the SiO₂ layer 504 underneath. A second Ti adhesion layer 510 is deposited between the first conductive layer 508 and a TiO₂ layer 512 above. The deposition of the first conductive layer and the Ti adhesion layer may use sputtering, or physical vapor deposition (PVD), among others. The deposition of TiO₂ may use CVD, or PECVD, among others. The TiO₂ layer 512 acts as an adhesion layer to the oxide layer (e.g. SiO₂) above (not shown).

[00215] FIG. 6 shows a cross-sectional view of deposition of a conductive layer as a metallic reflector on a second portion of the wafer in accordance with embodiments of the disclosure. A second conductive layer 602 is deposited over a second portion of the wafer 502. The second conductive layer 602 acts as the metal reflector for the holographic element.

[00216] An oxide layer 606 may be deposited over the second conductive layer 602, for example, using CVD, or PECVD, among others. The oxide layer 606 may include Al₂O₃, which acts as an etch stop layer. Again, a Ti adhesion layer 604 is deposited between the second conductive layer 602 and the SiO₂ layer 504. The SiO₂ layer 504 is deposited over the wafer 502. The second conductive layer 602 may include Cu, Al, or other CMOS compatible metals, among others. The deposition of the metal reflector and the Ti adhesion layer may use sputtering, or physical vapor deposition (PVD), among others.

[00217] FIG. 7 shows a cross-sectional view of plasma enhanced chemical vapor deposition (PECVD) of dielectric layer (e.g. SiO₂) over the conductive layers and etching the dielectric layer in accordance with embodiments of the disclosure. As shown, an oxide layer 702, such as SiO₂, can be deposited over the first conductive layer 508 and a portion of the second conductive layer 602 by PECVD or CVD.

[00218] FIG. 8 shows a cross-sectional view of PECVD and etching of the dielectric layer (e.g. SiO₂) after the step of FIG. 7 in accordance with embodiments of the disclosure. As shown, a thin SiO₂ 802 is deposited over the Al₂O₃ layer 606. Also, the SiO₂ layers 702 and 802 as well as TiO₂ layer 512 are etched to expose the Ti layer 510 for the wirebond region.

[00219] FIG. 9 shows a cross-sectional view of PECVD of amorphous silicon after the step of FIG. 8 in accordance with embodiments of the disclosure. As shown, a-Si layer 902 is deposited over the entire region including, both, the holographic region and the interconnect region. The Ti layer 510 allows bidirectional charge flow of the a-Si layer 902. Most interfaces

between metal and semiconductor form a 'schottky barrier', with diode behavior (i.e. one-way flow). The interface between Ti and a-Si, however, forms an 'ohmic contact' which readily conducts charge in either direction. The thin SiO₂ layer 802 acts as an adhesion layer between the Al₂O₃ layer 606 and the dielectric layer (e.g. a-Si) 902.

[00220] FIG. 10 shows a cross-sectional view of deposition of a hard mask (e.g. Al₂O₃) after the step of FIG. 9 in accordance with embodiments of the disclosure. As shown in FIG. 10, a hard mask 1002, such as Al₂O₃ is deposited over the a-Si layer 902. The hard mask 1002 is partially etched away to expose the a-Si layer in the wirebond region by low resolution process. Up to this stage, all these processes in FIGs. 1-10 are low resolution processes.

[00221] FIG. 11 shows a cross-sectional view of e-beam lithography of resist (e.g. PMMA) after the step of FIG. 10 in accordance with embodiments of the disclosure. The cross-sectional view includes a side view of an interconnect region including the first conductive layer (e.g. wire bond) on the left side, which may only need a low resolution process. The cross-sectional view also includes a front view of a holographic region 1106 including the second conductive layer (e.g. metallic reflector) on the right side, which may need a high resolution process. As shown in FIG. 11, a poly (methyl methacrylate) (PMMA) resist 1102 may be patterned to have a nano-scale gap 1104 in the holographic region 1106 by e-beam lithography or deep UV immersion lithography, each of which is a high resolution process.

[00222] FIG. 12 shows a cross-sectional view of etching of the hard mask (e.g. Al₂O₃) with a patterned resist (e.g. PMMA) to form a nano-scale gap in the hard mask after the step of FIG. 11 in accordance with embodiments of the disclosure. The hard mask 1002, such as Al₂O₃, may form a nano-scale gap 1202 by plasma etching through using the patterned PMMA resist 1102. The nano-scale gap 1202 in the dielectric layer has substantially the same width as the nano-scale gap 1104 in the PMMA resist 1102. The plasma etching may include a mixture of Cl₂ and Ar plasma. Again, the etching of the hard mask is performed by e-beam lithography or deep UV immersion lithography, each of which is a high resolution process.

[00223] FIG. 13 shows a cross-sectional view of stripping the resist (e.g. PMMA) after the step of FIG. 12 in accordance with embodiments of the disclosure. As shown, the PMMA resist 1102 may be stripped by using a chemical process. The PMMA resist may be removed by being exposed to an electron beam in e-beam lithography or exposed to UV light in deep UV immersion lithography. The PMMA resist can then be dissolved by using a developer. For

example, the PMMA resist 1102 may be soaked in a solvent, such as acetone, until the PMMA resist is completely removed or stripped. Again, this step is a high resolution process.

[00224] FIG. 14 shows a cross-sectional view of etching the a-Si layer with the patterned hard mask to form a nano-scale gap of a high aspect ratio between the a-Si pillars in the a-Si layer and to expose the titanium layer after the step of FIG. 13 in accordance with embodiments of the disclosure. As shown, a-Si is etched to form a nano-scale gap 1402 by e-beam lithography or deep UV immersion lithography. Also, the a-Si layer 902 and the TiO₂ layer 512 are etched such that the Ti layer 510 is exposed in the interconnect region. Again, this step is a high resolution process.

[00225] In some embodiments, the nano-scale gap 1402 may be 100 nm wide and 840 nm deep, and the a-Si pillars may be 170 nm wide, which corresponds to a laser wavelength of 1550 nm. In some embodiments, the nano-scale gap 1402 has a width of 60 nm, a depth of 480 nm, the pillars may be 100 nm wide, which corresponds to a laser wavelength of 905 nm.

[00226] FIG. 15 shows a cross-sectional view of wet etching the titanium layer to expose the conductive layer after the step of FIG. 14 in accordance with embodiments of the disclosure. As shown, the Ti adhesion layer 506 is etched away in the interconnect region. This is a low resolution process.

[00227] FIG. 16 shows a cross-sectional view of wire bonding to the conductive layer after the step of FIG. 15 in accordance with embodiments of the disclosure. As shown, a wire bus 1602 is wire bonded to the first conductive layer 508. This is also a low resolution process.

[00228] FIG. 17 shows a cross-sectional view of applying liquid crystal to fill the gap in the a-Si layer after the step of FIG. 16 in accordance with embodiments of the disclosure. As shown, liquid crystal 1702 is applied to cover the entire interconnect region and the holographic region including the nano-scale gap 1402.

Pseudo-Bosch Process at Cryogenic Temperatures

[00229] The disclosure provides methods of performing the pseudo-Bosch process at cryogenic temperatures. FIG. 18 illustrates processing issues including undercut near amorphous silicon pillar in accordance with embodiments of the disclosure. The etching of the a-Si pillars may be characterized by geometric parameters defined in FIG. 18. An undercut 1802 is the distance between the edge of the hard mask and the actual feature wall.

[00230] Practically, a required undercut is given by the following equation:

$$\text{Allowable undercut} = (\text{Target etch width} - \text{minimum resolution})/2$$

For example, if the target is a 100 nm trench and the e-beam can create 50 nm features, then the maximum allowable undercut is 25 nm. The undercut should be not more than 40 nm.

[00231] In some embodiments, the undercut is less than 40 nm. In some embodiments, the undercut is less than 30 nm. In some embodiments, the undercut is less than 20 nm. In some embodiments, the undercut is less than 15 nm. In some embodiments, the undercut is less than 10 nm. In some embodiments, the undercut is less than 5 nm.

[00232] A sidewall angle 1804 is the angle between the etch stop layer 1812 over the substrate and the wall 1810 of the dielectric pillar. Theoretically, the sidewall angle is 90°. Practically, as depicted, the sidewall angle 1804 may be above 80°, for example, 93°.

[00233] In some embodiments, the sidewall angle is equal to or less than 100°. In some embodiments, the sidewall angle is equal to or less than 98°. In some embodiments, the sidewall angle is equal to or less than 96°. In some embodiments, the sidewall angle is equal to or less than 94°. In some embodiments, the sidewall angle is equal to or less than 92°. In some embodiments, the sidewall angle is equal to or less than 90°. In some embodiments, the sidewall angle is equal to or less than 88°. In some embodiments, the sidewall angle is equal to or less than 86°. In some embodiments, the sidewall angle is equal to or less than 84°. In some embodiments, the sidewall angle is equal to or less than 82°. In some embodiments, the sidewall angle is greater than 80°. In some embodiments, the sidewall angle is greater than 82°. In some embodiments, the sidewall angle is greater than 84°. In some embodiments, the sidewall angle is greater than 86°. In some embodiments, the sidewall angle is greater than 88°. In some embodiments, the sidewall angle is greater than 90°. In some embodiments, the sidewall angle is equal to or less than 92°. In some embodiments, the sidewall angle is equal to or less than 94°. In some embodiments, the sidewall angle is equal to or less than 96°. In some embodiments, the sidewall angle is equal to or less than 98°.

[00234] In some embodiments, both the notching 1806 and footing 1808 have a characteristic size of less than 50 nm. In some embodiments, both the notching and footing have a characteristic size of less than 40 nm. In some embodiments, both the notching and footing have a characteristic size of less than 30 nm. In some embodiments, both the notching and footing have a characteristic size of less than 20 nm. In some embodiments, both the notching and footing have a characteristic size of less than 10 nm. In some embodiments, the

notching and footing may be smaller than half of the width of the element, which may cause a minor degradation in optical performance.

[00235] In some embodiments, the etch depth of the nano-scale gap between the dielectric pillars is deep, for example, 840 nm. The hard mask material may be selected as Al_2O_3 , such that the hard mask may have an etch rate of at least 30 times slower than that of a-Si, which can reduce the undercut.

[00236] In some embodiments, the disclosed method may avoid to produce nanospikes, which are commonly called 'Si Black' or 'Grass'.

[00237] In some embodiments, the etching may be performed by using a plasma etcher, such as an Oxford PlasmaLab 100 Inductively Coupled Plasma Etcher among others. A Pseudo-Bosch process may be used to perform the etching with a mixture of SF_6 and C_4F_8 gases. The SF_6 etching has both isotropic and anisotropic components and can etch anisotropically downwards. However, the C_4F_8 gas isotropically deposits an isotropic protective layer or protective coating and can be used to reduce the etch rate in all directions.

[00238] As an example, SF_6 alone may etch laterally at a first rate, e.g. 100 nm/min, and etch downwards at a second rate, e.g. 200 nm/min. The C_4F_8 may deposit a protective layer that reduces the etch rate by 100 nm/min in all directions. Hence, the net etch rate is zero laterally, and 100 nm/min downwards.

[00239] The pseudo-Bosch process includes various etching parameters, such as gas concentration, chamber pressure and plasma power, temperature, to control undercut and sidewall angles, among others. When an etching parameter, such as C_4F_8 concentration, decreases, the undercut may increase and the sidewall angle may be reduced such that the trench may become wider with depth.

[00240] The undercut may also vary with the material. For example, when the same etching parameters for mono-crystalline or poly-crystalline silicon are used for amorphous silicon, the undercut is significantly large, such as 200 nm or more for amorphous silicon. The large undercut in a-Si may limit its use to a micron scale application.

[00241] Applicants surprisingly discover that cryogenically cooling amorphous Si to a temperature below room temperature can etch the amorphous silicon with a reduced undercut, for example, less than 10 nm. It is believed that a lower temperature may increase the rate of protective C_4F_8 deposition and may also decrease the random thermal energy in the amorphous Si. As such, more energy may be required to break the bonds between a-Si atoms at reduced

temperature, which may bring the behavior closer to that of crystalline or poly-crystalline silicon.

[00242] In some embodiments, the a-Si may be etched at temperatures below room temperature to obtain an undercut of less than 50 nm, preferably 10 nm. In some embodiments, the a-Si may be cooled to 10°C or below. In some embodiments, the a-Si may be cooled to 5°C or below. In some embodiments, the a-Si may be cooled to 0°C or below. In some embodiments, the a-Si may be cooled to -5°C or below. In some embodiments, the a-Si may be cooled to -10°C or below. In some embodiments, the a-Si may be cooled to -15°C or below. In some embodiments, the a-Si may be cooled to -20°C or below. In some embodiments, the a-Si may be cooled to -30°C or below. In some embodiments, the a-Si may be cooled to -40°C or below. In some embodiments, the a-Si may be cooled to -50°C or below. In some embodiments, the a-Si may be cooled to -60°C or below. In some embodiments, the a-Si may be cooled to -70°C or below. In some embodiments, the a-Si may be cooled to -80°C or below. In some embodiments, the a-Si may be cooled to -90°C or below. In some embodiments, the a-Si may be cooled to -100°C or below. In some embodiments, the a-Si may be cooled to -110°C or below.

[00243] In some embodiments, the etching parameters may be adjusted at room temperature to obtain an undercut of less than 50 nm, preferably 10 nm.

II. Overview-Control Circuitry For 1D Optical Metasurfaces

[00244] The disclosure provides a hologram chip including a 1D array of hologram elements. Each hologram elements includes a pair of dielectric pillars or nano walls. The disclosure also provides methods for connecting the hologram chip to a control circuit chip by using flip-chip bonding. In one embodiment, the control circuit chip is bonded to the hologram chip on the same side as the hologram chip. In another embodiment, the control circuitry chip is bonded to the hologram chip on the opposite side from the hologram chip, using through-silicon vias (TSVs) to route the wire bus to the opposite side. In a further embodiment, for a large hologram chip, the array may be divided onto sub-arrays. Each sub-array is on a separate chip which is smaller than a single large chip. Then, by using flip-chip bonding, the control circuitry chip(s) are bonded to the sub-array chips onto a common carrier or an interposer.

[00245] FIG. 19 shows a cross-sectional view of a bus connection to a-Si pillars in accordance with embodiments of the disclosure. As shown in FIG. 19, a reflector layer 1918

and a bus connection 308 are disposed over a wafer substrate 1910. A dielectric pillar 1902, such as a-Si pillar, directly contacts the bus connection 1908 through a titanium (Ti) adhesion layer 1912. The a-Si pillar 1902 is disposed over an oxide layer 1924, which is disposed over the reflector layer 1918. The reflector layer 1918 may be formed of a metal, such as Cu, among others. The oxide 1924 may be formed of Al_2O_3 . The bus connection 1908 may also be formed of a metal, such as Cu among others.

Hologram Systems Including Control Circuit Chip

[00246] FIG. 20A is a side view of a hologram system including a hologram chip and a control circuit chip (e.g. CMOS chip) on the same side of the hologram chip in accordance with embodiments of the disclosure. FIG. 20B is a top view of the hologram system of FIG. 20A. As shown, a hologram system 2000 includes a hologram chip 2002 that connects to a control circuit chip 2004 having a plurality of conductive pads 2028.

[00247] The hologram chip 2002 includes a wafer substrate 2010 and an array of hologram elements 2006 on the top side of the wafer substrate 2010. The wafer substrate 2010 includes a first plurality of conductive pads 2042 in a hologram region 2022, which is on the right side of the wafer as pointed by arrow toward the right. The first plurality of conductive pads 2012 are directly connected to the hologram elements 2006.

[00248] The wafer substrate 2010 also includes a second plurality of conductive pads 2008 in an interconnect region 2020 which is on the left side of the wafer substrate 2010, as pointed by arrow toward the left. The conductive pads 2008 on the top-surface of the interconnect region can directly bond to the plurality of conductive pads 2028 of the control circuit chip 2004 through solder bumps 2014. The wafer substrate also includes an interconnection wire bus 2016 having a plurality of wires that connect the first plurality of conductive pads 2012 to the second plurality of conductive pads 2008.

[00249] To attach the hologram chip 2002 to the control circuit chip, the solder bumps may be deposited on the conductive pads on the top side of the control circuit chip. Then, the control circuit chip 2004 can be inverted or flipped to bring the solder bumps down onto the conductive pads 2008 on the wafer substrate 2010. As such, the control circuit chip 2004 connects to the hologram chip 2002.

[00250] The hologram system 2000 is small. The hologram chip and the CMOS chip sit directly on the wafer. The short wires greatly reduce inductance, allowing higher-speed signals, and also conduct heat better.

[00251] FIG. 21A is a side view of a hologram system including two or more hologram chips and two or more control circuit chips on the same side of the hologram chips in accordance with embodiments of the disclosure. FIG. 21B is a top view of the hologram system of FIG. 21A. As shown, a hologram system 2100 includes a hologram chip 2102 and connects to a control circuit chip 2104. The control circuit chip 2104 may include control logic circuit, memory, input and output (I/O).

[00252] The hologram chip 2102 includes two or more arrays of hologram elements, e.g. 2106A and 2106B, on small wafer substrates 2126A and 2126B. The hologram chip 2102 may also include an interposer 2118 which connects to the small wafer substrates 2126A-B and also connects to the control circuit chip 2104. By using multiple small wafer substrates, the hologram chip 2102 may have a lower failure rate and a higher production yield than a large hologram chip. The manufacturing of small chips may also be simpler than for a large chip.

[00253] The interposer 2118 is an electrical interface routing between the small hologram chips including wafer substrates 2126A-B and arrays of hologram elements 2106A-B and the control circuit chip 2104. The interposer 2118 can spread a connection to a wider pitch. The interposer 2118 can also reroute a connection to a different connection.

[00254] The interposer 2118 may have very flat surfaces for the control circuit chip 2104 to mount. The flatness may be difficult to maintain as the interposer may change its temperature, due to environment, or electric currents. Also, the short connections may be very stiff and thus the thermal expansion of the control circuit chip may need to match to the interposer.

[00255] The interposer 2118 includes a plurality of conductive pads 2116 on its top side in a hologram region 2122, on the right side of the interposer, as pointed by arrow toward the right. The interposer 2118 also includes a plurality of conductive pads 2124 in an interconnect region 2120, on the left side of the interposer, as pointed by an arrow toward the left. The conductive pads 2124 on the top-surface of the interconnect region can directly bond to the plurality of conductive pads 2124 of the control circuit chip 2104 through solder bumps 2112. The interposer 2118 also includes an interconnection wire bus 2116 having a plurality of wires that connect the first plurality of conductive pads 2114 to the second plurality of conductive pads 2124.

[00256] As shown in FIG. 21A, each wafer substrate 2126A or 2126B includes a plurality of through-silicon vias (TSVs), which are vertical interconnections that pass through each silicon wafer substrate 2126A or 2126B. The TSV(s) are used as an alternative

to wire-bond and flip chips to create 3D packages and 3D integrated circuits. The density of the TSVs is substantially high, and the length of the connections are short.

[00257] By using TSVs, it is possible to achieve connections between the hologram chip including hologram elements on the top side of the wafers and the interposer 2118. The TSVs may induce thermo-mechanical stress in the wafer, which may affect the performance of the system.

[00258] The TSVs are formed in the wafer substrates and can connect to a plurality of conductive pads 2110 formed on the bottom side of the wafer 2126A or 2126B. The TSVs form interconnects between the hologram elements and the conductive pads 2110, eliminate wire bonds, and allows for reduced form factor and higher-density interconnects. The conductive pads 2110 of the small hologram chips may bond to conductive pads 2114 on the interposer 2118 via solder bumps 2112. As such, the control circuit chip 2104 connects to the hologram chip 2102.

[00259] Turning to FIG. 21A again, the control circuit chip 2104 is on the same side as the small hologram chips. This can be accomplished by flipping the control circuit chip 2104, and bonding the control circuit chip 2104 onto the top of the interposer 2118 in the interconnect region 2120.

[00260] An underfill material 2132 may fill the space between the interposer 2118 and the control circuit chip 2104. The underfill material may act as an intermediate between the difference in coefficient of thermal expansion (CTE) of the control circuit chip and the interposer. In some embodiments, an electrically-insulating adhesive may be used to fill the space, also referred to underfill material, and thus provides a stronger mechanical connection and ensures the solder joints are not stressed due to differential heating of the CMOS chip and the remaining system. The underfill material distributes the thermal expansion mismatch between the chip and the interposer, and may reduce stress concentration in the solder joints, and thus may lead to a reduced failure.

[00261] FIG. 22 shows a side view of a hologram system including a hologram chip and a control circuit chip on an opposite side of the hologram elements in accordance with embodiments of the disclosure. As shown, a hologram system 2200 includes a hologram chip 2216 having a hologram metasurface 2202 on the top of a wafer substrate 2204. The hologram metasurface 2202 includes an array of hologram elements that are connected to conductive pads 608 through TSVs 2206 formed in the wafer substrate 2204.

[00262] The hologram system 2200 also includes a CMOS chip 2214 on the bottom of the wafer substrate 2204. The CMOS chip connects to the hologram chip 2216 via bonding conductive pads 2208 on the bottom of the wafer substrate 2204 to conductive pads 2212 on the top of the CMOS chip via solder bumps 2210.

[00263] FIG. 23 shows a side view of a hologram system including two or more hologram chips and two or more control circuit chips on an opposite side of the hologram elements in accordance with embodiments of the disclosure. As shown, a hologram system 2300 includes at least two hologram chips 2216A-B connected to a common control circuit chip 2314, such as a CMOS chip. Each of the hologram chips 2216A-B connects to the CMOS 2314 by bonding to conductive pads 2312 via solder bumps 2310.

Fabrication Processes

[00264] FIG. 24 is a flow chart illustrating steps for fabricating a hologram system with a control circuit chip and a hologram chip on the same side of a wafer in accordance with embodiments of the disclosure. As shown, a method 2400 may include fabricating a hologram chip and assembling the hologram chip with a control circuit chip, such as a CMOS chip.

[00265] The method 2400 starts with fabricating a first plurality of conductive pads in a hologram region of a wafer at operation 2402, followed by forming a second plurality of conductive pads in an interconnect region of the wafer at operation 2406. The method 2400 also includes fabricating an interconnecting wire bus on the wafer substrate to connect the first plurality of conductive pads to the second plurality of conductive pads at operation 2410.

[00266] The method 2400 may also include forming an array of sub-wavelength hologram elements over the wafer substrate in the hologram region at operation 2414, such that the array of sub-wavelength hologram elements is respectively directly coupled to the first plurality of conductive pads. The sub-wavelength hologram elements are integrated with a refractive index tunable core material.

[00267] The assembling of the hologram chip with the control circuit chip may include flipping a control circuit chip having a third plurality of conductive pads at operation 2418, such that the third plurality of conductive pads faces down at operation 2418. Flip chip bonding is a method for interconnecting the hologram chip to the control circuit chip, such as CMOS chip(s), via solder bumps. The solder bumps may be deposited on the conductive pads on the top side of the control circuit chip. When the control circuit chip is on the same

side as the hologram chip, the control circuit chip can be flipped over, so that its top side faces down to mount on the wafer in the interconnection region.

[00268] The method 2400 may further include connecting the control circuit chip to the interconnection region at operation 2422. The second plurality of conductive pads in the interconnect region is bonded to the third plurality of conductive pads via solder bumps. The control circuit chip may be positioned such that its conductive pads align with respective conductive pads in the interconnect region of the wafer.

[00269] The solder bumps may be heated to be above the melting point of the solder to produce an electrical connection, for example, using a Thermosonic bonding or a reflow solder process. Reflowing the solder balls includes heating the solder bumps to a temperature above the melting temperature of the solder bumps, such that the solder bumps melt and bond the conductive pads. This also leaves a small underlying space between the control circuit chip and the wafer or an underlying mounting. The underlying space may be filled with the underfill material as discussed earlier.

[00270] The solder bumps provide the contact between the hologram chip and the wafer and also between the control circuit chip and the interposer. The solder bumps are small spheres of solder that are bonded to the contact areas or conductive pads of the control circuit chip. The solder bumps can be used for face-down bonding. The solder bumps can be held in place with a tacky flux.

[00271] In some embodiments, the solder bumps may include gold stud bumps, conductive epoxy, copper balls, or lead-free solders. The solder balls may be selected to absorb the stresses related to CTE mismatch, drop shock, and temperature cycle test.

[00272] The length of the electrical connections between the control circuit chip and wafer or interposer can be controlled by placing solder bumps on the control circuit chip (e.g. CMOS chip), then flipping the CMOS chip over, aligning the solder bumps with the conductive pads on the wafer substrate or the interposer, and re-flowing the solder balls or solder bumps in a furnace to establish the bonding between the conductive pads of the CMOS chip and the wafer substrate or the interposer.

[00273] FIG. 25 is a flow chart illustrating steps for fabricating a hologram system with a control circuit chip and two or more hologram chips on the same side of an interposer in accordance with embodiments of the disclosure. A method 2500 includes fabricating an array of sub-wavelength hologram elements on a first side of a wafer substrate at operation 2502. The method 2500 also includes forming through-silicon vias on the wafer substrate at operation

2506. The method 2500 further includes forming a first plurality of conductive pads on a second side of the wafer substrate at operation 2510. The sub-wavelength hologram elements are respectively coupled to the first plurality of conductive pads via the through-silicon vias. The sub-wavelength hologram elements are also integrated with a refractive index tunable core material.

[00274] The method 2500 also includes fabricating an interposer at operation 2514. The interposer includes a second plurality of conductive pads in a hologram region and a third plurality of conductive pads in an interconnect region. The second plurality of conductive pads is electrically connected to the third plurality of conductive pads via an interconnecting wire bus.

[00275] It will be appreciated by those skilled in the art that the sequence of the steps 2502, 2506, 2510, and 2514 may vary. In an alternative embodiment, the method may include operations or steps 2510, 2506, 2502, and then 2514. In other embodiments, the method may include steps or operations 2502, 2506, 2510, and 2514 in any order.

[00276] The method 2500 further includes flipping a control circuit chip having a fourth plurality of conductive pads such that the fourth plurality of conductive pads faces down toward the third plurality of conductive pads at operation 2518.

[00277] The method 2500 further includes connecting the array of hologram elements to a control circuit chip via the interposer at operation 2522. The connecting includes bonding the first plurality of conductive pads of each of the one or more hologram chips to the second plurality of conductive pads in the hologram region of the interposer via solder bumps, such that the one or more hologram chips connect to the interposer. The connecting also includes bonding a fourth plurality of conductive pads of the control circuit chip to the third plurality of conductive pads in the interconnect region of the interposer via solder bumps, such that the control circuit chip connects to the interposer. The connecting further includes bonding the fourth plurality of conductive pads to the third plurality of conductive pads to electrically couple the arrays of sub-wavelength hologram elements of the one or more hologram chips to the control circuit chip.

[00278] FIG. 26 is a flow chart illustrating steps for fabricating a hologram system with a control circuit chip and a hologram chip on opposite sides of a wafer in accordance with embodiments of the disclosure. A method 2600 includes fabricating an array of sub-wavelength hologram elements on a first side of a wafer substrate at operation 2602, followed by forming through-silicon vias on the wafer substrate at operation 2606. The method

2600 continues with fabricating a first plurality of conductive pads on a second opposite side of the wafer substrate to form a first hologram chip at operation 2610.

[00279] It will be appreciated by those skilled in the art that the sequence of the steps 2602, 2606, and 2610 may vary. In an alternative embodiment, the method may include operations 2610, 2606, and then 2602. In other embodiments, the method may include operations 2602, 2606, and 2610 in any order.

[00280] The method 2600 further includes bonding a second plurality of conductive pads on a first region of the control circuit chip to the first plurality of conductive pads of the first hologram chip at operation 2614, such that the control circuit chip connects to the hologram elements of the first hologram chip. In some embodiments, bonding a second plurality of conductive pads on a first region of the control circuit chip to the first plurality of conductive pads of the first hologram chip is via solder bumps. The sub-wavelength hologram elements are integrated with a refractive index tunable core material.

[00281] The method 2600 further includes forming a second hologram chip at operation 2618 by repeating operations 2602, 2606, and 2610. The method also includes connecting the second hologram chip to the control circuit chip at operation 2622. The connecting includes bonding the second plurality of conductive pads on a second region of the control circuit chip to the first plurality of conductive pads of the second hologram chip, such that the control circuit chip connects to the hologram elements of the second hologram chip.

III. Overview- Control Circuitry For 2D Optical Metasurfaces

[00282] The disclosure also provides a 2D hologram system having a 2D array of sub-wavelength hologram elements. In some embodiments, the 2D hologram system may include a matrix control circuitry having CMOS layers under a metal reflector layer which is under the 2D array of sub-wavelength hologram elements. The CMOS layers include a plurality of CMOS transistors that are electrically coupled to the respective hologram elements above the metal reflector layer.

[00283] The individual addressing of the 2D array of sub-wavelength hologram elements may be achieved with an active matrix addressing scheme or a passive matrix addressing scheme, depending upon the refractive index tunable core material utilized.

[00284] The disclosure also provides methods for fabricating the 2D sub-wavelength hologram elements including the matrix control circuitry having the CMOS layers under the 2D array of hologram elements. The hologram elements can be formed over the CMOS layers

by using a nano-scale process, while the CMOS layers can be formed using a CMOS process over an underlying silicon wafer. In addition to material compatibility with CMOS processes, the geometry of the hologram elements is configured such that the hologram system can be fabricated monolithically over the matrix control circuitry.

[00285] FIG. 27 shows a perspective view of a 2D hologram system in accordance with embodiments of the disclosure. As shown in FIG. 27, a 2D hologram system or a 2D optical metasurface 2700 includes a 2D array of hologram elements 2702, which includes a pair of dielectric pillars 2706A-B and a refractive index tunable core material 2704 between the dielectric pillars 2706A-B. Each of the dielectric pillars 2706A-B extends sideways and has an extension 2708 that makes contact with a metal via 2710.

[00286] In one embodiment, the 2D hologram system 2700 may include a matrix control circuitry for actively controlling the hologram elements. The matrix control circuitry may include CMOS layers, which will be described in details below. The hologram system 2700 may use an active matrix addressing scheme. In another embodiment, the 2D hologram system 2700 does not include the matrix control circuitry. The hologram system 2700 may use a passive matrix addressing scheme. In some embodiments, each hologram element is addressed individually or independently.

Matrix Control Circuitry

[00287] FIG. 28 shows a side view of one sub-wavelength hologram element of a 2D hologram system with a matrix control circuitry in accordance with embodiments of the disclosure. As shown, a 2D hologram system 2800 includes optical layers 2820 disposed over metallization layers 2822, which are deposited over CMOS layers 2824 including a silicon wafer 2814 at the bottom of the CMOS layers 2824.

[00288] As shown in FIG. 28, each sub-wavelength hologram element 2702 includes a pair of dielectric pillars 2706A-B with a gap 2704 between the dielectric pillars 2706A-B. In one embodiment, the dielectric pillars 2706A-B may be amorphous silicon pillars (a-Si). The gap 2704 may be filled or integrated with a refractive index tunable core material. In some embodiments, the refractive index tunable core material may include liquid crystals, chalcogenide glasses, and electro-optic (EO) polymers, among others.

[00289] The dielectric pillars 2706A-B may have side extensions 2708 that contact metal vias 2710 underneath. The metal vias 2710 may extend down from the dielectric pillars to the CMOS layers 2824 to couple the CMOS layers 2824 to the hologram elements 2702 in

the optical layer 2820. The CMOS layers 2824 include a 2D array of CMOS transistors electrically coupled to the dielectric pillars 2706A-B of the respective hologram elements 2702. Each CMOS transistor includes a Gate 2810, a Drain or Source 2812, and a Source or Drain 2816.

[00290] A control voltage is applied across the two dielectric pillars 2706A-B. The electric and magnetic energy densities are across the hologram element 2702. The dielectric pillars 2706A-B are disposed over the third oxide layer 2806C, which may include aluminum oxide (Al_2O_3), as an etch stop layer.

[00291] A metal reflector 2802 is positioned under the dielectric pillars 2706A-B and above the CMOS layers 2824. The oxide layer 2806C also surrounds the metal reflector 2802. In some embodiments, the metal reflector 2802 may be made from copper, aluminum, or other CMOS-compatible metal, without sacrificing performance. The grazing incidence of the incident wave excites magnetic-like Mie resonances in the a-Si pillars with a high Q factor, enabling dynamic modulation of the phase. Additionally, the a-Si pillars are deposited over the metal reflector 2802, which makes the structure operate as a reflect-array and thus is possible to integrate with control circuitry. The resonator or hologram element 2702 includes two dielectric pillars 2706A-B that are separated by the tunable core material 2704 having a tunable refractive index. Under the grazing incidence excitation, the electric field is strongly localized in the core between the pillars, while the magnetic field is strongly localized to the entire hologram element including the pillars and the core.

[00292] The metallization layers 2822 may include upper metal vias 2710 that contact the extension 2708 of the dielectric pillars 2706A-B, and lower metal vias connected to the CMOS transistors. Each of the CMOS transistor may include a Gate 2810, a Drain 2812, and a Source 2816. The metallization layers 2822 may also include at least one patterned metal layer 2804 that extends sideways, i.e. parallel to the wafer substrate 2814. The at least one patterned metal layer 2804 connects between the upper metal via 2710 and the respective lower metal via 2808, which connects to the Drain 2812. The Gate 2810 is configured to connect to a first external wire such that a voltage can be applied to the Gate 2810. The Source 2816 is also configured to connect to a second external wire such that a second voltage can be applied to the Source 2816.

[00293] The metallization layers 2822 may also include the reflector layer 2802. The reflector layer 2802 only extends underneath the gap or core 2704 between the dielectric pillars 2706A-B of the hologram element 2702, where the electric field primarily resides.

[00294] As shown, a first oxide layer 2806A covers the CMOS layers 2824 and lower metal vias 2808. The first oxide layer 2806A may include SiO₂, among others. A second oxide layer 2806B covers the metal layer 2804 and a lower portion of the upper metal vias 2710. The second oxide layer 2806B may include silicon oxide (SiO₂) among others. The second oxide layer 2806 is planarized to provide a nano-scale flatness for the metal reflector layer 2802 and sub-wavelength hologram elements 2802 in the optical layer 2820. A third oxide layer 2806C covers the metal reflector layer 2802 and an upper portion of the upper metal vias 2710. The pillars 2706A-B are formed over the third oxide layer 2806C and the upper metal vias 2710.

[00295] In the illustrative embodiment described above, the gap or core 2704 between the pillars 2706A-B is about 60 nm. Each pillar has a width of about 100 nm and a depth of about 480 nm. The hologram element has a pitch of about 400 nm, which is on a similar scale to the pixel pitch of modern CMOS imaging sensors, which have a typical pixel size of 1000 nm. It will be appreciated by those skilled in the art that these dimensions may vary.

Active Matrix Addressing Scheme

[00296] An active matrix addressing scheme uses CMOS transistors to control hologram elements 2702, such as metal-oxide-semiconductor field-effect transistors (MOSFETs), to connect a desired analog voltage to one of the hologram elements 2702.

[00297] The active matrix addressing scheme may be suitable for implementations that use EO polymers, as the EO polymers have an extremely fast response time, such as several femtoseconds, i.e. 10⁻¹⁵ second. Thus, each hologram element may act as a storage capacitor, which is able to keep the applied analog voltage. The two a-Si pillars may act as electrical conductors of a capacitor, and the tunable core material between the a-Si pillars may act as the dielectric material between the electrical conductors. As such, the hologram element is represented by a capacitor.

[00298] FIG. 29 shows an active matrix addressing scheme for the 2D hologram system of FIG. 27 having a matrix control circuitry of FIG. 28 in accordance with embodiments of the disclosure. As shown, a 2D hologram system includes an array of hologram elements 2906 electrically coupled to an array of CMOS transistors 2910. The 2D array of hologram elements includes 9 hologram elements 2906AA, 2906AB, 2906AC, 2906BA, 2906BB, 2906BC, 2906CA, 2906CB, and 2906CC, as an example. Each CMOS transistor 2910 includes a Gate (G) (e.g. Gate 2810) electrically coupled to the respective ROW line 2902, a Source (S) (e.g. Source 2816) electrically coupled to a respective COLUMN line 2904, and a Drain (D) (e.g.

Drain 2812) electrically coupled to one conductor of a respective capacitor 2906. An opposite conductor of the capacitor 2906 connects to ground 2908.

[00299] In the active matrix addressing scheme, the ROW lines 2902 are digitally controlled, for example, a binary control, “on” and “off.” The COLUMN lines 2904 are controlled by analog voltages. The hologram elements 2702 act as a capacitor 2906. When a ROW line 2902 is in an “off” state, the capacitor 2906 holds the voltage. The stability of the capacitor 2906 depends upon the core material. When the ROW line 2902 is in an “on” state, the voltage of the capacitor or hologram element can be changed.

[00300] During operation, the digital ROW line 2902 activates the Gates of all CMOS transistors, such as MOSFETs, in a specific row. The COLUMN line 2904 applies an analog voltage to the hologram elements in a specific column through the Drains of the CMOS transistors 2910. When the ROW line 2902 changes the CMOS transistors in the specific row to be an “off” state, the capacitors, unit cells, or hologram elements 2906 keep the applied analog voltage due to the inherent capacitance of the hologram elements.

[00301] As an example, when the ROW line 2902A is turned “on,” an analog voltage of 2 V, as an example, is applied to a first hologram element 2906AA, which is on the first row of and the first column of the 2D array, by applying the analog voltage from the first COLUMN line 2904A. The first row of the 2D array is coupled to the first ROW line 2902A, while the first column of the 2D array is coupled to the first COLUMN line 2904A. Then, the first ROW line 2902A is turned “off,” such that the first hologram element 2906AA has an analog voltage of 2 V.

[00302] Next, the second ROW line 2902B may be turned “on,” and a second analog voltage of 3 V, as an example, may be applied to the second hologram element 2906BB, which is on the second row and the second column of the 2D array, by applying the analog voltage from the second COLUMN line 2904B. The second row of the 2D array is coupled to the second ROW line 2902B, while the second column of the 2D array is coupled to the second COLUMN line 2904B. Then, the second ROW line 2902B is turned off again, such that the second hologram element 2906BB keeps an analog voltage of 3 V. By doing so, each hologram element can be controlled independently in a sequential manner.

[00303] It will be appreciated by those skilled in the art that the analog voltage may vary. In some embodiments, the analog voltage may be equal to or greater than -5V. In some embodiments, the analog voltage may be equal to or greater than -4V. In some embodiments, the analog voltage may be equal to or greater than -3V. In some embodiments, the analog

voltage may be equal to or greater than -2V. In some embodiments, the analog voltage may be equal to or greater than -1V. In some embodiments, the analog voltage may be equal to or greater than 0V. In some embodiments, the analog voltage may be equal to or greater than 1V. In some embodiments, the analog voltage may be equal to or greater than 2V. In some embodiments, the analog voltage may be equal to or greater than 3V. In some embodiments, the analog voltage may be equal to or greater than 4V.

[00304] In some embodiments, the analog voltage may be equal to or less than 5V. In some embodiments, the analog voltage may be equal to or less than 4V. In some embodiments, the analog voltage may be equal to or less than 3V. In some embodiments, the analog voltage may be equal to or less than 2V. In some embodiments, the analog voltage may be equal to or less than 1V. In some embodiments, the analog voltage may be equal to or less than 0V. In some embodiments, the analog voltage may be equal to or less than -1V. In some embodiments, the analog voltage may be equal to or less than -2V. In some embodiments, the analog voltage may be equal to or less than -3V. In some embodiments, the analog voltage may be equal to or less than -4V.

[00305] FIG. 30 is a flow chart illustrating the steps for operating the 2D hologram system of FIG. 28 with the active matrix addressing scheme of FIG. 29 in accordance with embodiments of the disclosure. Operation 3000 may include adjusting a binary voltage to a first ROW line from an “off” state to an “on” state at step 3002, followed by applying a first analog voltage to a first COLUMN line at step 3004. A first hologram element at the first row and the first column of the 2D array now has the first analog voltage. The operation 3000 continues with changing the first ROW line to an “off” state at step 3006, then adjusting a second ROW line from an “off” state to an “on” state at step 3008, and applying a second analog voltage to a second COLUMN line at step 3010. A second hologram element at the second row and the second column of the 2D array now has the first analog voltage. With the operation 3000, each hologram element can be controlled by an analog voltage independently in a sequential manner.

Passive Matrix Addressing Scheme

[00306] In some embodiments, the hologram system uses a passive matrix addressing scheme without a matrix control circuitry. The hologram system is as shown in FIGs. 1A-1C and 2A-2B, as described early. The manufacturing of this system is much simpler than the hologram system including a matrix control circuitry and the active matrix addressing scheme. The passive matrix addressing scheme does not require the use of MOSFETs in the hologram

system and is thus a simpler design than the hologram system with the active matrix addressing scheme. However, the operation of the passive matrix addressing scheme is more complex than the operation of the active matrix addressing scheme, which is described below.

[00307] In the passive matrix addressing scheme, the tunable core materials in the hologram elements experience the sum of the analog voltages applied to their ROW and COLUMN lines during all operations, even those targeted for other hologram elements. However, the tunable core material may be most sensitive to the maximum voltage. Therefore, if a refresh rate of the analog voltage is fast enough compared to the relaxation time of the tunable core material, such as liquid crystal, the total average state may be nearly constant.

[00308] FIG. 31 shows a passive matrix addressing scheme for the 2D hologram system of FIG. 27 without any matrix control circuitry in accordance with embodiments of the disclosure. As shown, a 2D array of hologram elements includes 9 hologram elements 3106AA, 3106AB, 3106AC, 3106BA, 3106BB, 3106BC, 3106CA, 3106CB, and 3106CC, as an example. Each row of hologram elements is all coupled to a respective ROW line 3102A, 3102B, or 3102C. Each column of hologram elements of the 2D array is all coupled to a respective COLUMN line 3104A, 3104B, or 3104C. The example is simplified for illustration purposes. The 2D array may be configured such that all the rows may have the same number of hologram elements and all the columns may have the same number of hologram elements. It will be appreciated by one of skilled the art that the number of hologram elements may vary with the array.

[00309] The passive matrix addressing scheme for the 2D array of hologram elements is provided below. The hologram elements are sequentially and independently controlled. Each hologram element can be individually switched to a different state. For example, a first hologram element 3106AA is on a first row coupled to the first ROW line 3102A and a first column coupled to the first COLUMN line 3104A. A first analog voltage may be applied to the first ROW line 3102A while a second analog voltage may be applied to the first COLUMN line 3104A. A first total analog voltage applied to the first hologram element 3106AA is the sum of the first analog voltage applied to the ROW line 3102A and the second analog voltage applied to the COLUMN line 3104A.

[00310] In the case of liquid crystals, the passive matrix addressing can be utilized since the molecular orientation has some memory, on the scale of several milliseconds. The passive matrix addressing is also compatible with chalcogenide glasses, since the chalcogenide glasses

have a long-term memory. When the tunable core material has a long term memory, such as liquid crystal or chalcogenide glasses, the tunable core material may have a relaxation time significantly longer than a refreshing time of the analog voltage. In other words, the analog voltage can be applied at a high refreshing rate such that the refreshing time is shorter than the relaxation time of the tunable core material. For example, the refresh rate is at least three times faster than the relaxation rate. In one embodiment, the relaxation time may be 1000 times longer than the refreshing time. If the tunable core material has a relaxation time corresponding to a frequency of 30 kHz, the refresh rate for the analog voltage may be is at least 30 MHz.

[00311] The state of the first hologram element 3106AA is stable until a newly applied total analog voltage exceeds the first total voltage, assuming that the tunable core material has a relaxation time longer than the refreshing time of applying the analog voltage. As an example, a third analog voltage may be applied to the first ROW line 3102A or to the first COLUMN line 3104A in a refreshing time shorter than a relaxation time of the refractive index tunable core material, which is integrated with a pair of dielectric pillars of each of the 2D array of sub-wavelength hologram elements. Now, a second total analog voltage is equal to the sum of the third analog voltage and the first or second analog voltage. In one embodiment, if the second total analog voltage is smaller than the first total analog voltage, the state of the refractive index tunable core material of the first hologram element 3106AA remains substantially constant. In another embodiment, if the second total analog voltage is greater than the first total analog voltage, the state of the refractive index tunable core material of the first hologram element 3106AA is changed according to the second total analog voltage.

[00312] With respect to a second hologram element 3106BB in a second row coupled to the second ROW line 3102B and in a second column coupled to the second COLUMN line 3104B, a total analog voltage applied to the second hologram element 3106BB equals to the sum of the analog voltage on the second ROW line 3102B and the second COLUMN line 3104B. Likewise, with respect to a third hologram element 3106AB in the first row and the second column, a total analog voltage applied to the third hologram element 3106AB equals to the sum of the analog voltage on the first ROW line 3102A and the second COLUMN line 3104B. Similarly, with respect to a fourth hologram element 3106BA in the second row and the first column, a total analog voltage applied to the fourth hologram element 3106BA equals to the sum of the analog voltage on the second ROW line 3102B and the first COLUMN line 3104A. As shown by the above examples, each of the hologram elements is individually applied to a total analog voltage.

[00313] FIG. 32 illustrates a waveform of voltage vs time applied to a hologram element using the passive matrix addressing scheme of FIG. 30 in accordance with embodiments of the disclosure. As shown in FIG. 32, the liquid crystal (LC) state is stable at a first voltage V_1 , such as 5V, equal to a sum of a row voltage applied to a ROW line and a column voltage applied to a COLUMN line for a period of time $\Delta t_1 = t_2 - t_1$. Then, the voltage V_1 may decay to a lower voltage V_2 during a period of time $\Delta t_2 = t_3 - t_2$. This voltage decay process is referred to relaxation of the liquid crystal. A second voltage V_1 , such as 5V, is applied at time t_3 , the LC remains stable for a period of time Δt_1 , and then the voltage V_1 may decay again.

[00314] It will be appreciated by one of skilled in the art that the liquid crystal may be replaced by any tunable core material that has a long term memory or a long relaxation time.

[00315] FIG. 33 is a flow chart illustrating the steps for operating the 2D hologram system of FIG. 27 with the passive matrix addressing scheme of FIG. 31 in accordance with embodiments of the disclosure. Operation 3300 may include applying a first analog voltage to a first ROW line at step 3302. The first ROW line is coupled to a first row of a 2D array of sub-wavelength hologram elements.

[00316] The operation 3300 may also include applying a second analog voltage to a first COLUMN line at step 3304. The first COLUMN line is coupled to a first column of the 2D array of sub-wavelength hologram elements. The operation 3300 continues with applying a third analog voltage to the first ROW line or the first COLUMN line in a refreshing time shorter than the relaxation time of the tunable core material between the pillars of the hologram element at step 3306. The first hologram element in the first row and the first column has a first total analog voltage equal to a sum of the first analog voltage and the second analog voltage. A second total analog voltage is equal to the sum of the third analog voltage and the first or second analog voltage. If the second total analog voltage is smaller than the first total analog voltage, the state of the refractive index tunable core material of the first hologram element remains substantially constant. If the second total analog voltage is greater than the first total analog voltage, the state of the refractive index tunable core material of the first hologram element is changed according to the second total analog voltage.

Fabrication of Hologram System having Matrix Control Circuitry

[00317] In some embodiments, the disclosure provides methods for fabricating the 2D hologram system including a matrix control circuitry, suitable for large-scale commercial fabrication. The disclosure provides a process suitable for large-scale commercial fabrication.

The dielectric pillars, such as amorphous silicon (a-Si) or poly-crystalline silicon, may be deposited by using plasma-enhanced chemical vapor deposition (PECVD) or CVD.

[00318] The nano-scale gaps between the dielectric pillars may be formed by etching using either electron beam lithography, for smaller production volumes (e.g. prototyping), or with deep UV immersion lithography, for large production volumes.

[00319] The complementary metal-oxide-semiconductor (CMOS) transistors can be fabricated on a wafer, such as a crystalline silicon wafer. Then, the CMOS transistors can be connected through metal vias to the dielectric pillars for applying a voltage to each pair of pillars, which acts as a capacitor. The metal vias can be planarized with deposition of an oxide layer (e.g. SiO₂ deposition), followed by chemical mechanical polishing (CMP) to achieve sub-nanometer surface flatness over the wafer. The CMOS transistors may be metal-oxide-semiconductor field-effect transistors (MOSFETs). The fabrication processes are compatible with CMOS processes.

[00320] In some embodiments, the fabrication proceeds as follows. FIG. 34 is a flow chart illustrating the steps for fabricating the hologram system including the active matrix control circuitry of FIG. 29 in accordance with embodiments of the disclosure. Process 3400 may include fabricating a matrix control circuitry having a 2D array of CMOS transistors over a wafer at step 3402. Referring to FIG. 28 again, the CMOS transistors can be first fabricated on the crystalline silicon wafer 2814. Then, in a standard CMOS fashion, the CMOS transistors can be connected to the ROW and COLUMN lines of the active matrix addressing scheme by using patterned metallization layers 2822.

[00321] The process 3400 may also include forming metallic interconnects to the matrix control circuitry at step 3404. During the metallization step, metal vias 2710 in the patterned metallization layers 2822, as shown in FIG. 28, are connected to the dielectric pillars 2706A-B to control each hologram element 2702. The metal vias 2710 are also connected to the patterned metal layer 2804, which is also referred to a metal interconnect. Lower metal vias 2808 are connected between the patterned metal layer 2804 and the CMOS transistors in the CMOS layers 2824.

[00322] The process 3400 may be followed by depositing an oxide layer over the metallic interconnects at step 3406 and planarizing the oxide layer at step 3408. The patterned metal layer 2804 and the lower metal vias 2808 and lower portion of the upper metal vias 2810 can be planarized with an oxide deposition, followed by CMP to achieve sub-nanometer

surface flatness. The deposition and planarization processes are also standard CMOS processes.

[00323] The process 3400 may continue with disposing a reflector layer over the planarized oxide layer at step 3410. The metal reflector layer 2802 and the dielectric pillars 2706A-B, e.g. a-Si pillars, can be fabricated on the planarized matrix control circuitry, as described above, with each dielectric pillar 2706A-B connected to the exposed upper metal vias 2710. Up to this stage, all fabrication and processes is entirely CMOS compatible.

[00324] The process 3400 may further include fabricating 2D array of sub-wavelength hologram elements over the planarized oxide layer at step 3412. The tunable core material can be integrated into the gap 2704 between the dielectric pillars. Liquid crystals and EO polymers can be deposited directly via spin coating, and fill the gap via capillary action. The surface may be prepared appropriately to be either hydrophobic or hydrophilic, depending on the tunable core material. In the case of chalcogenide glass, such as $\text{Ge}_2\text{Sb}_2\text{Te}_5$ (GST), sputtering can be employed, followed by a masked wet or dry etch to remove the GST from all areas except inside the core between the pillars.

[00325] Any ranges cited herein are inclusive. The terms “substantially” and “about” used throughout this Specification are used to describe and account for small fluctuations. For example, they can refer to less than or equal to $\pm 5\%$, such as less than or equal to $\pm 2\%$, such as less than or equal to $\pm 1\%$, such as less than or equal to $\pm 0.5\%$, such as less than or equal to $\pm 0.2\%$, such as less than or equal to $\pm 0.1\%$, such as less than or equal to $\pm 0.05\%$.

[00326] Having described several embodiments, it will be recognized by those skilled in the art that various modifications, alternative constructions, and equivalents may be used without departing from the spirit of the invention. Additionally, a number of well-known processes and elements have not been described in order to avoid unnecessarily obscuring the present invention. Accordingly, the above description should not be taken as limiting the scope of the invention.

[00327] Those skilled in the art will appreciate that the presently disclosed embodiments teach by way of example and not by limitation. Therefore, the matter contained in the above description or shown in the accompanying drawings should be interpreted as illustrative and not in a limiting sense. The following claims are intended to cover all generic and specific features described herein, as well as all statements of the scope of the present method and system, which, as a matter of language, might be said to fall in between.

CLAIMS

What is claimed is:

1. A method for fabricating an optical metasurface, the method comprising:
 - depositing a conductive layer over a holographic region of a wafer;
 - depositing a dielectric layer over the conducting layer;
 - patterning a hard mask on the dielectric layer; and
 - etching the dielectric layer to form a plurality of dielectric pillars with a plurality of nano-scale gaps between the pillars.
2. The method of claim 1, wherein the plurality of dielectric pillars comprises amorphous silicon.
3. The method of any one of claims 1-2, wherein the plurality of dielectric pillars comprises a constant gap between each of the pillars or wherein the plurality of dielectric pillars comprises a plurality of pairs of dielectric pillars and the gap between each pair of pillars is smaller than the gap between two adjacent pairs of pillars.
4. The method of any one of claims 1-3, further comprising filling the plurality of nano-scale gaps with a refractive index tunable core material.
5. The method of any one of claims 1-4,
 - wherein the refractive index tunable core material comprises a liquid crystal or EO polymers,
 - the step of filling the plurality of nano-scale gaps comprising:
 - preparing the surface to be hydrophobic or hydrophilic;
 - spin coating the liquid crystal over the plurality of pillars;
 - filling the liquid crystal into the nano-scale gap by a capillary action; and
 - encapsulating the liquid crystal with a clear coating, or
 - the step of filling the plurality of nano-scale gaps comprising:
 - applying a coating to a first portion of the plurality of nano-scale gaps;
 - spin coating the liquid crystal onto the plurality of dielectric pillars;
 - filling the liquid crystal into a second portion of the plurality of nano-scale gaps by a capillary action; and

encapsulating the liquid crystal with a clear coating.

6. The method of any one of claims 1-5, wherein the refractive index tunable core material comprises chalcogenide glass, the step of filling the plurality of nano-scale gaps comprising:
 - depositing the chalcogenide glass over the dielectric pillars by sputtering; and
 - removing the chalcogenide glass from all areas except inside the plurality of nano-scale gaps.
7. The method of any one of claims 1-6, the step of depositing a dielectric layer over a conducting layer comprising:
 - depositing an etch-stop dielectric layer over the conducting layer; and
 - depositing the dielectric layer over the etch-stop dielectric layer.
8. The method of any one of claims 1-7, the step of patterning a hard mask on the dielectric layer comprising:
 - depositing a hard mask over the dielectric layer;
 - patterning the hard mask to remove a first portion of the hard mask near an interconnect region;
 - patterning the hard mask by a high resolution process to form the nano-scale gap;
 - plasma etching the hard mask to remove a second portion of the hard mask in the nano-scale gap to expose the dielectric layer.
9. The method of any one of claims 1-8, wherein patterning the hard mask to remove a first portion of the hard mask near an interconnect region is performed by a low resolution process.
10. The method of any one of claims 1-9, further comprising forming a plurality of conductive contacts over an interconnect region of the wafer for wire bonding to a CMOS, the plurality of conductive contacts configured to apply voltage to the plurality of dielectric pillars.
11. A method for fabricating dielectric pillars having a nano-scale gap according to any one of claims 1-10, the method comprising:
 - depositing a dielectric layer over a conducting layer;
 - patterning a hard mask on the dielectric layer by a high resolution process; and

applying a plasma to etch a portion of a dielectric layer at a temperature below room temperature in a chamber to form dielectric pillars with the nano-scale gap.

12. The method of any one of claims 1-11, wherein the plasma comprises a mixture of gases, wherein the mixture of gases comprises SF₆ gas for anisotropic etching, and wherein the mixture of gases comprises C₄F₈ gas for reducing the etching rate isotropically.

13. The method of any one of claims 1-12, further comprising increasing the concentration of the C₄F₈ gas to reduce the undercut of the dielectric pillars.

14. The method of any one of claims 1-13, further comprising decreasing the concentration of the C₄F₈ gas to reduce the sidewall angle of the dielectric pillars from the conducting layer.

15. The method of any one of claims 1-14, wherein the sidewall angle ranges between 80° and 100°.

16. The method of any one of claims 1-15, further comprising adjusting the pressure of the chamber to reduce the undercut of the dielectric pillars or adjusting the power of the plasma to reduce the undercut of the dielectric pillars.

17. The method of any one of claims 1-16, the step of patterning a hard mask on the dielectric layer by a high resolution process comprising:

depositing a hard mask over the dielectric layer;

patterning the hard mask by a low resolution process to remove a first portion of the mask near a wire contact region;

patterning the hard mask to form the nano-scale gap by a high resolution process;

applying a plasma to etch the hard mask to remove a second portion of the hard mask in the nano-scale gap to expose the dielectric layer.

18. The method of any one of claims 1-17, wherein the high resolution process comprises e-beam lithography or deep UV immersion lithography.

19. An optical metasurface fabricated by the method of any of any one of claims 1-10.

20. A plurality of dielectric pillars fabricated by the method of any of any one of claims 11-18.

21. A hologram system comprising:

a first hologram chip comprising a wafer substrate having a first plurality of conductive pads on a hologram surface region connected to a second plurality of conductive pads on an interconnect surface region and an array of sub-wavelength hologram elements integrated with a refractive index tunable core material on the hologram region of the wafer substrate; and

a control circuit chip having a third plurality of conductive pads connected to the second plurality of conductive pads on the interconnect region of the wafer substrate,

wherein the interconnect region is on the same side of the wafer substrate as the hologram region, and

wherein the first plurality of conductive pads is directly connected to the array of sub-wavelength hologram elements.

22. The hologram system of claim 21, wherein the array of sub-wavelength hologram elements is a plurality of nano-walls arranged in a one-dimensional array, and the plurality of nano-walls is respectively coupled to the first plurality of conductive pads.

23. The hologram system of any one of claims 21-22, wherein the first plurality of conductive pads is connected to the second plurality of conductive pads by an interconnecting wire bus, and wherein the second plurality of conductive pads is connected to the third plurality of conductive pads via solder bumps.

24. The hologram system of any one of claims 21-23, wherein the chip is a CMOS chip and wherein the wafer substrate comprises silicon.

25. The hologram system of claim 21-24, wherein each of the first, second, and third plurality of conductive pads comprises a respective first, second, and third plurality of sub-group of conductive pads, wherein the first plurality of sub-group of conductive pads are electrically connected to the second plurality of sub-group of conductive pads, and wherein the second plurality of sub-group of conductive pads are electrically connected to the third plurality of sub-group of conductive pads.

26. A method of fabricating a first hologram chip of a hologram system according to any one of claims 21-25, the method comprising:

fabricating a first plurality of conductive pads in a hologram region of a wafer substrate;

forming a second plurality of conductive pads in an interconnect region of the wafer substrate;

fabricating an interconnecting wire bus on the wafer substrate to connect the first plurality of conductive pads to the second plurality of conductive pads; and

forming an array of sub-wavelength hologram elements over the wafer substrate in the hologram region such that the array of sub-wavelength hologram elements is respectively directly coupled to the first plurality of conductive pads.

27. The method of claim 26, further comprising bonding a third plurality of conductive pads on the control circuit chip to the second plurality of conductive pads via solder bumps such that the control circuit chip connects to the first hologram chip.

28. A method of assembling a first hologram chip and a control circuit chip of a hologram system according to any one of claims 21-25, the method comprising:

providing a first hologram chip having a wafer substrate having a first plurality of conductive pads in a hologram region and a second plurality of conductive pads in an interconnect region and an array of sub-wavelength hologram elements in the hologram region on the wafer substrate, the first plurality of conductive pads electrically connected to the hologram elements;

flipping a control circuit chip having a third plurality of conductive pads such that the third plurality of conductive pads face down; and

bonding the second plurality of conductive pads in the interconnect region to the third plurality of conductive pads such that the control circuit chip is electrically connected to the first hologram chip.

29. The method of claim 28, wherein the second plurality of conductive pads is electrically connected to the first plurality of conductive pads on the wafer substrate by an interconnecting wire bus on the wafer substrate.

30. The method of any one of claims 28-29, wherein bonding the second plurality of conductive pads in the interconnect region to the third plurality of conductive pads comprises bonding via solder bumps.

31. The method of any one of claims 28-30, wherein the array of sub-wavelength hologram elements comprises a plurality of nano-walls arranged in a one-dimensional array, and the plurality of nano-walls is respectively coupled to the first plurality of conductive pads.

32. A method of fabricating a hologram system according to any one of claims 21-25, the method comprising:

- (a) fabricating an array of sub-wavelength hologram elements on a first side of a wafer substrate;
- (b) forming through-silicon vias on the wafer substrate;
- (c) fabricating a first plurality of conductive pads on a second opposite side of the wafer substrate to form a first hologram chip;
- (d) bonding a second plurality of conductive pads on a first region of the control circuit chip to the first plurality of conductive pads of the first hologram chip such that the control circuit chip connects to the hologram elements of the first hologram chip.

33. The method of claim 32, wherein bonding a second plurality of conductive pads on a first region of the control circuit chip to the first plurality of conductive pads of the first hologram chip is via solder bumps.

34. The method of any one of claims 32-33, further comprising:

- forming a second hologram chip by repeating steps (a) to (c);
- bonding the second plurality of conductive pads on a second region of the control circuit chip to the first plurality of conductive pads of the second hologram chip such that the control circuit chip connects to the hologram elements of the second hologram chip; and
- wherein the sub-wavelength hologram elements of the second hologram chip are integrated with a refractive index tunable core material.

35. The method of any one of claims 32-34, wherein bonding a second plurality of conductive pads on a second region of the control circuit chip to the first plurality of conductive pads of the second hologram chip is via solder bumps.

36. A 2D hologram system with a matrix addressing scheme, the system comprising:
a 2D array of sub-wavelength hologram elements integrated with a refractive index tunable core material on a wafer substrate; and
a matrix addressing scheme coupled to the 2D array of sub-wavelength hologram elements and configured to independently control each of the sub-wavelength hologram elements by applying a voltage.
37. The hologram system of claim 36, further comprising an active matrix addressing scheme for controlling the 2D array of sub-wavelength hologram elements,
wherein the refractive index tunable core material comprises EP polymer.
38. The hologram system of any one of claims 36-37, wherein the wafer substrate comprises a matrix control circuitry having a 2D array of CMOS transistors.
39. The hologram system of any one of claims 36-38,
wherein each of the 2D array of CMOS transistors has a Drain connected to each of the hologram elements,
wherein all Gates of each row of the 2D array of CMOS transistors are coupled together to a respective ROW line and all Sources of each column of CMOS transistors are coupled together to a respective COLUMN line,
wherein each ROW line is configured to digitally control each Gate of the CMOS transistors in the respective row to be “on” and “off”, and
wherein each COLUMN line is configured to apply an analog voltage through each Source of the CMOS transistors in the column to each of the hologram elements when the Gate of the CMOS transistors is in an “on” state.
40. The hologram system of any one of claims 36-39,
wherein each of the hologram elements comprises two dielectric pillars and acts as a capacitor, at least one of the two dielectric pillars being grounded, and
wherein the 2D array of sub-wavelength hologram elements are aligned with each other.

41. A method of operating a 2D hologram system having a 2D array of hologram elements with the active matrix addressing scheme according to any one of claims 36-40, the method comprising:

- adjusting a binary voltage on a first row to change the first row from an “off” state to an “on” state;

- applying a first analog voltage to a first column such that the first analog voltage is stored in a first hologram element in the first column and the first row;

- changing the first row to an “off” state;

- adjusting a second row from an “off” state to an “on” state;

- applying a second analog voltage to a second column such that the second analog voltage is stored in a second hologram element in the second column and the second row.

42. A method of fabricating a hologram system according to any one of claims 36-40, the method comprising:

- fabricating a matrix control circuitry having a 2D array of CMOS transistors over a wafer;

- forming metallic interconnects to the matrix control circuitry;

- depositing an oxide layer over the metallic interconnects;

- planarizing the oxide layer;

- disposing a reflector layer over planarized oxide layer; and

- fabricating a 2D array of sub-wavelength hologram elements over the reflector layer.

43. The method of claim 42, wherein the metallic interconnects comprise metal vias connecting between the sub-wavelength hologram elements and the respective CMOS transistors.

44. The method of any one of claims 42-43, the step of fabricating the 2D array of sub-wavelength hologram elements comprises a high resolution nano-scale process, and filling a gap between the dielectric pillars with the refractive index tunable core material,

- wherein the reflector layer is under the gap between the dielectric pillars and has a pitch smaller than a pitch of the hologram element.

45. The hologram system of claim 36, wherein the matrix addressing scheme comprises a passive matrix addressing scheme for controlling the 2D array of sub-wavelength hologram elements.

46. The hologram system of claim 45,
wherein the wafer substrate comprises silicon,
wherein the refractive index tunable core material comprises liquid crystals or chalcogenide glasses,
wherein each of the hologram elements comprises a first dielectric pillar and a second dielectric pillar,
wherein the tunable core material is positioned between the first and second dielectric pillars, and
wherein each hologram element acts as a capacitor.
47. The hologram system of any one of claims 45-46,
wherein the first dielectric pillars of each row of the hologram elements are all connected to a ROW line applied with a first analog voltage, and the second dielectric pillars of each column of the hologram elements are all connected to a COLUMN line applied with a second analog voltage, and
wherein a total analog voltage applied to each of the hologram elements is the sum of the first analog voltage and the second analog voltage.
48. The hologram system of any one of claims 45-47,
wherein the total analog voltage has a refresh rate of at least 1 k Hz,
wherein each of the first analog voltage and the second analog voltage has a refresh rate of at least 1000 times higher than the relaxation rate of the refractive index tunable core material,
wherein the refractive index tunable core material in the hologram element has a long term memory such that the hologram element remains stable until a refreshed total analog voltage exceeds a previous value, and
wherein each of the hologram elements is configured to switch to a different state by refreshing the first analog voltage and/or the second analog voltage.
49. A method of operating a hologram system having a 2D array of sub-wavelength hologram elements, with the passive matrix addressing scheme according to any one of claims 45-48, the method comprising:

applying a first analog voltage to a first ROW line, wherein a first row of a 2D array of sub-wavelength hologram elements is coupled to the first ROW line;

applying a second analog voltage to a first COLUMN line, wherein a first column of the 2D array of sub-wavelength hologram elements is coupled to the first COLUMN line;

applying a third analog voltage to the first ROW line or to the first COLUMN line in a refreshing time shorter than a relaxation time of a refractive index tunable core material integrated with a pair of dielectric pillars of each of the 2D array of sub-wavelength hologram elements;

wherein a first hologram element in the first row and the first column has a first total analog voltage equal to a sum of the first analog voltage and the second analog voltage,

wherein a second total analog voltage is equal to the sum of the third analog voltage and the first or second analog voltage,

if the second total analog voltage is smaller than the first total analog voltage, the state of the refractive index tunable core material of the first hologram element remains substantially constant, or

if the second total analog voltage is greater than the first total analog voltage, the state of the refractive index tunable core material of the first hologram element is changed according to the second total analog voltage.

50. The method of claim 49, further comprising:

applying a fourth analog voltage to a second ROW line, wherein a second row of the 2D array of sub-wavelength hologram elements is coupled to the second ROW line; and

applying a fifth analog voltage to a second COLUMN line, wherein a second column of the 2D array of sub-wavelength hologram elements is coupled to the second COLUMN line,

wherein the second hologram element has a total analog voltage equal to the sum of the fourth analog voltage and the fifth analog voltage, such that the second hologram element is independently controlled from the first hologram element.

1/24

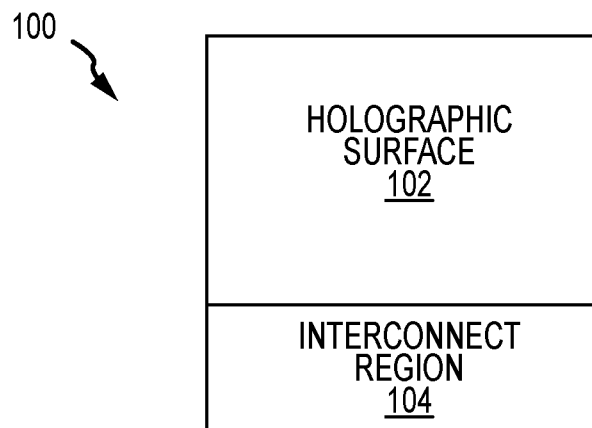


FIG. 1A

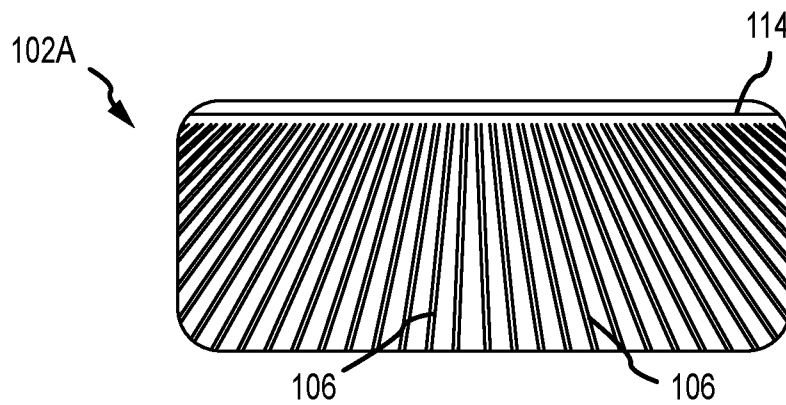


FIG. 1B

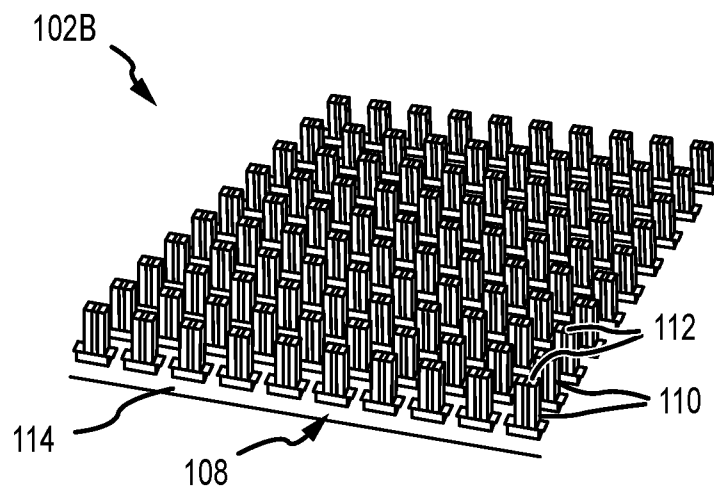


FIG. 1C

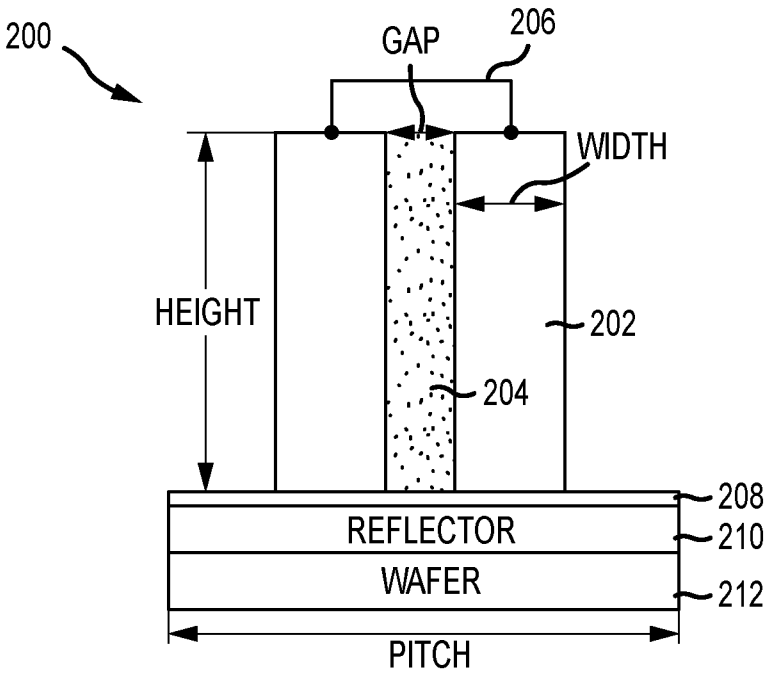


FIG.2A

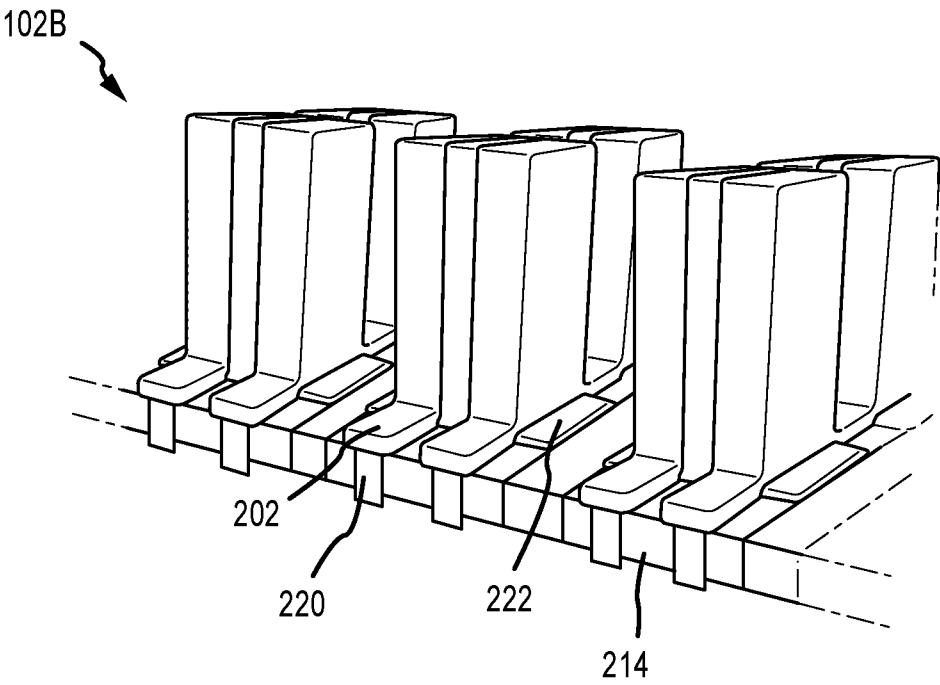


FIG.2B

3/24

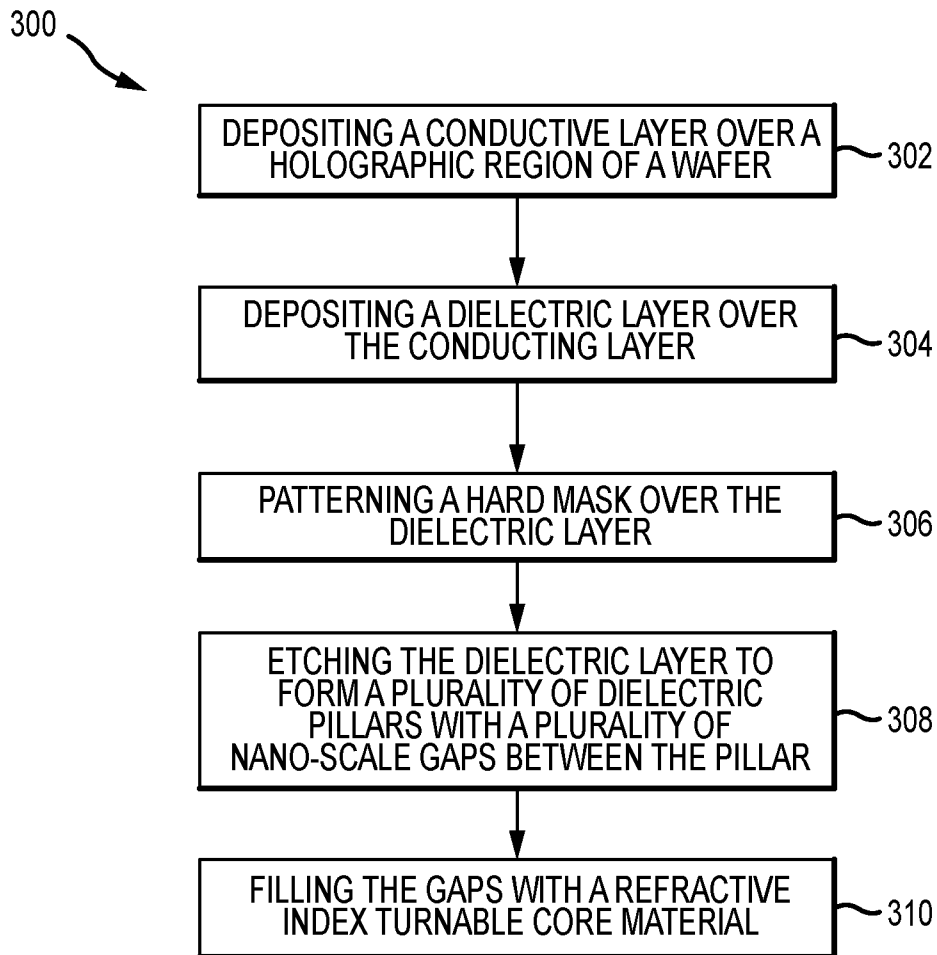


FIG.3

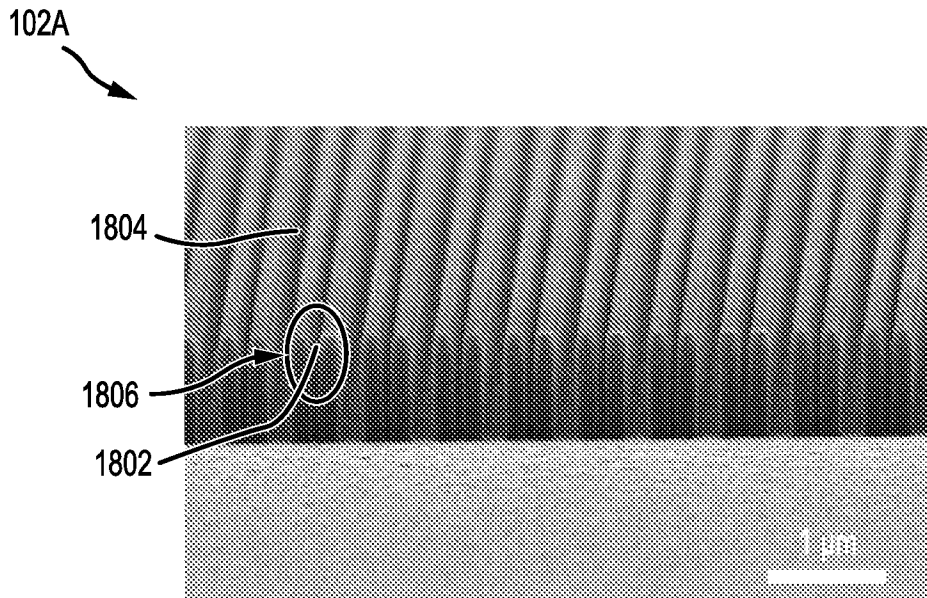


FIG.4A

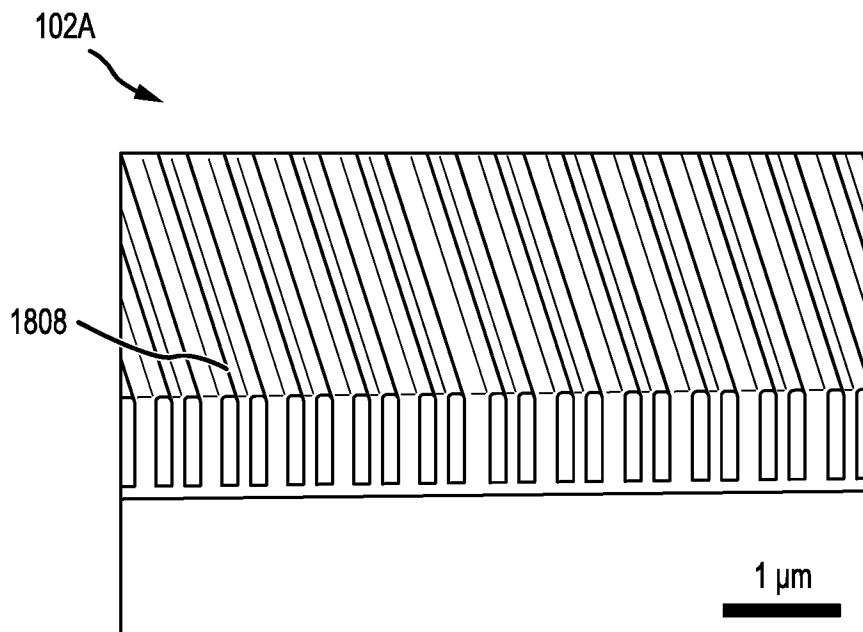


FIG.4B

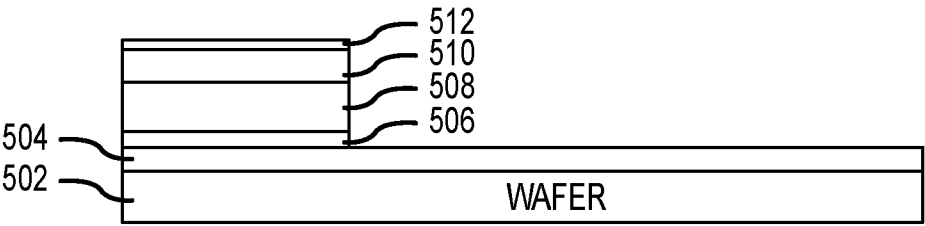


FIG.5

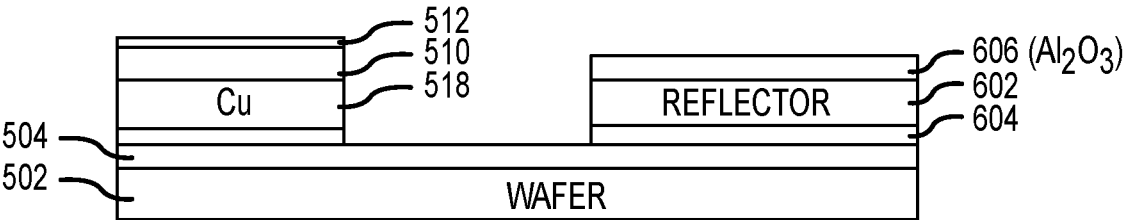


FIG.6

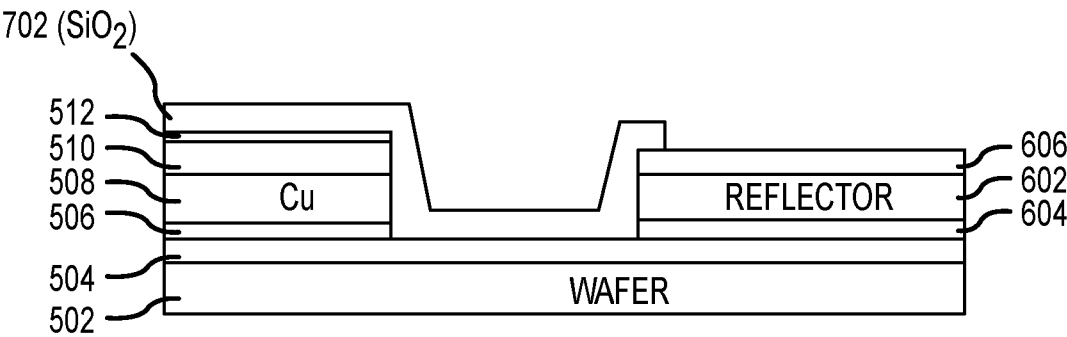


FIG.7

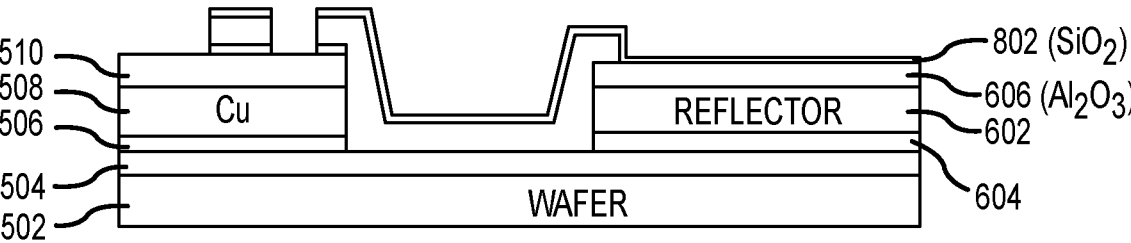


FIG.8

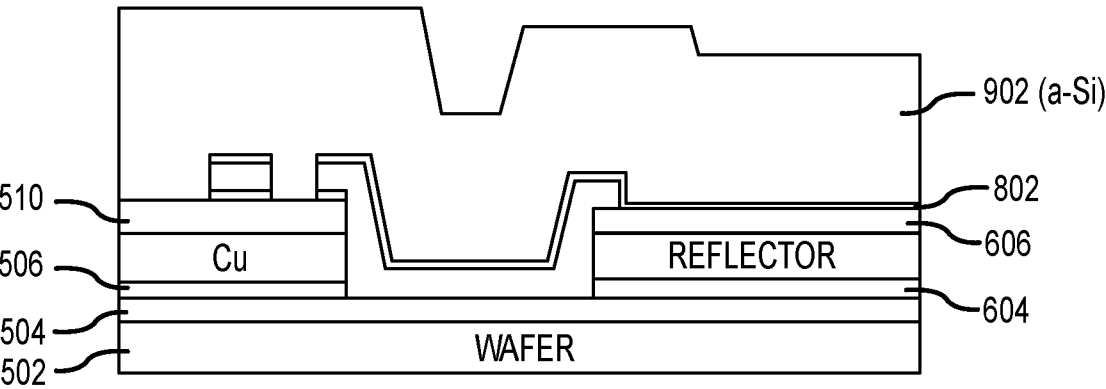


FIG.9

7/24

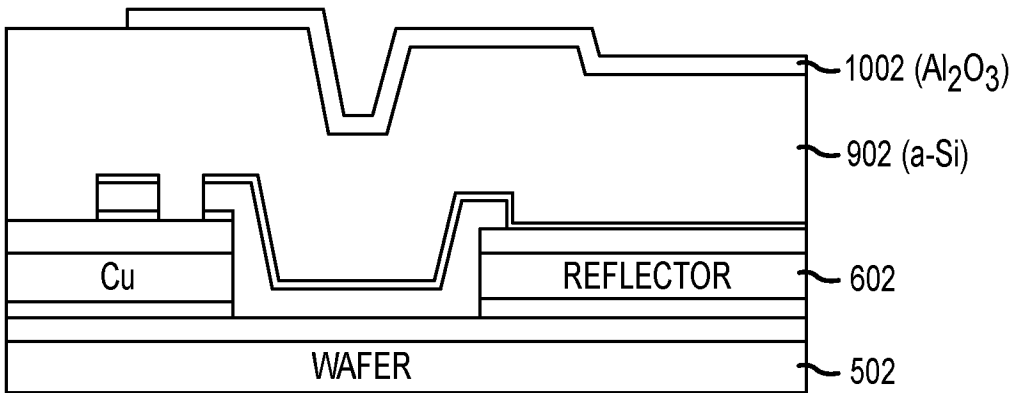


FIG.10

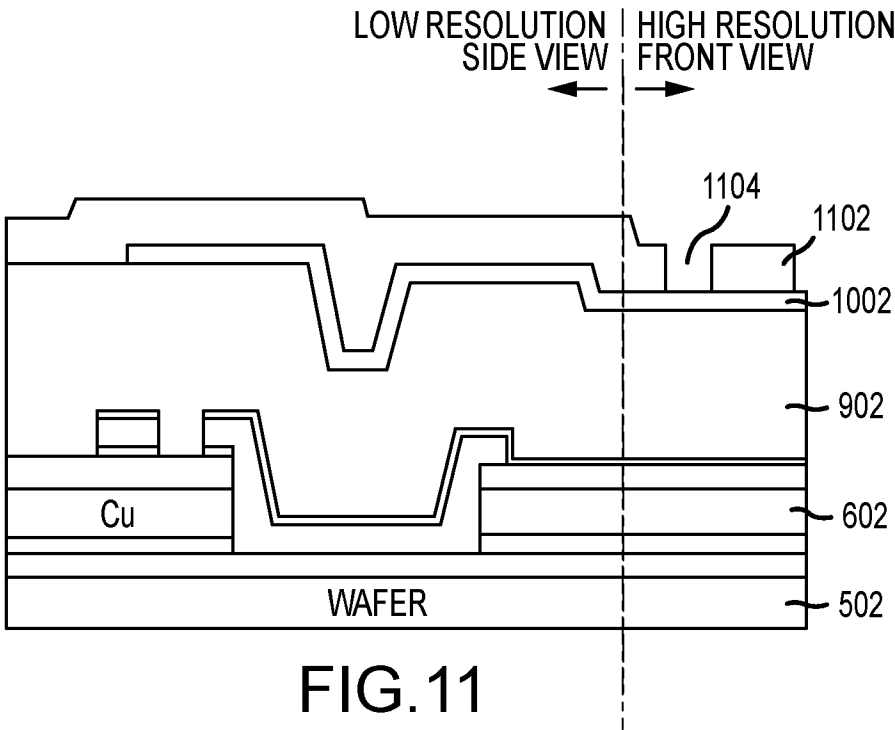


FIG.11

8/24

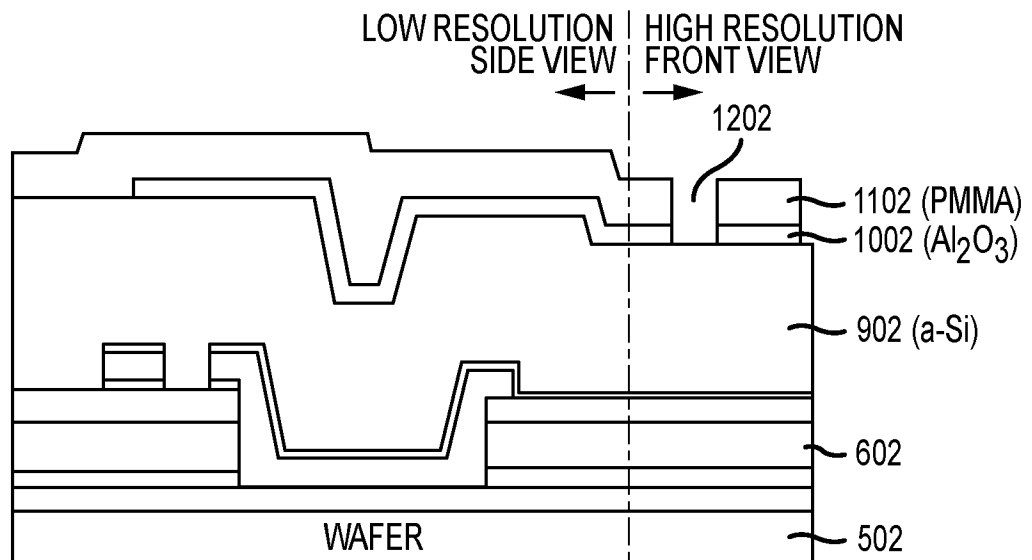


FIG.12

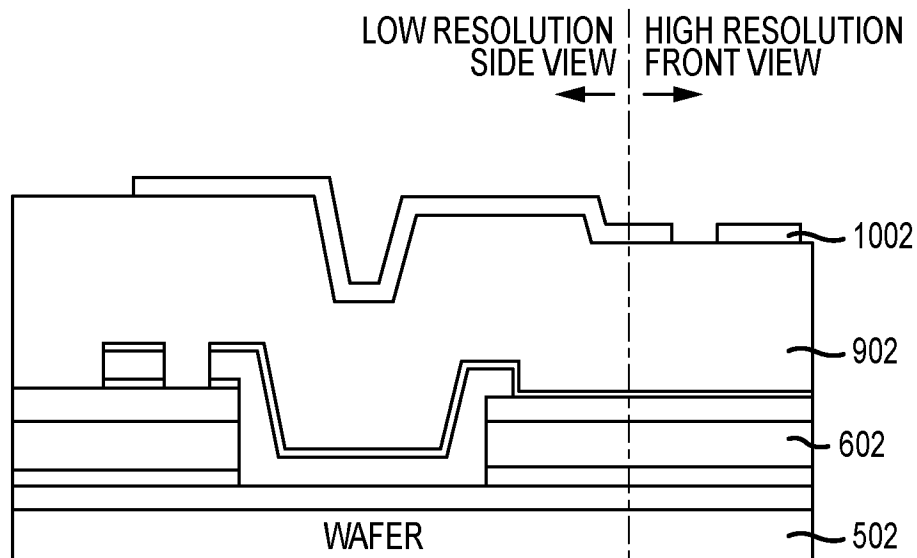


FIG.13

9/24

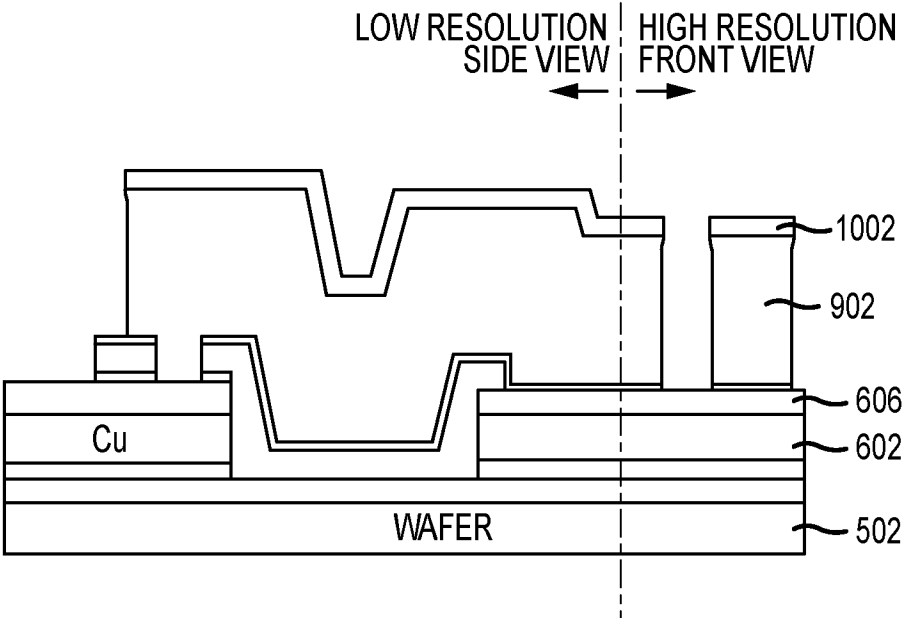


FIG.14

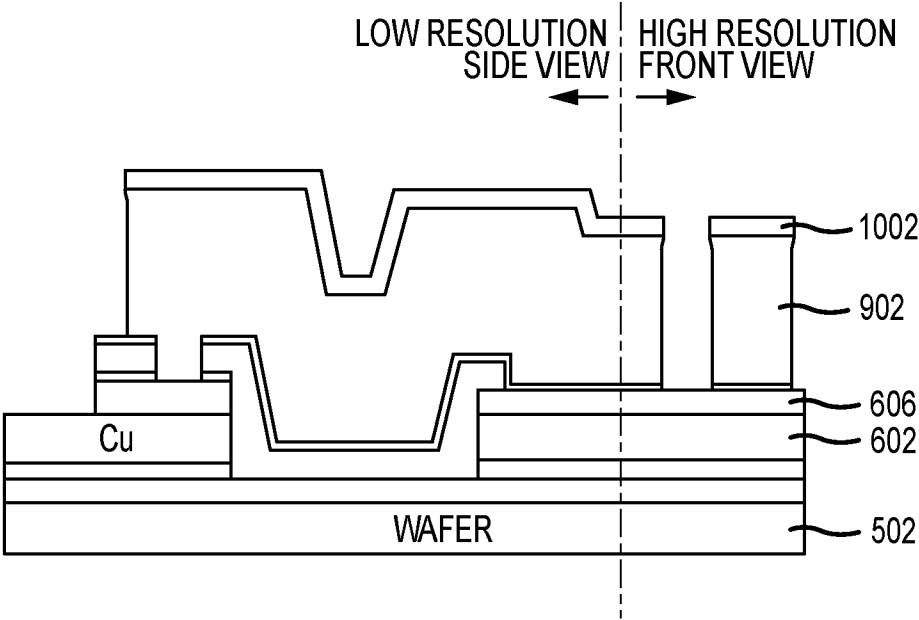


FIG.15

10/24

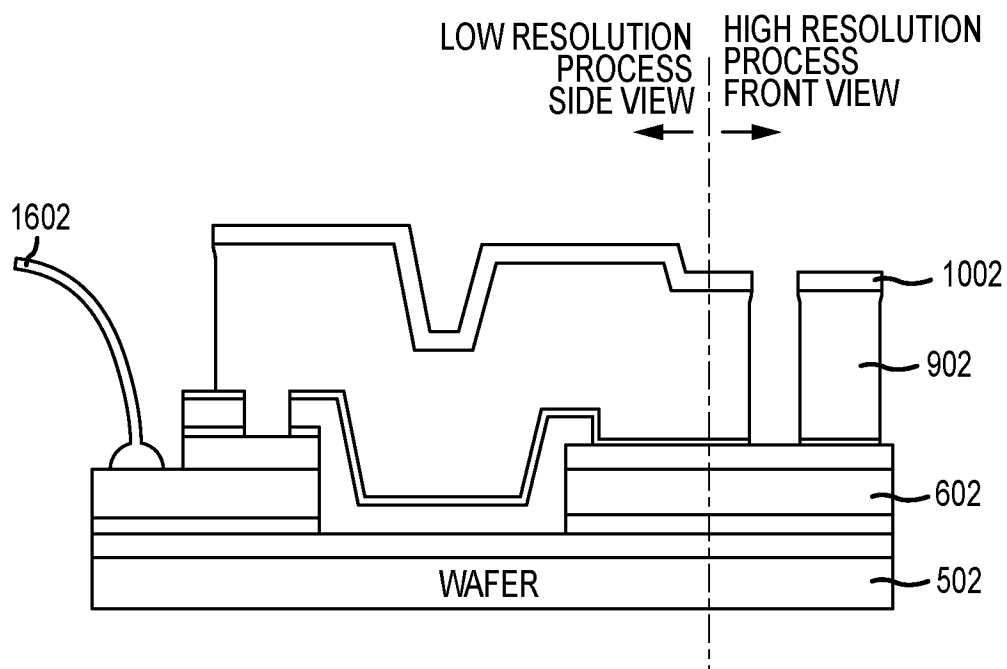


FIG. 16

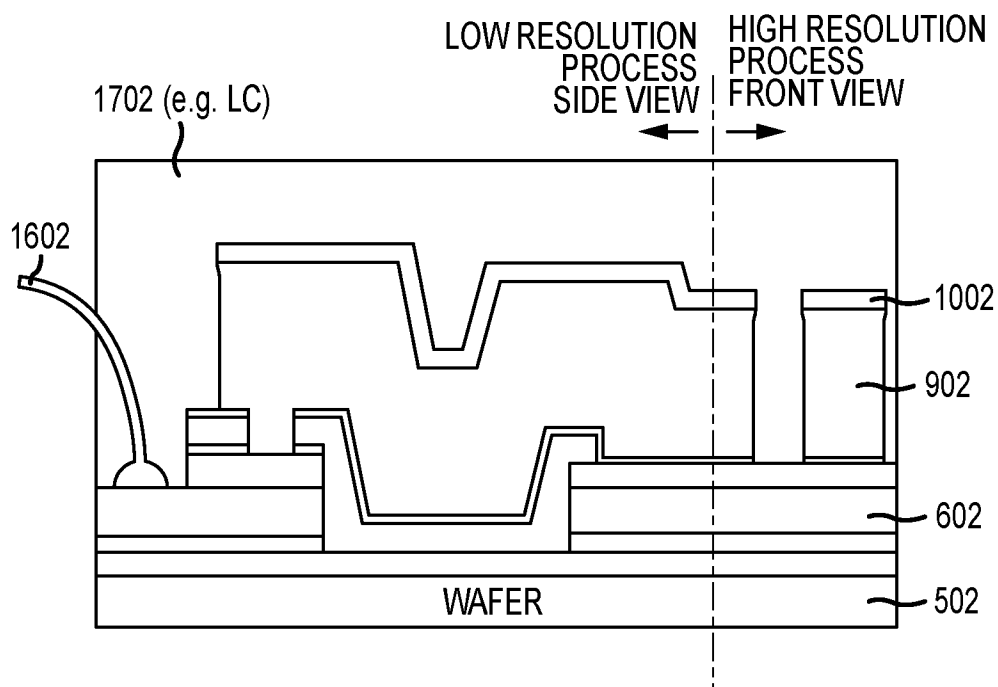


FIG. 17

11/24

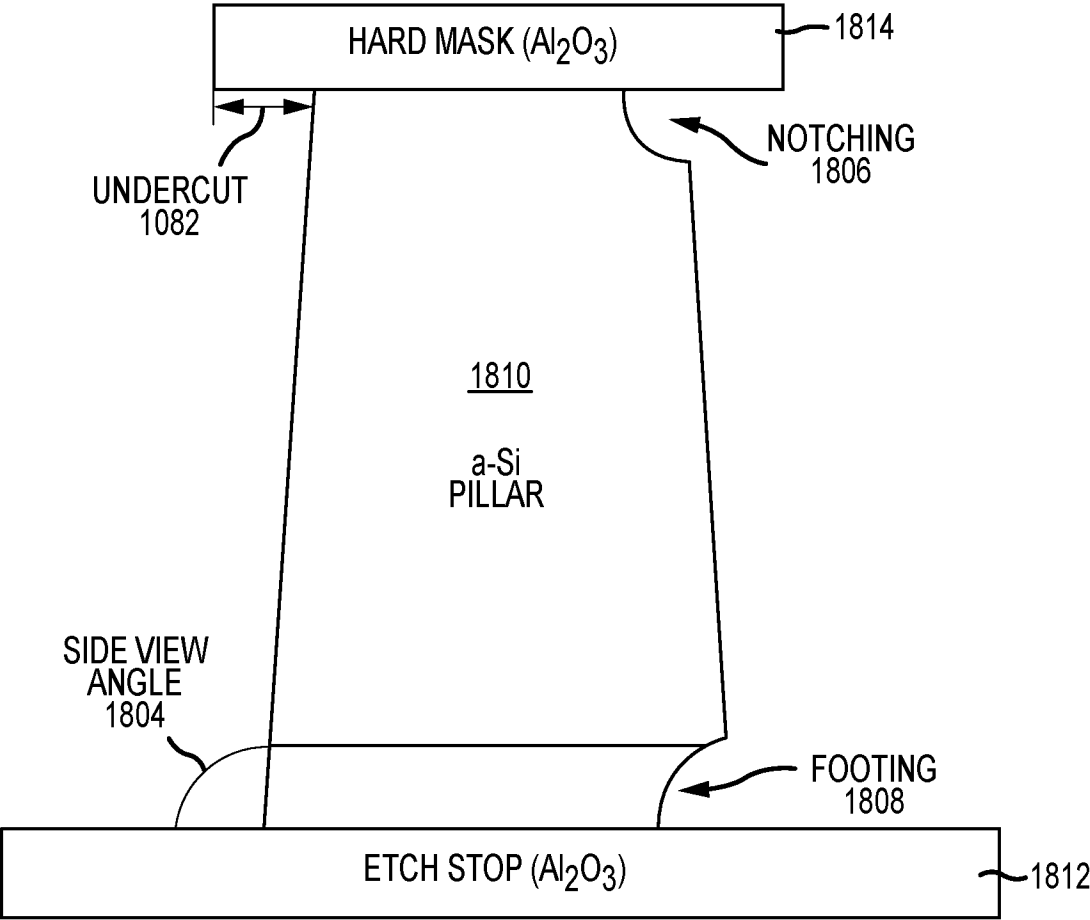


FIG.18

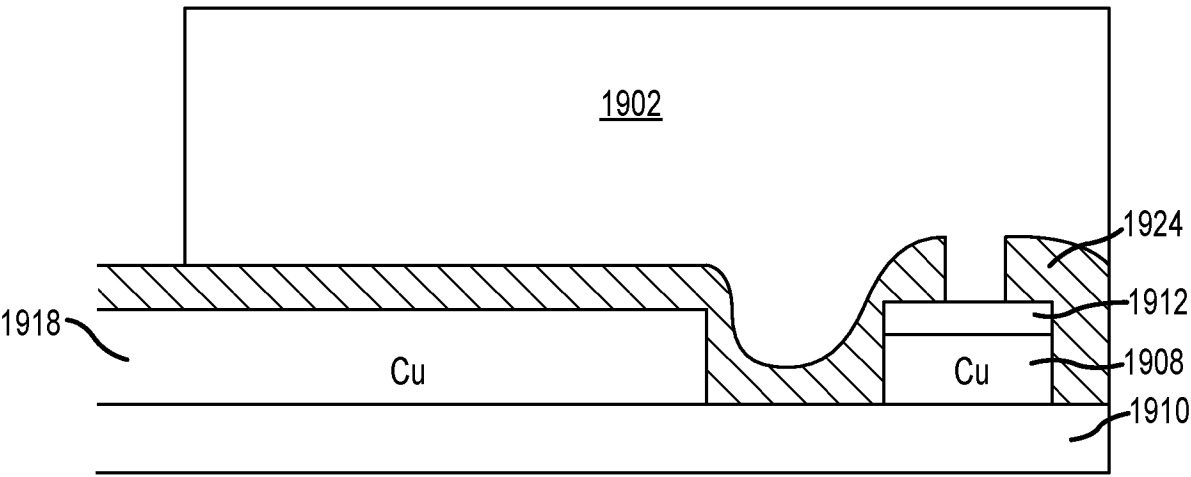
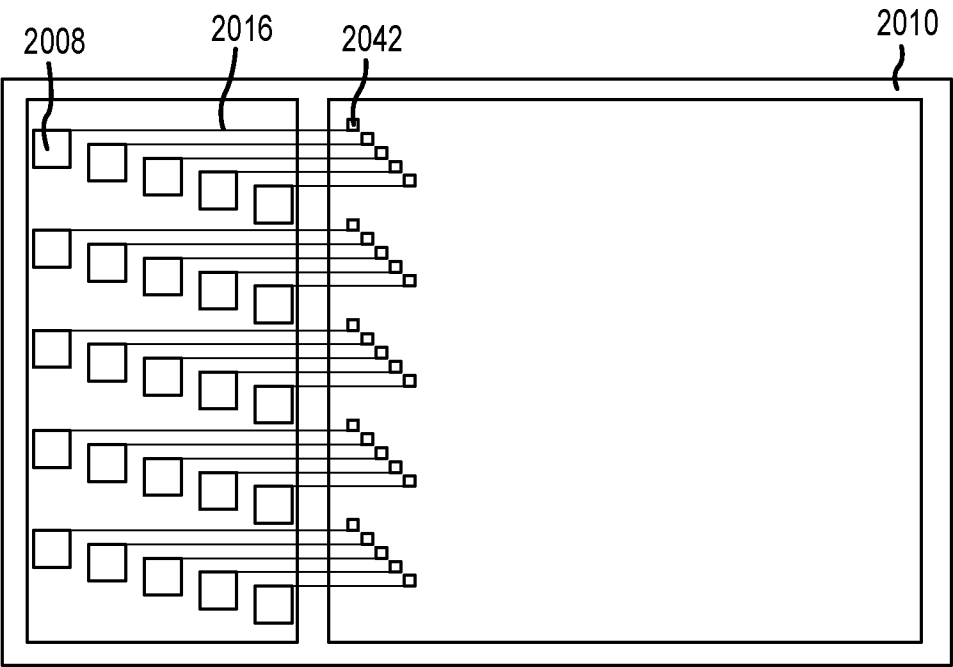
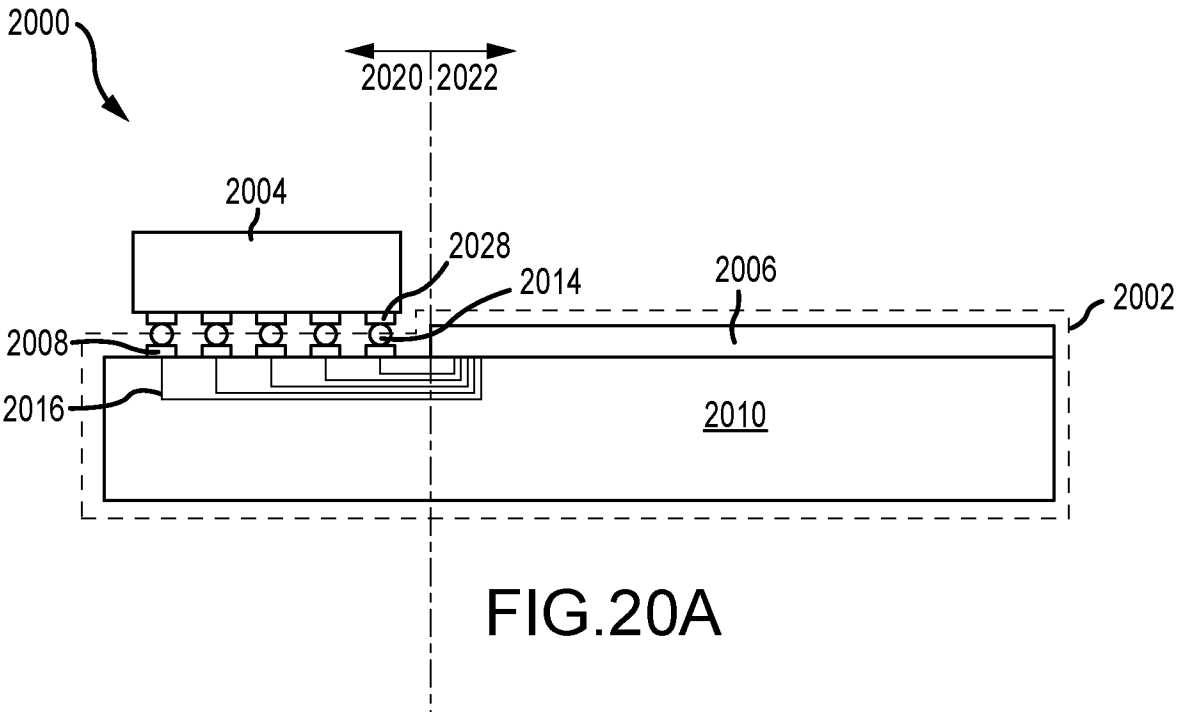


FIG.19



14/24

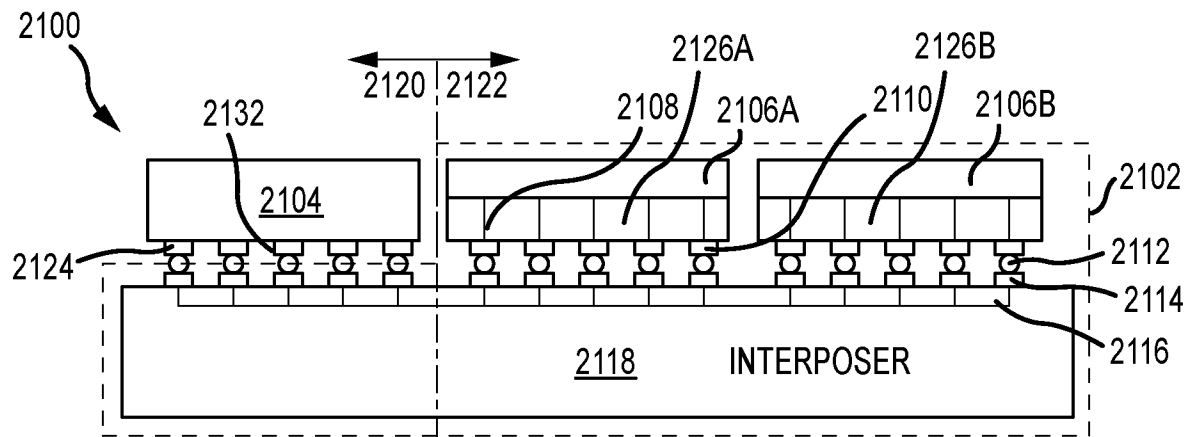


FIG.21A

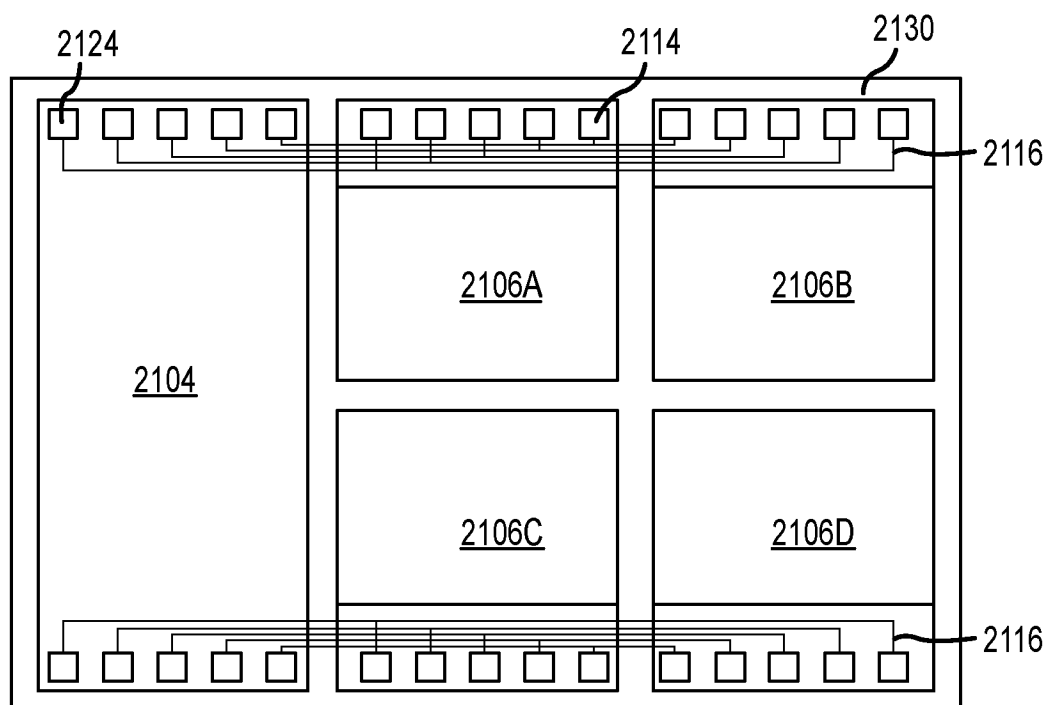


FIG.21B

15/24

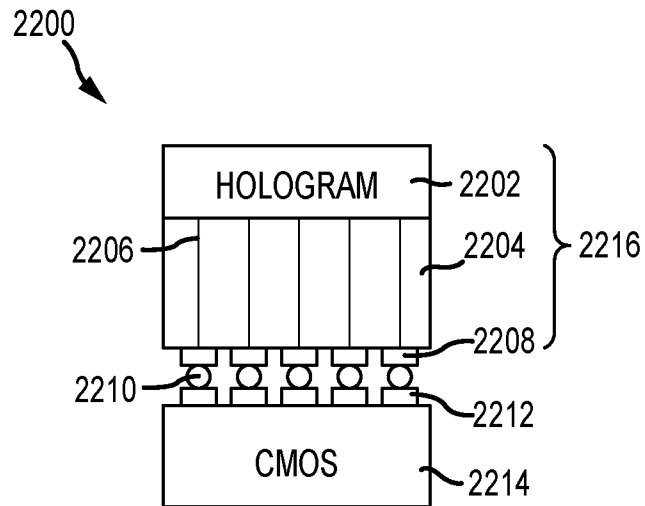


FIG.22

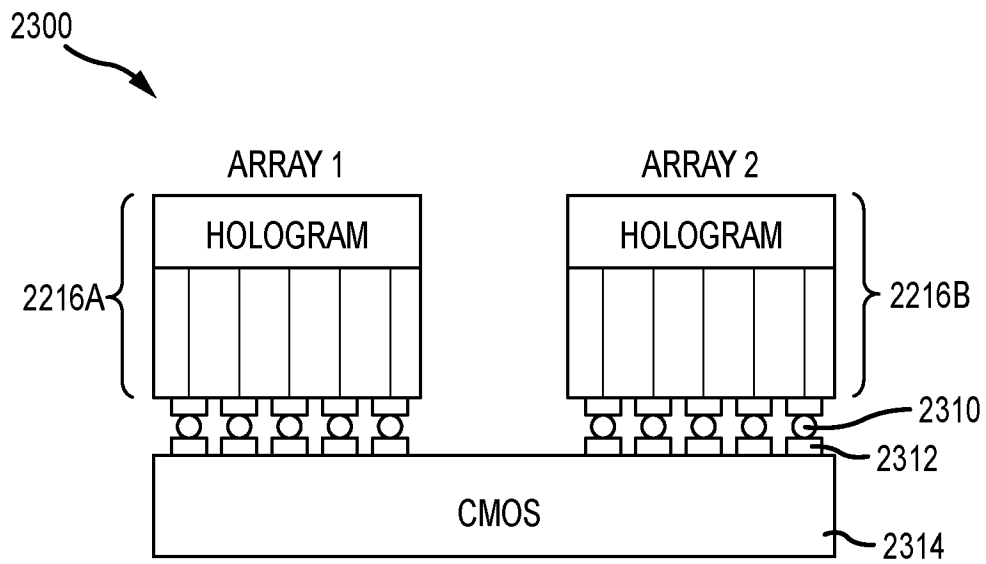


FIG.23

16/24

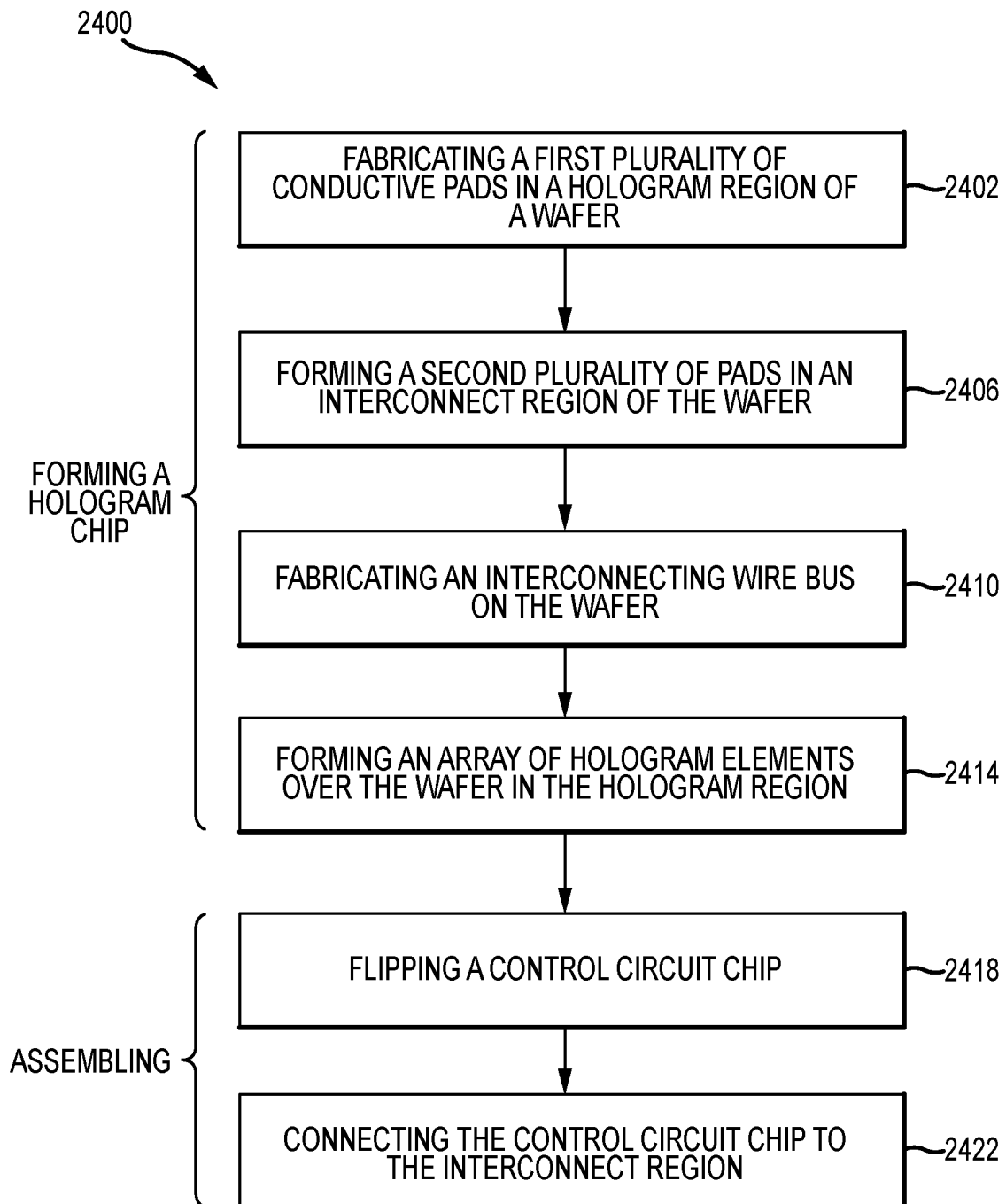


FIG.24

17/24

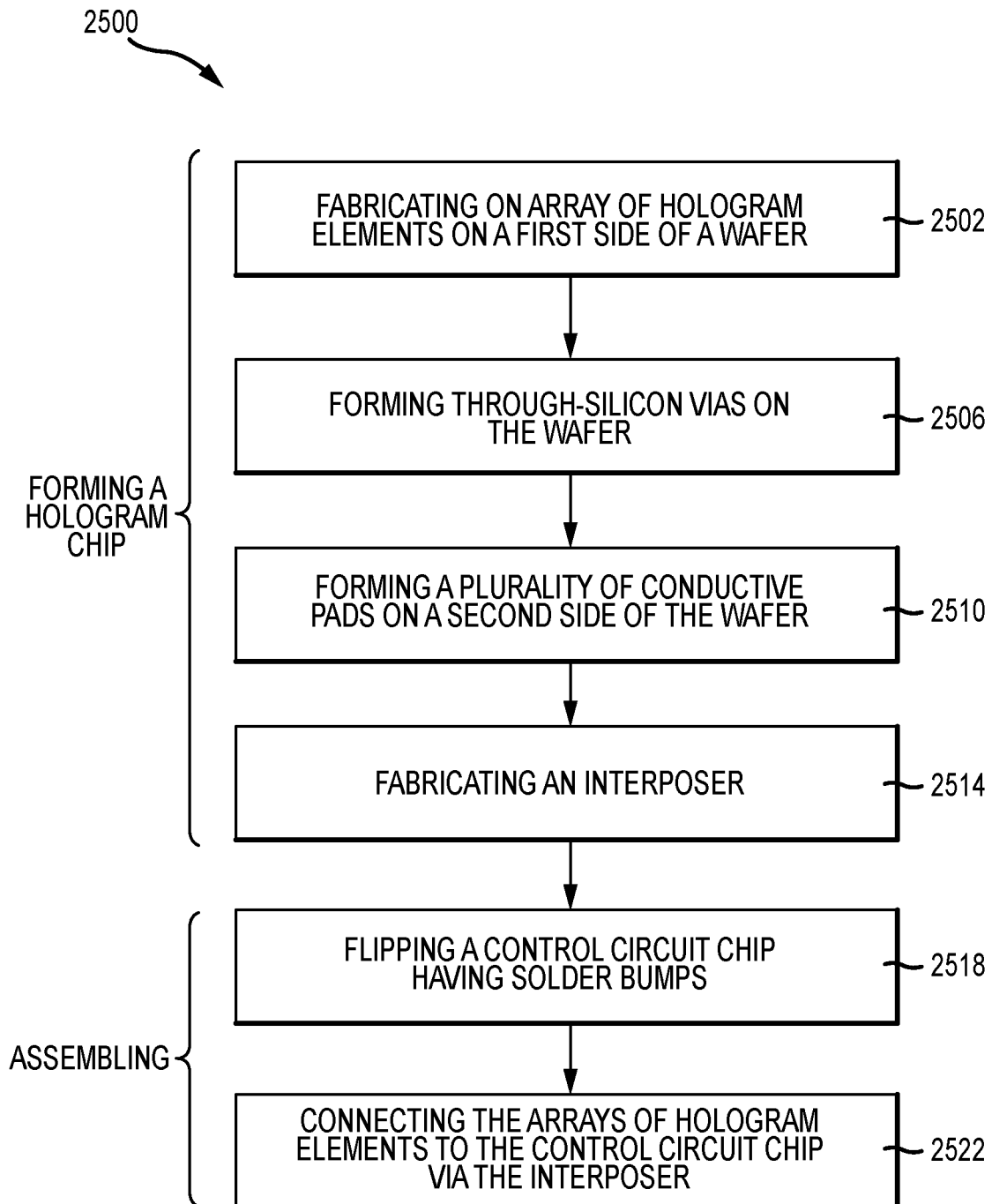


FIG.25

18/24

2600

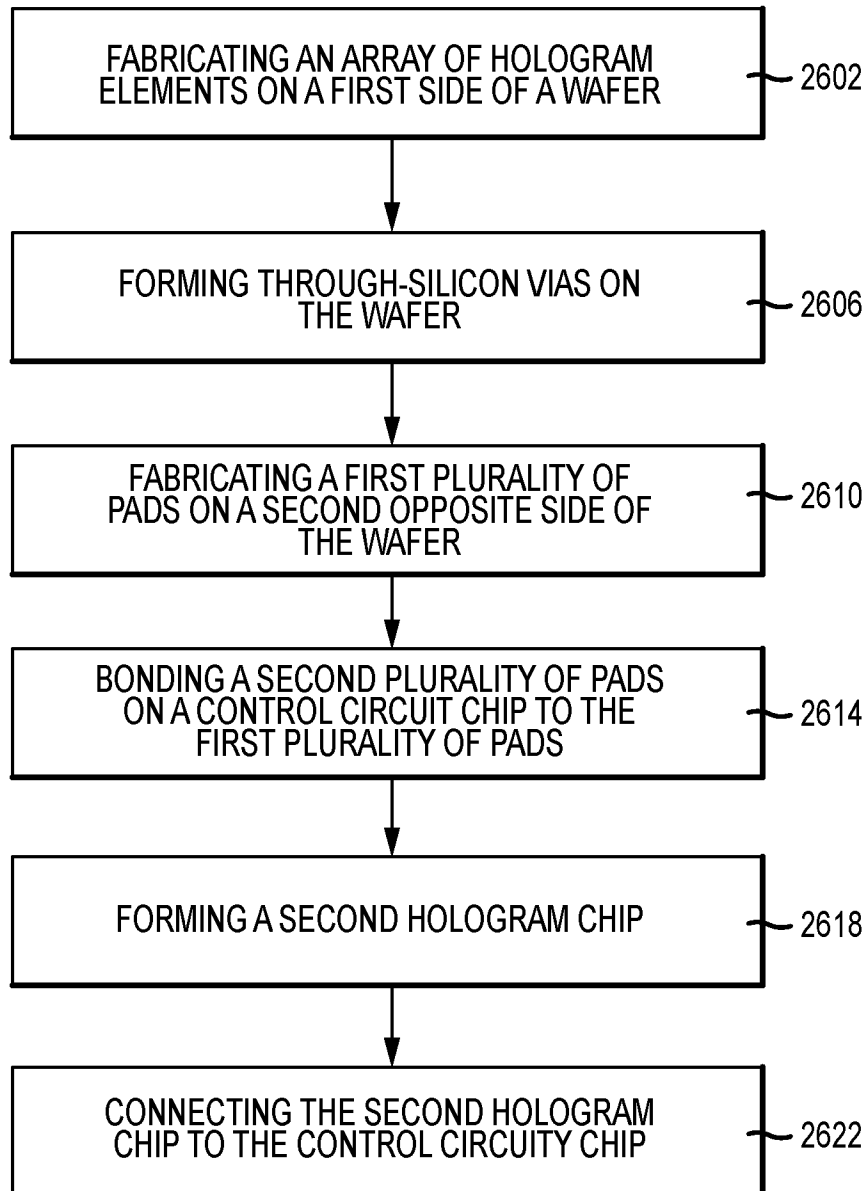
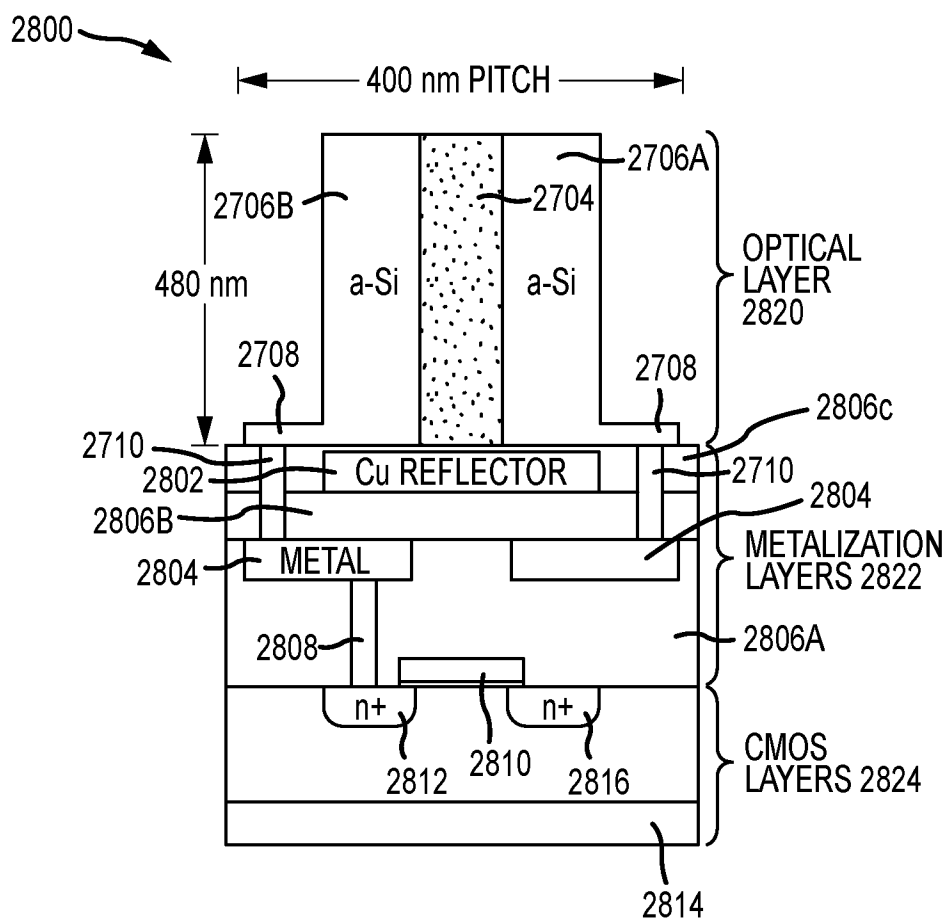
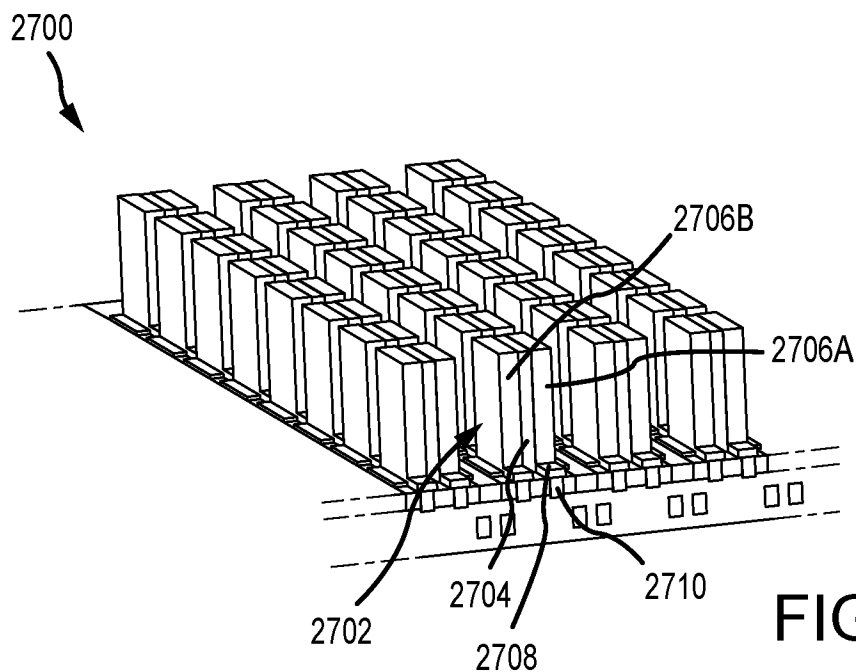


FIG.26

19/24



20/24

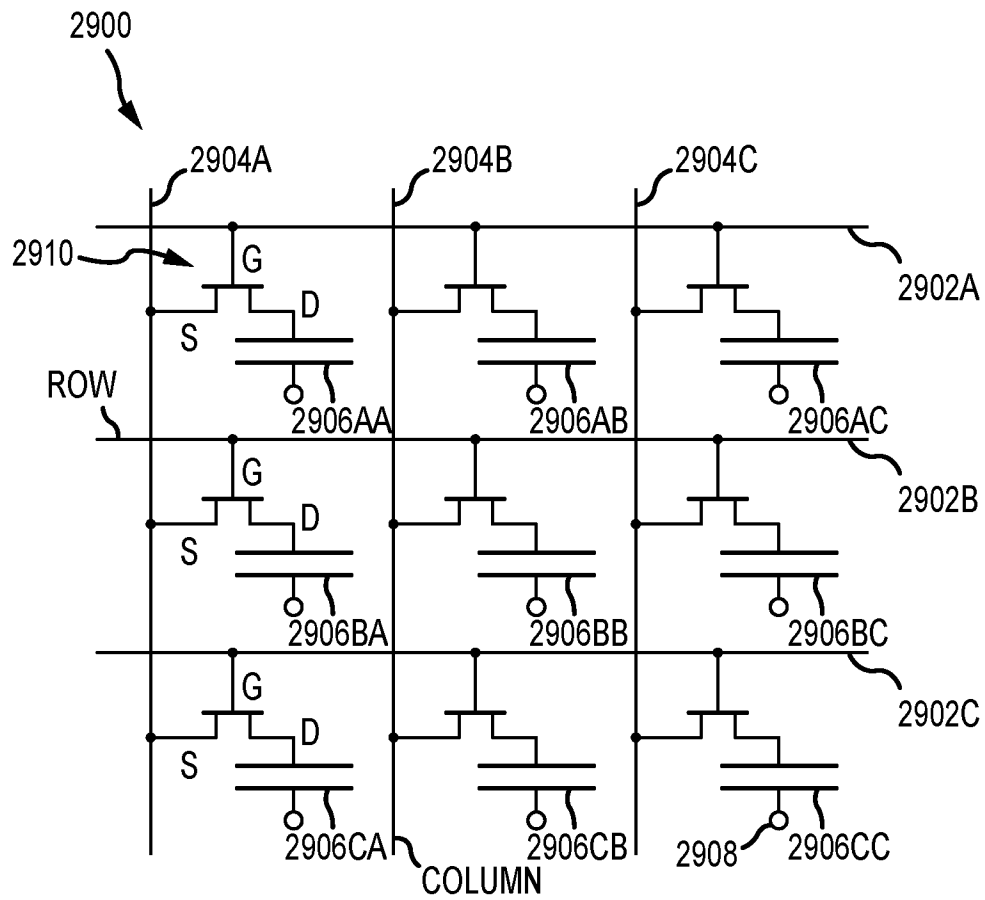


FIG.29

21/24

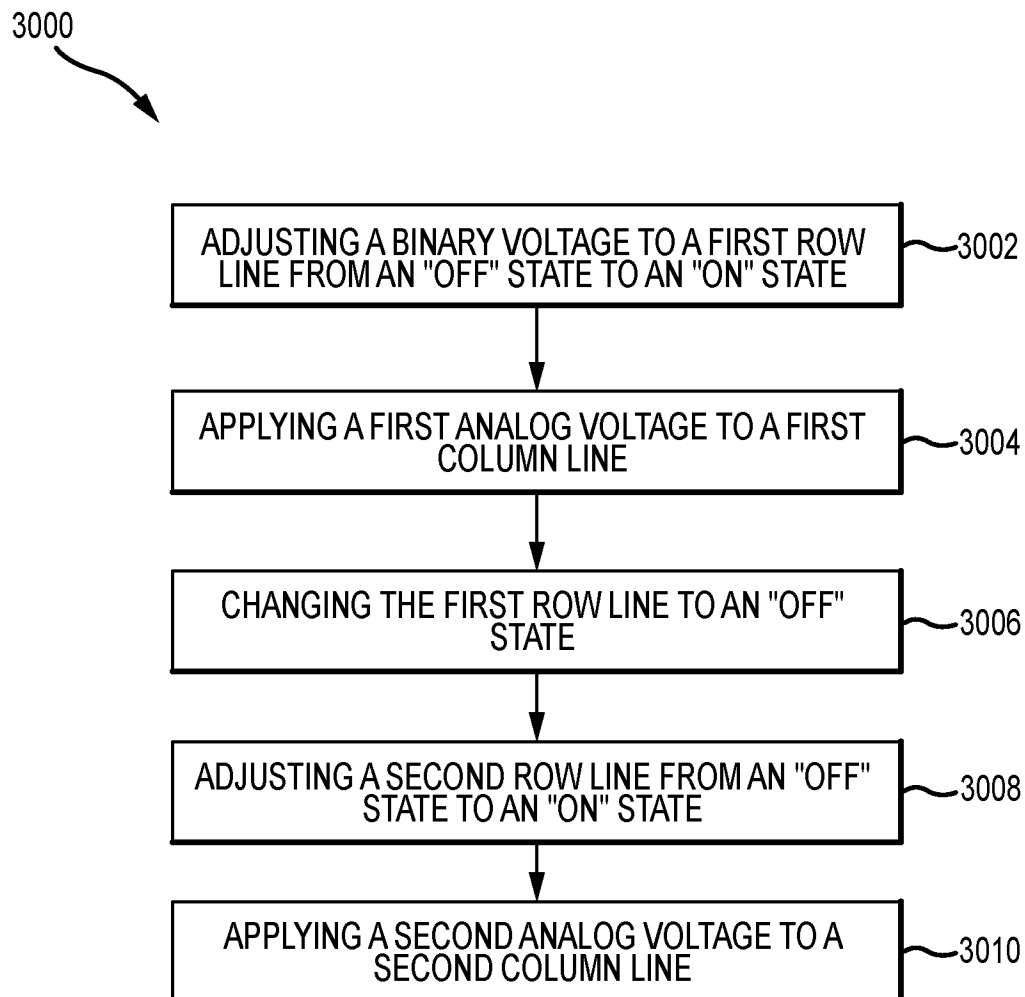


FIG.30

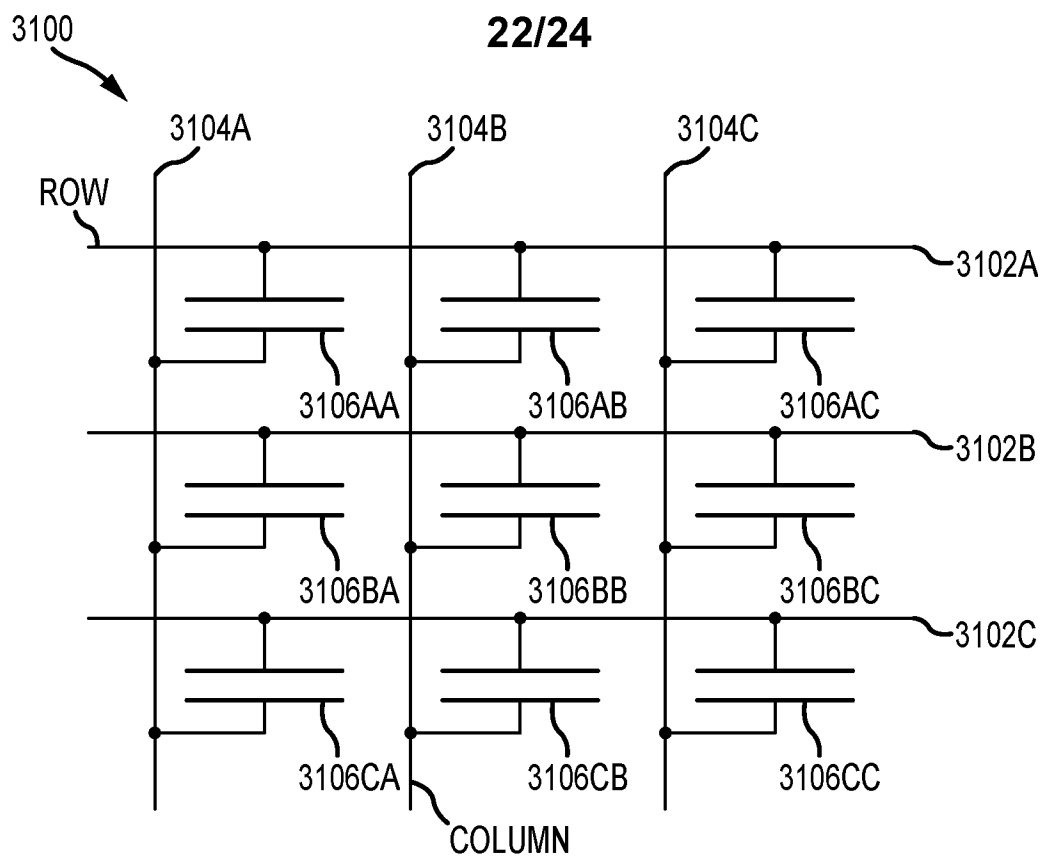


FIG.31

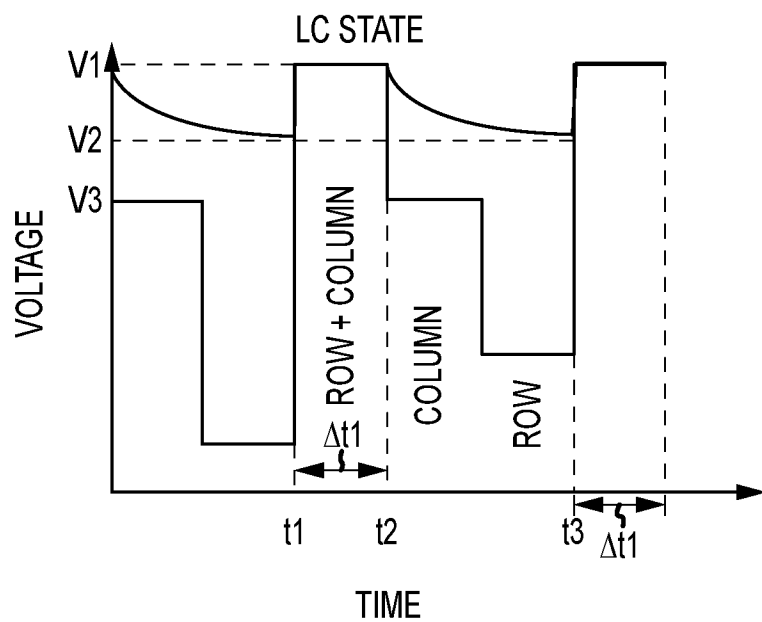


FIG.32

23/24

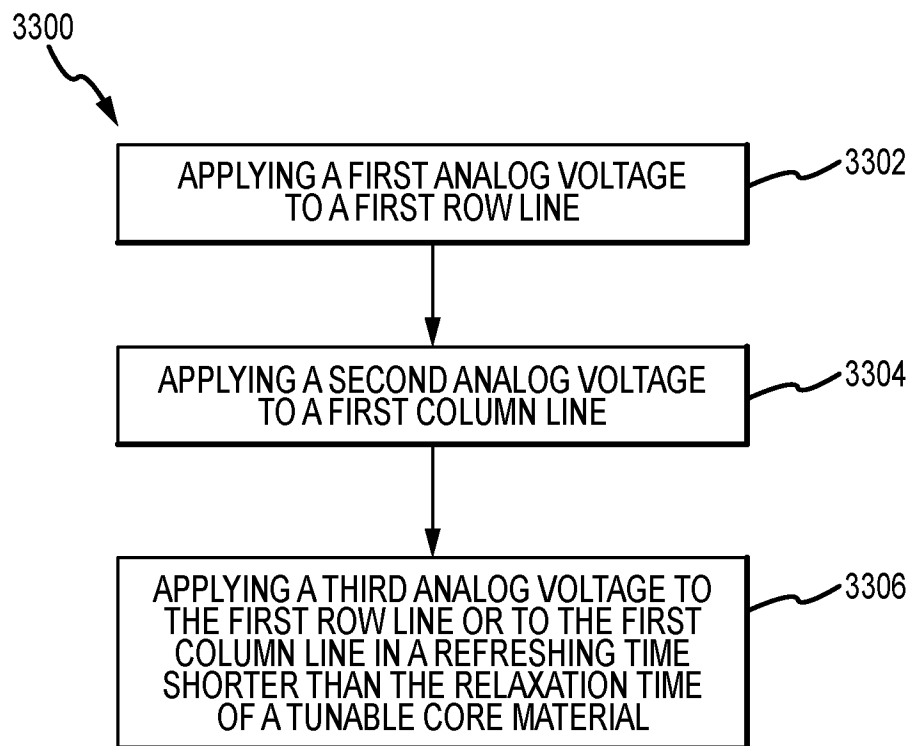


FIG.33

24/24

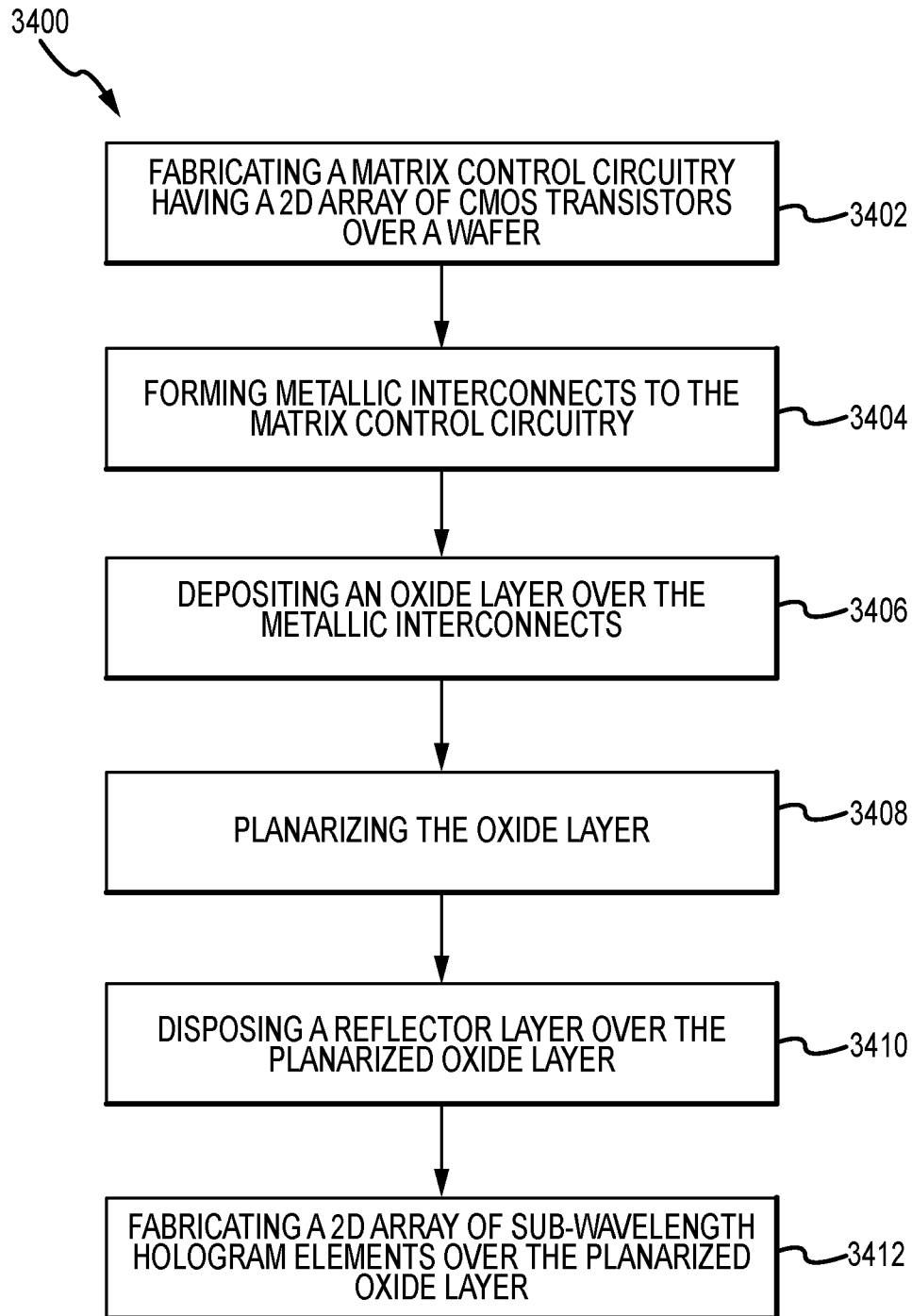


FIG.34

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2018/019269**A. CLASSIFICATION OF SUBJECT MATTER****G03F 7/20(2006.01)i, H01L 21/768(2006.01)i, H01L 21/8238(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G03F 7/20; B23P 17/04; H01P 1/20; H01L 25/16; H04J 14/02; H01Q 15/00; H01L 27/00; H01L 27/12; H01L 21/768; H01L 21/8238

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: manufacturing, metamaterial, wafer, copper, amorphous silicon, system, hologram, control, chip

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	ARBABI, AMIR et al. "Dielectric metasurfaces for complete control of phase and polarization with subwavelength spatial resolution and high transmission", Nature Nanotechnology, 2015, vol. 10, pages 937-943 (internal pages 1-8) See abstract; pages 1, 6; sample fabrication section; and figures 1b, 4b.	36-38, 45-47
Y		1-3, 21-23
Y	CN 103259097 A (UNIVERSITY OF ELECTRONIC SCIENCE AND TECHNOLOGY OF CHINA) 21 August 2013 See paragraph [0026]; and claim 5.	1-3
Y	US 2017-0047312 A1 (INTERNAL BUSINESS MACHINES CORPORATION) 16 February 2017 See paragraphs [0030], [0033], [0037]; and figure 1.	21-23
A	US 2011-0280573 A1 (COLLINGS, NEIL et al.) 17 November 2011 See the whole document.	1-3, 21-23, 36-38, 45-47
A	US 2005-0253211 A1 (MINAMIO, MASANORI et al.) 17 November 2005 See the whole document.	1-3, 21-23, 36-38, 45-47



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

01 June 2018 (01.06.2018)

Date of mailing of the international search report

04 June 2018 (04.06.2018)

Name and mailing address of the ISA/KR

International Application Division

Korean Intellectual Property Office

189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea



Facsimile No. +82-42-481-8578

Authorized officer

LEE, Ki Cheul

Telephone No. +82-42-481-3353



INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2018/019269

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☒ Claims Nos.: 27, 29, 33, 43, 50
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:
Claims 27, 29, 33, 43, and 50 refer to multiple dependent claims which do not comply with PCT Rule 6.4(a).

3. ☒ Claims Nos.: 4-20, 24-26, 28, 30-32, 34, 35, 39-42, 44, 48, 49
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of any additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

- ☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
- ☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
- ☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2018/019269

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
CN 103259097 A	21/08/2013	CN 103259097 B	20/01/2016
US 2017-0047312 A1	16/02/2017	US 2017-0186670 A1	29/06/2017
		US 2017-0186739 A1	29/06/2017
		US 2018-0040597 A1	08/02/2018
		US 2018-0114785 A1	26/04/2018
		US 9786641 B2	10/10/2017
		US 9935088 B2	03/04/2018
		US 9935089 B2	03/04/2018
US 2011-0280573 A1	17/11/2011	CN 102282508 A	14/12/2011
		EP 2364460 A1	14/09/2011
		JP 2012-508908 A	12/04/2012
		KR 10-2011-0097777 A	31/08/2011
		WO 2010-055351 A1	20/05/2010
US 2005-0253211 A1	17/11/2005	CN 100459138 C	04/02/2009
		CN 1697190 A	16/11/2005
		JP 2005-327893 A	24/11/2005
		JP 4606063 B2	05/01/2011
		KR 10-0665786 B1	09/01/2007
		KR 10-2006-0047180 A	18/05/2006
		TW 200537685 A	16/11/2005
		TW 1278992 B	11/04/2007
		US 2008-0304790 A1	11/12/2008
		US 7436053 B2	14/10/2008
		US 7563644 B2	21/07/2009