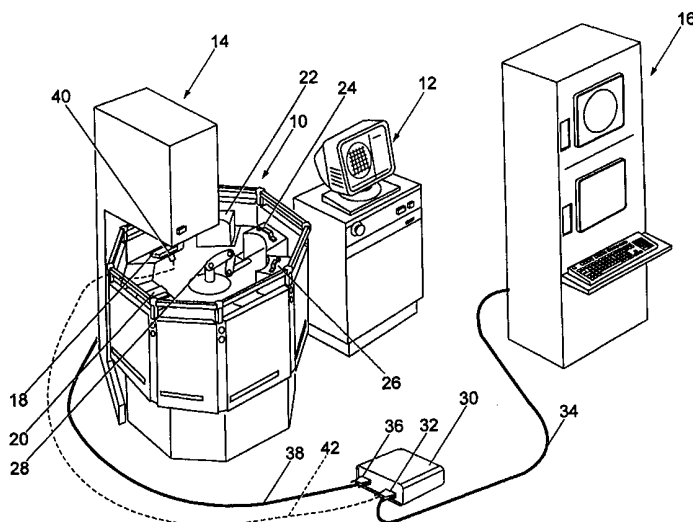




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<p>(21) International Application Number: PCT/GB99/00536 (22) International Filing Date: 22 February 1999 (22.02.99) (30) Priority Data: 9803842.5 25 February 1998 (25.02.98) GB (71) Applicant (for all designated States except US): SHIN-ETSU HANDOTAI EUROPE LIMITED [GB/GB]; Wilson Road, Toll Roundabout, Eliburn, Livingston, West Lothian EH54 7DA (GB). (72) Inventor; and (75) Inventor/Applicant (for US only): DAVIDSON, Brian [GB/GB]; Shin-Etsu Handotai Europe Limited, Wilson Road, Toll Roundabout, Eliburn, Livingston, West Lothian EH54 7DA (GB). (74) Agent: MURGITROYD & COMPANY; 373 Scotland Street, Glasgow G5 8AQ (GB).</p>		<p>(81) Designated States: GB, JP, KR, US, European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE). Published <i>With international search report.</i></p>

(54) Title: SEMICONDUCTOR WAFER INSPECTION APPARATUS



(57) Abstract

An inspection system for semiconductor wafers comprises a first inspection machine (10) including a wafer alignment station (18), at least one wafer inspection station (20), wafer loading, accept and reject stations and means (28) for transferring wafers between said stations; and a visual inspection machine including a camera unit (14) arranged to generate images of wafers located at the alignment station of the first inspection machine and a processor unit (16) connected to the camera unit and adapted to process said images and to generate accept and reject signals according to the result of the processing. The system further includes interface means (30) interconnecting the first inspection machine and the processor unit of the visual inspection machine. The interface is adapted to receive the accept and reject signals generated by the processor unit, to convert said signals into a format capable of interpretation by the first inspection machine, and to transmit the converted signals to the first inspection machine. The invention also includes an interface unit for use in the system.

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1 **"Semiconductor Wafer Inspection Apparatus"**

2

3 Field of the Invention

4

5 The present invention relates to apparatus employed in
6 the manufacture of wafers for use in the semiconductor
7 industry, particularly, but not exclusively, silicon
8 single crystal wafers. More particularly, the
9 invention relates to improvements in apparatus for the
10 inspection of wafers for quality control purposes
11 during the manufacturing process.

12

13 Background to the Invention

14

15 The inspection of wafers commonly involves the use of
16 different apparatus for checking different properties
17 of the wafers, such as flatness, thickness, resistivity
18 and surface defects. It is known to use a first item
19 of equipment to check flatness, thickness and
20 resistivity. An example of such equipment is known as
21 the ADE 9600. It is also known to use a second item of
22 equipment to perform automatic surface inspection of
23 the wafer. An example of such equipment is known as an
24 ORP.

25

1 The first item of equipment (referred to hereinafter as
2 the "first inspection machine") typically comprises:

3 at least one station for receiving a batch of
4 wafers which are to be inspected, the wafers being
5 contained in cassettes or baskets, an alignment station
6 at which individual wafers are aligned to a
7 predetermined orientation (using the orientation flat
8 or orientation notch which is formed in each wafer, as
9 is well known in the art);

10 at least one inspection station at which at least
11 one inspection operation is carried out;

12 at least one station for receiving wafers which
13 are judged to be acceptable following inspection;

14 at least one station for receiving wafers which
15 are rejected following inspection; and

16 robot handling means for transferring wafers
17 between the various stations.

18

19 The second item of equipment (referred to hereinafter
20 as the "visual inspection machine") typically comprises
21 a camera unit, which is used to generate an image of
22 the wafer under inspection, and a processor unit, which
23 processes the image generated by the camera and makes a
24 judgement as to whether the wafer ought to be accepted
25 or rejected.

26

27 It has been found to be convenient to set up the camera
28 of the visual inspection machine adjacent the alignment
29 station of the first inspection machine, such that the
30 camera views the wafer when it is located on the
31 alignment station. This allows the wafer to be aligned
32 by the first machine and visual inspection to be
33 carried out by the visual inspection machine prior to
34 further inspection by the first machine.

35

36 If a wafer fails inspection by the visual inspection

1 machine, it can be rejected prior to further inspection
2 by the first machine. A manual "reject" signal is
3 input to the first machine via a keypad by the operator
4 and the wafer is transferred from the alignment station
5 to the reject station by the robot handling means. If
6 the wafer passes visual inspection by the visual
7 inspection machine, a manual "accept" command is input
8 to the first machine in a similar manner. The wafer is
9 then transferred from the alignment station to the
10 inspection station(s) and inspection by the first
11 machine proceeds in the normal manner.

12
13 The first inspection machine and the visual inspection
14 machine are quite separate items of equipment which are
15 not designed to cooperate with one another and which
16 are not directly connected to one another. The
17 arrangement described above enables the alignment
18 system of the first machine to be employed for the
19 purposes of the visual inspection system. However,
20 manual input is required to the first machine following
21 visual inspection in order for the inspection process
22 to proceed. This necessarily reduces the overall
23 efficiency of the inspection process.

24
25 Summary of the Invention

26
27 In accordance with a first aspect of the invention,
28 there is provided a wafer inspection system comprising:
29 a first inspection machine including a wafer
30 alignment station, at least one wafer inspection
31 station, wafer loading, accept and reject stations and
32 means for transferring wafers between said stations;
33 and
34 a visual inspection machine including a camera
35 unit arranged to generate images of wafers located at
36 the alignment station of said first inspection machine

1 and a processor unit connected to said camera unit and
2 adapted to process said images and to generate accept
3 and reject signals according to the result of said
4 processing; characterised in that:

5 the system further includes interface means
6 interconnecting said first inspection machine and said
7 processor unit of said visual inspection machine, said
8 interface means being adapted to receive said accept
9 and reject signals generated by said processor unit, to
10 convert said signals into a format capable of
11 interpretation by said first inspection machine, and to
12 transmit said converted signals to said first
13 inspection machine.

14

15 Preferably, the system further includes sensor means
16 associated with said alignment station and adapted to
17 detect the presence of a wafer at said alignment
18 station and to transmit a signal to said processor unit
19 indicating the presence of a wafer at said alignment
20 station.

21

22 Preferably also, said sensor means is connected to said
23 processor unit via said interface means, said interface
24 means including timer means adapted to send a start
25 signal to said processor means after a predetermined
26 time period has elapsed following receipt of said
27 signal from said sensor means, said time period being
28 selected to be sufficient to allow the wafer to be
29 properly aligned at the alignment station.

30

31 Preferably also, said interface means is adapted to be
32 connected to an existing I/O port of said processor
33 unit and to an existing keypad connector port of said
34 first inspection machine, and to convert said accept
35 and reject signals received from said processor unit so
36 as to mimic manually input keystrokes which would

1 normally be transmitted to said keypad connector port
2 from a keypad.

3

4 In accordance with a second aspect of the invention,
5 there is provided interface apparatus for use in a
6 wafer inspection system in accordance with the first
7 aspect of the invention, comprising an interface unit
8 including a first input means for receiving a first
9 signal from a wafer detection sensor means, timer means
10 responsive to said first signal for outputting a start
11 signal after a predetermined time period following
12 receipt of said first signal, a first output means for
13 outputting said start signal, second and third input
14 means for receiving respective accept and reject
15 signals, first and second signal conversion means for
16 converting said accept and reject signals into a format
17 mimicking keypad keystrokes, and second output means
18 for outputting said converted signals.

19

20 Preferably, the interface apparatus further includes
21 wafer detection sensor means adapted to be mounted on
22 said alignment station of said first wafer inspection
23 machine, said wafer detection sensor means being
24 connected to said first input means of said interface
25 unit.

26

27 Preferably also, the interface apparatus, further
28 includes connector means for connecting said first
29 output means and said second and third input means to
30 an I/O port of said visual inspection machine and for
31 connecting said second output means to a keypad
32 connector port of said first inspection machine.

33

34 Brief Description of the Drawings

35

36 An embodiment of the invention will now be described,

1 by way of example only, with reference to the
2 accompanying drawings in which:

3

4 Fig. 1 is a perspective view of wafer inspection
5 apparatus incorporating an interface unit in accordance
6 with the invention; and

7 Fig. 2 is a circuit diagram of the interface unit
8 of Fig. 1.

9

10 Description of the Preferred Embodiment

11

12 Referring now to Fig. 1 of the drawings, a wafer
13 inspection system includes a first wafer inspection
14 machine, such as an ADE 9600, comprising a main wafer-
15 handling and inspection unit 10 and a control console
16 12, and a visual inspection machine, such as an ORP,
17 comprising a camera unit 14 and a processor unit 16.

18

19 As described above, the inspection unit 10 includes an
20 alignment station 18, inspection station(s) 20,
21 stations for receiving wafer cassettes 22, 24, 26 for
22 loading batches of wafers into the unit 10 and for
23 receiving accepted and rejected wafers, and a robot
24 handling arm 28. The visual inspection camera unit 14
25 is located over the alignment station 18 and is
26 connected by a cable or the like (not shown) to the
27 processor unit 16.

28

29 The arrangement described thus far is conventional, as
30 described above. A wafer located at the alignment
31 station 18 would be imaged by the camera unit 14 and
32 the image would be processed by the processor unit 16,
33 which would display an accept or reject signal
34 depending on the outcome of the visual inspection. An
35 operator would then manually input a corresponding
36 accept or reject signal to the first inspection machine

1 10, 12, by means of a keypad connected to a keypad port
2 on the first machine.

3
4 In accordance with the present invention, there is
5 provided an interface unit 30 which connects the visual
6 inspection processor 16 directly to the first
7 inspection machine 10, 12 so as to provide a greater
8 degree of automation in the use of the overall
9 inspection system. The interface unit has a first
10 input/output (I/O) port 32 connected by a first cable
11 34 to an existing I/O port (not shown) of the visual
12 inspection processor unit, and a second I/O port 36
13 connected by a second cable 38 to an existing keypad
14 connection port (not shown) of the first inspection
15 machine 10,12.

16
17 Further in accordance with the invention, there is
18 provided a sensor 40 which is mounted on or adjacent to
19 the alignment station 18 of the first inspection
20 machine 10 and which is adapted to detect the presence
21 of a wafer at the alignment station. The sensor 40 may
22 be of any suitable type, such as an optical sensor.
23 The sensor 40 is also connected to the first I/O port
24 of the interface unit 30, by a further cable indicated
25 schematically by broken line 42.

26
27 The system in accordance with the invention operates as
28 follows.

29
30 A batch of wafers is loaded into the first inspection
31 machine 10. The robot arm 28 transfers a first wafer
32 to the alignment station 18. The sensor 40 detects the
33 presence of the wafer and transmits a signal to the
34 interface unit 30 (input "OPTO" on I/O port 32, Fig.
35 2). The signal starts a timer (IC1 and associated
36 circuitry, Fig. 2) in the interface unit 30. The timer

1 provides a predetermined delay (suitably 20 seconds)
2 while the wafer is aligned by the alignment station 18.

3
4 Once the delay period has elapsed, the timer generates
5 an output signal which energises a first relay 44,
6 which in turn transmits a "Start" signal to the visual
7 inspection processor 16. Components IC4 serve to
8 convert the transient output from the timer into a
9 square wave suitable for controlling the relay 44.

10
11 Once the Start signal is received, the processor unit
12 processes the image of the pre-aligned wafer generated
13 by the camera unit 14, and generates either an Accept
14 signal or a Reject signal depending on the results of
15 the inspection process. These signals are transmitted
16 via the I/O port of the processor unit 16 to respective
17 pins of the first I/O port of the interface unit 30.
18 The Accept and Reject signals control the operation of
19 respective pairs of ganged relays 46 and 48. The
20 relays are in turn connected to the second I/O port 36
21 of the interface unit 30, and thence to the keyboard
22 connector port of the first inspection machine 10. In
23 each case, one of the relays is normally closed and the
24 other is normally open. This arrangement enables the
25 output signals from the interface unit 30 to the first
26 inspection machine 10 to mimic the keystroke signals
27 which the first inspection machine 10 would normally
28 receive from a manually operated keypad; i.e. an Accept
29 or Reject keystroke followed by an "Enter" or "Carriage
30 Return" keystroke.

31
32 The invention thus allows the first inspection machine
33 10,12 and the visual inspection machine 14,16 to
34 operate together in a fully integrated manner, without
35 the need for manual intervention by an operator and
36 without any modification of either of the inspection

1 machines 10,12 and 14,16, other than the mounting of
2 the sensor 40 on the alignment station 18 of the first
3 machine 10,12.

4
5 It is possible that the function of the sensor 40 could
6 be performed by a sensor forming an integral part of
7 the first inspection machine. However, this would
8 require a degree of internal modification of the first
9 machine to enable such a sensor to communicate with the
10 processor unit of the visual inspection machine. The
11 interface unit could also be incorporated into either
12 the first inspection machine or the visual inspection
13 machine. Again, this would require a degree of
14 modification to the relevant machine.

15

16 Improvements and modifications may be incorporated
17 without departing from the scope of the invention.

18

1 **Claims**

2

3 1. A wafer inspection system comprising:

4 a first inspection machine including a wafer
5 alignment station, at least one wafer inspection
6 station, wafer loading, accept and reject stations and
7 means for transferring wafers between said stations;
8 and

9 a visual inspection machine including a camera
10 unit arranged to generate images of wafers located at
11 the alignment station of said first inspection machine
12 and a processor unit connected to said camera unit and
13 adapted to process said images and to generate accept
14 and reject signals according to the result of said
15 processing; characterised in that:

16 the system further includes interface means
17 interconnecting said first inspection machine and said
18 processor unit of said visual inspection machine, said
19 interface means being adapted to receive said accept
20 and reject signals generated by said processor unit, to
21 convert said signals into a format capable of
22 interpretation by said first inspection machine, and to
23 transmit said converted signals to said first
24 inspection machine.

25

26 2. A system as claimed in Claim 1, further including
27 sensor means associated with said alignment station and
28 adapted to detect the presence of a wafer at said
29 alignment station and to transmit a signal to said
30 processor unit indicating the presence of a wafer at
31 said alignment station.

32

33 3. A system as claimed in Claim 2, wherein said
34 sensor means is connected to said processor unit via
35 said interface means, said interface means including
36 timer means adapted to send a start signal to said

1 processor means after a predetermined time period has
2 elapsed following receipt of said signal from said
3 sensor means, said time period being sufficient to
4 allow the wafer to be properly aligned at the alignment
5 station.

6
7 4. A system as claimed in any preceding Claim,
8 wherein said interface means is adapted to be connected
9 to an existing I/O port of said processor unit and to
10 an existing keypad connector port of said first
11 inspection machine, and to convert said accept and
12 reject signals received from said processor unit so as
13 to mimic manually input keystrokes which would normally
14 be transmitted to said keypad connector port from a
15 keypad.

16
17 5. Interface apparatus for use in a wafer inspection
18 system as claimed in any one of Claims 1 to 4,
19 comprising an interface unit including a first input
20 means for receiving a first signal from a wafer
21 detection sensor means, timer means responsive to said
22 first signal for outputting a start signal after a
23 predetermined time period following receipt of said
24 first signal, a first output means for outputting said
25 start signal, second and third input means for
26 receiving respective accept and reject signals, first
27 and second signal conversion means for converting said
28 accept and reject signals into a format mimicking
29 keypad keystrokes, and second output means for
30 outputting said converted signals.

31
32 6. Interface apparatus as claimed in Claim 5, further
33 including wafer detection sensor means adapted to be
34 mounted on said alignment station of said first wafer
35 inspection machine, said wafer detection sensor means
36 being connected to said first input means of said

1 interface unit.

2

3 7. Interface apparatus as claimed in Claim 5 or Claim
4 6, further including connector means for connecting
5 said first output means and said second and third input
6 means to an I/O port of said visual inspection machine
7 and for connecting said second output means to a keypad
8 connector port of said first inspection machine.

9

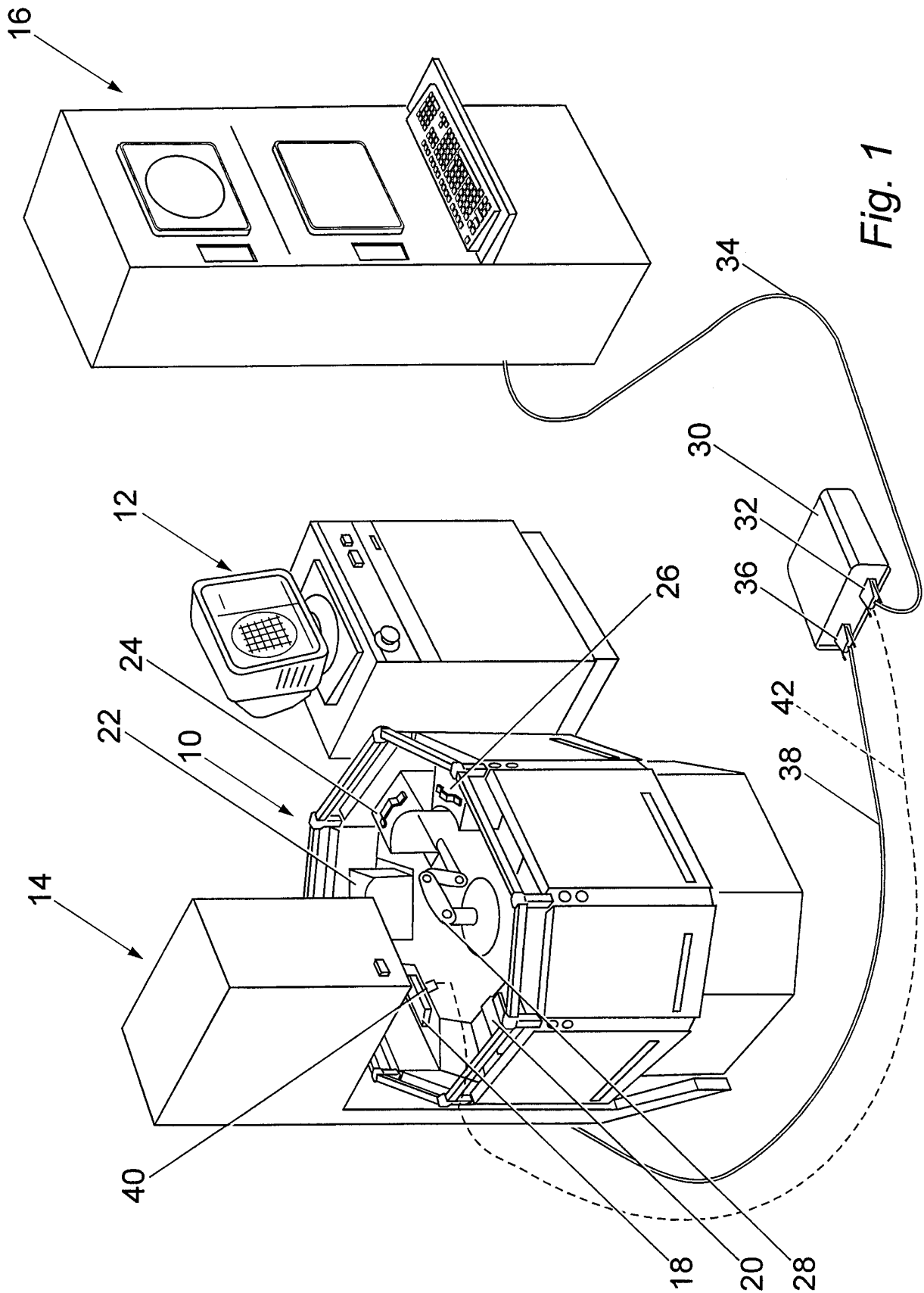
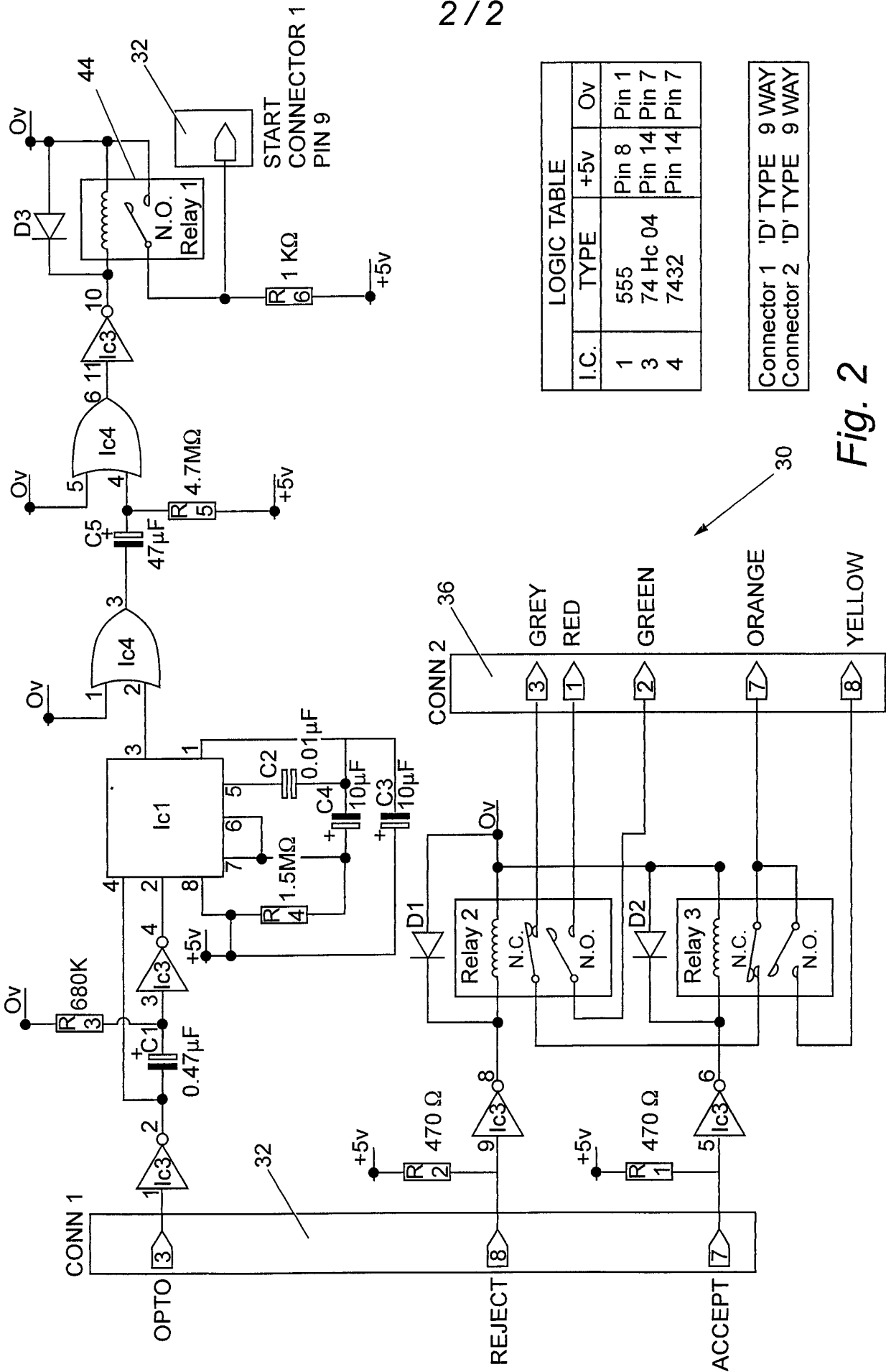


Fig. 1



INTERNATIONAL SEARCH REPORT

International Application No
PCT/GB 99/00536

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H01L21/66

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	PATENT ABSTRACTS OF JAPAN vol. 013, no. 005 (E-701), 9 January 1989 & JP 63 216354 A (MITSUBISHI ELECTRIC CORP), 8 September 1988 see abstract ---	1,2
Y	PATENT ABSTRACTS OF JAPAN vol. 097, no. 010, 31 October 1997 & JP 09 167788 A (SHIN ETSU HANDOTAI CO LTD), 24 June 1997 see abstract ---	1,2
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Date of the actual completion of the international search 11 May 1999	Date of mailing of the international search report 20/05/1999
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INTERNATIONAL SEARCH REPORT

International Application No

PCT/GB 99/00536

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No

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