Abstract: The present invention relates to a system comprising at least a first and a second essentially digital portion, and an essentially digital portion, said first and said second analogue portion forming a part of a unidirectional circular network, and further comprising - first communication means provided between said digital portion and said first analogue portion, - second communication means provided between said at least first and second analogue portions, whereby said first and second communication means are configurable for establishing communication between said digital portion and said second analogue portion and whereby said first and second communication means are arranged to determine if a packet communicated over said first or second communication means is of interest for any of said analogue portions.
— before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.
SYSTEM WITH DISTRIBUTED ANALOGUE RESOURCES

Field of the invention

[0001] The present invention relates to a system comprising at least two analogue network parts and a digital network part. It also relates to a method for controlling and managing such a system.

State of the art

[0002] An increasing number of consumer devices get equipped with wireless interfaces. The number of different wireless interfaces in a single device rises. Cost pressure requires the implementation of multiple wireless standards e.g. in a single package or on a single chip. Analogue/RF front-end designers aim at software-reconfigurable (SRR) or software-defined radios (SDR), which share a significant amount of front-end building blocks. When shared, however, these blocks have to be adjustable and/or programmable, hence the amount of control signals increases. In addition, the usage of more advanced technology (130-nm, 90-nm, ...) degrades the reliability of the manufactured designs. To avoid too large design margins (and the accompanying cost), digital compensation techniques become a must to compensate for the analogue imperfections. Again, these techniques require more programmability and observability of the front-end; also here, more control pins (control & monitoring) are required.
Flexible front-end designs feature an increasing amount of control pins. Single standard front-ends may face more control pins since digital compensation techniques will be used. For multiple standard front-ends, flexibility requires an increase of control facilities. As a consequence, the amount of control pins is tremendously increasing.

Since current front-end designs still exhibit only a moderate amount of functionality to monitor and steer, state-of-the-art solutions for interconnect schemes essentially rely on point-to-point or bus-based topologies and plain digital solutions. These approaches however have significant disadvantages in the context of analogue/RF designs.

Point-to-point topologies essentially scale linearly with at least the number of control points in the analogue design. When implemented digitally, they also scale linearly with the number of control bits per control point. This introduces a significant routing overhead and design and verification cost. Three major issues arise with current state-of-the-art solutions.

The first issue relates to point-to-point routing of the control pins to each analogue block on the chip. The main disadvantage of such approach is missing scalability. Adding control bits requires a change in the floorplanning, routing, connections per module, and possibly even in the I/O pads of the chip.

Secondly, digital Network-on-Chip (NoC) solutions (layer 3) are too complicated. Digital bus solutions (layer 2) usually require parallel busses and do not take into account crosstalk requirements on analogue/RF chips. Bus-based solutions come with a large overhead in routing area and control logic. Moreover, parallel busses have a higher cross-talk potential and are harder to shield.
than a single bit line. Moreover, bus protocols are not necessarily made for the specific requirements in a front-end context (slow vs. fast, short vs. long instruction words, broadcast/multi-cast to different receiving nodes).

Thirdly, the usage of plain digital signalling may be considered. A better choice is the usage of e.g. differential and low-voltage signalling (e.g. Low Voltage Differential Signalling (LVDS)).

Hence, flexible front-ends are a necessity in the context of reactive, software-reconfigurable, software-defined or cognitive radios. An essential feature is controllability and observability of all front-end resources in order to guarantee reliable, energy-efficient, and quality-aware operation.

Patent application EP1351403-A2 relates to a transceiver with front-end reconfiguration. The described interconnect scheme facilitates the access of an essentially digital controller to the resources on an analogue/RF chip for both steering and monitoring purposes.

Aims of the invention

The present invention aims to provide a front-end design with improved controllability and observability capabilities.

Summary of the invention

The present invention relates to a system comprising at least a first and a second essentially analogue portion and an essentially digital portion. The first and second analogue portions form a part of a unidirectional circular network. The system further comprises a first communication means provided between the digital portion and the first analogue portion.
second communication means provided between the at least first and second analogue portions, whereby the first and second communication means are configurable for establishing communication between the digital portion and the second analogue portion and whereby the first and second communication means are arranged to determine if a packet communicated over the first or second communication means is of interest for any of the analogue portions.

In a preferred embodiment each of the first and the second communication means comprises interface circuitry for each circuit connected by the communication means.

In a specific embodiment the analogue portions and the second communication means are on one chip. Alternatively, they are implemented in a single integrated circuit or in a single package.

Preferably the first and second communication means are digital.

Advantageously the system is arranged for providing an information flow for controlling and monitoring the analogue portions guided by the first and second communication means. The analogue portions are preferably part of analogue RF front ends.

In a preferred embodiment the parameters for communication over the first and second communication means are selectable such that interference of the RF functionality is minimised. The parameters for communication are preferably selected from the group of parameters comprising \{frequency, signal amplitude, packet length, packet format\}.

In another preferred embodiment the digital portion is a part of a baseband processor. Advantageously the baseband processor is implemented in the same
integrated circuit as the rest of the system. Alternatively, the baseband processor is implemented in the same package as the rest of the system.

[0019] In an advantageous embodiment the digital portion is provided with a Quality of Experience manager.

[0020] Preferably the communication over the first and the second communication means is differential. The first and second communication means are advantageously arranged for low voltage differential signalling.

[0021] In another preferred embodiment the communication on the first or the second communication means is unidirectional. The communication advantageously is one-bit communication.

[0022] In a specific embodiment the length of said packets is adaptable to at least two speeds of communication.

[0023] In a further embodiment the system further comprises a plurality of additional analogue portions arranged for forming together the first and the second analogue portion the unidirectional circular network.

[0024] The present invention also relates to a system comprising a first subsystem being a system as previously described, a second subsystem also being a system as described and an additional digital portion for connecting the first and the second subsystem.

[0025] In another aspect the invention relates to a method for controlling an information flow in a system as previously described, comprising the steps of:

- receiving configuration information for at least one of the analogue portions,

- arranging the configuration information in the digital portion, and
transmitting the arranged configuration information over the unidirectional circular network.

Preferably the configuration information comprises packet format information.

In a further aspect the invention relates to a method for managing a system as previously described, comprising the steps of:

- transmitting with the digital portion over the unidirectional circular network a request for status information of at least one of the analogue portions,
- receiving said request with the at least one analogue portion,
- providing to the digital portion the status information.

The digital portion is preferably provided with a Quality of Experience manager. In a specific aspect the invention relates to the use of this method for Quality-of-Experience management.

### Short description of the drawings

Fig. 1 represents a digitally-controlled analogue/RP chip.

Fig. 2 represents a network segment with a closed ring structure and bridge to connect to a second segment.

Fig. 3 represents a combination of multiple single network segments.

Fig. 4 represents an alternative combination of multiple single network segments.

Fig. 5 represents an architecture of the master node.

Fig. 6 represents an architecture of the slave node.
Fig. 7 represents an example instantiation of a control network.

**Detailed description of the invention**

The present invention relates to a RF, analogue or mixed-signal communications front-end system with an essentially digital interconnect scheme that links a distributed set of analogue/RF resources (that altogether may form a transceiver solution) to a digital control unit for steering and monitoring purposes. It establishes essentially a second interconnect for control and management purposes besides the typically analogue or mixed-signal data path.

The proposed solution describes a complete architecture of a simple-to-implement and scalable network-on-chip specifically designed for integration on analogue/RF chips (see Fig.1). Details of this architecture and its implementation are described further on. The solution extends to an off-chip network that is implemented in the same way. In this case, a bridge functionality is needed that connects the two independent networks (on-chip, off-chip). Also a splitting of the on-chip network into several network segments is possible. In this case, network segments are connected by bridges, too.

The generic architecture concept introduces an implementation manager and a network on the analogue chip. The network takes care of exchanging information between the implementation manager and preferably at least two distributed analogue/RF blocks on the chip. The architecture concept comprises an on- and off-chip communication network, the logical packet-based communication scheme and the node architectures, whereby distinction is made between master nodes and slave nodes.
Single Network Segment

[0038] Important for a single network segment is the closed ring structure (see Fig. 2). The use of this structure allows eliminating layer 3 networking complexity. Moreover, the usage of a distinct send/receive end allows a strict split of the medium.

[0039] Information travels unidirectionally. The closed ring structure allows each node being reachable by every other node. The main mode is however that the bridge initiates communication. Hence, the ring is logically broken at the bridge. The terms 'bridge' and 'master node' are synonyms. Slave nodes are also referred to as nodes. The master node determines the main signalling format and is used - if needed - to provide clocking. The master node is also the only connection to another network segment or to an off-chip network.

Operation principle

[0040] A communication network architecture is proposed based on a ring topology (unidirectional circular topology). The network can be subdivided into segments that are linked with each other through bridges. Communication in a single segment is unidirectional. The ring topology allows the bridge to pass information to the node as well as to receive information from a node reusing the same path.

[0041] Important is the closed ring structure. The use of this structure allows eliminating layer 3 networking complexity. Moreover, the usage of a distinct send/receive end (see node description below) allows a strict split of the medium.

[0042] Information travels unidirectionally. The closed ring structure allows each node to be reachable by every other node. Main mode is however that the bridge
initiates communication. Hence, the ring is logically-broken at the bridge.

[0043] The master node determines the main signalling format and is used -if needed- to provide clocking. The master node is also the only connection to another network segment or an off-chip network.

**Extension to Multiple Network Segments**

[0044] A network comprising multiple instantiations of the single network segment architecture and additional bridging functionality linking them is a straightforward extension of the ring topology (Fig. 3). In this case, bridge functionality is needed to connect the two independent networks (on-chip, off-chip). Also a splitting of the on-chip network into several network segments is possible. Also in this case, the various network segments are connected by bridges (Fig. 4).

[0045] A first application is when placing multiple front-end chains on the same chip. A second application concerns the link between an on-chip network and an off-chip network. In this case, the bridge connects the chip to the printed circuit board.

[0046] A single network-segment based on a ring topology can also hook up through a bridge with a classical network segment, e.g. a bus or a point-to-multipoint segment. This does not require any modification of the single circular network segment architecture.

**Considerations concerning the Physical Interconnect**

[0047] Interconnection between the nodes can use all physical communication schemes known in the communications domain. In particular, but not limited thereto, reference is made to bus-based parallel communication and serial communication.
Specifically for analogue/RF transmission, it is important to use analogue-friendly signalling over the connections between the nodes (e.g. low crosstalk).

A serial communication scheme is particularly interesting, since it does not require topology changes if the amount of payload changes (e.g. no increase of the bus width). Instead, higher throughput translates into higher clock frequency or more frequent packet transmission. Hence, one can advantageously opt for a serial communication scheme.

An investigation of the required communication throughput and latency for typical analogue/RF transceiver control reveals that a clock frequency of about 120 MHz is sufficient for IEEE 802.11-compliant WLAN designs. This is a moderately low frequency that allows low-cost implementation and -together with the possibility to easily adjust this frequency in the same range- prevents creation of disturbing spurs for the analogue/RF data path. The latter feature is of primordial importance in this context and is a problem which is not of any significance in a purely digital context.

Differential signalling on-chip is used. On-board this is a standard technique both for analogue design and high-speed digital design. However, it is normally not used for busses etc. The advantage is a balanced cross-talk signal that compensates itself. Moreover, lower digital signal levels are used, i.e. in particular, the usage of LVDS on-chip is preferable. LVDS is normally used off-chip on boards. LVDS is a mixed-signal solution working with small voltage signals (and differential); this means 300-400 mV instead of e.g. 1.2V for a 130-nm technology. Driver and receiver have built-in DC offset compensation to allow resistance against drifts.
A further advantage of LVDS is low power consumption due to the low voltage signals and current mode operation. The difference between LVDS off-chip and on-chip is that one can design for much lower capacitance drive on-chip. Hence, only existing LVDS solutions have to be resized, which keeps the approach cheap. The resized version uses even less power than the off-chip version.

Regarding node architecture and functionality distinction is made between two types of nodes: master nodes and slave nodes.

Architecture of a Master Node

The master node consists of an off-chip I/O interface (modrxoff, modtxoff), an on-chip I/O interface (modrxon, modtxon), and the bridge module (modbridge) (Fig. 5).

A functional description is now given. The I/O interfaces make abstraction of the physical communication interface. The blocks can be transparent since a serial 1-bit protocol and digital CMOS levels are used. Alternatively, these blocks could contain the differential and low-voltage/CMOS-level conversion functionality. The bridge may perform the following functions.

- Serial read and interpretation of the packet structure including Wait for trailing sync bit, Retrieve slow/fast flag, Retrieve read/write flag, Retrieve address (serial-to-parallel conversion), Retrieve payload (serial-to-parallel-conversion).
- Propagation of the incoming off-chip packet to the on-chip side which includes transparent propagation and appending additional clock cycles (NumAddClk).
- Propagation of the incoming on-chip packet (through the loop back) to the off-chip side.
- Address matching for its own addresses (see recognised addresses) which includes address matching and storage of received parameters.

[0056] Some control issues are now discussed. The master is also the entry point for the externally provided clock and reset signals. In a specific implementation, three signals may be provided through the off-chip interface: a chip enable (NocCE), a clock signal (NocCLK), and an asynchronous reset signal (NocRST). Regarding recognised addresses, the following is to be noted. The amount of additional clock cycles that are appended to a packet to compensate for the on-chip clock propagation delays, is made programmable. The master node recognises a specific address (1000 0000) through which the number of additional clock cycles (NumAddClk) can be programmed.

Architecture of a Slave Node

[0057] A slave node consists of an input interface (modrx), an output interface (modtx), MAC functionality (modmac), and the specific functionality that connects to the analogue block (modbitdec, modbufstg) as illustrated in Fig. 6.

[0058] Concerning the functional description it is noted that the I/O blocks have the same functionality as for the on-chip interface (modrxon, modtxon) of the master node. The MAC block performs the same packet identification and propagation functionality as in the master node. Retrieved flag, address and payload information is passed to the bit decoder (modbitdec). The bit decoder performs the address matching with a set of programmed addresses and performs the mapping of bits in the payload to analogue.
control pins. It also includes the storage register file for holding all initial values at reset and the current values. The buffer stage performs the buffering of the register file outputs to the individual digital control pins that are routed towards the analogue blocks.

Detailed View on the Node Interface

Extending this initial view, a specific mixed-signal interface can be added between the digital and the analogue block. Furthermore, one can refer to modrx and modtx as physical receivers and physical drivers in general. This means that these blocks can also incorporate signal format conversions to adapt from e.g. CMOS logic voltage levels to other appropriate signalling formats for the interconnect (e.g. LVDS).

Logical MAC Functionality

The logical MAC functionality can be implemented in plain digital CMOS. This part has two functions in combination with a logical packet-based communication scheme, which transports information on the network segment:

(a) receive: Its function is to identify packets that are intended for a specific node. In this case, the packet information is retrieved and communicated to the mixed-signal interface.

If the address matches the node address, information is taken from the packet and processed. If the address does not match, the packet is propagated to the physical send part, such that it travels to the next node. If a packet sent by the bridge returns to the bridge unchanged, it means that no node reacted on the packet. The bridge then knows that the packet has not been processed correctly by a node and it can e.g. signal an error or retry the transmission. Packets sent by the bridge that reach the
bridge or that have the bridge as a receiver address, are taken off the ring.

(b) transmit: Two modes can be foreseen. If the node has a permanent clock, it can trigger transmissions itself. In this case, it monitors the activity on the physical receive end. If no activity is found, it can create a packet itself and place it on the physical transmit end. If the node is not self-clocked, it requires a clock provided by the physical receive end. In this case, it is the responsibility of the on-chip bridge to create specific packets that trigger the MAC in a particular node to send information. In this case, the MAC derives the address from the incoming packet, and if it matches the node address, the packet is withheld and not passed on further. Instead, a new packet is constructed, local node information obtained from e.g. the analogue block is placed in this packet and the packet is sent on the transmit end. Note that, in this case, the target address of this packet is usually the bridge. The bridge is then able to receive this information (since a closed ring is used).

Example
[0060] As an example one can consider a network with one network segment on-chip and one network segment off-chip (Fig. 7). Both segments are connected through the master node, which acts as a bridge. The on-chip segment contains the master node and 5 slave nodes. The off-chip segment contains at least the master node and a programming node.

Logical Packet-Based Communication Scheme
[0061] A serial communication scheme needs to define a packet structure to sequentialise all information, covering both synchronisation, control, and data payload information.
Data Communication: bit-serial (1-bit) communication is assumed between the nodes. Each node has 1-bit input and 1-bit output ports.

Signalling and synchronisation between slave nodes and master node (bridge): Clock signals can be propagated together with the packets on the communication bus. In this case, modules can work without a clock, but need a PLL. In this case, each node requires a small digital PLL to recover the clock information from e.g. Manchester-coded digital signalling. Two issues should be considered. Firstly, in order to propagate a constant clock to all modules, this clock can be enabled/disabled centrally and allows a clock gating operation. Secondly, relying on the fact that modules do not operate if there is no activity on the ring.

All clock pulses must be provided by the master in this case (the bridge). Also clock pulses for e.g. delayed processing in the node must originate from the bus. The bridge shall increase the amount of clock pulses to cover all processing needs in the complete ring.

Support for Multiple Packet Types

Since delay and throughput requirements vary, it is desirable to have slow and fast packet types. Fast adaptation of parameters is required e.g. when adapting the gain settings for automatic gain control. Similarly, it is desirable to set all parameter bits at the same time for a particular parameter, i.e. the length of the packet payload should be determined by the maximum length of a parameter (e.g. PLL programming parameters with 15 or 16 bits). On the other hand, not all parameters require fast programming or such long word lengths. Hence, one can opt for a scheme with two types of packets, namely slow (S) packets for simple control or short control words and fast (F) packets
for complete control words. The choice for two packet types reduces in general energy consumption and activity on the bus. This scheme can be extended to more and different combinations of packet types depending on the usage patterns and the actual design constraints. It is assumed that the clock is passed through the ring. Hence, each node has one clock input and one 'clock output. The clock is propagated. For resetting all nodes to a known state, an asynchronous reset is assumed. The reset is also propagated through all nodes. Each node has one reset input and one reset output.

Positive Consequences for the Routing and the Design Cost for Routing

The consequent use of propagation both for data, synchronisation, and control information allows the usage of routing channels between the nodes. Each node has 3 input pins and 3 output pins for data, clock, and reset, respectively. The usage of routing channels greatly simplifies the effort of routing. It is to be noted that these channels do not need to be adapted even if the number of bits to control per node, control frequency, or the number of nodes change.

Example for the Packet Structure

A packet consists of synchronisation, control, and payload information:

| Sync | S/F packet indication | R/W flag | MAC address | Payload information | Additional clock pulses |

For each field in the packet, function and size are defined in the following Table 1.
Table 1

<table>
<thead>
<tr>
<th></th>
<th>Size</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sync</td>
<td>1 bit</td>
<td>Always '1'</td>
</tr>
<tr>
<td>S/F packet</td>
<td>1 bit</td>
<td>'1' = slow ; '0' = fast</td>
</tr>
<tr>
<td>indication</td>
<td></td>
<td></td>
</tr>
<tr>
<td>R/W flag</td>
<td>1 bit</td>
<td>'0' = read ; '1' = write</td>
</tr>
<tr>
<td>MAC address</td>
<td>4 bit (fast packet) ; 8 bit (slow packet)</td>
<td></td>
</tr>
<tr>
<td>Payload</td>
<td></td>
<td></td>
</tr>
<tr>
<td>information</td>
<td>24 bit (fast packet) ; 12 bit (slow packet)</td>
<td></td>
</tr>
</tbody>
</table>
| Additional       | Programmable from 0 to 41 | Always '0' 
| clock pulses     |               |                            |

Table 1

Table 2 then shows the sizes and time duration thus obtained for a single packet in slow and fast version.

<table>
<thead>
<tr>
<th>Packet type</th>
<th>Total packet length in bits (15 additional clock cycles)</th>
<th>Time duration for 120-MHz clock (in µs)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Slow</td>
<td>3+8+12+15 = 38</td>
<td>3.17</td>
</tr>
<tr>
<td>Fast</td>
<td>3+4+24+15 = 46</td>
<td>3.83</td>
</tr>
</tbody>
</table>

Table 2

[0064] Determining the amount of sufficient additional clock pulses: The number of required additional clock pulses depends on the amount of nodes in the segment and the delay per node. The delay per node is the processing delay introduced between the input stage and the output stage of the node. A typical value for this delay is 3 clock cycles. The number of slave nodes is 5. Hence, at least $5 \times 3 = 15$ clock cycles need to be appended by the master node to guarantee that all slave nodes receive enough clock cycles for proper operation.

[0065] Two solutions can be envisaged for clock propagation along the network path. The first one has been previously described. A second one balances the clock propagation delay and the data propagation delay in each node. In the first solution, the clock activity profile over time ramps up in a triangular shape creating an
integrated noise energy proportional to \( N \times \frac{N}{2} \times \) (propagation delay per node) \( \times \) noise density with \( N \) nodes. Depending on the propagation delay and the number of nodes, noise energy density peaks can amount up to \( N \times \) noise density. The second solution reduces the integrated noise energy to \( N \times \) (propagation delay per node) \( \times \) noise density. A reduction of the overall noise energy per packet transmission can result in less interference with the operation of the analogue/RF circuitry and hence result in better performance.

[0066] A variation of the previous solution for the local storage of a single configuration in each node in the writing mode is its extension to store at least 2 such configurations. This allows programming at non-critical times (i.e. at idle time and not during the operation of the analogue/RF circuitry) and activation of one of the configurations through a simple command instruction (e.g. a short packet) that does not contain all individual configuration bits. This solution requires a duplication of the configuration registers in each node (cfr. mbdbufstg) and either a dedicated packet instruction for activation per node or for groups of nodes or for all nodes together or the usage of a dedicated activation line which is routed together with the clock and data signal path from node to node. The dedicated activation line results in a very fast, parallel activation in all nodes since this operation can be performed at the buffer stage (modbufstg) without the need for clock support (hence, propagation delay through the network is completely eliminated).

Combinations of both techniques (one activation line and dedicated activation packets) are particularly interesting. [0067] Fail-safe operation of the control network can be guaranteed by routing the digital supply voltage together with the signal, clock, reset, and activation line
(optional) signal in the existing i0uting channels. Ground signals from the shielding of these channels can be optionally reused; otherwise, a dedicated ground signal should be routed in parallel with the supply voltage signal. This supply voltage feeds all digital logic in the nodes. The low power requirements for the operation of the control network allow the usage of a single supply pair at one entry point in the control network. The supply and ground voltage paths can be closed or not (in the circular topology). This technique can improve fail-safe operation compared to the classical approach where each node would be supplied through a pair of pads closest to the chip boundary and eventually even shared with the adjacent digital supply for an analogue/mixed-signal block. Even when disabling intentionally the supply for the analogue/mixed-signal block (e.g. to save energy) or in case of a malfunctioning of the analogue/mixed-signal block (short-circuit, voltage drop due to high load, overheating, etc.), the control network remains fully operational.
CLAIMS

1. System comprising at least a first and a second essentially analogue portion and an essentially digital portion, said first and said second analogue portion forming a part of a unidirectional circular network, and further comprising
   - first communication means provided between said digital portion and said first analogue portion,
   - second communication means provided between said at least first and second analogue portions,
   whereby said first and second communication means are configurable for establishing communication between said digital portion and said second analogue portion and whereby said first and second communication means are arranged to determine if a packet communicated over said first or second communication means is of interest for any of said analogue portions.

2. System as in claim 1, whereby each of said first and said second communication means comprises interface circuitry for each circuit connected by said communication means.

3. System as in claim 1 or 2, wherein said analogue portions and said second communication means are on one chip.

4. System as in claim 1 or 2, implemented in a single integrated circuit.

5. System as in claim 1 or 2, implemented in a single package.

6. System as in any of claims 1 to 5, wherein said first and said second communication means are digital.

7. System as in any of the previous claims, arranged for providing an information flow for controlling
and monitoring said analogue portions guided by said first and second communication means.

8. System as in claim 7, wherein said analogue portions are part of analogue RF front ends.

9. System as in claim 8, arranged for selecting parameters for communication over said first and second communication means such that interference of the RF functionality is minimised.

10. System as in claim 9, wherein said parameters for communication are selectable from the group of parameters comprising \{frequency, signal amplitude, packet length, packet format\}.

11. System as in claim 7, wherein said digital portion is a part of a baseband processor.

12. System as in claim 11, wherein said baseband processor is implemented in the same integrated circuit as the rest of said system.

13. System as in claim 11, wherein said baseband processor is implemented in the same package as the rest of said system.

14. System as in any of the previous claims, wherein said digital portion is provided with a Quality of Experience manager.

15. System as in any of the previous claims, wherein the communication over said first and said second communication means is differential.

16. System as in claim 15, wherein said first and said second communication means are arranged for low voltage differential signalling.

17. System as in any of the previous claims, wherein communication on said first or said second communication means is unidirectional.

18. System as in claim 17, wherein said communication is one-bit communication.
19. System as in any of the previous claims, the length of said packets is adaptable to at least two speeds of communication.

20. System as in any of the previous claims, further comprising a plurality of additional analogue portions arranged for forming together said first and said second analogue portion said unidirectional circular network.

21. System comprising a first subsystem as in any of claims 1 to 20, a second subsystem as in any of claims 1 to 20 and an additional digital portion for connecting said first and said second subsystem.

22. Method for controlling an information flow in a system as in any of claims 1 to 21, comprising the steps of
- receiving configuration information for at least one of said analogue portions
- arranging said configuration information in said digital portion
- transmitting said arranged configuration information over said unidirectional circular network

23. Method for controlling as in claim 22, wherein said configuration information comprises packet format information.

24. Method for managing a system as in any of claims 1 to 21, comprising the steps of
- transmitting with said digital portion over said unidirectional circular network a request for status information of at least one of said analogue portions,
- receiving said request with said at least one analogue portion,
- providing to said digital portion said status information.
25. Method for managing a system as in claim 24, wherein said digital portion is provided with a Quality of Experience manager.

26. Use of the method as in claim 24 or 25 for Quality-of-Experience management.
Fig. 1

Fig. 2
INTERNATIONAL SEARCH REPORT

A. CLASSIFICATION OF SUBJECT MATTER
INV. H04L 12/42 H04B 1/40 H04L 12/28 H04L 12/56
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H04L H04B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

<table>
<thead>
<tr>
<th>Category</th>
<th>Citation of document, with indication, where appropriate, of the relevant passages</th>
<th>Relevant to claim No</th>
</tr>
</thead>
<tbody>
<tr>
<td>Y</td>
<td>US 5 699 356 A (BEEVER ET AL) 16 December 1997 (1997-12-16) column 1, line 7 - column 2, line 52 figures 1, 3</td>
<td>8-13, 15, 16, 22, 24, 14, 19</td>
</tr>
<tr>
<td>A</td>
<td>Further documents are listed in the continuation of Box C</td>
<td>1-7, 14, 19</td>
</tr>
</tbody>
</table>

See patent family annex

Further special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier document but published on or after the international filing date
"L" document which may throw doubts on the novelty of the claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means of publication prior to the international filing date but later than the priority date claimed

"I" later document published after the international filing date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance, the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance, the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

Date of the actual completion of the international search
1 February 2007

Date of mailing of the international search report
12/02/2007

Name and mailing address of the ISA
European Patent Office, P B 5816 Patentlaan 2 NL - 2280 HV Rijswijk Tel (+31-70) 340-2040, Tx 31 651 epo nl, Fax (+31-70) 340-3016

Authorized officer
Vaskimo, Kimmo
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<th>Relevant to claim No.</th>
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### Box II  Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This International Search Report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos because they relate to subject matter not required to be searched by this Authority, namely

2. ☐ Claims Nos because they relate to parts of the International Application that do not comply with the prescribed requirements to such an extent that no meaningful International Search can be carried out, specifically

3. ☐ Claims Nos because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 64(a)

### Box III  Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

- see additional sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this International Search Report covers all searchable claims.

2. ☒ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this International Search Report covers only those claims for which fees were paid, specifically claims Nos:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this International Search Report is restricted to the invention first mentioned in the claims; it is covered by claims Nos:

### Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest.

☐ No protest accompanied the payment of additional search fees

Form PCT/ISA/210 (continuation of first sheet (2)) (January 2004)
This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1-21

A system comprising plural analog portions and a digital portion, said portions forming a unidirectional circular network, where means are provided for the analog portions to communicate, where the means are arranged for determining if a packet communicated over said communications means are of interest for any analog portions, and where said communication means and analog portions are arranged into a single package.

1.1. claims: 1,22,23

A system comprising plural analog portions and a digital portion, said portions forming a unidirectional circular network, where means are provided for the analog portions to communicate, where the means are arranged for determining if a packet communicated over said communications means are of interest for any analog portions, and where said digital portion transmits configuration information over said communication means.

1.2. claims: 1,24-26

A system comprising plural analog portions and a digital portion, said portions forming a unidirectional circular network, where means are provided for the analog portions to communicate, where the means are arranged for determining if a packet communicated over said communications means are of interest for any analog portions, where the digital portion requests the analog devices to transmit their status information, and where said analog devices transmit their status information to said digital portion.
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Form PCT/ISA/210 (patent family annex) (April 2005)