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GB 1305753
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(54) **Analog electronic timepiece**

(57) An analog electronic timepiece comprises a first step motor (4) for driving a first hand (5) which indicates time of day and a second step motor (20) which drives a second hand (21) for indicating time information other than time of day, for example, elapsed time or split time. A common divider circuit (2) provides a clock signal to drive both the first and second step motors. Switches (6, 7, 8, 9 and 30) control the second step motor independently of the first step motor. A drive control circuit (15) selectively supplies an operating signal for operating the second hand and a correcting signal for altering the display produced by the second hand.

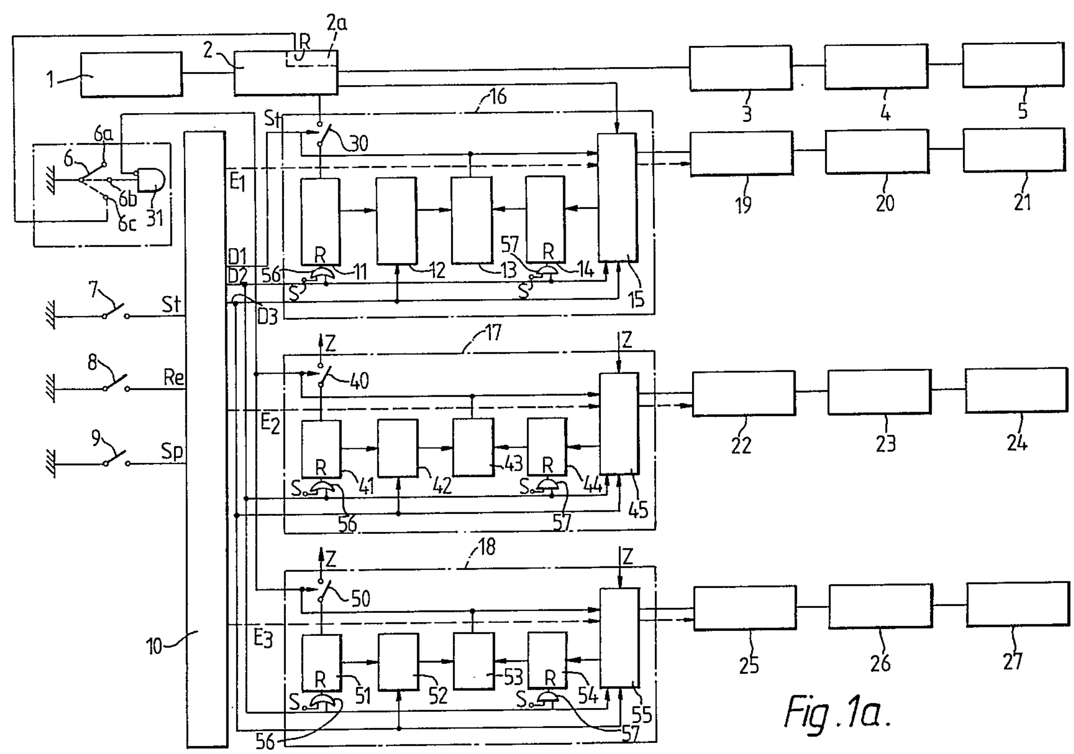

Fig. 1a.

The drawing(s) originally filed was/were informal and the print here reproduced is taken from a later filed formal copy.

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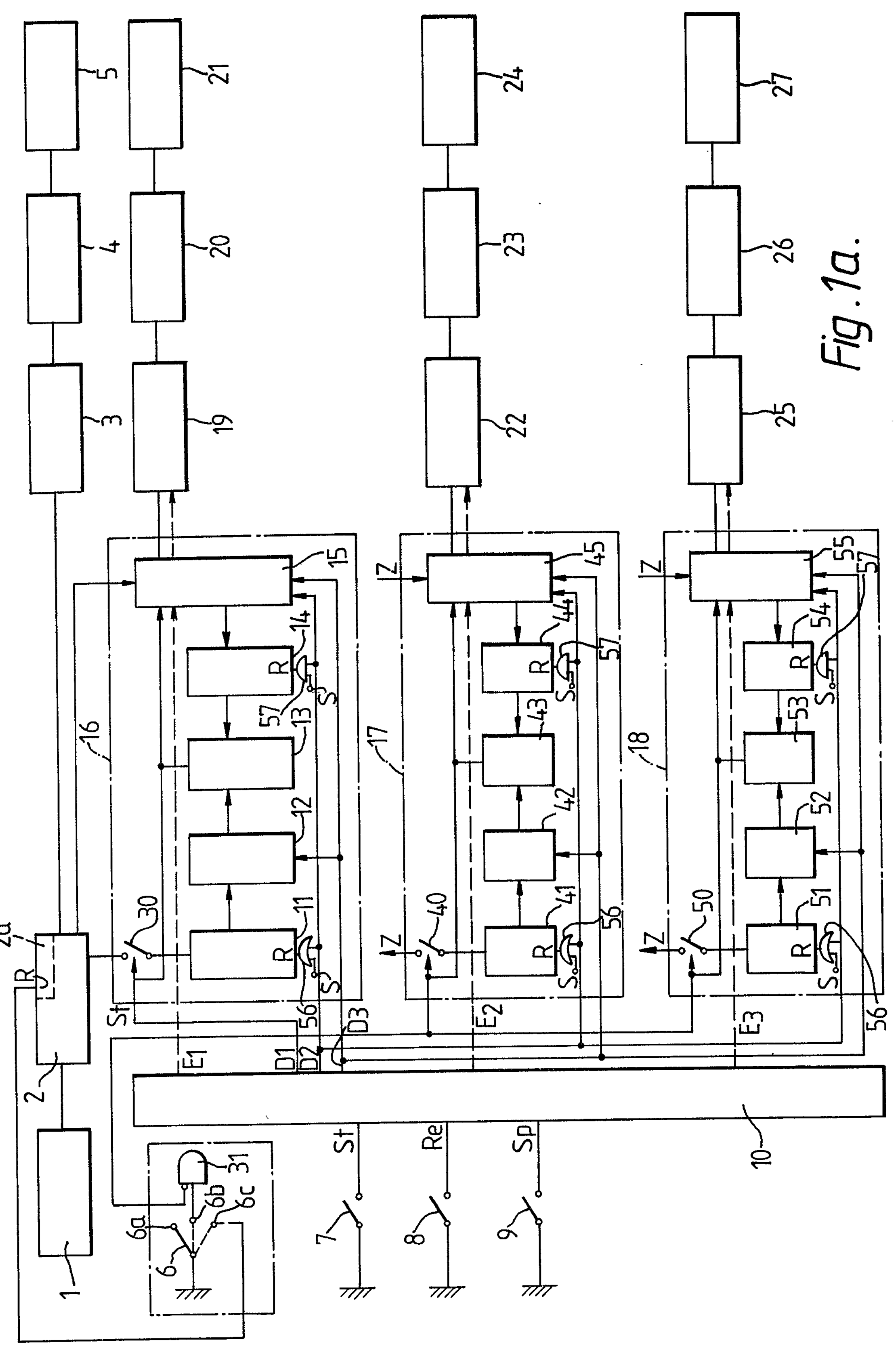

1
2
2a
R
3
4
5
6
6a
6b
6c
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
30
31
40
41
42
43
44
45
50
51
52
53
54
55
56
57
St
Re
Sp
E1
E2
E3
D1
D2
D3
Z
S

Fig. 1a.

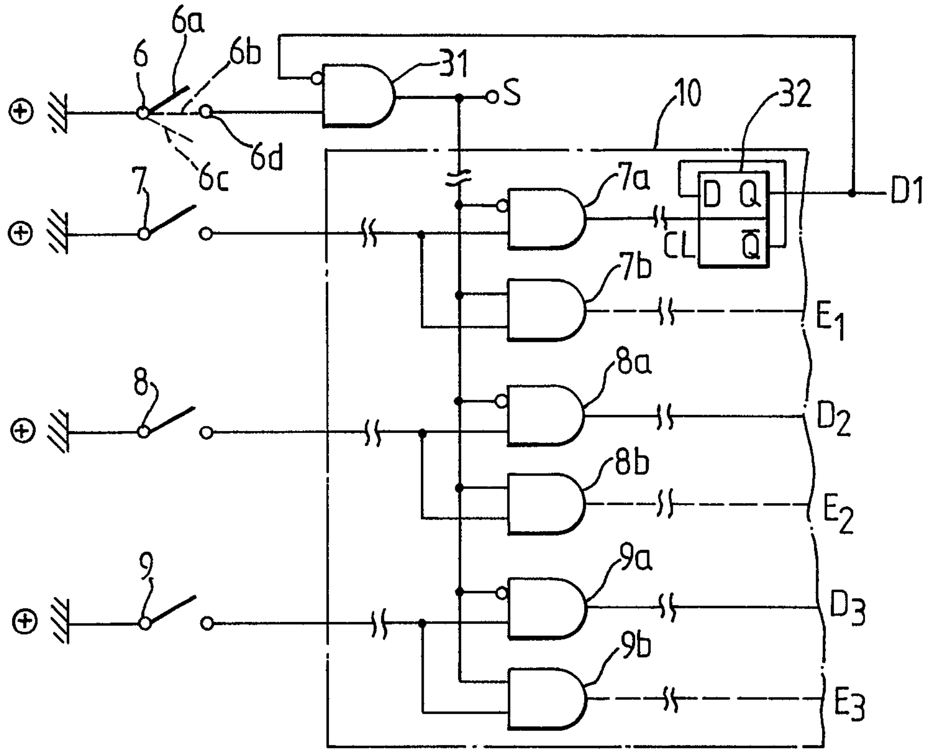

6a
6
6b
31
S
10
32
6d
6c
7
7a
D Q
CL Q̄
D1
7b
E1
8
8a
D2
8b
E2
9
9a
D3
9b
E3

Fig. 1(b).

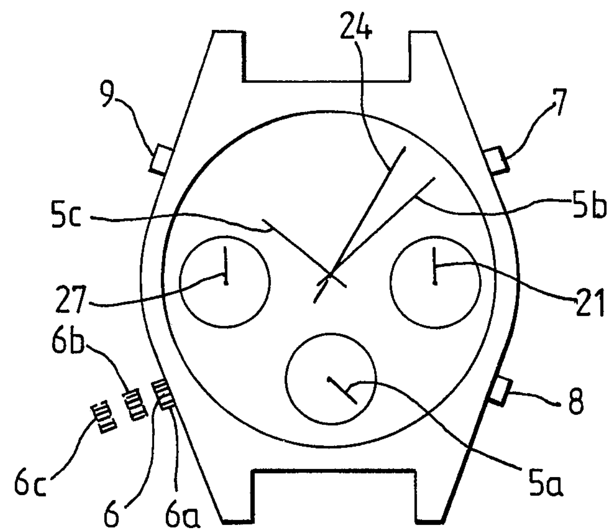

24
9
7
5c
5b
27
21
6b
8
6c
6
6a
5a

Fig. 2.

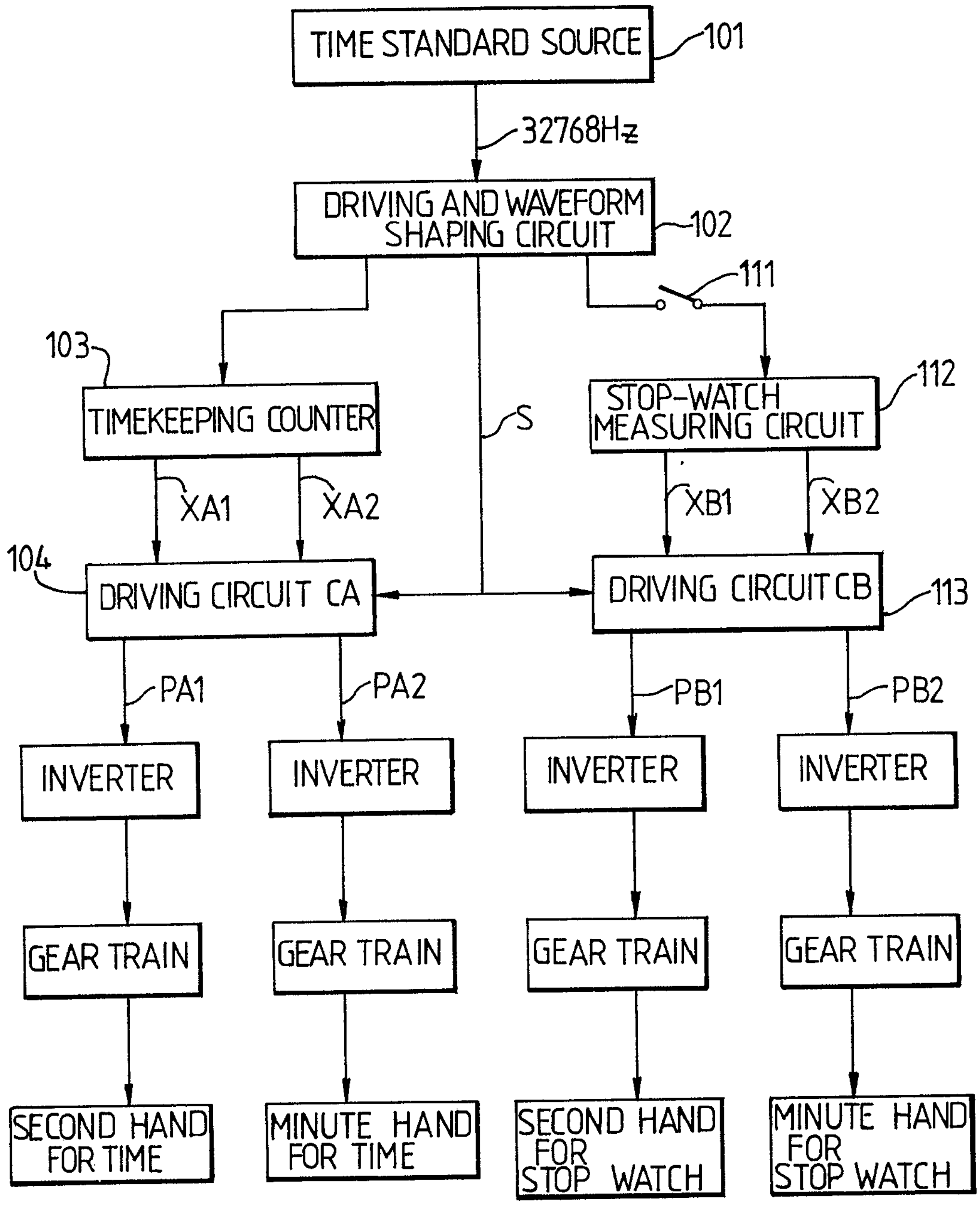
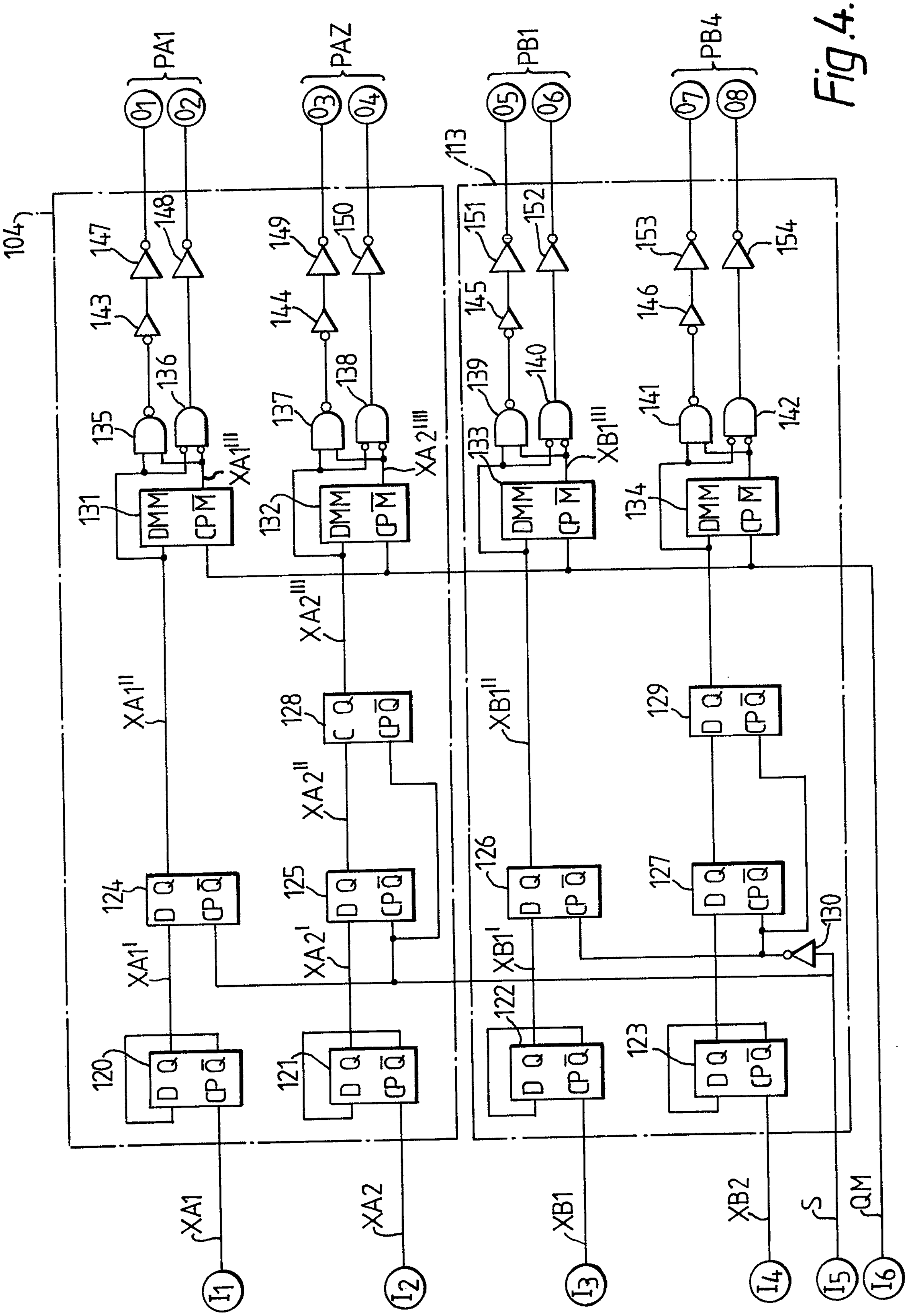

TIME STANDARD SOURCE
101
32768Hz
DRIVING AND WAVEFORM SHAPING CIRCUIT
102
111
103
TIMEKEEPING COUNTER
S
STOP-WATCH MEASURING CIRCUIT
112
XA1
XA2
XB1
XB2
104
DRIVING CIRCUIT CA
DRIVING CIRCUIT CB
113
PA1
PA2
PB1
PB2
INVERTER
INVERTER
INVERTER
INVERTER
GEAR TRAIN
GEAR TRAIN
GEAR TRAIN
GEAR TRAIN
SECOND HAND FOR TIME
MINUTE HAND FOR TIME
SECOND HAND FOR STOP WATCH
MINUTE HAND FOR STOP WATCH

Fig.3.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I2
I3
I4
I5
I6
XA1
XA2
XB1
XB2
S
QM
104
113
120
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122
123
124
125
126
127
128
129
130
131
132
133
134
135
136
137
138
139
140
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145
146
147
148
149
150
151
152
153
154
PA1
PAZ
PB1
PB4
01
02
03
04
05
06
07
08

Fig.4.

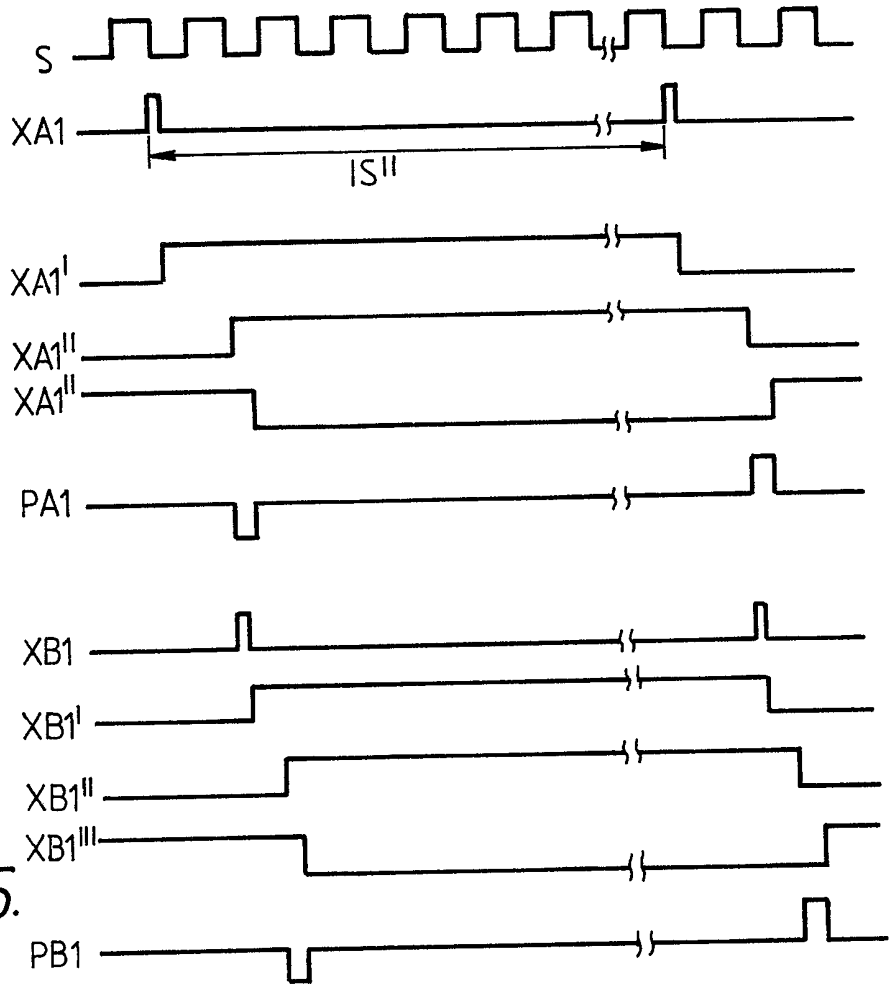
S
XA1
IS''
XA1'
XA1''
XA1''
PA1
XB1
XB1'
XB1''
XB1'''
PB1

Fig. 5.

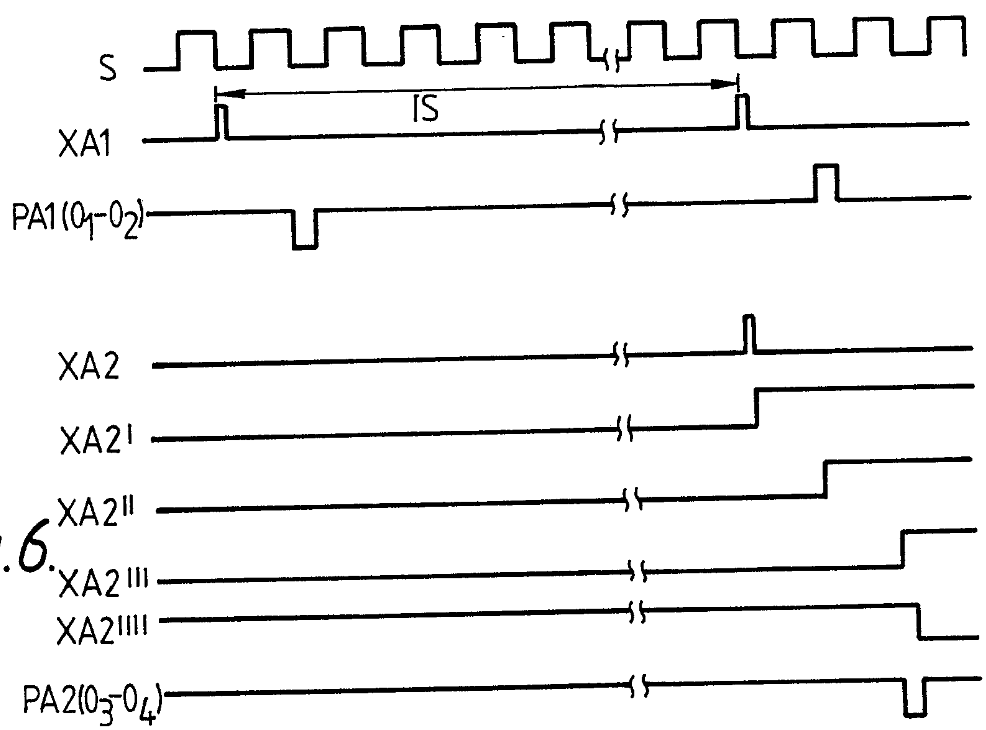
S
IS
XA1
PA1 (01-02)
XA2
XA2'
XA2''
XA2'''
XA2''''
PA2(03-04)

Fig. 6.

SPECIFICATION

Analog electronic timepiece

This invention relates to analog electronic timepieces, for example, analog electronic chronographs.

Recent developments in digital electronic timepiece technology have produced chronographs or stopwatches capable of measuring not only total elapsed time but also split (or lapsed) time (that is, measuring intermediate elapsed time). This is mainly because it is has become possible to integrate electronic circuits to a greater degree.

Usually, the hands of a chronograph timepiece having a mechanical analog display are reset by using a heart-shaped cam. However, this mechanism is so complicated that an analog chonograph timepiece having split time display is not readily obtainable unless provided with a hand specifically for displaying split time.

A conventional digital chronograph timepiece may be operated by two buttons, that is a start-stop button and a lap-reset button but a user cannot always understand what is being measured at a particular instant. Therefore, it is usually to provide such a time piece with a display of the current operational mode such as displaying LAP when split time is being displayed.

Although the present invention is primarily directed to any novel integer or step, or combination of integers or steps, herein disclosed and/or as shown in the accompanying drawings, nevertheless, according to one particular aspect of the present invention to which, however, the invention is in no way restricted, there is provided an analog electronic timepiece comprising: a first step motor for driving a first hand which indicates the time of day; a second step motor which drives a second hand for indicating time information other than time of day; a common divider circuit for providing a clock signal to drive both the first and second step motors; switch means for controlling the second step motor independently of the first step motor; and a drive congrol circuit for selectively supplying an operating signal for operating the second hand and a correcting signal for altering the time information displayed by the second hand.

In a preferred embodiment the timepiece includes phase control means for shifting the phase of drive signals applied to the step motors relative to one another so that driving pulses of the drive signals are not simultaneously applied to both step motors.

A third step motor may be provided, the second and third step motors together indicating said time information other than time of day. Thus the switch means may be arranged to control operation of the third step motor independently of the first step motor.

Preferably the timepiece includes a chronograph measuring circuit for causing said second hand to display chronograph time information.

The invention is illustrated, merely by way of example, in the accompanying drawings in which:-

Figure 1(a) is a block diagram of one embodiment of an electronic timepiece according to the present invention;

Figure 1(b) is a circuit diagram of a part of a switch control circuit of an electronic timepiece according to the present invention;

Figure 2 is an external view of the electronic timepiece of Figure 1(a);

Figure 3 is a block diagram of another embodiment of an electronic timepiece according to the present invention;

Figure 4 shows an embodiment of a driving circuit of the electronic timepiece of Figure 3; and

Figures 5 and *6* are timing charts illustrating the operation of the driving circuit of Figure 4.

Figure 1(a) is a block diagram of one embodiment of an analog quartz electronic timepiece according to the present invention. The timepiece comprises a basic watch unit including a time standard source 1, a frequency divider 2, a motor driving circuit 3, a timepiece step motor 4, and a time indicator 5 comprises of, as well known, an hours hand 5*c*, a minutes hand 5*b* and a seconds hand 5*a* (Figure 2). The timepiece has step motors 23, 26 for the chronograph function. The timepiece of Figure 1 includes a switch 6 which is operated by an external operating stem and push button switches 7, 8, 9. The timepiece also has a switch control circuit 10 and electronic measuring circuitry 16, 17, 18 for chronograph time measurement. The electronic measuring circuits 16, 17, 18 each comprise respectively timekeeping counters 11, 41, 51, respective latch circuits 12, 42, 52, respective coincidence detectors 13, 43, 53, respective hand position counters 14, 44, 54 and respective drive control circuits 15, 45, 55. A digital timepiece would not, of course, require hand position counters 14, 44, 54.

Input signals are applied to the timekeeping counters 11, 41, 51 from the divider 2 by operating switches 30, 40, 50 by means of the output from the switch control circuit 10.

Motor driving circuits 19, 22, 25 operate independently of one another and drive the respective chronograph motors 20, 23, 26. Chronograph indicators 21, 24, 27 are hands which operate independently and indicate the elapsed time in different time units. In this embodiment, for example, the indicator 21 can measure the elapsed time in 1/10th of seconds it taking one second for the hand to complete a revolution of a dial scale graduated in tenths of a second. Indicator 24 is provided at the centre of the dial and its hand can be replaced by a small seconds hand 5*a* for a timepiece in position. It takes one minute for the indicator 24 to complete one revolution. A dial scale for the indicator 24 is graduated in sixty divisions so that the indicator can measure elapsed time in seconds. The indicator 27 takes 30 minutes to complete one revolution. The indicator moves by one step each minute on a dial scale graduated in thirty divisions so that elapsed time of up to thirty minutes can be measured by all three indicators 21, 24, 27. The maximum elapsed time to be measured is changeable: for example, elapsed time of up to 60 minutes can be measured by changing the steps of the indicator 27 and the graduations of the associated graduated scale. The divided signals fed to the electronic measuring circuits 16, 17, 18 from the divider 2 correspond to each measured unit of the elapsed time.

The operation of the switches 6, 7, 8, 9 of the timepiece will now be described. Switch 6 in Figure 1(a) is operated by the external operating stem. Switch position *6a* is an ordinary position of the switch 6 with the stem in a first position, switch position *6b* is achieved by pulling the stem out to a second position and switch position *6c* is achieved by pulling the stem out to a third position. The switch 6 is open in position *6a* and in position *6c*, whilst it is closed in position *6b*. The switches 7, 8, 9, which are push button switches, respectively are ON the instant they are pushed and OFF the instant they are released. This is achieved by providing a coil spring or level spring in each of the push button switches.

Operation of the switches 6, 7, 8, 9 when the stem is in the first position will now be described. Referring, in particular, to Figure 1(b) showing a part of the switch control circuit 10 in detail, the switch terminal *6d* is low level and the output of an AND gate 31 is low level irrespective of the level of a signal D_1 fed to the AND gate 31, thereby providing a signal of high level to one input of AND gates *7a*, *8a*, *9a* so that they are ready to receive inputs from the switches 7, 8, 9. When the inputs are provided from the switches 7, 8, 9, the gate *7a* causes a D-type flip-flop 32 to produce the signal D_1 gate *8a* to produce a signal D_2 and a gate *9a* to produce a signal D_3.

Operating of the switches 6,7. 8,9 when the stem is in the second position will now be described. The signal from the AND gate 31 is controlled in response to the level of the signal D_1. When the signal D_1 is low level, the output of the AND gate 31 becomes high legal and the AND gates *7a*, *8a*, *9a* do not open since the signal applied thereto is low level. AND gates *7b*, *8b*, *9b* are ready to pass signals from switches 7, 8, 9. In this condition when the switches 7, 8, 9 are closed, the gate *7b* produces an output signal E_1, the gate *8b* produces an output signal E_2 and the gate *9b* produces an output signal E_3. The signals E_1, E_2, E_3 are supplied to the motor driving circuits 19, 22, 25 through the drive control circuits 15, 45, 55 respectively as shown in Figure 1(a).

When the stem is further pulled out to the third position, the switch 6 is open again. In this state, operation of the timepiece is the same as when the stem is in the first position. When the switches 7, 8, 9 are closed, the gate *7a*, the gate *8a* and the gate *9a* deliver the signals D_1, D_2, D_3 respectively.

Next the operation of the switches 7, 8, 9 will be described in detail.

A wearer of the timepiece can determine the time of day from the analog time indicator 5. As shown in Figure 1, the signal from the oscillator 1 is frequency divided by the divider 2 and shaped by the motor driving circuit 3. Then the step motor 4 is driven by the shaped signal to operate the time indicator 5. Thus the hands *5a*, *5b*, *5c* indicate the time of day.

For chronograph time measurement, the switch 6 is closed by moving the stem to the second position. To correct the time of day the switch 6 is opened by moving the stem to the third position. The hours hand and minutes hand for indicating time of day are corrected by rotating the stem clockwise or counter-clockwise when in the third position which is performed *via* a changeover mechanism (not shown).

Chronograph time measurement is performed with the stem either in the first position or the second position. First of all, the chronograph function will be explained in the case where the stem is in the first position. Signals from the switches 7, 8, 9 are applied to the switch control circuit 10. Actuation of the switch 7 causes starting and stopping of measurement of elapsed time. Actuation of the switch 8 causes resetting of the chronograph display. Actuation of the switch 9 causes split time measurement.

In Figure 1(b), when the switch 7 is depressed and thereby closed with the switch 6 open a high level signal is fed to the AND gate *7a* to be applied to the flip-flop 32 as a clock signal. The signal D_1 delivered from terminal Q of the flip-flop 32 goes to high level the moment the first clock signal pulse from the AND gate *7a* is received and remains at high level until a second clock signal is received. Then the signal D_1 goes to low level owing to the second clock signal from the AND gate *7a* and remains at low level until a third clock signal is received. Subsequently the signal D_1 goes to high level at the moment the third clock signal is received. Thus a clock signal is applied to the flip-flop 32 each time the switch 7 is closed. The elapsed time is measured when the signal D_1 is high level. When the signal D_1 is low level the chronograph is stopped, namely, the elapsed time is not measured. Thus the signal for starting and stopping measurement of elapsed time is produced by operating the switch 7.

The time measuring circuit 16 comprises the timekeeping counter 11, the latch circuit 12, the coincidence detecting circuit 13, the hand position counter 14, the drive control circuit 15 and the switch 30 which is disposed between the timekeeping counter 11 and the divider 2. When the switch 30 is turned ON, a signal whose period is the same as that for driving the step motor 4 is fed to the timekeeping counter 11 for a portion *2a* of the divider. The portion *2a* of the divider delivers a driving signal to the motor driving circuit 19 through the drive control circuit 15. The drive control circuit 15 produces a signal having the same number of pulses as the motor driving signal fed to the motor driving cicuit. The latch circuit 12 usually passes the counted state of the timekeeping counter 11 to the coincidence detecting circuit 13. The coincidence detecting circuit 13 compared the condition of the timekeeping counter 11 and the hand position counter 14. In the case where non-coincidence is found the coincidence detecting circuit 13 delivers a signal to the drive control circuit 15 so that the latter selects a quick feeding signal. When the counted values of the timekeeping counter 11 and the hand position counter 14 coincide, the coincidence detecting circuit 13 produces a signal so that the signal to the drive control circuit 15 once again delivers the motor driving signal. The quick-feeding signal is formed by taking a signal from an early stage of the divider 2. The latch circuit latches the counted value of the timekeeping counter 11 when a split signal is produced from the switch 9. The split signal is fed to the drive conrol circuit 15 to stop the motor driving signal being produced at the output thereof. Thus the coincidence detecting circuit 13 remains in the coincident condition. When the split signal is terminated by the switch 9, the coincidence detecting circuit takes in the counted value of the timekeeping counter 11 which has been counting the motor driving signal continuously whilst the split time is being displayed. The coincidence detecting circuit 13 detects the disagreement between the count in the timekeeping counter 11 and the count in the hand position counter 14 and causes the drive control circuit 15 to send the quick-feeding signal to the motor driving circuit 19. The drive control circuit selects the motor drive signal when the count in the hand position counter coincides with the count in the timekeeping counter. Thus the position of the indicators 21, 24, 27 whose movement is stopped when split time is displayed are adjusted at a rapid rate so that they then show elapsed time.

When the switch 6 is open, chronograph time measurement is started by depressing the switch 7 to close it. The signal D_1 actuates the switch 30 and then starts the timekeeping counter 11 counting and further operates the motor driving circuit 19 and the step motor 20 *via* the drive control circuit 15. Thus the chronograph indicator 21 is driven. The elapsed time is measured in small time units of less than 1 second, e.g. in 1/10 of a second. For example, it takes 1 second for the indicator 21 to make one complete revolution or 0.1 second to complete one step. Simultaneously, the electronic measuring counter 16 starts operation of the hand position counter 14.

Next, when the output of the AND gate 7*a* becomes high level upon operating the switch 7, measurement of elapsed time is stopped. Namely, the signal D_1 from the switch control circuit 10 stops the timekeeping counter 11 from counting the output and so the indicator 21 stops.

Operation of the switch 8 will now be described. The switch 8 performs a reset function. When the switch 8 is depressed the signal D_2 of the switch control circuit 10 resets the timekeeping counter 11 to 0 and simultaneously actuates the drive control circuit 15 to feed quickly the indicator 21 to the zero position. Namely, the timekeeping counter 11 is electronically set to zero and the indicator 21 is mechanically fed at a relatively rapid rate to a zero position. However, since the amount of quick feed is determined electrically, the indicator 21 is moved to only the position where the count in the timekeeping counter is zero. Accordingly, in Figure 2, when the indicator 21 starts rotating from a non-zero position, the position indicated thereby does not correspond to the count in the timekeeping counter. Thus the indicator 21 would reset to an incorrect zero position. In Figure 2, the indicators 21, 24, 27 are rotated by the circuitry described in Figure 1. All functions are stopped when a battery driving the timepiece is exchanged. In an ordinary wrist watch, where the only power source is a battery and no memory means are provided, when the battery is exchanged the circuitry starts the wrist watch operating either from a random state or from a reset state.

In the timepiece of Figure 1(a) when the battery is exchanged, the indicators 21, 24, 27 stop at a random position and the count in the timekeeping counter 11 is changed. Thus the position indicated by the indicators does not correspond to the count in the timekeeping counter when a new battery has been inserted into the timepiece. Accordingly, it is necessary to be able to correct the position of the indicators in order that their position corresponds to the count, namely zero, in the timekeeping counter.

While operating the switch 7, if the switch 9 which controls the split function, is actuated, the signal D_3 from the switch control circuit 10 operates the latch circuit 12 and the drive control circuit 15 temporarily. As a result the indicator 21 stops temporarily. However, the timekeeping counter 11 continues to count the motor driving signal. When the switch 9 is operated again, the indicator 21 moves to indicate the elapsed time since the quick-feed signal from the drive control circuit 15 is provided until the contents of the hand position counter and the timekeeping counter 11 coincide.

Operating switches 8, 8, 9 actuate the indicator 21 and simultaneously the electronic measuring circuits 17, 18, the motor driving circuits 22, 25 and the step motors 23, 26. Therefore the indicators 24, 27 are actuated like the indicator 21 during split time measurement.

Now the case where the stem 6 is pulled to the second position for correcting the chronograph time display will be described. The output of the switch 6 becomes high level or low level in response to whether the signal D_1 is high level or low level and this is fed to the AND gate 31. In the case where the signal D_1 is high level while chronograph time measurement is being performed, the chronograph time measurement continues even if the switch 6 is closed, that is, the stem is pulled out to the second position. This is, of course, the same as when the stem is in the first position.

When chronograph time measurement is stopped and the signal D_1 is low level, the AND gate 31 produces a signal of high level when the switch 6 is in position 6*b*.

When the stem 6 is pulled out to the second position and the switch 6 is thereby closed, each zero position indicated by the indicators 21, 24, 27 can be readily corrected. With the switch 6 closed, signals E_1, E_2, E_3 are produced in response to operation of the switches 7, 8, 9 respectively.

When the switch 6 is closed a signal S from the AND gate 31 becomes high level and resets the electronic measuring counters 11, 41, 51 *via* an OR gate 56. When the measuring counters 11, 41, 51 are reset, the quick-feed signal is supplied to the step motors 22, 23, 26 through the respective drive control circuits 19, 22, 25 until the hand position counters 14, 44, 54 coincide with the condition of the timekeeping counters 11, 41, 51. When the count in both counters coincide, the step motors stop. As a result, it is possible to confirm clearly how far the position indicated by the indicators is from the zero position in the case where the timekeeping counters contain a count of zero. In the case where the position is displaced from the zero position, the amount of shifting is corrected by operating the switches 7, 8, 9. For example, when the position of the indicator 21 is displaced from the zero position, operation of the switch 7 drives the step motor 20 *via* the drive control circuit 15 with vthe signal E_1. The output of the switch 7 is connected to a reset terminal R of the hand position counter 14 *via* an AND gate 57. Accordingly, whenever the switch 7 is actuated, the hand position counter 14 is reset. The hand position counter remains with a count of zero even when the step motor 20 is driven.

To describe this in more detail, when the switch 7 is temporarily closed, the switch control circuit 10 produces the signal E_1. The quick-feed signal from the divider 2 is fed to the motor driving circuit 19 through the drive control circuit 15. Thus either the motor 20 rotates at least as fast as it does during chronograph time measurement or it is rotated by one step for each operation of the switch 7. As a result the indicator 21 is displaced by one step or at a high frequency whereby permitting correction of the position of the indicator. In this way, it is possible to adjust each of the indicators 21, 24, 27 using the switches 7, 8, 9 either to a zero position or to an optional position independently.

The adjustment of the mechanical zero position is as described above so that the mechanical zero position is made to coincide with the "zero position" of the circuitry. When the switch 6 is opened the switch control circuit 10 produces the signal D_1 at high level so that the electronic measuring circuit 16 and the timekeeping counter 11 are reset. As a result the circuitry is all reset to zero. Chronograph time measurement can then be performed.

In conventional analog electronic timepieces if actuation of a switch and operation of circuitry do not correspond with each other it is impossible to separate definitely the functions of correcting the position of the indicators by the switch and chronograph time measurement. Thus in the case where the indicators go out of the true position it is difficult for the wearer to correct the position and, for example, the movement must be taken out of its case to replace the indicators or otherwise a complex operation of various push button switches is required.

In the electronic timepiece according to the present invention and described above it is simple to reset the indications in the case where the mechanical zero position of the indicators does not coincide with the "zero position" of the circuitry.

The operation of the electronic timepiece when the stem 6 is pulled out to the third position will now be described. By pulling the stem 6 to the third position, the hours hand 5*c* and the minutes hand 5*b* can be adjusted and the seconds hand 5*a* can be corrected, in the same manner as in a conventional analog timepiece. In order to correct the time precisely a part of the divider 2 relating to the display of time of day can be reset.

Correction of the time of day is effected by means of the switches 7, 8, 9 as described above in relation to resetting the chronograph time measurement and no further explanation is considered necessary. Thus the seconds hand 5*a* is regulated and the time is corrected by adjusting the hours hand 5*c* and the minutes hand 5*b* with the stem in the third position. After correction, the stem is moved from the third position to the first position. In the course of this movement the switch 6 passes through position 6*b* but the indicators are not altered as long as the switches 7, 8, 9 are not operated. The seconds hand 5*a* precisely commences movement at the same time as the winding stem is pushed in whereby the time of day is precisely set. Next will be described how the indicators and the hand producing the time of day display are relevant to electronic circuitry at the time when the stem 6 is pulled out or pushed in.

The operation of the AND gate 31 and the flip-flop 32 has already been described. The signal D_1 is high level when chronograph time measurement takes place and is low level when it is not. When the stem is pulled from the first position to the second position the indicators cannot be corrected because no output is delivered from the AND gate 31. When the stem is subsequently pulled out to the third position whilst chronograph time measurement is performed, at the second position the signal applied through the switch 6 in position 6*c* is low level whereby the output of the AND gate 31 is low level. The gate 7*a* remains open so that chronograph time measurement continues.

On the other hand, the seconds hand 5*a* is stopped thereby permitting the hours and minutes hands to be corrected. In other words even if the stem is pulled out to the second and third positions during chronograph time measurement this is continued irrespective. Accordingly, when the stem is in the second position, in one case the indicators are not stopped and in the other case the indicators are stopped to enable adjustment.

At the first position of the stem, the switch 7 is pushed to chronograph time measurement on the announcement of a standard time signal, for example, over the radio. Thus the indicator 24 agrees with the standard time signal. The stem is then pulled to the third position which permits correction of the time of day. However, it may not have been desired to set the seconds hand 5*a* to zero so after the hours and minutes hands have been set to the desired positions, the stem is pushed from the third position to the first position when the indicator 24 agrees with the seconds hand 5*a*. Thus the seconds hand 5*a* moves accurately with the indicator 24. Consequently it is very easy to set an analog timepiece correctly in this manner.

In a conventional analog electronic timepiece it takes time to set the time of day display. Thus an external operational stem is pulled out when the seconds hand comes to the zero position and the hours and minutes hands are then corrected. The stem must then be pushed in. Thus in the case where the timepiece is fast, the time of day is corrected after the announcement of a standard time signal or in the case where the timepiece is slow, it takes about a minute to correct the time of day. In fact it can take several minutes to set the time of day precisely in conventional timepieces. However, the timepiece according to the present invention and described above enables time to be set easily because the indicator 21 can be operated with the standard time signal and to act as a reference time for the seconds hand 5*a*.

One known analog timepiece has a seconds hand for selectively indicating time of day and used for chronograph time measurement. It thus is relatively simple to reset automatically the seconds hand by pressing a button after elapsed time has been measured. However, this type of construction is not suited to electronic timepieces because it requires a counter for the chronograph time measurement and a memory for the time of day. Thus complex electronic circuitry such as a counter and a coincidence circuit are required. As the result, this type of conventional analog timepiece is unsuitable for small-sized equipment with relatively low power consumption such as wrist watches. In addition it is troublesome to adjust the time of day in this conventional analog electronic timepiece.

On the other hand the timepiece according to the present invention and described above is advantageous in that the indicator 21 continues to move even when correcting the time of day. The step motors and gear trains of the seconds hand 5*a* are independent so that the elapsed time can be measured whilst confirming the time of day. Moreover, it is relatively simple to adjust the time of day. Even if the stem is in the second position it is possible to condition the circuitry to allow correction of chronograph time measurement by stopping it when the switch 7 is operated.

It would be feasible to arrange for the stem ot have only two positions and so when the stem is pulled out the minutes hand 5 would be corrected by mechanically rotating the step, the seconds hand 5*a* being stopped. In the same stem position the switches 7, 8, 9 could be used to regulate the chronograph time measurement. However, there is the disadvantage that the time of day is liable to inadvertent change. However, in the embodiment of the present invention described above various operations of the stem, that is pushing or pulling are required in order to set the precise time of day. First of all, after the stem is moved from the first position to the second position the indicators are set to the zero position. After than the stem is pushed in to the first position and the indicators are set to the true time. The seconds hand the indicator 21 are made to correspond to each other.

In the above embodiment there is no calendar mechanism so that the timepiece can be manufactured at a low cost.

In Figure 2, the switch 7 is operated to start and stop measurement of elapsed time. The switch 9 operates to measure split time. A conventional digital electronic timepiece is usually provided with a switch for starting and stopping measurement of elapsed time and a switch for resetting chronograph time measurement and measuring split time. In a digital liquid crystal electronic timepiece the functions can be instantly displayed whereby the user recognises the function being performed at any given instant. However, it is difficult to comprehend the complex operation such as split time measurement.

The embodiment of the present invention has a simplified operation by combining the operation of various push button switches. Thus chronograph time measurement is performed by using the buttons on the right hand side of the timepiece. The more complex function of split time measurement is performed by using the switch on the left hand side. Namely, the switch for split time measurement is independent of the switches for chronograph time measurement of elapsed time and this avoids erroneous operation. In the case of a timepiece which does not have a split time function the switch 9 can be dispensed with.

The indicators are easily and independently corrected by means of the switches. When repairing the timepiece, a watchmaker can easily check shift in the graduated scale or loosening thereof by causing the indicators to move stepwise by operating the switches.

An analog electronic timepiece according to the present invention can be provided with a calendar mechanism as in a conventional analog timepiece. Such a calendar mechanism can be corrected in the conventional manner.

Analog display timepieces having a plurality of step motors in some instances are not practical because a large current flow is required to drive a plurality of step motors simultaneously. A large battery is thus required to produce this large current and this is not practical in the case of small sized devices such as analog display wrist watches. However this disadvantage may be overcome in one embodiment of an analog electonic timepiece according to the present invention whilst still enabling the time of day and chronograph time information to be displayed at the same time.

Referring now to Figure 3 there is shown a block diagram of a second embodiment of an analog electronic timepiece according to the present invention. A time standard source 101, such a microsized quartz crystal resonator or oscillator circuit generates a time standard signal of 32.768 Hz. A divider and a waveform shaping circuit 102 divides the time standard signal into a time signal of relatively low frequency and shapes the signal. The output of the circuit 102 is applied to a chronograph measuring circuit 112 and a timekeeping circuit 103, a switch 111 for causing chronograph time measurement being provided. The timekeeping circuit 103 feeds a one second signal XA1 and a 20-seconds signal XA2 to a driving circuit 104. The driving circuit 104 generates a driving pulse signal PA1 corresponding to the signal XA1 and driving pulse signal PA2 corresponding to the signal XA2 when a signal S from the circuit 102 is high level. The measuring circuit 112 produces a one seconds signal XB1 and a sixty seconds signal XB2 and applies them to a driving circuit 113. The driving circuit 113 generates a driving pulse signal PB1 corresponding to the signal XB1 and the driving pulse signal PB2 corresponding to the signal XB2 when the signal S from the circuit 102 is high level.

Figure 4 shows the construction of each of the driving circuits 104, 113 in greater detail. Reference numerals 120 to 129 are master-slave flip-flops wherein outputs Q and $\overline{Q}$ vary in synchronism with the fall of a clock pulse applied to a terminal CP. Reference numerals 131 to 134 indicate latch circuits which pass a data signal applied to a terminal DM when the level of clock pulse applied to the terminal CP is high level and hold the data signal when the level of the clock pulse is low level. Reference numerals 135, 137, 139, 141 indicate NAND gates. Reference numerals 136, 138, 140, 142 indicate NOR gates, reference numerals 130, 143, 144, 145, 146 indicate inverters and reference numerals 147 to 154 indicate inverters for supplying sufficient current to drive the step motors.

The operation of the driving circuit of Figure 4 will be described with reference to Figures 5 and 6.

A differential signal of 1Hz whose pulse width is 0.98 msec is delivered from the timekeeping circuit 103 *via* a terminal I_1 to the flip-flop 120. An output signal XA1′ of the flip-flop 120 is divided into 1/2 Hz and fed to a terminal D of the flip-flop 124. The flip-flop 124 outputs a signal XA1″ up to the fall of the signal S of 64 Hz from the circuit 102. The signal XA1″ is fed to the terminal DM of a latch circuit 131 and delayed by 1/256 seconds to form a signal XA1‴ by means of a signal OM of 128 Hz delivered from a terminal I_6 to the terminal CP of the latch circuit 131. The signals XA1″ and XA1‴ are fed to a terminal 01 through the NAND gate 135 and to a terminal 02. The driving pulse circuit PA1 having a pulse width of 39 msec appears between the terminals 01 and 02. The driving pulse signal PA1 is necessarily produced when the signal S is low level in synchronism with the rise and fall of the signal XA1″ which varies in synchronism with fall of the signal S.

The signal XB1 whose pulse width is 0.98 msec is delivered from the measuring circuit 112 *via* a terminal I_3. The driving pulse signal PB1 is in synchronism with rise and fall of a signal XB1″ and appears across terminals 05 and 06. The driving pulse signal PB1 is produced while the signal S is high level and the signal XB1″ is changed in synchronism with the rise of the signal S.

The signal XA2 whose pulse width is 0.98 msec is produced from the timekeeping circuit 103 once every 20 seconds with the same timing as the signal XA1. The driving pulse signal PA2 appears across terminals 03 and 04 in synchronization with the rise and fall of a signal XA2‴ and necessarily is produced while the signal S is low level. The driving pulse signal PA2 is never produced with the same timing as the driving pulse signal PA1.

The signal XB2 whose pulse width is 0.98 msec is fed to a terminal I_4 from the measuring circuit 112 and with the same timing as the signal XB1 every 60 seconds. The driving pulse signal PB2 appears across terminals 07 to 08 and is delayed relative to the signal PB1 for one period. Thus the signals XB1, XB2, XA1, XA2 are such that the driving pulse signals PA1, PA2, PB1, PB2 are never produced with the same timing so that driving pulses are not simultaneously applied to the step motors.

In the embodiment of the present invention described above a stopwatch function has been referred to but it is clear that the present invention is applicable to analog electronic timepieces with other functions such as dual time display. This can be done by changing the measuring circuit for respective exclusive timekeeping circuits providing dual time display.

Additionally in the embodiment of the present invention chronograph time measurement has been performed by using three separate step motors. However it will be appreciated that two step motors or more than three step motors may be used.

Moreover in the embodiments of the present invention described above there are a plurality of step motors for displaying the time of day TA and a plurality of step motors for displaying another function TB other than time of day. The step motors are not driven simultaneously even if the function TB is performed at the same time as time of day display. Thus a small sized power source can be used without reduction of voltage. As a result the circuitry can operate normally at all times and the step motors are free from erroneous operation. This enables a small sized analog electronic timepiece having many functions, high accuracy and reliability to be constructed.

Moreover, as already mentioned, a user can effect the chronograph time measurement simply. Thus an analog electronic timepiece having many functions can be constructed and complex explanation of the various operations and external operating members to perform the functions can be dispensed with.

CLAIMS

1. An analog electronic timepiece comprising: a first step motor for driving a first hand which indicates the time of day; a second step motor which drives a second hand for indicating time information other than time of day; a common divider circuit for providing a clock signal to drive both the first and second step motors; switch means for controlling the second step motor independently of the first step motor; and a drive control circuit for selectively supplying an operating signal for operating the second hand and a correcting signal for altering the time information displayed by the second hand.

2. A timepiece as claimed in claim 1 including phase control means for shifting the phase of drive signals applied to the step motors relative to one another so that driving pulses of the drive signals are not simultaneously applied to both step motors.

3. A timepiece as claimed in claim 1 or 2 in which a third step motor is provided, the second and third step motors together indicating said time information other than time of day.

4. A timepiece as claimed in claim 3 in which the switch means is arranged to control operation of the third step motor independently of the first step motor.

5. A timepiece as claimed in any preceding claim including a chronograph measuring circuit for causing said second hand to display chronograph time information.

6. An analog electronic timepiece substantially as herein described with reference to and as shown in the accompanying drawings.

7. An analog electronic timepiece comprising a first step motor for driving a first indicating hand which indicates ordinary time and a second step motor for driving a second indicating hand which indicates the time except the ordinary time, characterised in that there are provided common divider for sending clock signal to driving circuit of said first step motor and said second step motor, switch means disposed between said divider and said driving circuit of second step motor so as to operate or stop said second step motor independently, selective and driving controlling circuit for supplying selectively operational signal and correction signal to said driving circuit of second step motor, and phase controlling means adapted to shift the phase so as not to superimpose each driving signal between said driving circuit of the first step motor and said driving circuit of the second step motor.

8. Any novel integer or step, or combination of integers or steps, hereinbefore described irrespective of whether the present claim is within the scope of, or relates to the same or a different invention from that of, the preceding claims.

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