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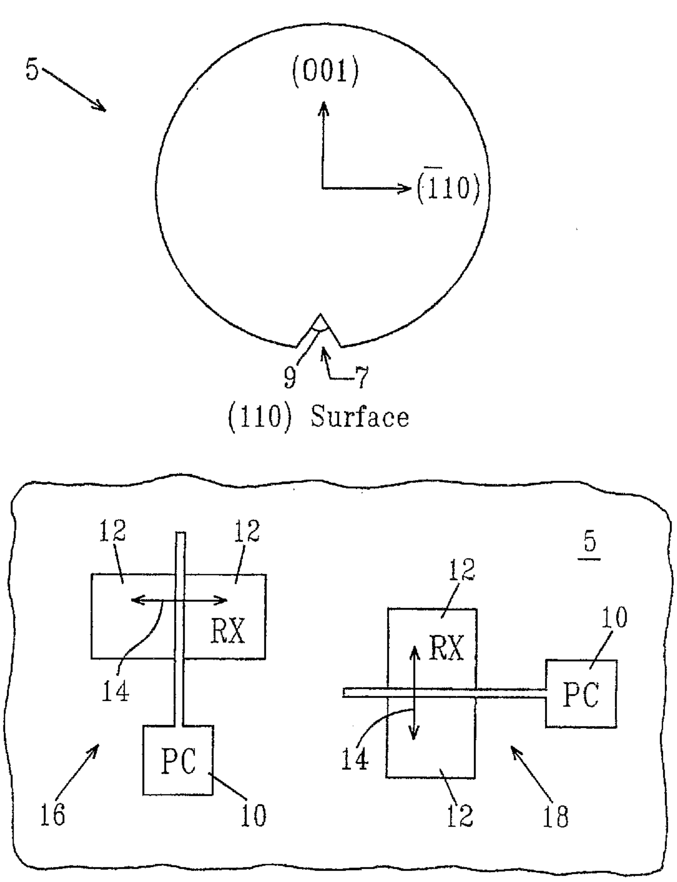
[Continued on next page]

(54) Title: SUBSTRATE ENGINEERING FOR OPTIMUM CMOS DEVICE PERFORMANCE



(57) Abstract: An integrated semiconductor structure having different types of complementary metal oxide semiconductor devices (CMOS), i.e., PFETs and NFETs, located atop a semiconductor substrate, wherein each CMOS device is fabricated such that the current flow for each device is optimal is provided. Specifically, the structure includes a semiconductor substrate that has a (110) surface orientation and a notch pointing in a <001> direction of current flow; and at least one PFET and at least one NFET located on the semiconductor substrate. The at least one PFET has a current flow in a <110> direction and the at least one NFET has a current flow in a <100> direction. The <110> direction is perpendicular to the <100> direction. A method of fabricating such as integrated semiconductor structure is also provided.

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Description

SUBSTRATE ENGINEERING FOR OPTIMUM CMOS DEVICE PERFORMANCE

Technical Field

[001] The present invention relates to integrated semiconductor structures, and more particularly to an integrated semiconductor structure having different types of complementary metal oxide semiconductor devices (CMOS), i.e., PFETs and NFETs, located atop a semiconductor substrate, wherein each CMOS device is fabricated such that the current flow for each device is optimal. The present invention also relates to a method of forming such an integrated semiconductor structure.

Background Art

[002] In the semiconductor industry, it has become more and more difficult in recent years to improve device performance. Mobility enhancement is a known way to improve complementary metal oxide semiconductor (CMOS) device performance. For example, it is known that the electron and hole mobility are affected by the wafer surface orientations as well as the current flow directions. This is because of the anisotropic effective mass behaviors of the inversion layer carriers.

[003] Currently, CMOS devices are formed on a semiconductor wafer that is based on a (100) surface orientation, i.e., crystal plane, with a notch or wafer flat located at the <011> direction. Such a wafer is shown, for example, in FIG. 1A. The surface orientation is defined as the surface normal vector out of the crystal plane of the semiconductor wafer. The standard notation for crystal planes is illustrated in FIGS. 2A, 2B and 2C. The current direction of a MOSFET can be designed at device layout. Under normal operation, the MOSFET current always flows from the source to the drain side modulated by the gate terminal. Therefore, the current flow direction can be controlled by rotating the PC (i.e., polysilicon mask) and RX (i.e., active silicon) masks with respect to the wafer notch.

[004] FIG. 1B is another pictorial representation of a semiconductor wafer having a (100) surface orientation with a notch located at the <011> direction. For a (100) oriented semiconductor wafer, the current flow is insensitive to the current flow directions, if polySi gates are laid out either parallel or perpendicular to the wafer notch.

[005] It is also known in the semiconductor industry that the substantial enhancement of hole mobility (2.7x) can be achieved by using a (110) surface-oriented semiconductor wafer. The enhancement factor is directional dependent. For example, there is more enhancement for the <110> direction than that of the <100> direction. However, electron mobility is known to be degraded in a (110) surface oriented wafer by a

comparable percentage. This electron mobility degradation on a (110) wafer is also directional dependent. For example, there is less degradation from the <100> direction than that of the <110> direction.

[006] In view of the state of the art mentioned above, there is a need for providing semiconductor substrate engineering for obtaining CMOS devices having optimum performance.

Disclosure of Invention

[007] The present invention provides a method as claimed in claim 1 and a structure as claimed in the independent structure claim. Preferred features are recited in the dependent claims.

[008] The present invention thus has advantages over other mobility enhancement techniques known in the art. For example, mobility enhancement caused by forming strained Si on a relaxed SiGe layer will affect dopant diffusion, defect density, and self-heating. The CMOS devices fabricated with the method of the present invention provide a net gain in mobility without affecting many of the other device characteristics. The additional cost to implement this feature is insignificant.

Brief Description of the Drawings

[009] The preferred embodiment of the present invention, which provides substrate engineering for optimum device performance, will now be described in greater detail by referring to the drawings that accompany the present application. In the accompanying drawings, like reference numerals are used for describing like and corresponding elements.

[010] FIGS. 1A-1B are pictorial representations of a standard prior art semiconductor wafer that is based on a (100) surface orientation with a notch located at a <011> direction.

[011] FIGS. 2A-2C are pictorial representations illustrating that the surface orientation is defined as the surface normal vector out of the crystal plane of the semiconductor wafer.

[012] FIG. 3 is a pictorial representation of a semiconductor substrate of a preferred embodiment of the present invention that is based on a (110) surface orientation with a notch located at a <001> direction.

[013] FIG. 4 is a pictorial representation (through a top-down view) showing the direction of current flow of the integrated semiconductor structure of the preferred embodiment of the present invention.

[014] FIGS. 5A-5F are pictorial representations (through cross-sectional views) showing the basic processing steps used in the preferred embodiment of the present invention.

Mode for the Invention

[015] As stated in the background section of the present application, the prior art typically forms its' semiconductor devices on a semiconductor substrate having a (100) surface orientation and a notch pointing at the <011> direction of current flow; See, for example, FIGS. 1A-1B. Applicants have determined through surface engineering that the prior art semiconductor substrate having a (100) surface orientation and a notch at the <011> direction of current flow is insensitive to current flow directions if the gates of the FET are laid out either parallel or perpendicular to the wafer notch.

[016] In an attempt to determine the optimum surface orientation and current flow for fabricating high performance semiconductor devices, the IV characteristics for PFETs and NFETs on semiconductor substrates with various surface orientations and current flow directions were determined. In particular, the applicants of the present application performed experimentation, in the terms of IV characteristics, to illustrate the enhancement (degradation) factor for PFETs and NFETs with various surface orientation and current flow. The following table summarizes the enhancement and degradation factors with respect to the current for various substrates.

Table 1

	(100) surface <100> direction	(110) surface <110> direction	(100) surface <100> direction
NFET	1	0.428	0.568
PFET	1	2.38	1.61

[017] From this table, the applicants of the present application have determined that in order to obtain optimal CMOS device performance the initial or starting semiconductor substrate should have a (110) surface orientation, i.e., a (110) crystal plane. It is also deduced from the above that when a semiconductor substrate having a (110) surface orientation is used, the NFETs should be laid out such that the current flows in the <100> direction, while the PFETs should be laid out such that the current flows in the <110> direction. Such a layout will provide an approximate 2.4x PFET current with NFET current reduced to about 57 % compared to that on a (100) wafer. Thus, by using a starting semiconductor substrate having a (110) surface orientation substantial PFET current enhancement with relatively small NFET current degradation will be obtained in the embodiment.

[018] FIG. 3 provides a pictorial representation of the initial or starting semiconductor substrate (labeled as 5) that is employed in the present invention. FIG. 3 includes the <001> direction and the <110> direction of current flow. The <100> direction of current flow is perpendicular to both the <001> and the <110>; hence the <100> direction is coming out of the plane of the drawing. The term "semiconductor

substrate" is used herein to denote any semiconducting material including, but not limited to: Si, SiGe, SiC, SiGeC, GaAs, InAs, InP or other like III/V compound semiconductors. A preferred semiconductor substrate is a Si substrate.

[019] As illustrated, the initial semiconductor substrate has a notch (labeled as 7) in which the apex (labeled as 9) is pointing at the <001> direction. The notch is formed in the semiconductor substrate using standard techniques that are well known to those skilled in the art.

[020] After providing the semiconductor substrate having a (110) surface orientation and a notch at the <001> direction of current flow, at least one NFET and a least one PFET are formed on the semiconductor substrate in a manner such that the at least one NFET has a current flow in the <100> direction, while the at least one PFET has a current flow in the <110> direction. That is, the NFETs are formed so as to be perpendicular to the PFETs. This configuration for the at least one NFET and the at least one PFET is shown, for example, in FIG. 4. In FIG. 4, PC (labeled as element 10) denotes the gate region, while RX (labeled as 12) denotes the source/drain regions. The direction of current flow is labeled as 14. The NFET is labeled as 16, while the PFET is labeled as 18.

[021] The integrated semiconductor structure of the preferred embodiment of the present invention thus includes a semiconductor substrate 5 having a (110) surface orientation and a notch 7 pointing in a <001> direction of current flow (see FIG. 3); and at least one PFET 18 and at least one NFET 16 located on the semiconductor substrate 5, wherein said at least one PFET 18 has a current flow in a <110> direction and the at least one NFET 16 has a current flow in a <100> direction, said <110> direction is perpendicular to the <100> direction (see FIG. 4).

[022] The at least one NFET and at least one PFET are formed using conventional CMOS processing steps that are well known to those skilled in the art except that the NFETs and PFETs are fabricated such that they have current flow that is perpendicular to each other. The process flow will now be described in greater detail with reference to FIGS. 5A-5F. The process flow for fabricating such NFETs and PFETs may begin with forming one or more isolation regions (not specifically shown), such as trench isolation regions or local oxidation of silicon (LOCOS) isolation regions, in the substrate.

[023] The formation of the LOCOS oxidation region includes the use of a standard LOCOS process. The trench isolation regions are formed by first forming a sacrificial material (not shown), such as an oxide, on the surface of the semiconductor substrate. The sacrificial material may be formed by deposition or by a thermal process such as oxidation. Trench regions are then formed into the semiconductor substrate by applying a photoresist to the sacrificial material, exposing the photoresist to a pattern of radiation, developing the pattern into the exposed photoresist using a conventional

resist developer, and transferring the pattern from the photoresist into the sacrificial material and then the semiconductor substrate using an etching process such as reactive-ion etching (RIE). After pattern transfer, the photoresist may or may not be removed from the structure utilizing a conventional resist stripping process. A trench liner, such as TiN, may be formed onto the exposed sidewalls of the trench by deposition or a thermal technique and then the trench is filled with a trench dielectric material such as, for example, a high density plasma oxide or tetraethylorthosilicate (TEOS). After trench fill, the structure may be planarized to the top surface of the semiconductor substrate. The isolation regions may be located between the NFETs and the PFETs.

[024] A gate dielectric 50 (see FIG. 5A) is formed on a surface of the semiconductor substrate 5 by deposition or thermal oxidation, nitridation or oxynitridation. Combinations of the aforementioned processes may also be used in forming the gate dielectric 50. The gate dielectric 50 is comprised of an insulating material including, but not limited to: an oxide, nitride, oxynitride or any combination thereof.

[025] A highly preferred insulating material that is employed in the present invention as the gate dielectric 50 is SiO_2. Although it is preferred to use SiO_2 as the gate dielectric material, the present invention also contemplates using insulating materials, i.e., dielectrics, which have a higher or lower dielectric constant, k, than SiO_2. For example, the gate dielectric 50 may be comprise a high-k oxide such as Al_2O_3 or a perovskite-type oxide.

[026] The physical thickness of the gate dielectric 50 may vary, but typically the gate dielectric 50 has a thickness of from about 0.5 to about 20 nm, with a thickness of from about 1.0 to about 10.0 nm being more highly preferred.

[027] After forming the gate dielectric 50, a gate conductor 52 is formed on at least the exposed upper surface of the gate dielectric 50 (see, FIG. 5B). The gate conductor 52 is comprised of a conductive material including, but not limited to: elemental metals such as W, Pt, Pd, Ru, Re, Ir, Ta, Mo or combinations, including alloys, and multilayers thereof; silicides and nitrides of the foregoing elemental metals; polysilicon either doped or undoped; or combinations and multilayers thereof. One highly preferred conductive material employed as the gate conductor 52 is doped polysilicon.

[028] The gate conductor 52 is formed utilizing a deposition process such as CVD, plasma-assisted CVD, sputtering, evaporation, chemical solution deposition or plating. When metal silicides are employed, a conventional silicidation process may be used in forming the same. On the other hand, when doped polysilicon is employed as the gate conductor 52, the doped polysilicon may be formed by an in-situ doping deposition process, or alternatively, a layer of undoped silicon is first deposited and thereafter an ion implantation process is employed in doping the undoped polysilicon. The doping

of the undoped polysilicon may occur immediately after deposition or in a later processing step.

[029] The physical thickness of the gate conductor 52 formed at this point of the present invention may vary depending on the conductive material employed as well as the process used in forming the same. Typically, however, the gate conductor 52 has a thickness of from about 20 to about 400 nm, with a thickness of from about 50 to about 200 nm being more highly preferred.

[030] A hard mask, not shown, may be formed atop the gate conductor prior to patterning the gate conductor. The hard mask may be comprised of an oxide, nitride, oxynitride or any combination thereof.

[031] The gate conductor 52 (and optional hard mask) may be patterned at this point of the present invention utilizing lithography and an etching step to provide a plurality of patterned gate conductors 54. FIG. 5C shows the structure after the patterning step. The NFET device region is labeled as 100 and the PFET device region is labeled as 102. Although showing the presence of a single patterned gate conductor in each device region, a plurality of patterned gate conductors may be formed in each device region, as appropriate. The etching step may stop atop the gate dielectric 50 or it may remove the gate dielectric 50. In embodiments where a hard mask is employed, this etching step may also remove the hard mask from the structure. FIG. 5C shows a structure in which the etching stops atop the gate dielectric 50.

[032] Next, source/drain extensions (not shown) may be formed into the semiconductor substrate using an ion implantation process. Spacers 56 are then formed on the sidewalls of each patterned gate conductor 54. See FIG. 5D. The spacers 56 are comprised of a conventional insulating material such as an oxide, nitride, oxynitride or any combination including multilayers thereof. Preferably, the spacers 56 are composed of SiN or SiO_2, with SiN spacers being especially preferred in the present invention. The spacers 56 are formed by deposition and etching. Note that the spacers 56 can be formed atop a portion of gate dielectric as shown, or they may be formed directly atop the semiconductor substrate if the gate dielectric was previously removed. In embodiments where the gate dielectric was not previously removed, the unprotected portions of the gate dielectric 50 can be removed during or after the spacer etch. Note also that the hard mask may also be removed during this step.

[033] At this point, a block mask is formed over a portion of the semiconductor substrate in which either the NFET or PFET will be formed. FIG. 5E shows the case in which block mask 60 is formed atop the PFET device region 102.

[034] Next, source/drain regions 58 for the NFETs may be formed into the semiconductor substrate by ion implantation and annealing. The dopant for forming the NFETs is arsenic and/or phosphorus. The resultant structure including source/drain regions 58 is

shown, for example, in FIG. 5F.

[035] After forming the source/drain regions in the NFET gate region, the block mask 60 is removed from the structure using a conventional resist stripping process; another block mask is formed over the thus completed NFET region; and then the source/drain regions for PFETs are formed using boron and/or antimony, for example, as the dopant ion. In accordance with the present invention, the PFETs are formed such that the current flow is perpendicular to the current flow of the NFETs region. This can be accomplished by 1) placing the PFETs such that the direction indicated as 14 in FIG. 4 is pointing to the wafer notch, or 2) placing the NFETs such that the direction indicated as 14 of FIG. 4 is pointing to the direction perpendicular to the wafer notch.

[036] After forming the PFETs perpendicular to the NFET the other block mask is removed providing the structure shown in FIG. 4. Note that although the above describes forming the NFETs prior to the PFETs, the process flow works when the PFETs are formed prior to the NFETs.

Claims

[001] A method of forming an integrated semiconductor structure comprising the steps of: providing a semiconductor substrate that has a (110) surface orientation and a notch pointing in a <001> direction of current flow; and fabricating at least one PFET and at least one NFET on the semiconductor substrate, wherein said at least one PFET has a current flow in a <110> direction and the at least one NFET has a current flow in a <100> direction, said <110> direction is perpendicular to the <100> direction.

[002] The method of Claim 1 wherein said at least one PFET and at least one NFET are formed by the steps of: forming a gate dielectric on a surface of the semiconductor substrate; forming patterned gate conductors on the gate dielectric; blocking some of the patterned gate conductors with a block mask; forming source/drain regions in the unblocked areas; removing the block mask; forming another block mask over areas containing the source and drain regions; and forming source/drain regions in the previously unblocked areas.

[003] The method of Claim 2 further comprising forming spacers on exposed sidewalls of each patterned gate conductor prior to said blocking step.

[004] The method of Claim 2 wherein said gate dielectric is formed by a thermal process or deposition.

[005] The method of Claim 2 wherein the patterned gate conductors are formed by deposition and etching.

[006] The method of Claim 1 wherein the at least one NFET comprises source/drain regions formed by ion implanting a dopant selected from the group consisting of arsenic and phosphorus into the semiconductor substrate.

[007] The method of Claim 1 wherein the at least one PFET comprising source/drain regions formed by ion implanting a dopant selected from the group consisting of boron and antimony into the semiconductor substrate.

[008] The method of Claim 1 wherein the at least one PFET and the at least one NFET each include source/drain regions, wherein the source/drain regions of the at least one PFET lie perpendicular to the source/drains of the at least one NFET.

[009] The method of Claim 1 wherein said fabricating comprises placing the at least one PFET such that the current flow of the at least one PFET is pointed to the notch.

[010] The method of Claim 1 wherein said fabricating comprises placing the at least one NFET such that the current flow of the at least one NFET is perpendicular to the notch.

[011] An integrated semiconductor structure comprising a semiconductor substrate that

has a (110) surface orientation and a notch pointing in a <001> direction of current flow; and at least one PFET and at least one NFET located on the semiconductor substrate, wherein said at least one PFET has a current flow in a <110> direction and the at least one NFET has a current flow in a <100> direction, said <110> direction is perpendicular to the <100> direction.

[012] The integrated semiconductor structure of Claim 11 wherein said semiconductor structure is a semiconducting material selected from the group consisting of Si, SiGe, SiC, SiGeC, GaAs, InAs, InP and other like III/V compound semiconductors.

[013] The integrated semiconductor structure of Claim 12 wherein the semiconductor material is Si.

[014] The integrated semiconductor structure of Claim 11 wherein the at least one NFET and the at least one PFET each comprise a gate dielectric located on the semiconductor substrate, a patterned gate conductor located on portions of the gate dielectric, and spacers located on exposed sidewalls of the patterned gate conductor.

[015] The integrated semiconductor structure of Claim 14 wherein the gate dielectric is an oxide.

[016] The integrated semiconductor structure of Claim 14 wherein the patterned gate conductor comprises polySi.

[017] The integrated semiconductor structure of Claim 11 wherein the at least one PFET and the at least one NFET each include source/drain regions, wherein the source/drain regions of the at least one PFET lie perpendicular to the source/drains of the at least one NFET.

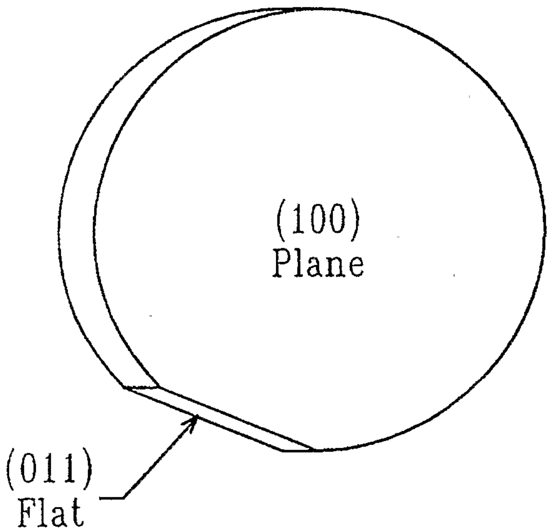


FIG.1A
(Prior Art)

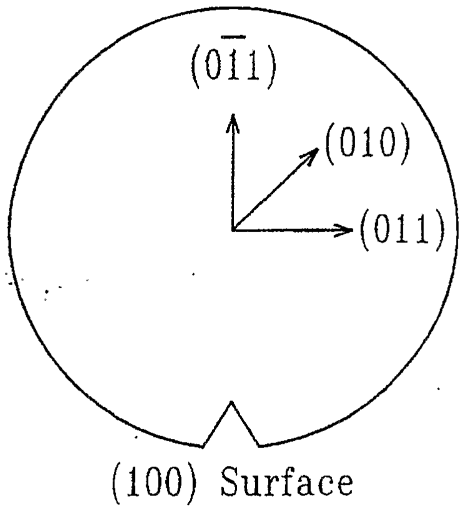


FIG.1B
(Prior Art)

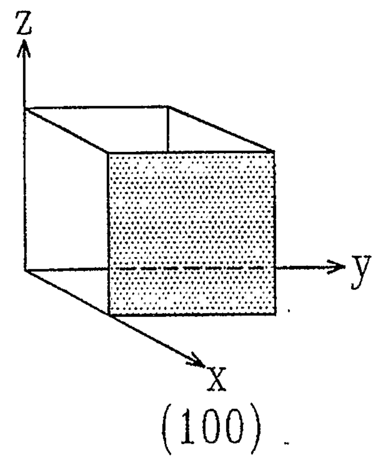


FIG.2A
(Prior Art)

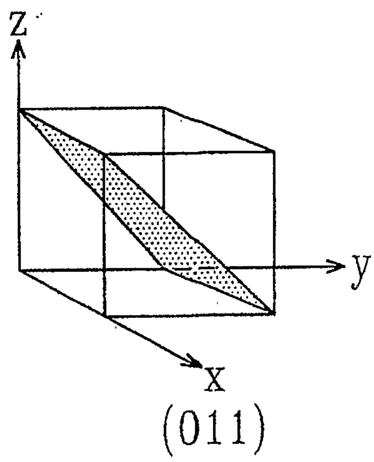


FIG.2B
(Prior Art)

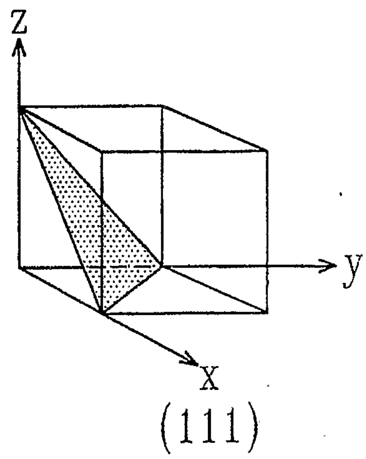


FIG.2C
(Prior Art)

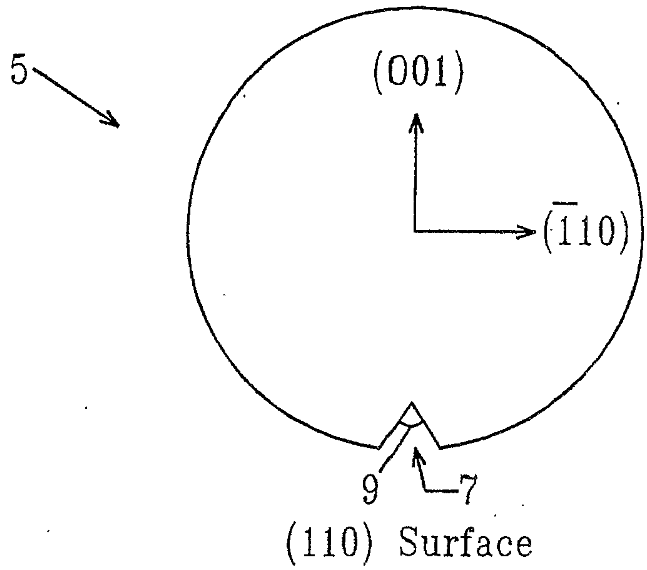
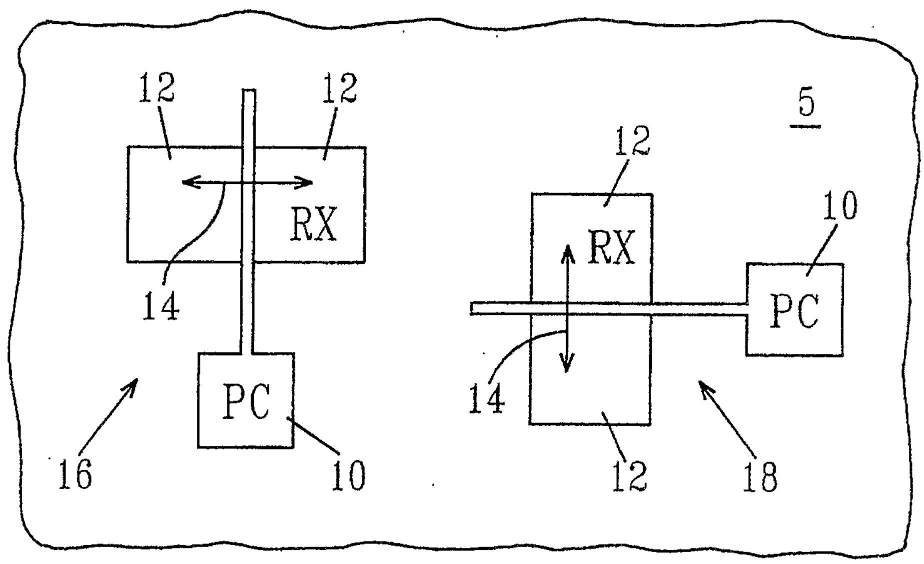

5
(001)
$(\bar{1}10)$
9
7
(110) Surface

FIG.3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12
RX
14
PC
16
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12
RX
10
PC
14
12
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FIG.4

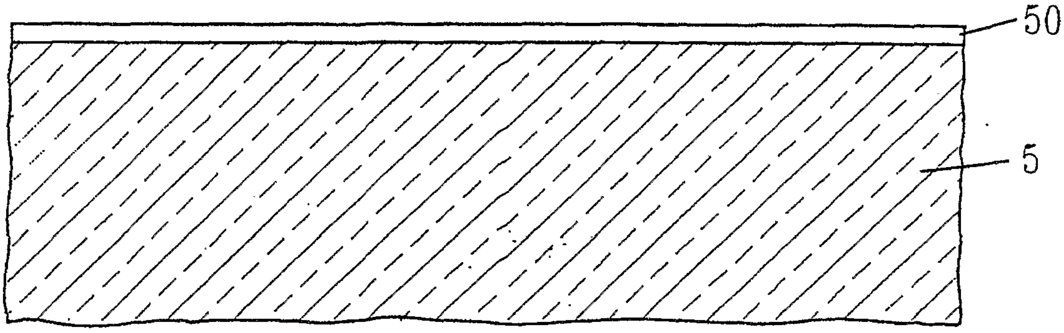

FIG.5A

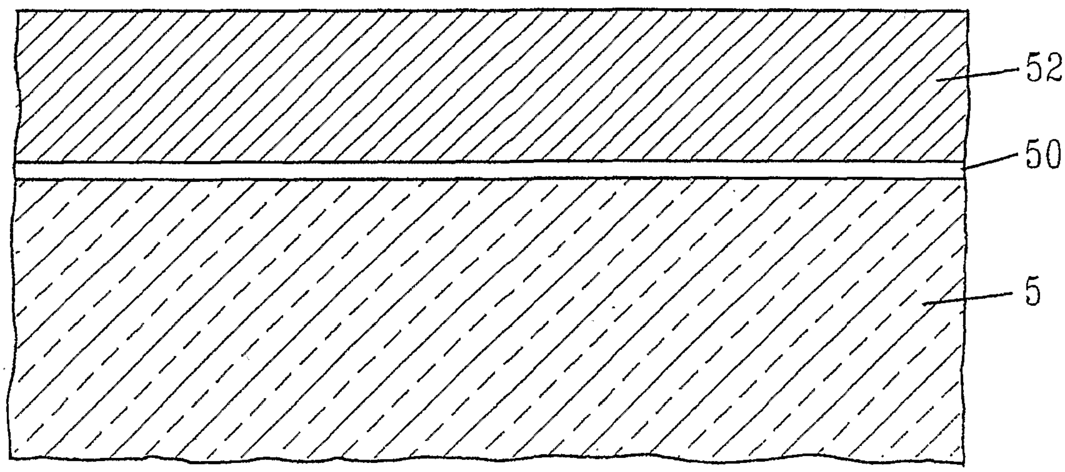

FIG.5B

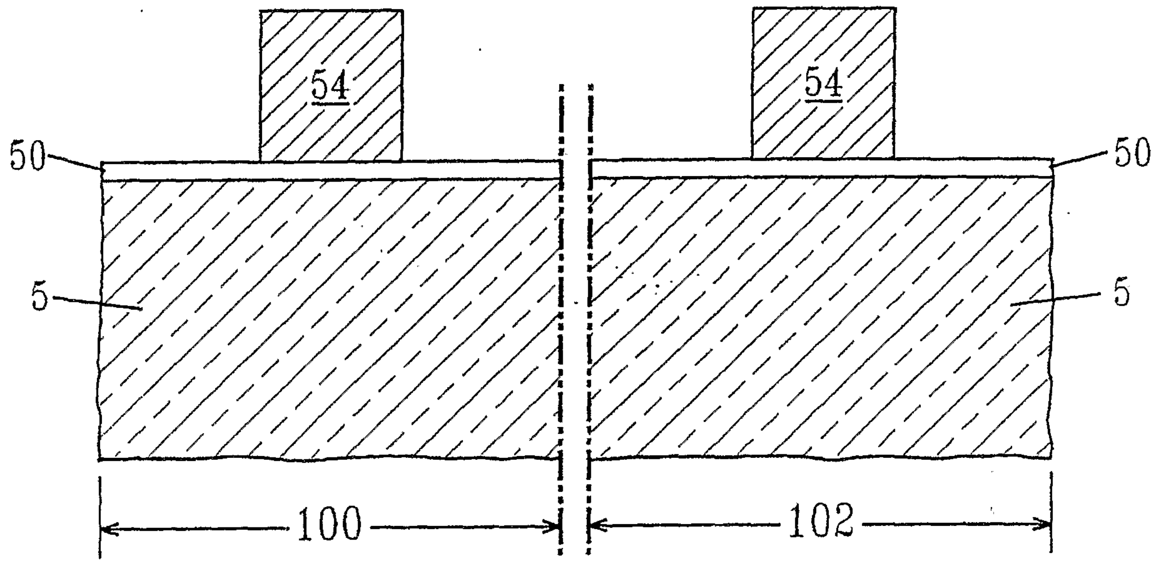

FIG.5C

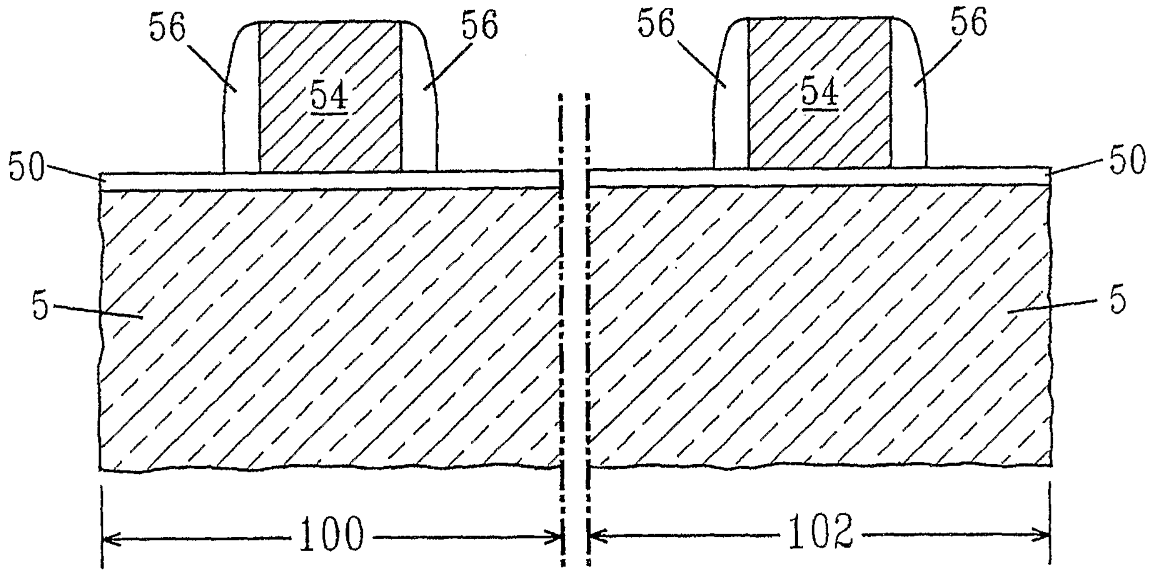

FIG.5D

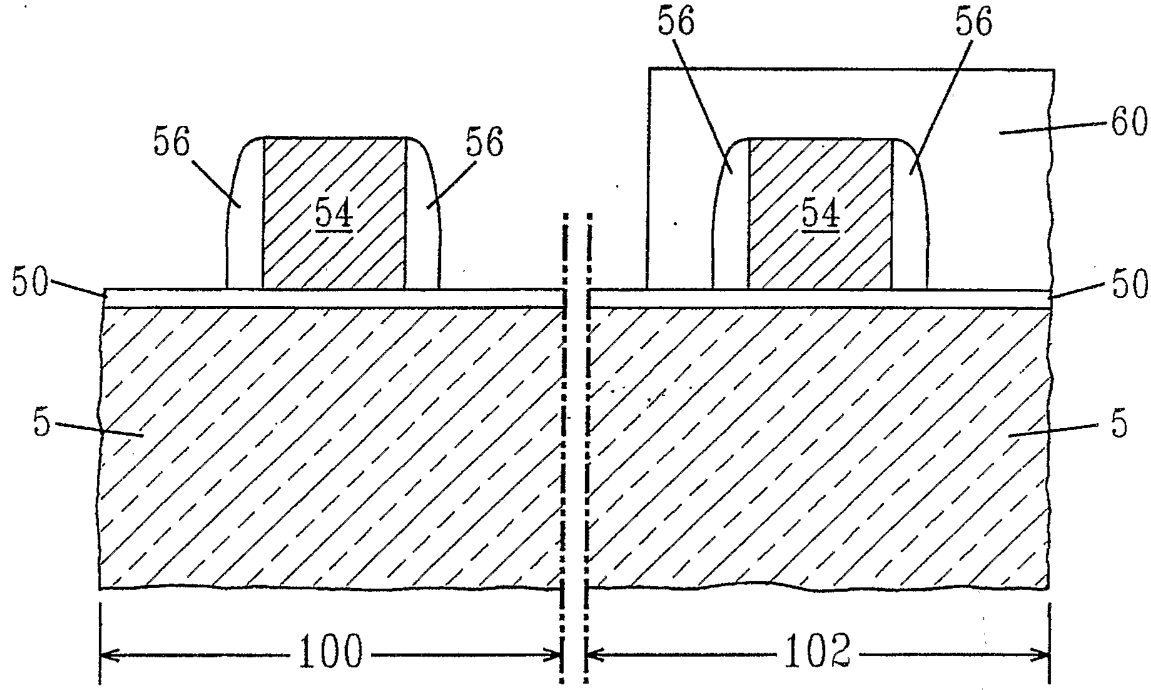
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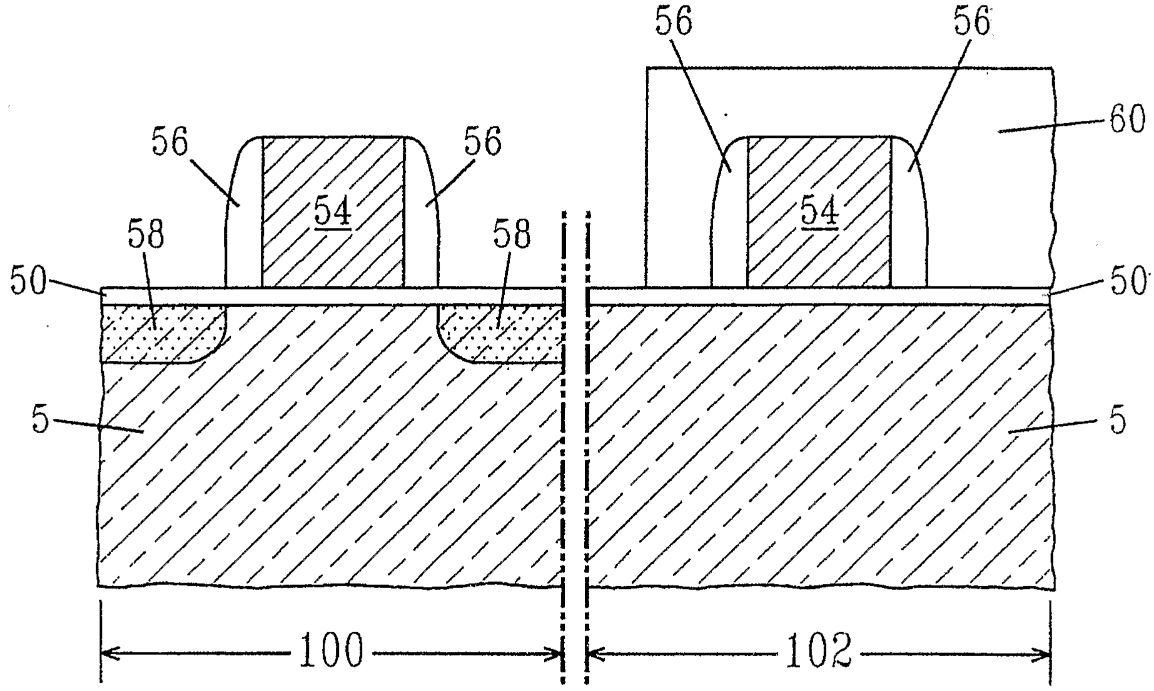
FIG.5E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100
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FIG.5F

INTERNATIONAL SEARCH REPORT

International Application No
PCT/EP2004/050879

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L21/8238 H01L27/092

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 317 175 A (THRONGNUMCHAI KRAISORN) 31 May 1994 (1994-05-31)	1,11-17
Y	column 2, line 65 - column 3, line 31 column 3, line 50 - column 6, line 58 figures 1,4,6	2-10
Y	US 2002/173093 A1 (JUENGLING WERNER) 21 November 2002 (2002-11-21) paragraph '0027! - paragraph '0054! figures 2-5	2-10
A	GB 1 229 946 A (TEXAS INSTRUMENTS INC) 28 April 1971 (1971-04-28) the whole document	1-17
A	US 2001/026006 A1 (FORBES LEONARD ET AL) 4 October 2001 (2001-10-04) the whole document	1-17

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
26 October 2004	03/11/2004

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International Application No
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