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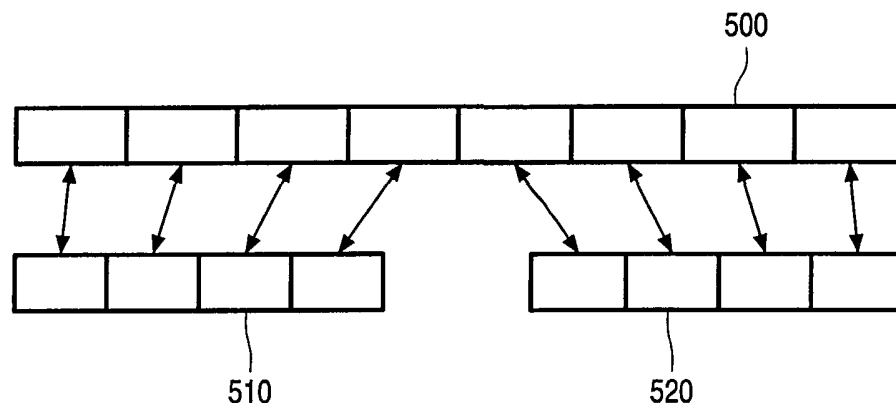
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(54) Title: AN ADDRESS GENERATION UNIT FOR A PROCESSOR



(57) Abstract: A processor includes a memory port for accessing a physical memory under control of an address. A processing unit executing instructions stored in the memory and/or operates on data stored in the memory. An address generation unit ("AGU") generates address for controlling access to the memory; the AGU being associated with a plurality of N registers enabling the AGU to generate the address under control of an address generation mechanism. A memory unit is operative to save/load k of the N registers, where $2 \leq k \leq N$, triggered by one operation. To this end, the memory unit includes a concatenator for concatenating the k registers to one memory word to be written to the memory through the memory port and a splitter for separating a word read from the memory through the memory port into the k registers.

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INTERNATIONAL SEARCH REPORT

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A. CLASSIFICATION OF SUBJECT MATTER
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According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 99/14663 A (SIEMENS MICROELECTRONICS INC) 25 March 1999 (1999-03-25) page 6, line 17 - page 7, line 27 abstract page 2, line 6 - page 3, line 10 page 4, line 20 - page 5, line 2	1, 3, 4, 7, 10
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A	EP 1 091 290 A (INFINEON TECHNOLOGIES AG) 11 April 2001 (2001-04-11)	

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Patent family members are listed in annex.

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