(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
07 April 2022 (07.04.2022)

WIPO | PCT

(10) International Publication Number
WO 2022/072085 A1

(51) International Patent Classification:
G06F 30/373 (2020.01) *G06N 3/08* (2006.01)
G06F 30/27 (2020.01) *G06F 119/18* (2020.01)
G06F 30/398 (2020.01) *G06F 119/22* (2020.01)
G06F 30/367 (2020.01)

(21) International Application Number:
PCT/US2021/047595

(22) International Filing Date:
25 August 2021 (25.08.2021)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
17/037,226 29 September 2020 (29.09.2020) US

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, IT, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, WS, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

(54) Title: TECHNIQUES FOR USING CONVEX FABRICATION LOSS FUNCTIONS DURING AN INVERSE DESIGN PROCESS TO OBTAIN FABRICABLE DESIGNS

(57) Abstract: In some embodiments, techniques for creating a fabricable segmented design for a physical device are provided. A computing system receives a design specification. The computing system generates a proposed segmented design based on the design specification. The computing system determines one or more fabricable segmented designs based on the proposed segmented design. The computing system determines an overall fabrication loss value based on the one or more fabricable segmented designs. The computing system backpropagates a gradient of the overall fabrication loss value to create an updated design specification.

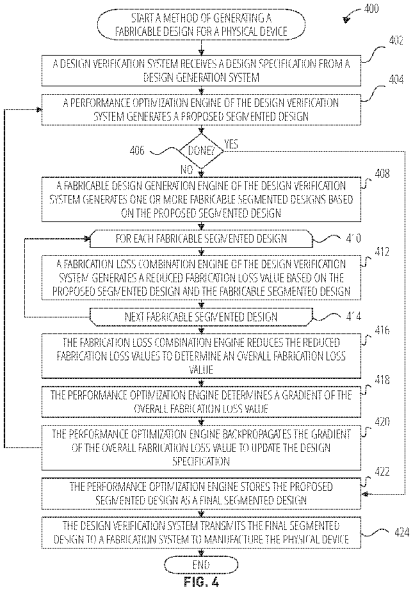

FIG. 4

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Published:
— *with international search report (Art. 21(3))*

TECHNIQUES FOR USING CONVEX FABRICATION LOSS FUNCTIONS DURING AN INVERSE DESIGN PROCESS TO OBTAIN FABRICABLE DESIGNS

TECHNICAL FIELD

[0001] This disclosure relates generally to designing and manufacturing physical devices, and in particular but not exclusively, relates to inverse design of optical and electromagnetic devices.

BACKGROUND

[0002] Optical and electromagnetic devices are devices that create, manipulate, propagate, and/or measure electromagnetic radiation. Their applications vary broadly and include, but are not limited to, acousto-optic modulators, optical modulators, optical ring resonators, distributed Bragg reflectors, lasers, lenses, transistors, waveguides, antennas, and the like. Design of these devices is sometimes determined through a simple guess and check method in which a small number of design parameters of a pre-determined design are adjusted for suitability to a particular application. However, in actuality, these devices may have design parameters ranging from hundreds all the way to many billions, dependent on the device size and functionality. As functionality of these optical and electromagnetic devices is increased and manufacturing improves to allow for smaller device feature sizes, it becomes increasingly important to take full advantage of these improvements via optimized device design.

[0003] Though some techniques for generating device designs exist, some of these techniques simply generate device designs without considering whether the generated designs can be fabricated. A need exists for techniques for measuring and verifying the fabricability of device designs.

BRIEF SUMMARY

[0004] In some embodiments, a non-transitory computer-readable medium is provided. The computer-readable medium has logic stored thereon that, in response to execution by one or more processors of a computing system, causes the computing system to perform actions for creating a fabricable segmented design for a physical device, the actions comprising: receiving, by the computing system, a design specification; generating, by the computing system, a proposed segmented design based on the design specification; determining, by the computing system, one or more fabricable segmented

designs based on the proposed segmented design; determining, by the computing system, an overall fabrication loss value based on the one or more fabricable segmented designs; and backpropagating, by the computing system, a gradient of the overall fabrication loss value to create an updated design specification.

[0005] In some embodiments, a method of creating a fabricable segmented design for a physical device is provided. A computing system receives a design specification. The computing system generates a proposed segmented design based on the design specification. The computing system determines one or more fabricable segmented designs based on the proposed segmented design. The computing system determines an overall fabrication loss value based on the one or more fabricable segmented designs. The computing system backpropagates a gradient of the overall fabrication loss value to create an updated design specification.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

[0006] Non-limiting and non-exhaustive embodiments of the invention are described with reference to the following figures, wherein like reference numerals refer to like parts throughout the various views unless otherwise specified. Not all instances of an element are necessarily labeled so as not to clutter the drawings where appropriate. The drawings are not necessarily to scale, emphasis instead being placed upon illustrating the principles being described. To easily identify the discussion of any particular element or act, the most significant digit or digits in a reference number refer to the figure number in which that element is first introduced.

[0007] FIG. 1A illustrates a demonstrative simulated environment describing a photonic integrated circuit, in accordance with an embodiment of the present disclosure.

[0008] FIG. 1B illustrates an example operational simulation of a photonic integrated circuit, in accordance with an embodiment of the present disclosure.

[0009] FIG. 1C illustrates an example adjoint simulation within the simulated environment by backpropagating a loss value, in accordance with an embodiment of the present disclosure.

[0010] FIG. 2 is a schematic drawing that illustrates a non-limiting example embodiment of a segmented design according to various aspects of the present disclosure.

[0011] FIG. 3 is a block diagram that illustrates a non-limiting example embodiment of a system according to various aspects of the present disclosure.

[0012] FIG. 4 is a flowchart that illustrates a non-limiting example embodiment of a method of generating a fabricable design for a physical device according to various aspects of the present disclosure.

DETAILED DESCRIPTION

[0013] FIG. 1A-FIG. 1C respectively illustrate an initial set up of a simulated environment describing a photonic device, performing an operational simulation of the photonic device in response to an excitation source within a simulated environment, and performing an adjoint simulation of the photonic device within a simulated environment. As illustrated in FIG. 1A-FIG. 1C, simulated environment is represented in two- dimensions. However, it is appreciated that other dimensionality (*e.g.*, 3-dimensional space) may also be used to describe simulated environment and the photonic device. In some embodiments, optimization of structural parameters of the photonic device illustrated in FIG. 1A-FIG. 1C may be achieved via an inverse design process including, *inter alia*, simulations (*e.g.*, operational simulations and adjoint simulations) that utilize a finite-difference time-domain (FDTD) method to model the field response (*e.g.*, electric and magnetic field) to an excitation source.

[0014] FIG. 1A illustrates a demonstrative simulated environment 106 describing a photonic integrated circuit (*i.e.*, a photonic device such as a waveguide, demultiplexer, and the like), in accordance with an embodiment of the present disclosure. More specifically, in response to receiving an initial description of a photonic device defined by one or more structural parameters (*e.g.*, an input design), a system configures a simulated environment 106 to be representative of the photonic device. As illustrated, the simulated environment 106 (and subsequently the photonic device) is described by a plurality of segments 112, which represent individual elements (*i.e.*, discretized) of the two-dimensional (or other dimensionality) space. Each of the segments 112 is illustrated as two-dimensional squares; however, it is appreciated that the segments may be represented as cubes or other shapes in three-dimensional space. It is appreciated that the specific shape and dimensionality of the plurality of segments 112 may be adjusted dependent on the simulated environment 106 and photonic device (or other physical device) being simulated. It is further noted that only a portion of the plurality of segments 112 are illustrated to avoid obscuring other aspects of the simulated environment 106.

[0015] Each of the plurality of segments 112 may be associated with a structural value, a field value, and a source value. Collectively, the structural values of the simulated environment 106 describe the structural parameters of the photonic device. In one embodiment, the structural values may correspond to a relative permittivity, permeability, and/or refractive index that collectively describe structural (*i.e.*, material) boundaries or interfaces of the photonic device. For example, an interface 116 is representative of where relative permittivity changes within the simulated environment 106 and may define a boundary of the photonic device where a first material meets or otherwise interfaces with a second material. The field value describes the field (or loss) response that is calculated (*e.g.*, via Maxwell's equations) in response to an excitation source described by the source value. The field response, for example, may correspond to a vector describing the electric and/or magnetic fields (*e.g.*, in one or more orthogonal directions) at a particular time step for each of the plurality of segments 112. Thus, the field response may be based, at least in part, on the structural parameters of the photonic device and the excitation source.

[0016] In the illustrated embodiment, the photonic device corresponds to an optical demultiplexer having a design region 114, in which structural parameters of the physical device may be updated or otherwise revised. More specifically, through an inverse design process, iterative gradient-based optimization of a loss metric determined from a loss function is performed to generate a design of the photonic device that functionally causes a multi-channel optical signal to be demultiplexed and guided from input port 102 to a corresponding one of the output ports 104. Thus, input port 102 of the photonic device corresponds to a location of an excitation source to provide an output (*e.g.*, a Gaussian pulse, a wave, a waveguide mode response, and the like). The output of the excitation source interacts with the photonic device based on the structural parameters (*e.g.*, an electromagnetic wave corresponding to the excitation source may be perturbed, retransmitted, attenuated, refracted, reflected, diffracted, scattered, absorbed, dispersed, amplified, or otherwise as the wave propagates through the photonic device within simulated environment 106). In other words, the excitation source may cause the field response of the photonic device to change, which is dependent on the underlying physics governing the physical domain and the structural parameters of the photonic device. The excitation source originates or is otherwise proximate to input port 102 and is positioned to propagate (or otherwise influence the field values of the plurality of segment) through the design region 114 towards output ports 104 of the photonic device. In the illustrated

embodiment, the input port 102 and output ports 104 are positioned outside of the design region 114. In other words, in the illustrated embodiment, only a portion of the structural parameters of the photonic device is optimizable.

[0017] However, in other embodiments, the entirety of the photonic device may be placed within the design region 114 such that the structural parameters may represent any portion or the entirety of the design of the photonic device. The electric and magnetic fields within the simulated environment 106 (and subsequently the photonic device) may change (*e.g.*, represented by field values of the individual segment that collectively correspond to the field response of the simulated environment) in response to the excitation source. The output ports 104 of the optical demultiplexer may be used for determining a performance metric of the photonic device in response to the excitation source (*e.g.*, power transmission from input port 102 to a specific one of the output ports 104). The initial description of the photonic device, including initial structural parameters, excitation source, performance parameters or metrics, and other parameters describing the photonic device, may be received by a system and used to configure the simulated environment 106 for performing a first-principles based simulation of the photonic device. These specific values and parameters may be defined directly by a user, indirectly (*e.g.*, by a system culling pre-determined values stored in a memory, local storage, or remote resources), or a combination thereof.

[0018] FIG. 1B illustrates an operational simulation of the photonic device in response to an excitation source within simulated environment 108, in accordance with various aspects of the present disclosure. In the illustrated embodiment, the photonic device is an optical demultiplexer structured to optically separate each of a plurality of distinct wavelength channels included in a multi-channel optical signal received at input port 102 and respectively guide each of the plurality of distinct wavelength channels to a corresponding one of the plurality of output ports 104. The excitation source may be selected (randomly or otherwise) from the plurality of distinct wavelength channels and originates at input port 102 having a specified spatial, phase, and/or temporal profile. The operational simulation occurs over a plurality of time steps, including the illustrated time step. When performing the operational simulation, changes to the field response (*e.g.*, the field value) for each of the plurality of segments 112 are incrementally updated in response to the excitation source over the plurality of time steps. The changes in the field response at a particular time step are based, at least in part, on the structural parameters,

the excitation source, and the field response of the simulated environment 110 at the immediately prior time step included in the plurality of time steps. Similarly, in some embodiments the source value of the plurality of segments 112 is updated (*e.g.*, based on the spatial profile and/or temporal profile describing the excitation source). It is appreciated that the operational simulation is incremental and that the field values (and source values) of the simulated environment 110 are updated incrementally at each time step as time moves forward for each of the plurality of time steps during the operational simulation. It is further noted that in some embodiments, the update is an iterative process and that the update of each field and source value is based, at least in part, on the previous update of each field and source value.

[0019] Once the operational simulation reaches a steady state (*e.g.*, changes to the field values in response to the excitation source substantially stabilize or reduce to negligible values) or otherwise concludes, one or more performance metrics may be determined. In some embodiments, the performance metric corresponds to the power transmission at a corresponding one of the output ports 104 mapped to the distinct wavelength channel being simulated by the excitation source. In other words, in some embodiments, the performance metric represents power (at one or more frequencies of interest) in the target mode shape at the specific locations of the output ports 104. A loss value or metric of the input design (e.g., the initial design and/or any refined design in which the structural parameters have been updated) based, at least in part, on the performance metric may be determined via a loss function. The loss metric, in conjunction with an adjoint simulation, may be utilized to determine a structural gradient (*e.g.*, influence of structural parameters on loss metric) for updating or otherwise revising the structural parameters to reduce the loss metric (*i.e.* increase the performance metric). It is noted that the loss metric may be further based on a fabrication loss value that is utilized to enforce a minimum feature size or other fabricability constraints of the photonic device to promote fabricability of the device.

[0020] FIG. 1C illustrates an example adjoint simulation within simulated environment 110 by backpropagating a loss metric, in accordance with various aspects of the present disclosure. More specifically, the adjoint simulation is a time-backwards simulation in which a loss metric is treated as an excitation source that interacts with the photonic device and causes a loss response. In other words, an adjoint (or virtual source) based on the loss metric is placed at the output region (*e.g.*, output ports 104) or other

location that corresponds to a location used when determining the performance metric. The adjoint source(s) is then treated as a physical stimuli or an excitation source during the adjoint simulation. A loss response of the simulated environment 110 is computed for each of the plurality of time steps (*e.g.*, backwards in time) in response to the adjoint source. The loss response collectively refers to loss values of the plurality of segment that are incrementally updated in response to the adjoint source over the plurality of time steps. The change in loss response based on the loss metric may correspond to a loss gradient, which is indicative of how changes in the field response of the physical device influence the loss metric. The loss gradient and the field gradient may be combined in the appropriate way to determine a structural gradient of the photonic device/simulated environment (*e.g.*, how changes in the structural parameters of the photonic device within the simulated environment influence the loss metric). Once the structural gradient of a particular cycle (*e.g.*, operational and adjoint simulation) is known, the structural parameters may be updated to reduce the loss metric and generate a revised description or design of the photonic device.

[0021] In some embodiments, iterative cycles of performing the operational simulation, and adjoint simulation, determining the structural gradient, and updating the structural parameters to reduce the loss metric are performed successively as part of an inverse design process that utilizes iterative gradient-based optimization. An optimization scheme such as gradient descent may be utilized to determine specific amounts or degrees of changes to the structural parameters of the photonic device to incrementally reduce the loss metric. More specifically, after each cycle the structural parameters are updated (*e.g.*, optimized) to reduce the loss metric. The operational simulation, adjoint simulation, and updating the structural parameters are iteratively repeated until the loss metric substantially converges or is otherwise below or within a threshold value or range such that the photonic device provides the desired performed while maintaining fabricability.

[0022] FIG. 2 is a schematic drawing that illustrates a non-limiting example embodiment of a segmented design according to various aspects of the present disclosure. The segmented design 200 is a non-limiting example of content suitable for insertion in the design region 114 described above (though not drawn to the scale or with the same granularity of segmentation). As shown, the segmented design 200 includes a plurality of segments 202 laid out in a two-dimensional grid. Each of the segments 202 represents a location in the proposed segmented design that can either include a material or not include

a material. As illustrated, segments that are white indicate a lack of the material, and segments that are dark (such as the first pattern 204, the second pattern 206, and the third pattern 208, indicate a presence of the material. For example, in a photolithography process, segments that are white may represent locations that are not exposed, and segments that are dark may represent locations that are exposed during the photolithography process. As another example, in an additive manufacturing process (e.g., a 3-D printer), segments that are white may represent locations that do not include material, and segments that are dark may represent locations that do include material.

[0023] This description is a non-limiting example only, and in some embodiments, the white and dark segments may have another meaning within the segmented design 200. In some embodiments, the segmented design 200 may include more than two colors. For example, a white segment may indicate a lack of material, a segment in a first color may indicate presence of a first material, and a segment in a second color may indicate a presence of a second material. In some embodiments, the segmented design 200 may be three-dimensional or one-dimensional, instead of the two-dimensional segmented design 200 illustrated in FIG. 2.

[0024] Typically, a fabrication system can duplicate any segmented design provided to it, subject to certain constraints. For example, a minimum feature size, a minimum feature shape, or any other constraint may be specified by the fabrication system as limitations on the segmented designs that the fabrication system can fabricate. From these constraints, a "paintbrush pattern" can be determined. In some embodiments, the paintbrush pattern represents a smallest feature that can be generated by a given fabrication system. If a given segmented design can be created by tiling the paintbrush pattern over the segmented design, then the segmented design is fabricable using the associated fabrication system. If one or more portions of the segmented design cannot be drawn with the paintbrush pattern, then the segmented design is not fabricable using the associated fabrication system. In some embodiments, if a fabrication system can fabricate devices with more than one material, separate constraints (and therefore separate paintbrush patterns) may be provided for each different material.

[0025] FIG. 3 is a block diagram that illustrates a non-limiting example embodiment of a system according to various aspects of the present disclosure. Overall, the illustrated embodiment of the system 300 is configured to generate design specifications, to determine fabricable segmented designs based on the design

specifications, and to fabricate physical devices based on the fabricable segmented designs.

[0026] Typically, performance of the segmented designs generated by the system 300 is improved using an inverse design process as discussed above (or another process). Sometimes, using such an inverse design process to generate performant segmented designs is based on a performance loss, and is initially unconstrained by consideration of fabricability. While this can result in designs that are theoretically highly performant, it also often results in designs that cannot be fabricated due to physical limitations of the fabrication system to be used and/or the materials that make up the design. In some embodiments of the present disclosure, the system 300 uses convex functions to determine a fabrication loss value. The gradient of this fabrication loss value may be backpropagated as part of the inverse design process, and since it is convex, it will guarantee that a fabricable design will eventually be generated.

[0027] As shown, the system 300 includes a design generation system 314, a fabrication system 316, and a design verification system 302. Communication between the design generation system 314, the design verification system 302, and the fabrication system 316 may occur via a network (not pictured), via exchange of a removable computer-readable medium (not pictured), or via any other suitable technique. Though the design generation system 314, fabrication system 316, and design verification system 302 are illustrated as separate systems, in some embodiments, some portions of these systems may be combined. As one non-limiting example, the design generation system 314 and the design verification system 302 may be combined in a single system. Also, in some embodiments, systems illustrated in FIG. 3 as a single system may be broken into multiple systems.

[0028] In some embodiments, the design generation system 314 may include one or more computing devices that are configured to generate design specifications for segmented designs that achieve a desired result. For example, the design generation system 314 may use forward simulation and backpropagation techniques to generate a segmented design for an electromagnetic device (or any other type of physical device) that has desired characteristics. This is a non-limiting example only, and any other technique, including but not limited to manual design, may be used by the design generation system 314 to create design specifications.

[0029] In some embodiments, the fabrication system 316 may be any suitable system for fabricating a segmented design. In some embodiments, the fabrication system 316 may be a photolithography system or an additive manufacturing system. In some embodiments, the fabrication system 316 may have characteristics that include a minimum feature size, a minimum feature shape, and/or other constraints that help define the segmented designs that the fabrication system 316 is capable of fabricating. To that end, the fabrication system 316 may provide a design rule checker that is configured to process proposed segmented designs to determine whether the proposed segmented designs comply with the constraints of the fabrication system 316. The design rule checker may be used to determine one or more paintbrush patterns that represent patterns embody the minimum feature size and/or minimum feature shape fabricable by the fabrication system 316.

[0030] In some embodiments, the design verification system 302 may be any suitable computing device or collection of computing devices configured to provide the described functionality. In some embodiments, the design verification system 302 may be a server computing device, a desktop computing device, a laptop computing device, a mobile computing device, a tablet computing device, or one or more computing devices of a cloud computing system.

[0031] As shown, the design verification system 302 includes one or more processors 310, a network interface 312, and a computer-readable medium 304. In some embodiments, the one or more processors 310 may include a plurality of processors and/or a plurality of processing cores in order to provide a large amount of computing power. In some embodiments, the network interface 312 may be configured to communicate with the design generation system 314 and/or the fabrication system 316 via any suitable type of wired network (including but not limited to Ethernet, FireWire, and USB), wireless network (including but not limited to 2G, 3G, 4G, 5G, LTE, Wi-Fi, WiMAX, and Bluetooth), or combinations thereof. In some embodiments, instead of a network interface 312, the design verification system 302 may be configured to communicate with the design generation system 314 and/or the fabrication system 316 via transfer of a removable computer-readable medium (not shown).

[0032] As shown, the computer-readable medium 304 has stored thereon logic that, in response to execution by the one or more processors 310, cause the design

verification system 302 to provide a performance optimization engine 306, a fabricable design generation engine 318, and a fabrication loss combination engine 308.

[0033] In some embodiments, the performance optimization engine 306 is configured to generate proposed segmented designs based on design specifications received from the design generation system 314. Typically, the performance optimization engine 306 uses an inverse design process that includes optimizing a performance loss value to generate the proposed segmented designs.

[0034] In some embodiments, the fabricable design generation engine 318 is configured to generate one or more fabricable segmented designs based on a given proposed segmented design that may or may not be fabricable. If the given proposed segmented design is already fabricable, then the fabricable design generation engine 318 may not make any changes. However, if the given proposed segmented design is not fabricable, then the fabricable design generation engine 318 may use a technique described below to remove unfabricable portions, thereby "snapping" the unfabricable proposed segmented design to a fabricable segmented design.

[0035] In some embodiments, the fabrication loss combination engine 308 is configured to determine differences between fabricable segmented designs and their corresponding proposed segmented designs, and to reduce the differences to a scalar value that represents a reduced fabrication loss value. In some embodiments, the fabrication loss combination engine 308 may also be configured to reduce multiple reduced fabrication loss values to create an overall fabrication loss value. The reduction functions used by the fabrication loss combination engine 308 are convex, thus ensuring that backpropagating the gradient of the overall fabrication loss value will push the proposed segmented design toward a fabricable design.

[0036] Further details of the configuration of the performance optimization engine 306, the fabricable design generation engine 318, and the fabrication loss combination engine 308 are provided below.

[0037] As used herein, "engine" refers to logic embodied in hardware or software instructions, which can be written in a programming language, such as C, C++, C#, COBOL, JAVA™, PHP, Perl, HTML, CSS, JavaScript, VBScript, ASPX, Go, Python, and/or the like. An engine may be compiled into executable programs or written in interpreted programming languages. Software engines may be callable from other engines or from themselves. Generally, the engines described herein refer to logical

modules that can be merged with other engines, or can be divided into sub-engines. The engines can be implemented by logic stored in any type of computer-readable medium or computer storage device and be stored on and executed by one or more general purpose computers, thus creating a special purpose computer configured to provide the engine or the functionality thereof. The engines can be implemented by logic programmed into an application-specific integrated circuit (ASIC), a field-programmable gate array (FPGA), or another hardware device.

[0038] As used herein, "computer-readable medium" refers to a removable or nonremovable device that implements any technology capable of storing information in a volatile or non-volatile manner to be read by a processor of a computing device, including but not limited to: a hard drive; a flash memory; a solid state drive; random-access memory (RAM); read-only memory (ROM); a CD-ROM, a DVD, or other disk storage; a magnetic cassette; a magnetic tape; and a magnetic disk storage. A computer-readable medium may also include multiple devices configured to collectively store the information described.

[0039] FIG. 4 is a flowchart that illustrates a non-limiting example embodiment of a method of generating a fabricable design for a physical device according to various aspects of the present disclosure. In the method 400, the system 300 determines fabrication loss using a convex function, thus ensuring that iterating through a forward simulation/backpropagation technique will eventually arrive at a fabricable design without getting stuck in a local non-zero minimum of the fabrication loss.

[0040] From a start block, the method 400 proceeds to block 402, where a design verification system 302 receives a design specification from a fabrication system 316. In some embodiments, the design specification may include a segmented design generated randomly, generated using a naïve optimization technique, using a technique similar to those used by the performance optimization engine 306, generated manually, or generated using any other suitable technique. In some embodiments, the design specification may include a linear function that represents a desired characteristic of the physical device, instead of specifying a segmented design. In some embodiments, the design specification may also include an indication of the desired performance characteristics of the physical device. For example, the design specification may include a performance loss function to be used to evaluate the performance of segmented designs during optimization. As another example, the design specification may include one or more parameters, including but not

limited to desired input and/or output wavelengths, to be used by a performance loss function built into the performance optimization engine 306.

[0041] At block 404, a performance optimization engine 306 of the design verification system 302 generates a proposed segmented design. Any suitable technique may be used by the performance optimization engine 306 to generate the proposed segmented design based on the design specification. As one non-limiting example, the forward-simulation/backpropagation technique described above in FIG. 1A - FIG. 1C may be used to create a proposed segmented design based on the design specification. In other examples, other techniques, including but not limited to other generative design techniques, genetic design techniques, or still other techniques may be used.

[0042] The method 400 then advances to decision block 406, where a determination is made regarding whether the proposed segmented design is acceptable and the method 400 is therefore done processing the design specification. In some embodiments, the determination regarding whether the proposed segmented design is acceptable based on whether a fabrication loss of the proposed segmented design meets a fabricability threshold. The performance optimization engine 306 may calculate the fabrication loss for the proposed segmented design, and then compare the calculated fabrication loss to the fabricability threshold. Typically, the fabricability threshold is configured to indicate whether the proposed segmented design is fabricable by the fabrication system 316. Accordingly, in some embodiments, any indication of a non-zero fabrication loss may fail to meet the fabricability threshold.

[0043] If the proposed segmented design is not yet acceptable, then the result of decision block 406 is NO, and the method 400 advances to block 408. At block 408, a fabrication loss combination engine 308 of the design verification system 302 generates one or more fabricable segmented designs based on the proposed segmented design. In some embodiments, the technique used to generate the fabricable segmented design may include some variability, in which case the fabrication system 316 may generate multiple slightly different fabricable segmented designs based on the single proposed segmented design. In some embodiments, the proposed segmented design may include likelihoods of various materials being present in a given segment (e.g., a given segment may have a 75% probability of containing a first material, and a 25% probability of containing a second material). In such embodiments, generating a fabricable segmented design may include

binarizing the proposed segmented design to indicate that a given material is either definitively present or not present in any given segment.

[0044] Multiple techniques exist to convert the proposed segmented design to a fabricable segmented design. For example, the fabrication loss combination engine 308 may use paintbrush patterns associated with the fabrication system 316 to generate a fabricable segmented design based on the proposed segmented design. One such technique is described in commonly owned, co-pending U.S. Application No. 16/805299, filed February 28, 2020, the entire disclosure of which is hereby incorporated by reference herein for all purposes. Other techniques are described in commonly owned, co-pending U.S. Application No. 17/036454, filed September 29, 2020, and U.S. Application No. 17/036397, filed September 29, 2020, the entire disclosures of which are hereby also incorporated by reference herein for all purposes.

[0045] The method 400 then advances to a for-loop defined between a for-loop start block 410 and a for-loop end block 414, wherein processing is performed for each of the one or more fabricable segmented designs. From the for-loop start block 410, the method 400 advances to block 412, where a fabrication loss combination engine 308 of the design verification system 302 generates a reduced fabrication loss value based on the proposed segmented design and the fabricable segmented design.

[0046] In some embodiments, the reduced fabrication loss value is a scalar value that represents an amount of difference between the proposed segmented design and the fabricable segmented design. For example, a fabrication loss matrix or array may be generated that includes each segment that is different between the proposed segmented design and the fabricable segmented design. In some embodiments, this array may have binary values that indicate whether a segment is different or the same in the fabricable segmented design compared to the proposed segmented design. In some embodiments, if the proposed segmented design has probability values for each segment instead of binary values, the array may store a difference between the probability value and the binarized value of the fabricable segmented design. For example, if the proposed segmented design indicates a 25% probability of the first material in a first segment and the fabricable segmented design indicates that the first material is not present in the first segment, then the array would store a value of .25 (.25 [probability] - 0 [binarized value]). Likewise, if the fabricable segmented design indicates that the first material is present in the first segment, then the array would store a value of -.75 (.25 [probability] - 1 [binarized value]).

[0047] In some embodiments, the scalar value may be determined based on the resulting fabrication loss matrix using any suitable technique. For example, the scalar value may be a sum of values in the fabrication loss matrix. As another example, the scalar value may be a sum of squares of values in the fabrication loss matrix. As still another example, the scalar value may be an average of values in the fabrication loss matrix.

[0048] The method 400 then proceeds to the for-loop end block 414. If further fabricable segmented designs remain to be processed, then the method 400 returns from for-loop end block 414 to for-loop start block 410 to process the next fabricable segmented design. Otherwise, if processing of all of the fabricable segmented designs has completed, the method 400 proceeds from for-loop end block 414 to block 416.

[0049] At block 416, the fabrication loss combination engine 308 reduces the reduced fabrication loss values to determine an overall fabrication loss value. Any suitable technique may be used to further reduce the reduced fabrication loss values. For example, in some embodiments, the fabrication loss combination engine 308 may determine a minimum value of the reduced fabrication loss values, and may use the minimum value as the overall fabrication loss value. As another example, in some embodiments, the fabrication loss combination engine 308 may multiply the reduced fabrication loss values to create the overall fabrication loss value. In some embodiments, the fabrication loss combination engine 308 may use a reduce_min function to determine the overall fabrication loss value.

[0050] At block 418, the performance optimization engine 306 determines a gradient of the overall fabrication loss value, and at block 420, the performance optimization engine 306 backpropagates the gradient of the overall fabrication loss value to update the design specification. One feature to note is that in the techniques described above, the gradients of the fabrication loss of the individual fabricable segmented designs will have a zero value, because the fabricable segmented designs will represent minima of the fabrication loss. The techniques described above for reducing the arrays to create the overall fabrication loss value will therefore provide a convex measurement of fabrication loss, in that the overall fabrication loss value will have one global minimum, and the gradient of the overall fabrication loss value will always point toward a fabricable design.

[0051] The method 400 then returns to block 404 to create a proposed segmented design based on the updated design specification.

[0052] Returning to decision block 406, if the proposed segmented design had been determined to be acceptable, then the result of decision block 406 is YES, and the method 400 proceeds to block 422.

[0053] At block 422, the performance optimization engine 306 stores the proposed segmented design as a final segmented design, and at block 424, the design verification system 302 transmits the final segmented design to a fabrication system 316 to manufacture the physical device. The method 400 then proceeds to an end block and terminates.

[0054] In the preceding description, numerous specific details are set forth to provide a thorough understanding of various embodiments of the present disclosure. One skilled in the relevant art will recognize, however, that the techniques described herein can be practiced without one or more of the specific details, or with other methods, components, materials, etc. In other instances, well-known structures, materials, or operations are not shown or described in detail to avoid obscuring certain aspects.

[0055] Reference throughout this specification to "one embodiment" or "an embodiment" means that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one embodiment of the present invention. Thus, the appearances of the phrases "in one embodiment" or "in an embodiment" in various places throughout this specification are not necessarily all referring to the same embodiment. Furthermore, the particular features, structures, or characteristics may be combined in any suitable manner in one or more embodiments.

[0056] The order in which some or all of the blocks appear in each method flowchart should not be deemed limiting. Rather, one of ordinary skill in the art having the benefit of the present disclosure will understand that actions associated with some of the blocks may be executed in a variety of orders not illustrated, or even in parallel.

[0057] The processes explained above are described in terms of computer software and hardware. The techniques described may constitute machine-executable instructions embodied within a tangible or non-transitory machine (e.g., computer) readable storage medium, that when executed by a machine will cause the machine to perform the operations described. Additionally, the processes may be embodied within hardware, such as an application specific integrated circuit ("ASIC") or otherwise.

[0058] The above description of illustrated embodiments of the invention, including what is described in the Abstract, is not intended to be exhaustive or to limit the

invention to the precise forms disclosed. While specific embodiments of, and examples for, the invention are described herein for illustrative purposes, various modifications are possible within the scope of the invention, as those skilled in the relevant art will recognize.

[0059] These modifications can be made to the invention in light of the above detailed description. The terms used in the following claims should not be construed to limit the invention to the specific embodiments disclosed in the specification. Rather, the scope of the invention is to be determined entirely by the following claims, which are to be construed in accordance with established doctrines of claim interpretation.

CLAIMS

What is claimed is:

1. A non-transitory computer-readable medium having logic stored thereon that, in response to execution by one or more processors of a computing system, causes the computing system to perform actions for creating a fabricable segmented design for a physical device, the actions comprising:

receiving, by the computing system, a design specification;

generating, by the computing system, a proposed segmented design based on the design specification;

determining, by the computing system, one or more fabricable segmented designs based on the proposed segmented design;

determining, by the computing system, an overall fabrication loss value based on the one or more fabricable segmented designs; and

backpropagating, by the computing system, a gradient of the overall fabrication loss value to create an updated design specification.

2. The non-transitory computer-readable medium of claim 1, wherein determining the overall fabrication loss value based on the one or more fabricable segmented designs includes determining, for each fabricable segmented design of the one or more fabricable segmented designs, a separate fabrication loss matrix by comparing the fabricable segmented design to the proposed segmented design.

3. The non-transitory computer-readable medium of claim 2, wherein determining the overall fabrication loss value based on the one or more fabricable segmented designs further includes reducing each separate fabrication loss matrix to a scalar value.

4. The non-transitory computer-readable medium of claim 3, wherein reducing each separate fabrication loss matrix to the scalar value includes at least one of:

determining a sum of values in the fabrication loss matrix;

determining a sum of squares of values in the fabrication loss matrix; and

determining an average of values in the fabrication loss matrix.

5. The non-transitory computer-readable medium of claim 3, wherein determining the overall fabrication loss value based on the one or more fabricable segmented designs further includes reducing the scalar values to an overall scalar value.

6. The non-transitory computer-readable medium of claim 5, wherein reducing the scalar values to the overall scalar value includes at least one of:

determining a minimum value of the scalar values; and

multiplying the scalar values.

7. The non-transitory computer-readable medium of claim 1, wherein the actions further comprise:

generating a new proposed segmented design based on the updated design specification.

8. The non-transitory computer-readable medium of claim 7, wherein the actions further comprise:

in response to determining that a fabrication loss of the new proposed segmented design fails to meet a fabricability threshold:

determining one or more new fabricable segmented designs based on the new proposed segmented design;

determining a new overall fabrication loss value based on the one or more new fabricable segmented designs; and

backpropagating a gradient of the new overall fabrication loss value to create a second updated design specification.

9. The non-transitory computer-readable medium of claim 8, wherein determining the new overall fabrication loss value based on the one or more new fabricable segmented designs includes determining the new overall fabrication loss value based on the one or more new fabricable segmented designs and the one or more fabricable segmented designs.

10. The non-transitory computer-readable medium of claim 7, wherein the actions further comprise:

in response to determining that a fabrication loss of the new proposed segmented design meets a fabricability threshold, providing the new proposed segmented design to a fabrication system to manufacture the physical device.

11. A method of creating a fabricable segmented design for a physical device, the method comprising:

receiving, by a computing system, a design specification;

generating, by the computing system, a proposed segmented design based on the design specification;

determining, by the computing system, one or more fabricable segmented designs based on the proposed segmented design;

determining, by the computing system, an overall fabrication loss value based on the one or more fabricable segmented designs; and

backpropagating, by the computing system, a gradient of the overall fabrication loss value to create an updated design specification.

12. The method of claim 11, wherein determining the overall fabrication loss value based on the one or more fabricable segmented designs includes determining, for each fabricable segmented design of the one or more fabricable segmented designs, a separate fabrication loss matrix by comparing the fabricable segmented design to the proposed segmented design.

13. The method of claim 12, wherein determining the overall fabrication loss value based on the one or more fabricable segmented designs further includes reducing each separate fabrication loss matrix to a scalar value.

14. The method of claim 13, wherein reducing each separate fabrication loss matrix to the scalar value includes at least one of:

determining a sum of values in the fabrication loss matrix;

determining a sum of squares of values in the fabrication loss matrix; and

determining an average of values in the fabrication loss matrix.

15. The method of claim 13, wherein determining the overall fabrication loss value based on the one or more fabricable segmented designs further includes reducing the scalar values to an overall scalar value.

16. The method of claim 15, wherein reducing the scalar values to the overall scalar value includes at least one of:

determining a minimum value of the scalar values; and

multiplying the scalar values.

17. The method of claim 11, further comprising:

generating a new proposed segmented design based on the updated design specification.

18. The method of claim 17, further comprising:

in response to determining that a fabrication loss of the new proposed segmented design fails to meet a fabricability threshold:

determining one or more new fabricable segmented designs based on the new proposed segmented design;

determining a new overall fabrication loss value based on the one or more new fabricable segmented designs; and

backpropagating a gradient of the new overall fabrication loss value to create a second updated design specification.

19. The method of claim 18, wherein determining the new overall fabrication loss value based on the one or more new fabricable segmented designs includes determining the new overall fabrication loss value based on the one or more new fabricable segmented designs and the one or more fabricable segmented designs.

20. The method of claim 17, further comprising:

in response to determining that a fabrication loss of the new proposed segmented design meets a fabricability threshold, providing the new proposed segmented design to a fabrication system to manufacture the physical device.

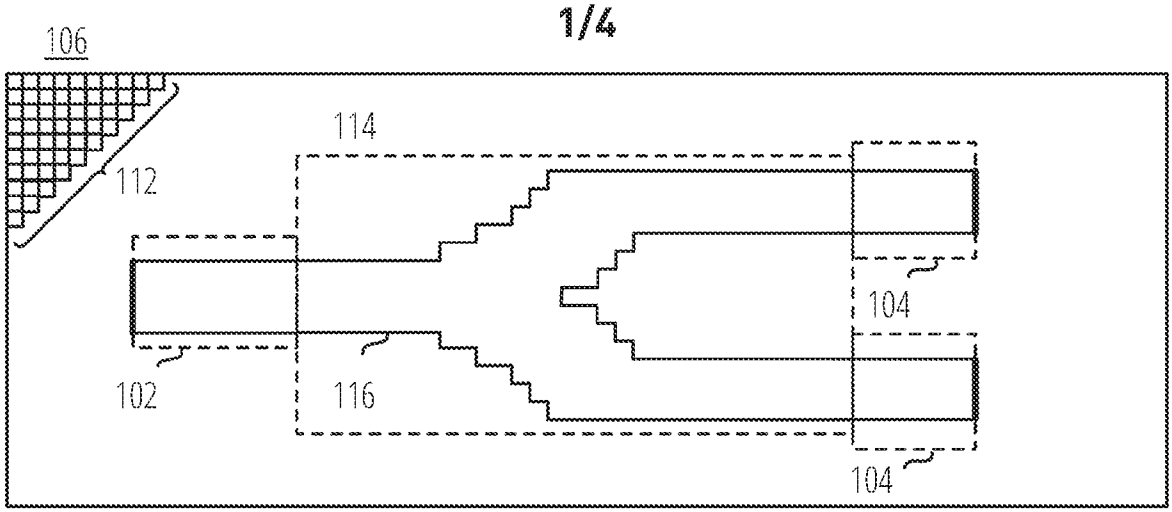

FIG. 1A

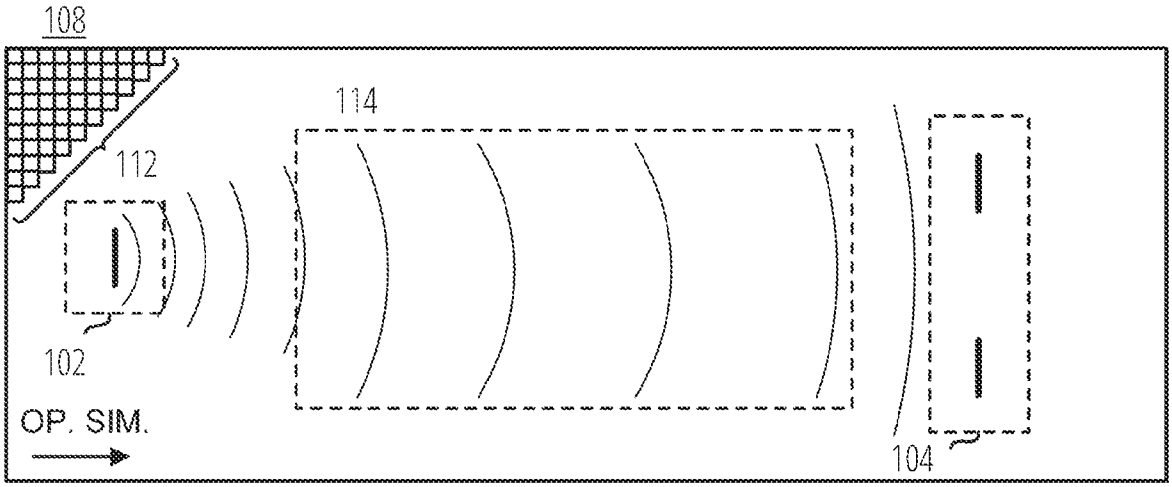

FIG. 1B

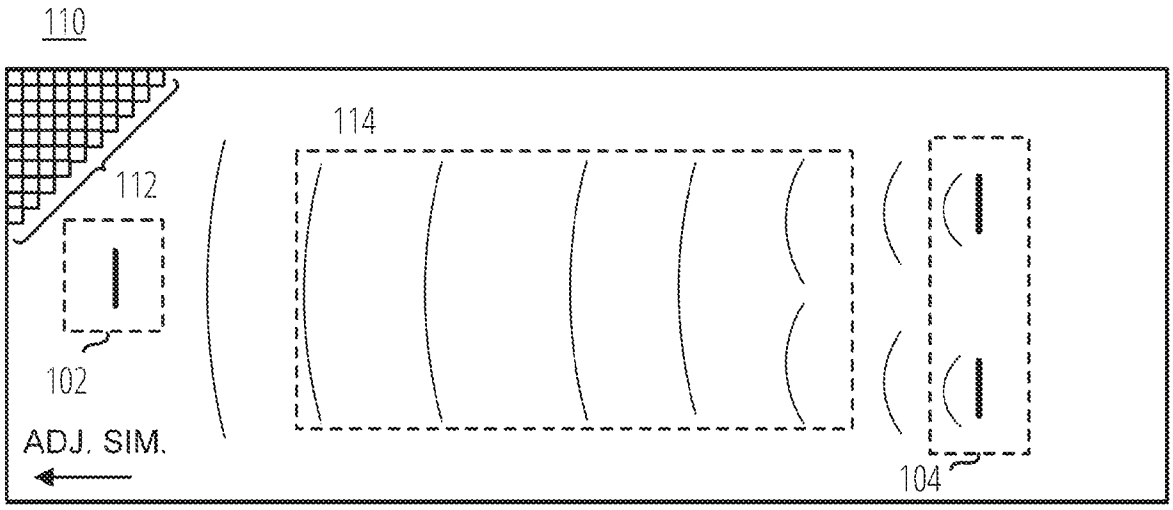

FIG. 1C

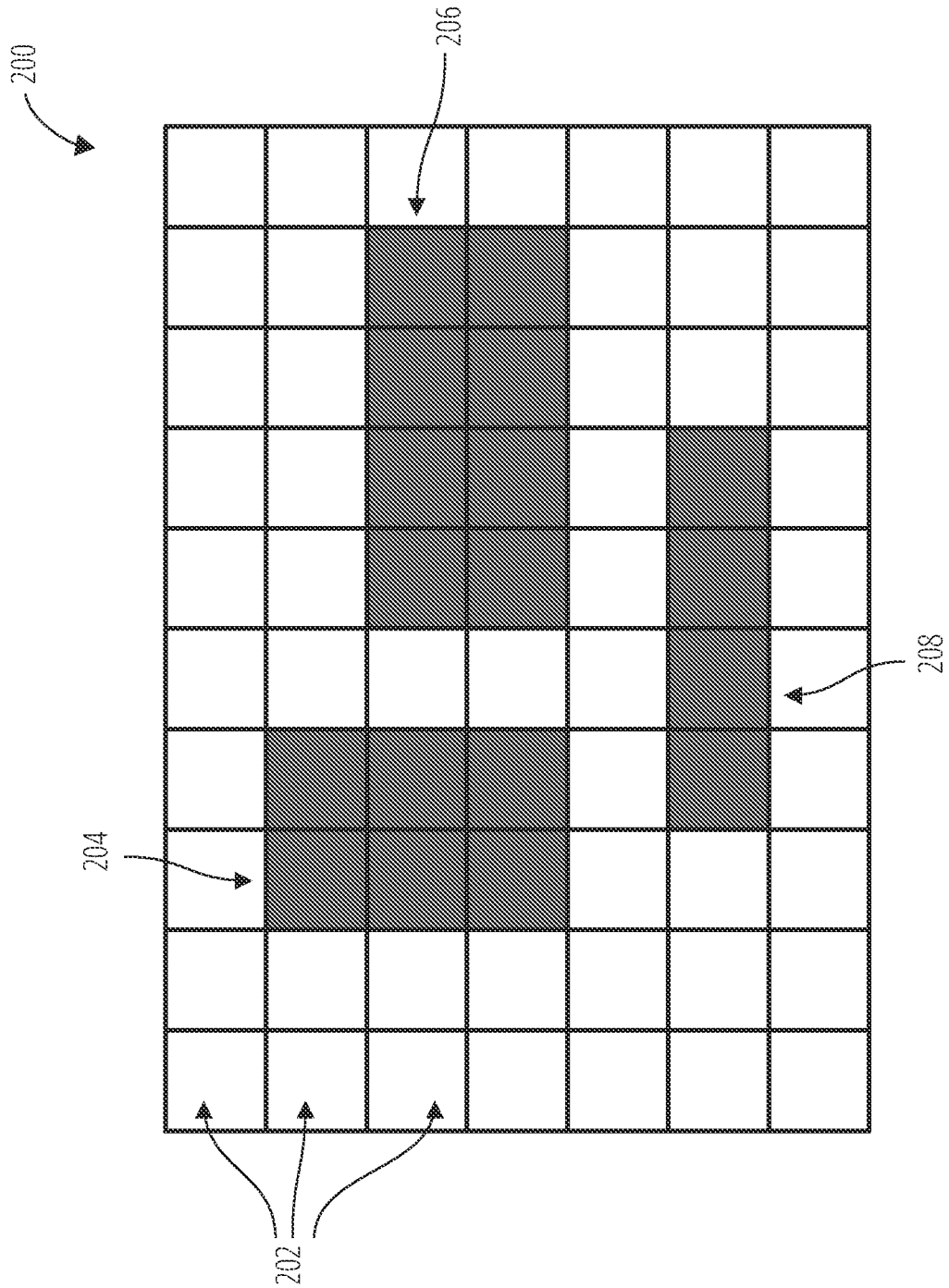

FIG. 2

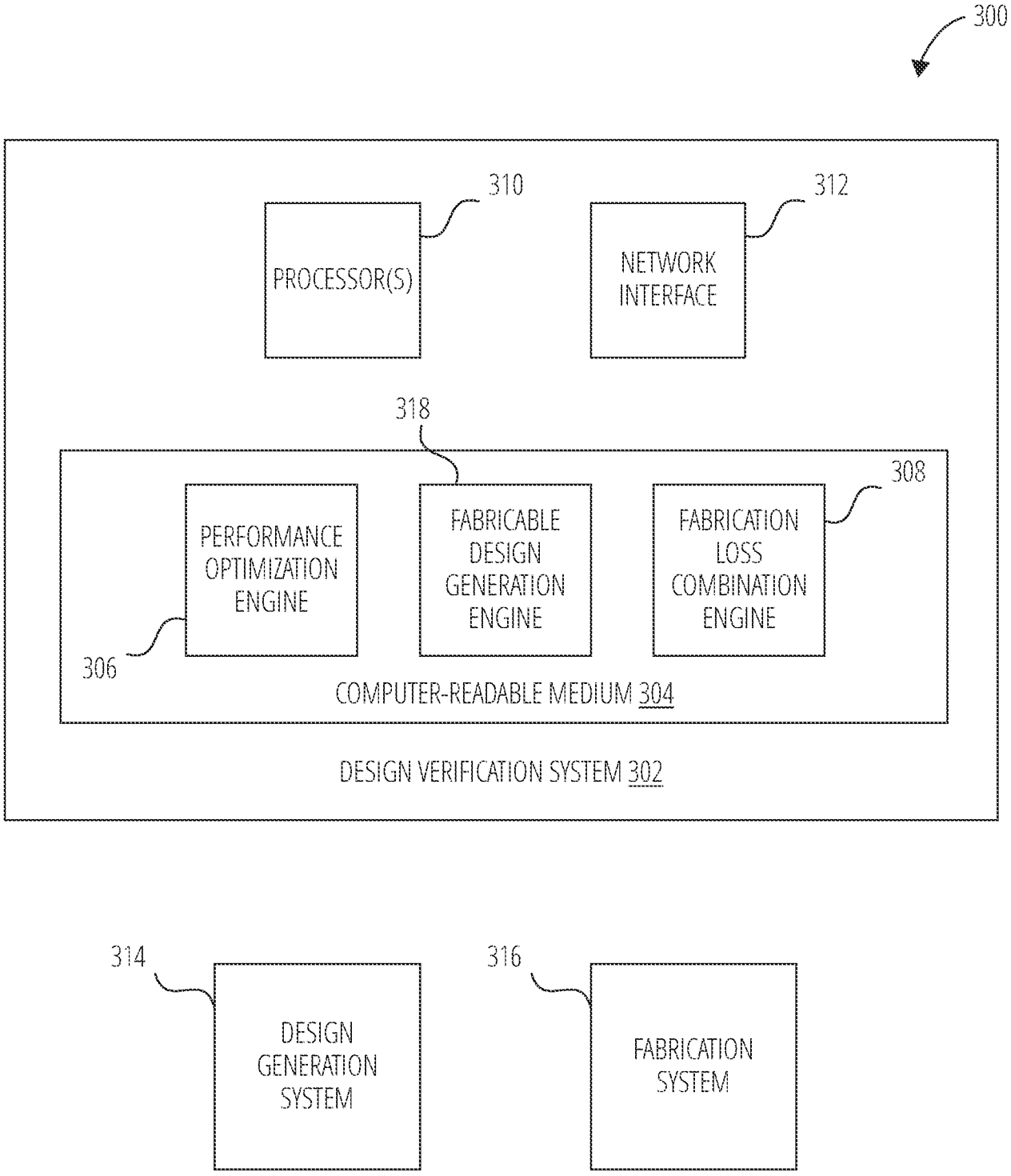
300
310
PROCESSOR(S)
312
NETWORK INTERFACE
318
308
PERFORMANCE OPTIMIZATION ENGINE
FABRICABLE DESIGN GENERATION ENGINE
FABRICATION LOSS COMBINATION ENGINE
306
COMPUTER-READABLE MEDIUM 304
DESIGN VERIFICATION SYSTEM 302
314
DESIGN GENERATION SYSTEM
316
FABRICATION SYSTEM

FIG. 3

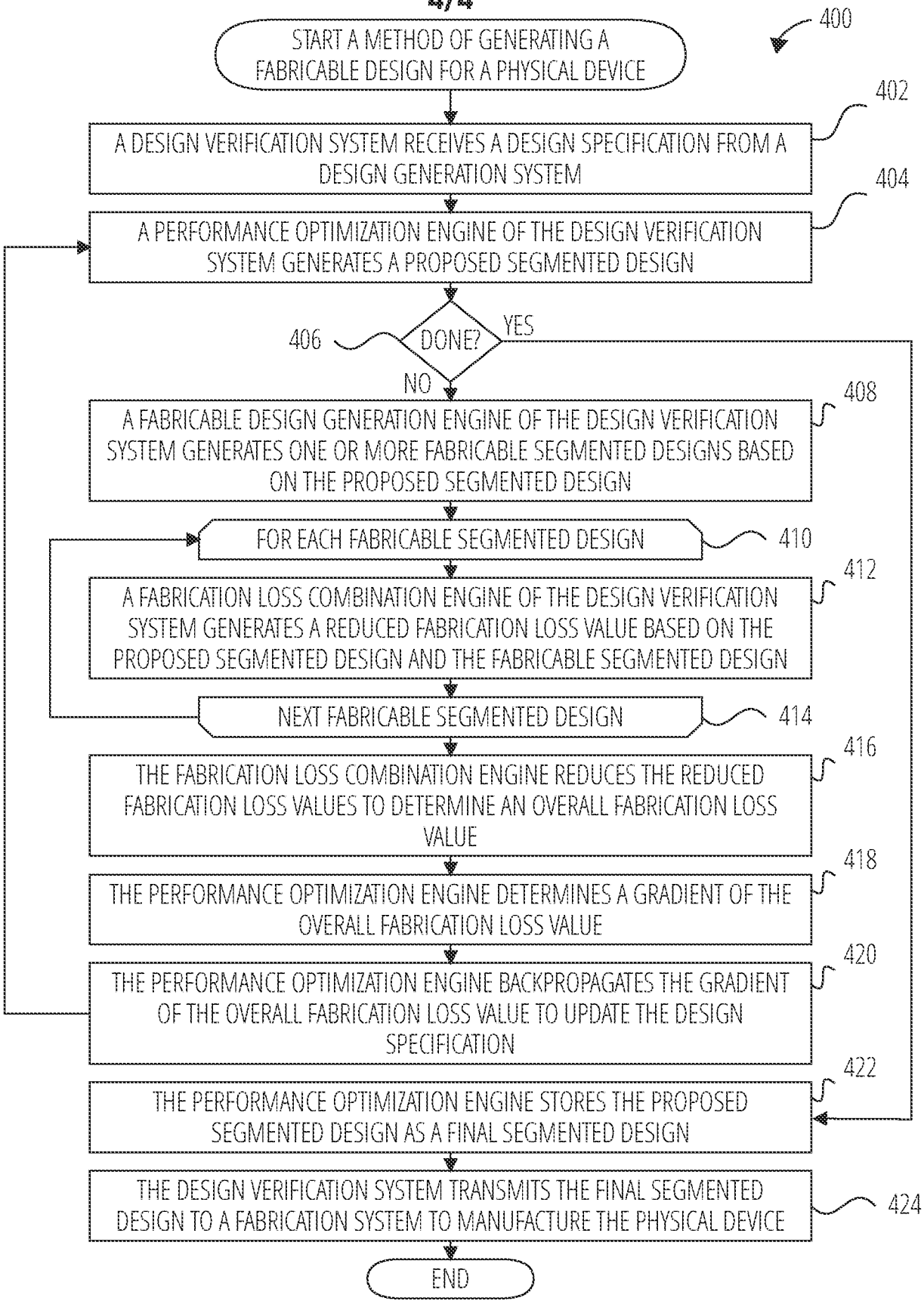
START A METHOD OF GENERATING A FABRICABLE DESIGN FOR A PHYSICAL DEVICE
400
A DESIGN VERIFICATION SYSTEM RECEIVES A DESIGN SPECIFICATION FROM A DESIGN GENERATION SYSTEM
402
A PERFORMANCE OPTIMIZATION ENGINE OF THE DESIGN VERIFICATION SYSTEM GENERATES A PROPOSED SEGMENTED DESIGN
404
406
DONE?
YES
NO
A FABRICABLE DESIGN GENERATION ENGINE OF THE DESIGN VERIFICATION SYSTEM GENERATES ONE OR MORE FABRICABLE SEGMENTED DESIGNS BASED ON THE PROPOSED SEGMENTED DESIGN
408
FOR EACH FABRICABLE SEGMENTED DESIGN
410
A FABRICATION LOSS COMBINATION ENGINE OF THE DESIGN VERIFICATION SYSTEM GENERATES A REDUCED FABRICATION LOSS VALUE BASED ON THE PROPOSED SEGMENTED DESIGN AND THE FABRICABLE SEGMENTED DESIGN
412
NEXT FABRICABLE SEGMENTED DESIGN
414
THE FABRICATION LOSS COMBINATION ENGINE REDUCES THE REDUCED FABRICATION LOSS VALUES TO DETERMINE AN OVERALL FABRICATION LOSS VALUE
416
THE PERFORMANCE OPTIMIZATION ENGINE DETERMINES A GRADIENT OF THE OVERALL FABRICATION LOSS VALUE
418
THE PERFORMANCE OPTIMIZATION ENGINE BACKPROPAGATES THE GRADIENT OF THE OVERALL FABRICATION LOSS VALUE TO UPDATE THE DESIGN SPECIFICATION
420
THE PERFORMANCE OPTIMIZATION ENGINE STORES THE PROPOSED SEGMENTED DESIGN AS A FINAL SEGMENTED DESIGN
422
THE DESIGN VERIFICATION SYSTEM TRANSMITS THE FINAL SEGMENTED DESIGN TO A FABRICATION SYSTEM TO MANUFACTURE THE PHYSICAL DEVICE
424
END

FIG. 4

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2021/047595

A. CLASSIFICATION OF SUBJECT MATTER

G06F 30/373(2020.01)i; **G06F 30/27**(2020.01)i; **G06F 30/398**(2020.01)i; **G06F 30/367**(2020.01)i; **G06N 3/08**(2006.01)i; **G06F 119/18**(2020.01)i; **G06F 119/22**(2020.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G06F 30/373(2020.01); G06F 17/50(2006.01); G06F 30/392(2020.01); G06N 3/08(2006.01); H01L 21/00(2006.01); H01L 21/66(2006.01)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: design specification, segmented design, loss, backpropagate, gradient, fabrication

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2019-0065630 A1 (SAMSUNG ELECTRONICS CO., LTD.) 28 February 2019 (2019-02-28) paragraphs [0071], [0125]; claims 1-11, 20; and figures 1B, 11	1-20
Y	US 2020-0184137 A1 (SEMICONDUCTOR ENERGY LABORATORY CO., LTD.) 11 June 2020 (2020-06-11) paragraph [0189]; claims 1-5; and figures 2, 6	1-20
Y	WO 2012-115912 A2 (KLA-TENCOR CORPORATION) 30 August 2012 (2012-08-30) claims 1-15; and figures 2, 7-8	2-6,12-16
A	US 2007-0256046 A1 (FEDOR G. PIKUS et al.) 01 November 2007 (2007-11-01) claims 1-12; and figure 6A-6B	1-20
A	US 6957402 B2 (MARK TEMPLETON et al.) 18 October 2005 (2005-10-18) column 5, lines 3-36; and claims 1-4	1-20

☐ Further documents are listed in the continuation of Box C. ☑ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"D" document cited by the applicant in the international application
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
07 December 2021	**08 December 2021**

Name and mailing address of the ISA/KR	Authorized officer
Korean Intellectual Property Office **189 Cheongsa-ro, Seo-gu, Daejeon** **35208, Republic of Korea**	**YANG, JEONG ROK**
Facsimile No. **+82-42-481-8578**	Telephone No. **+82-42-481-5709**

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/US2021/047595

Patent document cited in search report	Publication date (day/month/year)	Patent family member(s)	Publication date (day/month/year)
US 2019-0065630 A1	28 February 2019	CN 109426698 A	05 March 2019
		KR 10-2019-0023670 A	08 March 2019
		TW 201913849 A	01 April 2019
		US 10614186 B2	07 April 2020
US 2020-0184137 A1	11 June 2020	CN 110998585 A	10 April 2020
		US 10949595 B2	16 March 2021
		WO 2018-234945 A1	27 December 2018
WO 2012-115912 A2	30 August 2012	EP 2678880 A2	01 January 2014
		IL 228063 A	30 September 2013
		IL 228063 B	31 October 2017
		JP 2014-507808 A	27 March 2014
		JP 2016-191719 A	10 November 2016
		JP 2018-139304 A	06 September 2018
		JP 5980237 B2	31 August 2016
		JP 6329209 B2	23 May 2018
		JP 6498337 B2	10 April 2019
		KR 10-1931834 B1	24 December 2018
		KR 10-2021-0014756 A	09 February 2021
		KR 10-2051773 B1	03 December 2019
		KR 10-2212388 B1	08 February 2021
		SG 192891 A1	30 September 2013
		TW 201250503 A	16 December 2012
		US 10223492 B1	05 March 2019
		US 2012-0216169 A1	23 August 2012
		US 8656323 B2	18 February 2014
		WO 2012-115912 A3	22 November 2012
US 2007-0256046 A1	01 November 2007	WO 2007-133423 A2	22 November 2007
		WO 2007-133423 A3	02 May 2008
US 6957402 B2	18 October 2005	TW 200519667 A	16 June 2005
		TW I265439 B	01 November 2006
		US 2005-0066294 A1	24 March 2005