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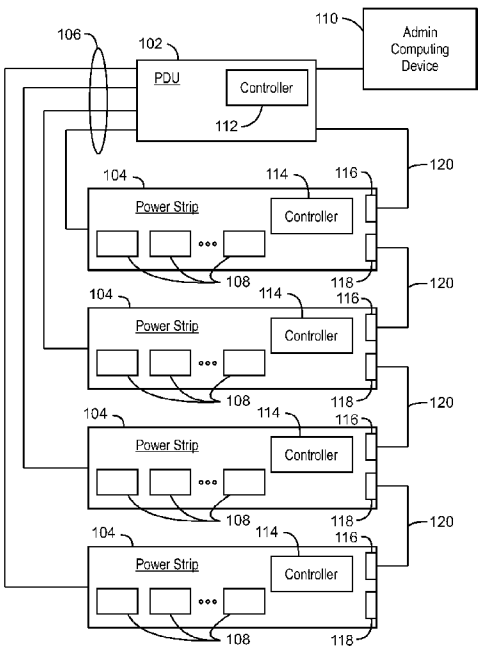
— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

[Continued on next page]

(54) Title: POWER OUTLET STRIPS

(57) Abstract: Examples disclosed relate to power outlet strips. For example, a system includes a power distribution unit and a plurality of power outlet strips coupled to the power distribution unit. The power distribution unit is to provide AC power to each of the power outlet strips. The system also includes a data bus that communicatively couples each of the plurality of power outlet strips to the power distribution unit. The data bus is routed serially through each of the plurality of power outlet strips.



100
FIG. 1

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POWER OUTLET STRIPS

BACKGROUND

[0001] Data centers generally include a large number of electronic devices such as servers, storage systems, routers, and the like. All of these devices are coupled to a power distribution unit that provides the electrical power. Many power distribution units also have the ability to monitor power consumption of each device, and enable remote monitoring and control of each power outlet.

BRIEF DESCRIPTION OF THE DRAWINGS

[0002] Certain exemplary embodiments are described in the following detailed description and in reference to the drawings, in which:

[0003] Fig. 1 is an example block diagram of a daisy-chained power delivery system;

[0004] Figs. 2A, 2B, and 2C are diagrams of the power delivery system 100 showing a more detailed example of a power strip 104;

[0005] Fig. 3 is a process flow diagram of an example method of configuring a daisy-chained power delivery system; and

[0006] Fig. 4 is an example circuit diagram of a reset circuit that can be used in the system shown in Fig. 1 and 2.

DETAILED DESCRIPTION OF SPECIFIC EMBODIMENTS

[0007] The present disclosure provides a power delivery system with daisy-chained power outlet strips. The power delivery system includes a Power Distribution Unit (PDU) that provides power to a number of power outlet strips, sometimes referred to herein simply as power strips. Each power strip includes a number of power outlets to which various devices can be coupled. The PDU also includes monitoring and control circuitry that enables the PDU to monitor each power strip and send commands to the power strips. Communication between the PDU and the power strips is implemented through a data bus.

[0008] In some cases, there may be a separate data connection between the PDU and each power strip. This data connection is usually embedded in a

specialized power cord. The present disclosure provides a power delivery system in which the power strips are daisy-chained with respect to the data bus. A daisy chain is a wiring technique in which multiple devices are wired together in sequence. The daisy-chained power strips are coupled in series through a single shared data bus that couples each power strip to the PDU. The data bus can be implemented using standard data cables and jacks. Thus, the use of specialized power cords can be avoided. Additionally, in the power delivery system disclosed herein, the conversion of power from Alternating Current (AC) to Direct Current (DC) is accomplished using circuitry in the PDU. Therefore, the power strips do not include an AC to DC converter, which simplifies the power strip circuitry and reduces heat generation in the power strips. As with the data bus, the DC power is provided to the power strips in a single daisy-chained bus.

[0009] Fig. 1 is a block diagram of a daisy-chained power delivery system. The power delivery system 100 includes a PDU 102 and a number of power strips 104. The PDU 102 provides AC electrical power to each power strip 104 through a number of separate power cables 106. With respect to AC power, the power strips 104 are connected to the PDU 102 in parallel.

[0010] The electrical power received from the PDU 102 can be delivered to a number of power outlets 108 included in the power strip 104. Any suitable type of electrical device can be coupled to a power outlet 108 to receive AC electrical power. Each power outlet 108 can be a standard power outlet for receiving a standard plug. For example, in the case of a server rack or data center power system, each power outlet 108 may be a standard C19 or C13 outlet configured to receive a standard C14 or C20 plug. In some examples, the PDU 102 and the power strips 104 are mounted to a rack, such as a server rack. However, other implementations are possible.

[0011] Data communication between the PDU 102 and the power strips 104 is accomplished through a data bus that couples the PDU 102 to each power strip. Data communication between the PDU 102 and the power strips 104 enables the PDU 102 to receive monitoring information from each power strip 104. For example, the power strips 104 may include circuitry for monitoring the

level of power being consumed at each of the power outlets 108 at any time. The PDU 102 can collect this information through the data bus. The PDU 102 can also use the data bus to communicate commands to each power strip. For example, each power strip 104 may include circuitry that enables it to switch selected power outlets 108 on or off. The PDU 102 can send commands through the data bus that will cause a selected power strip 104 to switch a selected power outlet 108 on or off. Various other commands and data can be communicated between the PDU 102 and the power strips 104.

[0012] The PDU 102 may also be communicatively coupled to an administrator computing device 110. The remote computing device enables the user to control the power delivery system 100 through the PDU 102. For example, monitored information received from the power strips 104 can be sent to the administrator computing device 110, and the user can turn specified power outlets 108 on or off by sending commands to the PDU 102. The PDU 102 can be coupled to the administrator computing device 110 through a direct connection or through a network, which may be a local area network (LAN), wide area network (WAN), a storage area network (SAN), or other suitable type of network.

[0013] The PDU 102 includes a controller 12 that enables it to perform various logic operations, such as sending data to the remote computing device, receiving monitoring data from the power strips 104, sending commands to the power strips 104, and the like. The PDU controller 112 can be implemented in any suitable hardware or combination of hardware and programming. For example, the PDU controller 112 can include a general purpose processor, an Application Specific Integrated Circuit (ASIC), a Field Programmable Gate Array (FPGA), microcontroller, and others.

[0014] Each power strip 104 also includes a controller 114 that enables it to communicate with the PDU 102, send commands to the power outlets 108, receive and record monitoring information, and the like. The power strip controller 114 can be implemented in any suitable hardware or combination of hardware and programming. For example, the power strip controller 114 can include general purpose processor, an Application Specific Integrated Circuit

(ASIC), a Field Programmable Gate Array (FPGA), a microcontroller, and others.

[0015] Each power strip 104 has two data ports, an upstream port 116 and a downstream port 118. The upstream port couples the power strip 104 to the PDU 102, either directly or through one or more additional power strips 104. The downstream port 118 enables additional power strips 104 to be connected to the chain of power strips 104. In the present description, "upstream" means toward the direction of the PDU 102 in the data bus among power strips 104, and "downstream" means away from the PDU 102 in the data bus among the power strips 104. Any suitable number of power strips 104 can be couple to the data bus, including one, two, three, four, or more.

[0016] The data bus is routed serially through each of the plurality of power outlet strips. This means that rather than coupling the PDU 102 directly to each power outlet strip 104 in a parallel configuration, the same data bus passes through each of the power outlet strips 104 in the chain and is shared between the power outlet strips. As shown in Fig. 1, the data bus is routed through cables 120 that couple the downstream port 118 of one power strip 104 to the upstream port 116 of the next power strip 104. In some examples, DC power is delivered from the PDU 102 to each power strip 104 through the same cables 120 that are used to route the data bus.

[0017] To enable the PDU 102 to identify and communicate with each power strip 104, the power strips 104 are enumerated, meaning that each power strip 104 is assigned a unique identifier. The unique identifier, referred to herein a Power Strip Identifier (PSID), may be used in all data communications between the PDU 102 and the power strips 104. The PSIDs can be assigned during a configuration process, which may be triggered upon the PDU 102 receiving power, or in response to changes in the power delivery system 100, such as addition or removal of a power strip 104. The configuration process can also be triggered in response to a reset command received, for example, from the administrator.

[0018] The power strips 104 can be configured such that, during the configuration process, each power strip 104 assigns a PSID to itself and

declares its PSID to the PDU 102. The self-assignment of a PSID can be based on the corresponding power strip's position on the data bus. An example process for assigning PSIDs is described in more detail in Figs. 2 and 3.

[0019] Figs. 2A, 2B, and 2C are diagrams of the power delivery system 100 showing a more detailed example of a power strip 104. In this example, each of the power strips 104 are identical. However, in other implementations there could be some differences between the power strips 104.

[0020] Figs. 2A, 2B, and 2C show three power strips 104, referred to herein as power strips A, B and C. The upstream port 116 of power strip A is coupled to the PDU 102. The downstream port 118 of power strip A of is coupled to the upstream port 116 of power strip B, and the downstream port 118 of power strip B is coupled to the upstream port 116 of power strip C. Power strip C is the last power strip on the data bus, and the downstream port 118 of power strip C is uncoupled.

[0021] Each of the power strips 104 is coupled together by a cable, all of which together form the daisy-chaining data bus. Each of the ports 116 and 118 may be configured to receive a standard plug in accordance with a particular protocol. For example, the ports 116 and 118 may be configured to receive any suitable type of Registered Jack (RJ) such as RJ-12 plugs, or others. In some examples, the ports 116 and 118 could also be configured to receive custom proprietary plug types.

[0022] Each port contains six conductors. Pin-outs for the ports are shown in the table below.

Table 1: Example pin-outs for power strip ports.

Upstream port
1. upstream indication (used for enumeration; pulled to ground)
2. DC power
3. DIFF+ (used for data communication)
4. DIFF- (used for data communication)
5. "next-device" indicator output (common collector)
6. ground
Downstream port
1. downstream detection (used for enumeration; pulled high)
2. DC power
3. DIFF+ (used for data communication)
4. DIFF- (used for data communication)
5. "next-device" indicator input (pulled high)
6. ground

[0023] Each power strip 104 includes a microcontroller 200 that controls various operations of the power strip circuitry. The microcontroller 200 is one example of the power strip controller 114 described in Fig. 1. Each power strip 104 also includes a power converter 202 that converts the DC power received from the PDU 102 to other suitable voltages. In this example, the power converter receives 24 Volt DC from the PDU 102 and generates 5 Volt DC and 3.3 Volt DC outputs. The PDU 102 includes an AC-to-DC converter 206 that converts AC electrical power to DC electrical power, which is provided to each of the power strips 104. As with the data bus, the DC power is routed serially through each of the plurality of power outlet strips 104. In this example, DC power is routed through pin 2 of the upstream port 116 and downstream port 118.

[0024] The data signals DIFF+ and DIFF- are a pair of differential signals for the data bus and facilitate the communication between the power strips 104 and the PDU 102, including the communication of power monitoring data and commands. The data signals can operate in accordance with any suitable signaling protocol, such as Universal Serial Bus (USB), RS-485, Controller Area Network (CAN) bus, and others. Although not shown in Figs. 2A, 2B, and 2C, the data signals DIFF+ and DIFF- are both coupled to the microcontroller 200 through a transceiver.

[0025] Each power strip 104 may include a termination circuit 204 that terminates the differential signal path with a suitable resistance. The termination resistance of a specific value may be specified by some signaling protocols. The termination circuit 204 includes a resistance R4 and a switch S1. If the power strip 104 is the last power strip on the data bus, the microcontroller 200 closes the switch S1 and thereby terminates the differential signal path.

[0026] Each power strip 104 also includes circuitry used to detect the connection of other power strips 104. For example, the upstream indication pin (upstream port, pin 1) is coupled to ground through a resistor. As shown in Figs. 2A-C, when two power strips 104 are coupled together, the upstream indication pin will be coupled to the downstream detection pin (downstream port, pin 1) of the upstream power strip 104. The downstream detection pin is coupled to 5 Volt DC through a resistor. Accordingly, a power strip 104 can detect whether it is the last power strip on the data bus by detecting the voltage on the downstream detection pin. If no downstream power strip is coupled, as shown in reference to power strip C, the microcontroller 200 will detect approximately 5 VDC on the downstream detection pin. If a downstream power strip is coupled, as shown in reference to power strip B, the microcontroller 200 will detect approximately 0 VDC on the downstream detection pin, because the pin will be coupled to ground through the downstream power strip. Accordingly, power strip C will determine that it is the last power strip because pin 1 on the D-port 118 is pulled to 5 Volts DC.

[0027] The “next-device” input pin (downstream port, pin 5), “next-device” output pin (upstream port, pin 5), and corresponding circuitry are used for determining a unique PSID for each power strip 104 during the configuration process. The next-device input pin is pulled high through a resistor R6. The next-device input pin is coupled to transistor Q1 of the downstream power strip through the next-device output pin of the downstream power strip. At the start of the configuration process, the transistor Q1 will be off and the upstream power strip will detect 5 Volts DC at the next-device input pin. When the microcontroller 200 of a power strip 104 turns on transistor Q1, the next-device input pin of the upstream power strip is pulled to ground. When a power strip

104 detects this voltage drop at the next-device input pin, this triggers the microcontroller 200 to self-assign a PSID to itself and declare its PSID to the other power strips 104 and to the PDU 102. A more detailed method of configuring the power delivery system 100 is described below in relation to Fig. 3.

[0028] Fig. 3 is a process flow diagram of a method of configuring a daisy-chained power delivery system. The process described in Fig. 3 can be performed by each of the power strips 104, for example, by the microcontroller 200 of each power strip 104. The method is described with reference to Figs 2A-C. The method begins at block 302 and can be triggered by several possible events, such as receiving electrical power and initiating a boot process of the microcontroller, receiving a reset signal, and others.

[0029] At block 304, the microcontroller of each power strip senses the downstream detection input (pin 5) of the downstream port. The sensed value of the downstream detection input is used at block 306.

[0030] At block 306, a determination is made regarding whether the power strip is the last power strip on the data bus, i.e., the power strip furthest downstream from the PDU. If the downstream detection input is high, then the power strip is the last on the data bus, and the process flow advances to block 308.

[0031] At block 308, the microcontroller of the power strip enables the termination resistor for the data bus, such as by closing switch S1. Enabling the termination resistor enables communication to take place on the data bus.

[0032] At block 310, the microcontroller self-assigns a PSID. Because this is the first iteration of block 310 for the entire power delivery system, the microcontroller will assign the first PSID. In some examples, the PSID may be an integer value that represents the power strips relative position on the data bus, with one being the first power strip, i.e., the furthest downstream power strip. Accordingly, at the first iteration of block 310, the microcontroller may assign the power strip a PSID of one.

[0033] At block 312, the microcontroller declares its PSID on the data bus. Declaring the power strip's PSID enables the PDU to identify the power strip in

future communications. Declaring the power strip's PSID also informs the remaining power strips that the PSID is taken.

[0034] At block 314, the microcontroller pulls the collector of switch Q1 low. This causes the next device output pin to be grounded and thereby set to low. Setting the next device output pin low triggers the next power strip on the data bus to process itself as the next power strip on the data bus. After, pulling the collector of switch Q1 low, the process ends for this particular power strip. The process flow continues for any remaining power strips in the daisy-chain that have not self-assigned a PSID.

[0035] Returning to block 306, if the downstream detection input is low, then the power strip senses that it is not the last in the daisy chain. If the power strip is not the last on the data bus, then the process flow advances to block 318.

[0036] At block 318, the microcontroller waits to receive a PSID declaration. The microcontroller records the value of the PSID declaration once it is received.

[0037] At block 320, the microcontroller senses the next device input pin, which is coupled to the next device output pin of the downstream power strip.

[0038] At block 322 a determination is made regarding the value of the next device input pin. If the next device input pin is high, the power strip is not the next power strip on the data bus, and the process flow returns to block 318 where it waits for the next PSID declaration. If the next device input pin is low, then the power strip is the next power strip on the data bus, and the process flow continues to block 310. At block 310, the most recently declared PSID is incremented and this next PSID becomes the PSID for the power strip. The process flow then continues with blocks 312, 314, and 316 as described above.

[0039] After the last power strip (the one closest to the PDU) has completed blocks 310, 312, and 314, the PDU senses a low on pin 5. At this point, the PDU sends a broadcast command to all power strips indicating that the discovery process is complete. Normal data communications would then commence and all power strip microcontrollers would de-assert "next-device output" on pin 5 of the upstream port. At the end of the configuration process, each power strip has a PSID, which it includes in any communications sent to

the PDU 102. Messages from the PDU also include the PSID depending on which power strip is being targeted. The power strip with the correct PSID would interpret the PDU message as intended for it. In other words, each power strip will act on those messages from the PDU that include the matching PSID.

[0040] Implementing the above process in the power delivery system 100 of Figs. 2A, 2B, and 2C would provide the following results. First, power strip C would detect that its downstream port 118 is uncoupled and is therefore the last power strip on the data bus. Power strip C would then enable the termination resistor for the differential bus, assign itself a PSID of 1, and declare itself to be PSID 1 by sending a message on the differential bus, and set the next-device output to ground.

[0041] Next power strip B would receive the PSID declaration on the bus and also detect that its next device input pin is low. Power strip B would then assign to itself a PSID of 2, and declare itself to be PSID 2 by sending a message on the differential bus, and the set the next-device output to ground.

[0042] The above process would be repeated for power strip A, at which point the PDU 102 would sense a low on pin 5. The PDU 102 then sends a broadcast command to all power strips 104 indicating that the discovery process is complete. Normal data communication would then commence as described above.

[0043] In some examples, each power strip 104 is configured to periodically sense the state of various indicators during normal communication. Periodically sensing the state of the indicators enables the power strip 104 to detect changes to the physical configuration of the power delivery system 100 and report the changes to the PDU. For example, if a new power strip is added at the downstream port of power strip C, the downstream detection pin (downstream port, pin 1) will be pulled low. In response to this change, the power strip 104 can report the addition of a new power strip to the PDU 102.

[0044] If one of the power strips is removed, the downstream detection pin will go from low to high. In response to this change, the power strip 104 can close its termination switch S1 and report to the PDU 102 that it is now the last

power strip on the data bus. Based on the PSID received, the PDU will be informed that any power strips 104 further downstream are now longer connected.

[0045] Fig. 4 is a block diagram of an example reset circuit that can be used in the power strip. As mentioned above, the power strips 104 may be configured to re-run the configuration process in response to a reset instruction. The reset instruction may be useful in cases in which one or more of the microcontrollers 200 in the power strips 104 or the PDU 102 encounters some sort of unrecoverable error.

[0046] A rest signal may be transmitted from the PDU 102 to each of the microcontrollers 200 through the differential bus. The reset signal may be sent automatically, for example, in response to a time-out. The reset signal may also be initiated by the administrator. The microcontroller 200 can include a dedicated input line that can detect a reset signal input and, in response, override any other process being performed by the microcontroller 200 and initiate the configuration process. This dedicated input line may be referred to herein as the reset interrupt 402.

[0047] The power strip includes reset circuitry 404 that is configured to recognize the reset signal transmitted on the differential bus and activate the reset interrupt 402. In some examples, the reset circuitry is configured to detect that both lines DIFF+ and DIFF- have gone low for a certain length of time. Other patterns could also be used to indicate a reset command. Furthermore, the reset circuitry 404 shown in Fig. 4 is only one example of a circuit capable of detecting a data pattern that represents a reset command.

[0048] As shown in Fig. 4, the microcontroller 200 is coupled to the differential bus through a transceiver 406. The reset circuitry 404 is coupled to DIFF+ and DIFF- at the input of the transceiver 406. The input of the reset circuitry 404 includes a pair of resistors 408 used for isolation. Both inputs are fed to separate NAND gates 410, each of which are configured as inverters. The output of each NAND gate 410 is sent to another NAND gate 412. The output of NAND gate 412 is passed through a low pass filter 414, which filters out short-lived transient signals. The output of the low pass filter 414 is sent to

another NAND gate 416, which is configured as another inverter. The output of NAND gate 416 is coupled to the gate of a transistor 418. The collector of the transistor 418 is coupled to the reset interrupt 402. The net result of the example reset circuitry 404 shown in Fig. 4 is that if the DIFF+ and DIFF- both go low for a certain length of time, the output of the NAND gate 416 will go high, turning on the transistor 418 and causing the reset interrupt 402 to go low, which triggers the microcontroller 200 to begin the reset process. The length of time that will trigger a reset is determined by the response characteristics of the low pass filter 414 and the propagation delay of the NAND gates 410, 412, and 416.

[0049] While the present techniques may be susceptible to various modifications and alternative forms, the exemplary examples discussed above have been shown only by way of example. It is to be understood that the technique is not intended to be limited to the particular examples disclosed herein. Indeed, the present techniques include all alternatives, modifications, and equivalents falling within the true spirit and scope of the appended claims.

CLAIMS

What is claimed is:

1. A system comprising:

a power distribution unit; and

a plurality of power outlet strips coupled to the power distribution unit, the power distribution unit to provide AC power to each of the power outlet strips; and

a data bus that communicatively couples each of the plurality of power outlet strips to the power distribution unit, wherein the data bus is routed serially through each of the plurality of power outlet strips.

2. The system of claim 1, wherein the power distribution unit includes an AC-to-DC converter that provides DC electrical power to each of the power outlets strips.

3. The system of claim 1, wherein each of the plurality of power outlet strips includes circuitry that uses DC power to operate, but none of the plurality of power outlet strips include an AC-to-DC converter.

4. The system of claim 1, wherein each of the plurality of power outlet strips is configured to self-assign a power strip identifier that is used in communications between the power outlet strip and the power distribution unit.

5. The system of claim 1, wherein each of the plurality of power outlet strips includes circuitry to detect whether it is the last power outlet strip on the data bus.

6. The system of claim 1, wherein each of the plurality of power outlet strips includes circuitry to provide an indication to an upstream power outlet strip that it is not the last power outlet strip on the data bus.

7. The system of claim 1, wherein each of the plurality of power outlet strips comprises reset circuitry to reset a controller of the power outlet strip in response to a reset command received on the data bus.

8. A power outlet strip, comprising:

an upstream port and a downstream port, wherein a data bus is coupled to and passes through the upstream port and downstream port;

a controller to:

self-assign a power strip identifier (PSID);

declare the PSID on the data bus; and

set a next-device output to a value that triggers a next power outlet strip to self-assign a next PSID.

9. The power outlet strip of claim 8, comprising a termination circuit, wherein the controller is to use the termination circuit to terminate the data bus with a resistance if the controller detects that it is the last power outlet strip coupled to the bus.

10. The power outlet strip of claim 8, wherein the power outlet strip is to receive DC power from a power distribution unit (PDU).

11. The power outlet strip of claim 8, comprising reset circuitry to reset a controller of the power outlet strip in response to a reset command received on the data bus.

12. A method performed by a power delivery system, comprising:

sensing, in a first controller of a first power outlet strip, that there is no downstream power outlet strip coupled to the first power outlet strip;

in response to the sensing:

terminating a data bus in the first power outlet strip;

assigning a first power strip identifier (PSID) to the first power outlet strip;

declaring the first PSID over the data bus; and

setting a next-device output to a new value.

13. The method of claim 12, comprising:

recording, in a second controller of a second power outlet strip, the PSID declared by the first power outlet strip;

sensing, in the second controller, the new value of the next-device output; and

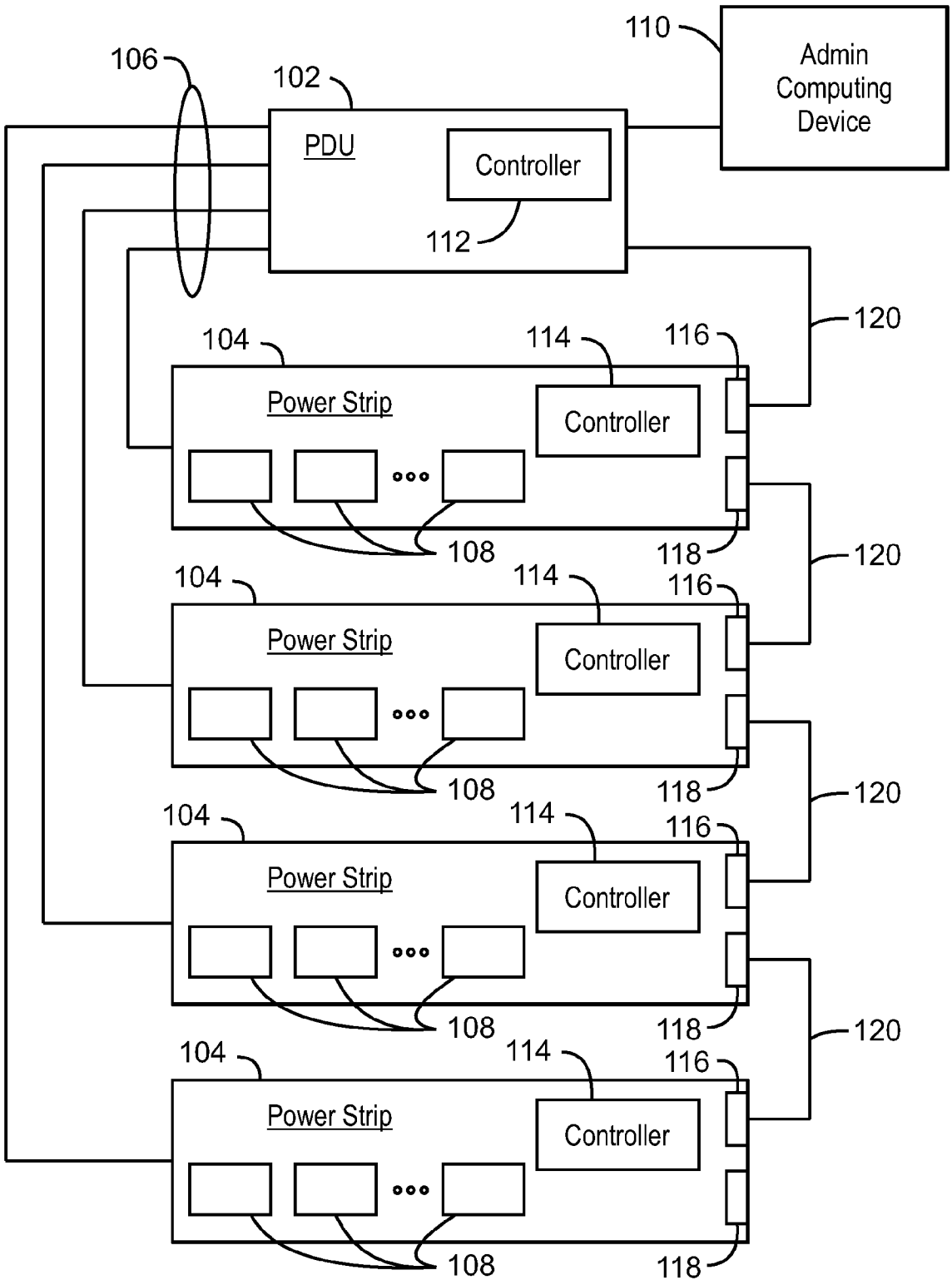
incrementing the PSID to a next PSID and self-assigning the next PSID to the second power outlet strip.

14. The method of claim 12, comprising:

sensing, in a Power Distribution Unit (PDU), the new value of the next-device output; and

declaring over the data bus that a configuration process has terminated.

15. The method of claim 14, comprising sending a message from the PDU to the first power outlet strip, wherein the first power outlet strip acts on the message if a PSID included in the message matches the first PSID.


110
Admin Computing Device
106
102
PDU
Controller
112
120
104
114
116
Power Strip
Controller
108
118
120
104
114
116
Power Strip
Controller
108
118
120
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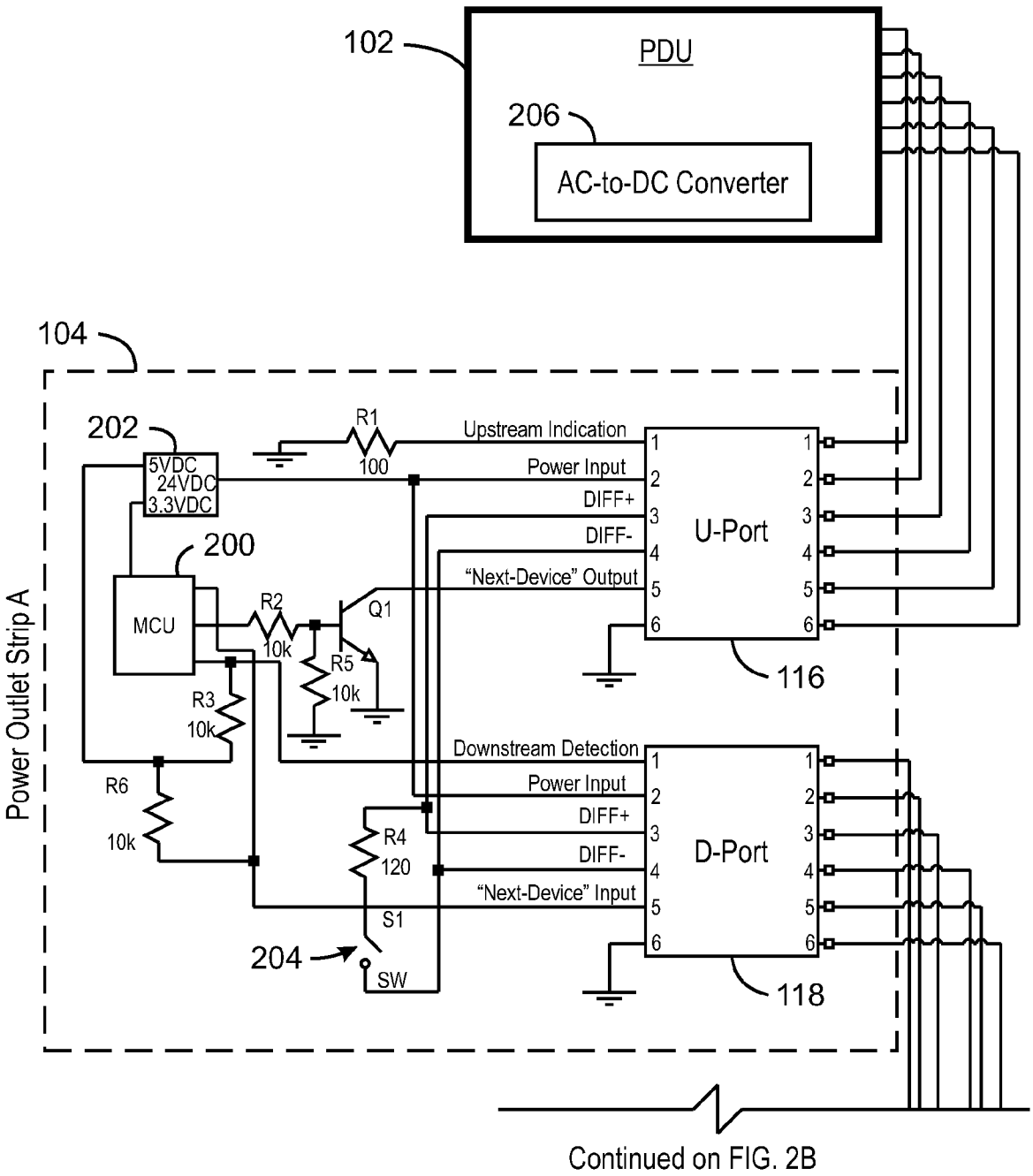
Controller
108
118
120
104
114
116
Power Strip
Controller
108
118

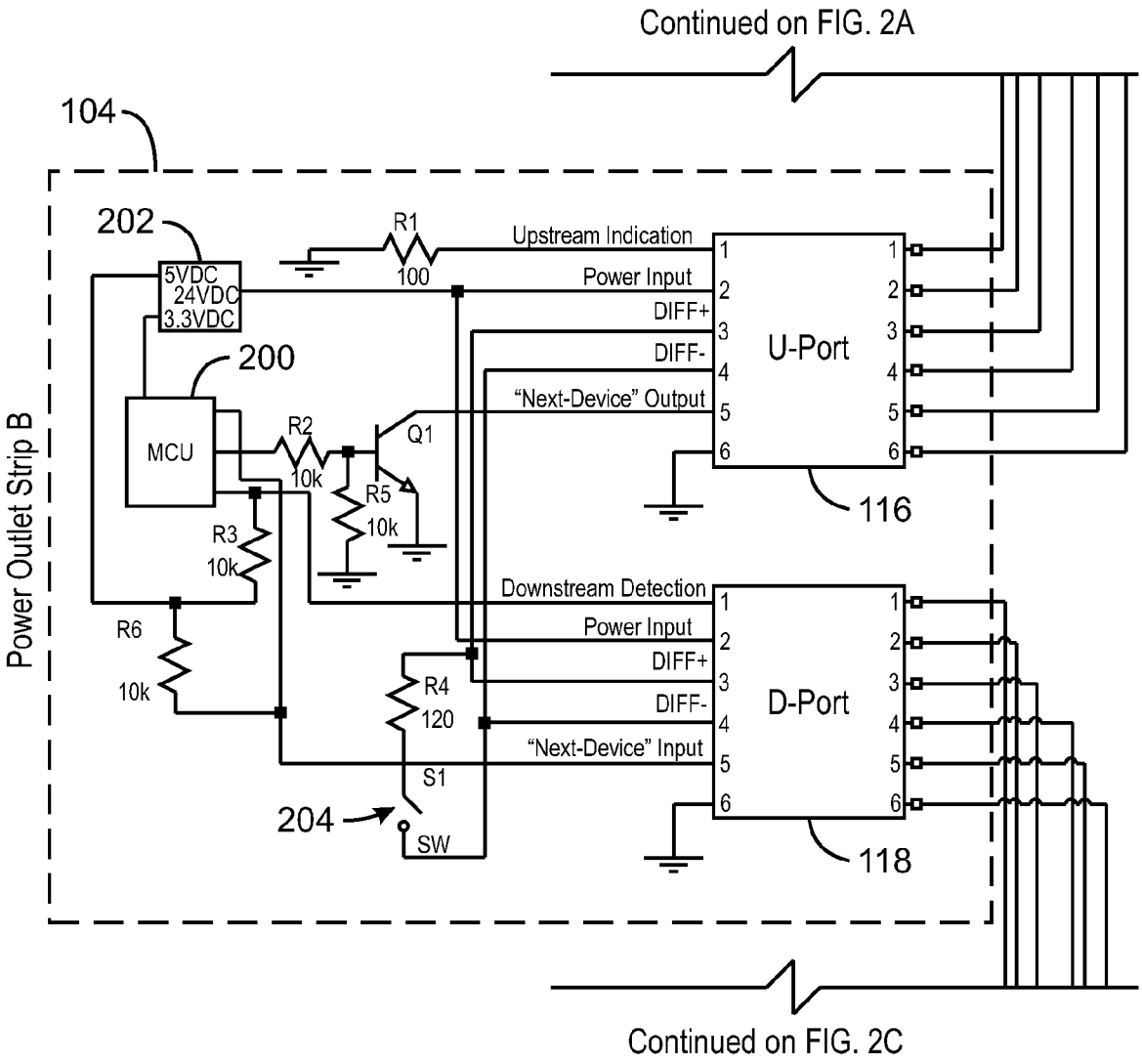
100

FIG. 1


102
PDU
206
AC-to-DC Converter
104
Power Outlet Strip A
202
5VDC
24VDC
3.3VDC
200
MCU
R1
100
R2
10k
Q1
R5
10k
R3
10k
R6
10k
R4
120
S1
204
SW
Upstream Indication
Power Input
DIFF+
DIFF-
"Next-Device" Output
U-Port
116
Downstream Detection
Power Input
DIFF+
DIFF-
"Next-Device" Input
D-Port
118
Continued on FIG. 2B

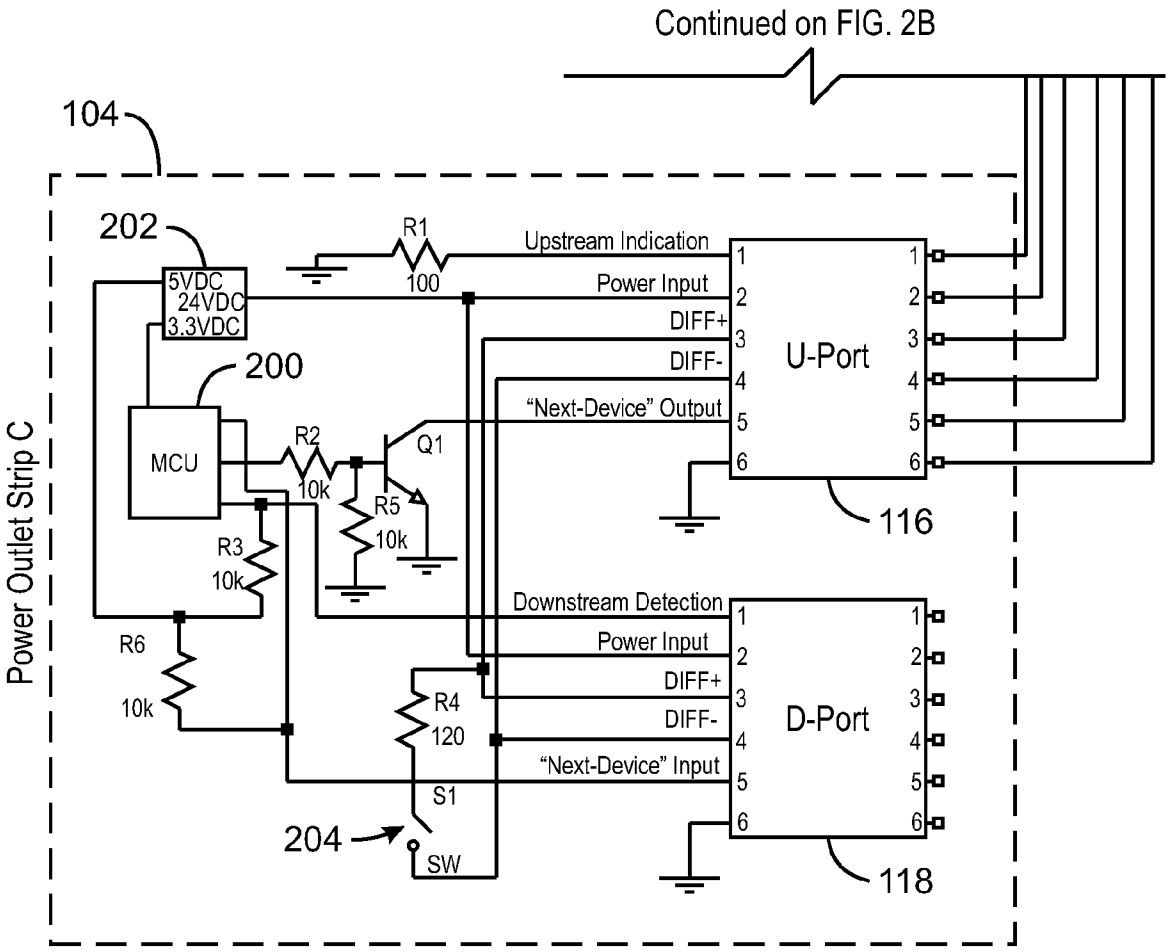
100

FIG. 2A


Continued on FIG. 2A
104
Power Outlet Strip B
202
5VDC
24VDC
3.3VDC
200
MCU
R1
100
R2
10k
Q1
R5
10k
R3
10k
R6
10k
R4
120
S1
204
SW
Upstream Indication
Power Input
DIFF+
DIFF-
"Next-Device" Output
U-Port
116
Downstream Detection
Power Input
DIFF+
DIFF-
"Next-Device" Input
D-Port
118
Continued on FIG. 2C

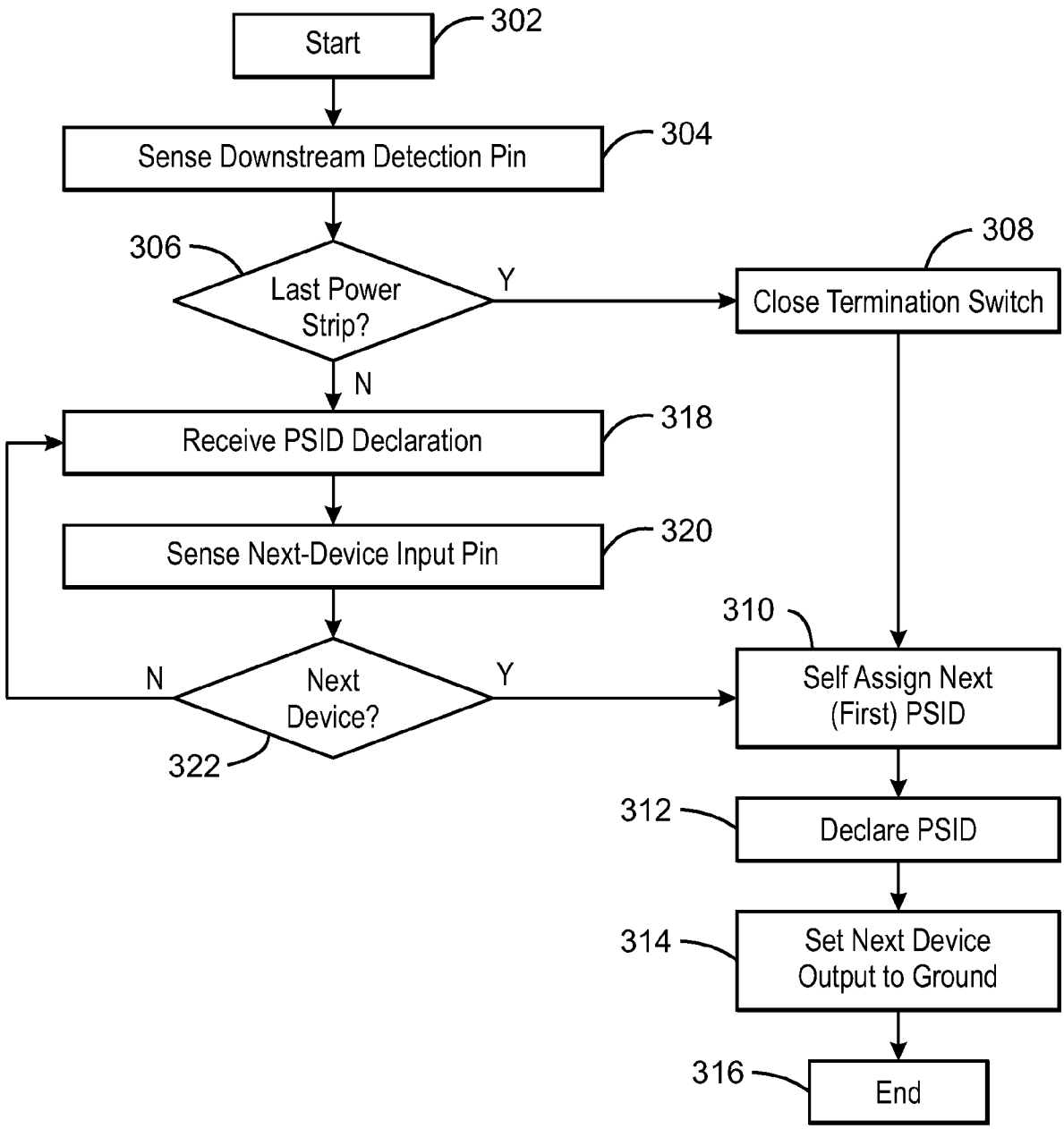
100

FIG. 2B


Continued on FIG. 2B
104
Power Outlet Strip C
202
5VDC
24VDC
3.3VDC
200
MCU
R1
100
R2
10k
Q1
R5
10k
R3
10k
R6
10k
R4
120
S1
204
SW
Upstream Indication
Power Input
DIFF+
DIFF-
"Next-Device" Output
U-Port
116
Downstream Detection
Power Input
DIFF+
DIFF-
"Next-Device" Input
D-Port
118

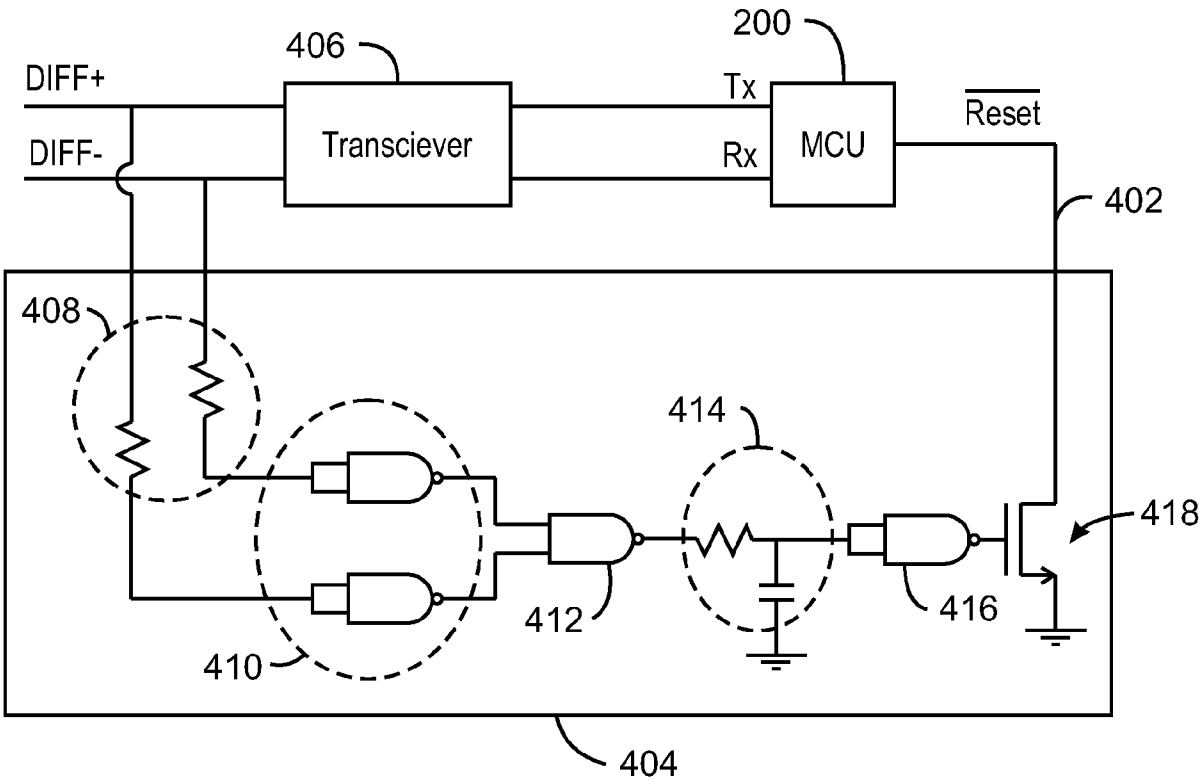
100

FIG. 2C


Start
302
Sense Downstream Detection Pin
304
306
Last Power Strip?
Y
308
Close Termination Switch
N
Receive PSID Declaration
318
Sense Next-Device Input Pin
320
310
N
Next Device?
Y
Self Assign Next (First) PSID
322
312
Declare PSID
314
Set Next Device Output to Ground
316
End

300

FIG. 3


406
200
DIFF+
DIFF-
Transciever
Tx
Rx
MCU
Reset
402
408
414
418
412
416
410
404

400

FIG. 4

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2015/026233

A. CLASSIFICATION OF SUBJECT MATTER

H02J 5/00(2006.01)i, H02J 4/00(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H02J 5/00; G06F 1/28; H02J 1/00; H02J 1/10; H02J 3/14; H04B 3/00; H02J 13/00; H02J 3/00; H02J 4/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & keywords: power distribution, strip, outlet, data bus, identifier, upstream, downstream

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2012-0195355 A1 (WAEL R. EL-ESSAWY et al.) 02 August 2012 See paragraphs 17, 27, 37-43, claim 21, and figure 2.	1-15
Y	WO 2015-007888 A1 (KONINKLIJKE PHILIPS N.V.) 22 January 2015 See page 2, lines 28-33, page 5, lines 3-8, page 7, lines 1-9, page 9, lines 3-4, page 12, lines 23-24, claims 1, 7, and figures 1-2.	1-15
A	JP 2013-218704 A (SERVER TECHNOLOGY INC.) 24 October 2013 See paragraphs 29-30, claim 1, and figure 2.	1-15
A	US 2009-0236909 A1 (PHILIP R. ALDAG et al.) 24 September 2009 See paragraphs 70-73, claim 1, and figures 2-3.	1-15
A	US 2013-0020868 A1 (CHIEN-LUNG WU et al.) 24 January 2013 See paragraphs 28-35, claims 1-4, and figures 5-6.	1-15

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
13 January 2016 (13.01.2016)	**14 January 2016 (14.01.2016)**

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2015/026233

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2012-0195355 A1	02/08/2012	US 8519843 B2	27/08/2013
WO 2015-007888 A1	22/01/2015	None	
JP 2013-218704 A	24/10/2013	CA 2713428 A1	09/07/2009
		CA 2713428 C	31/03/2015
		EP 2248044 A1	10/11/2010
		EP 2248044 A4	11/12/2013
		JP 2011-508352 A	10/03/2011
		JP 5710686 B2	30/04/2015
		US 2009-0234512 A1	17/09/2009
		US 2014-0236372 A1	21/08/2014
		US 8494661 B2	23/07/2013
		WO 2009-086485 A1	09/07/2009
		WO 2009-086485 A9	03/09/2009
US 2009-0236909 A1	24/09/2009	DE 112009000697 T5	10/02/2011
		US 2011-0237097 A1	29/09/2011
		US 2011-0244715 A1	06/10/2011
		US 7982335 B2	19/07/2011
		US 8207627 B2	26/06/2012
		US 8264099 B2	11/09/2012
		WO 2009-117500 A2	24/09/2009
		WO 2009-117500 A3	18/02/2010
US 2013-0020868 A1	24/01/2013	TW 201306420 A	01/02/2013
		TW I433420 B	01/04/2014