



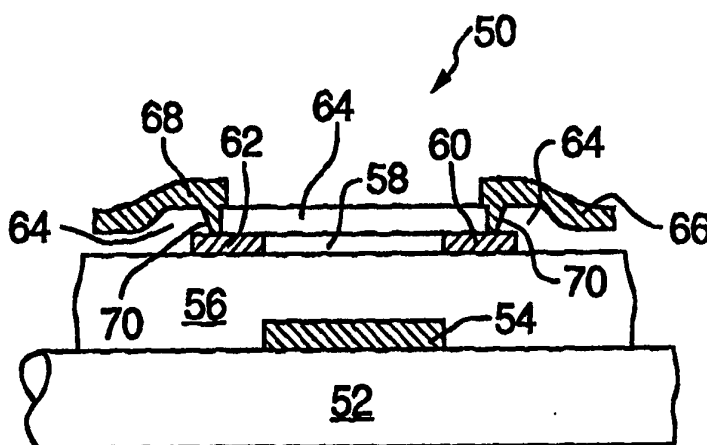
INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

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(21) International Application Number: PCT/CA95/00455 (22) International Filing Date: 31 July 1995 (31.07.95) (71) Applicant (for all designated States except US): LITTON SYSTEMS CANADA LIMITED [CA/CA]; 28 City View Drive, Etobicoke, Ontario M9W 5A7 (CA). (72) Inventor; and (75) Inventor/Applicant (for US only): FARRELL, James, F. [CA/CA]; 158 Beaver Bend Crescent, Etobicoke, Ontario M9W 5A7 (CA). (74) Agents: PERRY, Stephen, J. et al.; Sim & McBurney, Suite 701, 330 University Avenue, Toronto, Ontario M5G 1R7 (CA).		(81) Designated States: CA, JP, US, European patent (AT, BE, CH, DE, DK, ES, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE). Published With international search report.

(54) Title: METHOD OF FORMING SELF-ALIGNED THIN FILM TRANSISTOR

(57) Abstract

During the formation of a self-aligned thin film transistor (50), the semiconductor material channel layer (58) on the gate insulating layer (56) has a passivation shield (56) applied to it aligned with the gate electrode (54). The channel layer is then exposed to a reagent selected to yield a chemical reaction with the portions of the channel layer (58) not covered by the passivation shield (Ps) causing removal of a component of the semiconductor material thereby to change the electrical properties of those portions of the channel layer. In this manner, doped source and drain regions (60, 62) can be formed on opposite sides of the channel having edges that extend to the edges of the gate electrode avoiding any overlap therebetween and reducing the parasitic capacitance of the thin film transistor (50).



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METHOD OF FORMING SELF-ALIGNED THIN FILM TRANSISTOR**TECHNICAL FIELD**

5 The present invention relates to semiconductor fabrication methods and in particular to a method of doping a compound semiconductor material. More specifically, the present invention relates to a method of forming a self-aligned thin film transistor (TFT).

BACKGROUND ART

10 Self-aligned field effect transistors (FETS) are known in the art. During the formation of transistors of this nature, ion implantation has been used to form the heavily doped source and drain regions of the transistor so that the edges of the source and drain regions line up with the edges of the gate electrode. This doping of the source and drain regions is of course necessary since these regions are unmodulated by the gate electrode. Since there is no overlap of the source and drain regions with the gate electrode, the parasitic capacitance of the transistor is greatly reduced as compared to conventional transistors having gate electrodes and source and drain regions that overlap.

20 Parasitic capacitance affects the switching speed of a transistor. Therefore, in environments requiring high speed switching, such as in driver circuits for active matrix liquid crystal displays (AMLCDs), it is desired to minimize the parasitic capacitance of transistors to increase their switching speed. Although ion implantation methodology has allowed self-aligned transistors which reduce parasitic to be fabricated, ion implantation is a high energy process. Accordingly, alternative methods of doping semiconductor material and fabricating self-aligned transistors which reduce energy requirements are desired.

Therefore, it is an object of the present invention to provide a novel method of doping compound semiconductor material and a novel method of forming a self-aligned thin film transistor.

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DISCLOSURE OF THE INVENTION

According to one aspect of the present invention there is provided a method of doping a compound semiconductor material comprising the step of:

10 exposing the compound semiconductor material to a reagent selected to yield a chemical reaction with the semiconductor material causing removal of a component of said semiconductor material thereby to change its
15 electrical properties and dope said semiconductor material.

According to another aspect of the present invention there is provided a method of forming a self-aligned thin film transistor comprising the steps of:

20 depositing a gate electrode on a surface of a glass substrate and covering said surface and gate electrode with a gate insulating layer;

25 depositing a channel layer formed of compound semiconductor material on said gate insulating layer, said channel layer being positioned over and extending beyond said gate electrode;

30 depositing a shield on a portion of said channel layer aligned with and overlying said gate electrode;

35 subjecting the structure to a reagent selected to react with said semiconductor material causing removal of a component thereof, said reagent reacting with the portions of said channel layer not covered by said shield to form doped source and drain regions extending to the edges of said gate electrode and positioned on opposite sides of a channel; and

forming source and drain electrodes in contact with said respective source and drain regions.

In yet another aspect of the present invention there is provided in a self-aligned thin film transistor fabrication method wherein a gate electrode is deposited on a substrate, said substrate and gate electrode are covered by a gate insulating layer, a channel and doped source and drain regions on opposite sides of said channel are deposited on said gate insulting layer and source and drain electrodes are formed and contact the respective source and drain region, the improvement comprising:

depositing a channel layer formed of a compound semiconductor material on said gate insulating layer; shielding a portion of said channel layer overlying and aligned with said gate electrode; and doping portions of said channel layer not shielded by exposing the portions to a reagent selected to yield a chemical reaction with said compound semiconductor material causing removal of a component of said semiconductor material thereby to change its electrical properties and define said doped source and drain regions.

In still yet another aspect of the present invention there is provided a method of forming a self-aligned thin film transistor, wherein a gate insulating layer covers a gate electrode and a surface of a glass substrate, said method comprising the steps of:

depositing a channel layer formed of compound semiconductor material on said gate insulating layer, said channel layer being positioned over and extending beyond said gate electrode;

forming a shield over a portion of said channel layer aligned with and overlying said gate electrode;

subjecting the structure to a reagent selected to react with said semiconductor material causing removal of a component thereof, said reagent reacting with the portions of said channel layer not covered by said shield to form doped source and drain regions extending to the edges of said gate electrode and positioned on opposite sides of a channel; and

placing source and drain electrodes in contact with said respective source and drain regions.

Preferably, the compound semiconductor material is formed of one of CdSe, CdTe, CdS, InP and GaP. It is also preferred that the reagent is in the form of one of a gas, plasma or liquid chemical reagent.

The present invention provides advantages in that a low temperature and low energy process is used to fabricate a self-aligned transistor which makes use of the fact that most compound semiconductor materials will react with a reagent causing removal of one of the components of the semiconductor material and thereby causing the electrical properties of the semiconductor material to change.

BRIEF DESCRIPTION OF THE DRAWINGS

Embodiments of the present invention will now be described more fully with reference to the accompanying drawings in which:

Figures 1a, 1b and 1c are cross-sectional views of various prior art thin film transistors having inverted staggered structures;

Figure 2 is a cross-sectional view of a self-aligned thin film transistor having an inverted staggered structure and formed in accordance with the present method;

Figures 3a to 3f show fabrication steps performed during the formation of the thin film transistor of Figure 2;

5 Figure 4 is a cross-sectional view of an alternative embodiment of a self-aligned thin film transistor formed in accordance with the present method;

Figures 5a and 5b show fabrication steps performed during the formation of the thin film transistor of Figure 4; and

10 Figure 6 is a cross-sectional view of yet another embodiment of a self-aligned thin film transistor formed in accordance with the present method.

BEST MODES FOR CARRYING OUT THE INVENTION

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Figures 1a to 1c show a number of prior art thin film transistors T, each having an inverted staggered structure. Each transistor includes a substrate ST, a gate insulating layer GI and a semiconductor material channel C defining the source and drain regions of the transistor. Source and drain electrodes S and D respectively are located on the gate insulating layer adjacent the source and drain regions. A gate electrode G is located between the substrate and the gate insulating layer. In each of these transistors T, there is an overlap between the source and drain electrodes and the gate electrode. It is this overlap which is responsible for parasitic capacitance.

30 Figure 2 shows a self-aligned thin film transistor fabricated in accordance with the present method and is indicated generally by reference numeral 50. As can be seen, the transistor 50 includes a glass substrate 52 on which a Cr gate electrode 54 is located. A gate insulating layer 56 formed of SiO₂ overlies the gate electrode 54 and one surface of the glass substrate 52. A compound polycrystalline semiconductor material

35

channel 58 formed of Cadmium Selenide (CdSe) is on the gate insulating layer 56 above the gate electrode. Doped source and drain regions 60 and 62 respectively formed of semiconductor material are on opposite sides of the

5 channel 58. A passivation layer 64 in the form of a positive photoresist covers the source and drain regions 60 and 62, the channel 58 and the gate insulating layer 56. Source and drain electrodes 66 and 68 are located on the passivation layer 64 and contact a respective one of

10 the source and drain regions 60 and 62 through vias 70 formed in the passivation layer.

The present method of forming the transistor 50 will now be described with particular reference to

15 Figures 3a to 3f. During the fabrication process, after the gate electrode 54 and gate insulating layer 56 have been deposited on the glass substrate 52 (see Figure 3a), a channel layer 58 is deposited on the gate insulating layer 56 (see Figure 3b). As can be seen, the channel

20 layer overlies and extends beyond the gate electrode 54. A passivation shield P_s in the form of a positive photoresist is then deposited over the channel layer 58 and the gate insulating layer 56.

25 The structure is then exposed to UV radiation from the rear side (see Figure 3c). The glass substrate 52, gate insulating layer 56 and channel layer 58 are transparent; however, the gate electrode 54 is opaque. Because of this, only the portion of the passivation

30 shield P_s overlying and aligned with the gate electrode 54 polymerizes. After this, the portion of the passivation shield P_s that does not polymerize is removed.

Following this, the structure is exposed to a

35 reagent selected to react with the semiconductor material forming the channel layer 58 which will cause removal of a component of the semiconductor material and thereby

change its electrical properties in the desired manner (see Figure 3d). The passivation shield P_s prevents the portion of the channel layer 58 located directly below it from being exposed to the reagent. Therefore, the electrical properties of the portion of the channel layer 58 aligned with the gate electrode 54 remain unchanged. However, the portions of the channel layer 58 that are not covered by the passivation shield P_s react with the reagent. In this example, since the channel layer 58 is formed of CdSe, the CdSe layer is exposed to a Hydrogen (H) plasma reagent yielding a chemical reaction which selectively removes Selenium (Se) causing Selenium vacancies to be present in the polycrystalline semiconductor material (ie. $CdSe + H \rightarrow Cd + H_2Se$). The Selenium vacancies result in the semiconductor material becoming highly n^+ type (i.e. doped).

During this stage of the process, it is important to subject the semiconductor material to the reagent so that the semiconductor material becomes heavily doped. The parameters which affect the reaction between the reagent and the semiconductor material are exposure time, temperature, power and reagent concentration. By adjusting the reagent concentration, the exposure time can be set to give an adequate exposure time window.

Prior to performing this stage, calibration tests are performed on semiconductor material to determine the values of the parameters necessary to achieve the desired doping concentration while maintaining the desired exposure time window. Once the values of the parameters have been determined, they are used when subjecting the semiconductor material channel layer to the reagent.

Since the passivation shield P_s is aligned with the gate electrode 54, the portions of the channel layer 58 on opposite sides of the passivation shield that undergo changes in electrical properties (i.e. become heavily doped), define the source and drain regions of the transistor 50 and have edges that line up with the edges of the gate electrode (Figure 3e). In this way, there is no overlap of the source and drain regions with the gate electrode thereby reducing the parasitic capacitance of the transistor.

Once the source and drain regions have been formed, the passivation shield P_s is removed and the structure is covered with a passivation layer 64 (also see Figure 3e). Contact vias 70 are formed in the passivation layer 64 above the source and drain regions 60 and 62 respectively and the source and drain electrodes 66 and 68 respectively are then formed to complete the thin film transistor.

Referring now to Figure 4, a self-aligned film transistor fabricated using an alternative embodiment of the present method is shown. In this embodiment, like reference numerals will be used to indicate like components with a "100" added for clarity. In this embodiment, the transistor 150 is very similar to that shown in Figure 2 and includes a glass substrate 152, a gate electrode 154, a gate insulating layer 156 and a compound semiconductor material channel 158. Doped source and drain regions 160 and 162 respectively formed of semiconductor material are on opposite sides of the channel 158. Overlying the channel 158 and aligned with the gate electrode 154 is a shield 200 formed of SiO_2 . A passivation layer 164 covers the gate insulating layer 156, source and drain regions 160 and 162 and the passivation shield 200. Source and drain electrodes 166 and 168 contact a respective one of the source and drain

regions 160 and 162 through vias 170 formed in the passivation layer 164.

5 During formation of transistor 150, after the gate electrode 154, gate insulating layer 15 and channel layer have been formed on the substrate 15 and prior to exposing the structure to UV radiation, the structure is covered with a layer 200 of SiO_2 and then with a passivation shield P_s in the form of a positive
10 photoresist. The structure is then exposed to UV radiation causing the photoresist aligned with and overlying the gate electrode to polymerize (see Figure 5a). Once this has been done, the portion of the passivation shield P_s that does not polymerize is removed
15 and the exposed SiO_2 layer is etched from the structure. Following this, the structure is treated in the manner described previously by exposing the structure to a suitable reagent (see Figure 5b) and completing steps (iv) and (v) shown in Figures 3e and 3f.

20

If desired during the fabrication process, step (iv) illustrated in Figure 3d may be omitted so that once the structure has been subjected to the reagent to remove selectively a component of the semiconductor material to
25 form the doped source and drain regions and the passivation shield has been removed from the structure, the source and drain electrodes can be formed directly on the respective source and drain regions and the gate insulating layer. Figure 6 shows a self-aligned thin
30 film transistor formed in this manner. As can be seen, transistor 350 is very similar to those previously described except that the passivation layer has been removed avoiding the need to form contact vias.

35

Although the gate electrode has been described as being formed of Chromium, it should be realized that any refractory metal or combination of refractory and

high conductivity metals are suitable. The gate insulating layer may also be formed of materials other than SiO_2 , such as for example Si_3N_4 or any other dielectric material suitable for forming an isolation layer in a field effect transistor.

As one of skill in the art will appreciate, the channel layer must be formed of a compound semiconductor material which reacts with a reagent to yield a chemical reaction which selectively removes a component of the semiconductor material. Although the preferred embodiment describes the semiconductor material as being CdSe, other compound semiconductor materials can be used such as for example CdS, CdTe, InP and GaP. The reagent will of course be selected based on the type of compound semiconductor material forming the channel layer and may be a gas, plasma or liquid chemical reagent.

The preferred embodiments of the present invention have been described during formation of self-aligned thin film transistors. However, those of skill in the art will appreciate that the present method of doping compound semiconductor material can be used during the formation of virtually any semiconductor device.

When the thin film transistors are for use in an active matrix liquid crystal display or a flat panel detector for radiation imaging, an array of the transistors is formed simultaneously on a common substrate. Those of skill in the art will appreciate that the various layers forming the array of transistors are deposited on the substrate and etched as required.

Those of skill in the art will also appreciate that various modifications may be made to the present invention without departing from its scope as defined by the appended claims.

WHAT IS CLAIMED IS:

1. A method of doping a compound semiconductor material comprising the step of:
5 exposing the compound semiconductor material to a reagent selected to yield a chemical reaction with the semiconductor material causing removal of a component of said semiconductor material thereby to change its electrical properties and dope said semiconductor
10 material.
2. The method of claim 1 wherein portions of said semiconductor material are shielded from said reagent to dope selective portions of said semiconductor material
15 not shielded.
3. The method of claim 1 wherein said semiconductor material is formed of CdSe and said reagent is in the form of a hydrogen plasma.
20
4. The method of claim 1 wherein said semiconductor material is formed of one of CdSe, CdTe, CdS, InP and GaP.
- 25 5. The method of claim 1 wherein said reagent is in the form of one of a gas, plasma and liquid chemical reagent.
6. A method of forming a self-aligned thin film transistor comprising the steps of:
30 depositing a gate electrode on a surface of a glass substrate and covering said surface and gate electrode with a gate insulating layer;
depositing a channel layer formed of compound
35 semiconductor material on said gate insulating layer, said channel layer being positioned over and extending beyond said gate electrode;

depositing a shield on a portion of said channel layer aligned with and overlying said gate electrode;

5 subjecting the structure to a reagent selected
to react with said semiconductor material causing removal
of a component thereof, said reagent reacting with the
portions of said channel layer not covered by said shield
to form doped source and drain regions extending to the
edges of said gate electrode and positioned on opposite
10 sides of a channel; and
 forming source and drain electrodes in contact
with said respective source and drain regions.

7. The method of claim 6 wherein said shield is
15 formed on said channel layer using positive photoresist.

8. The method of claim 7 wherein prior to forming
said source and drain electrodes, said shield is removed
and a passivation layer is placed over said drain and
20 source regions, said channel and said gate insulating
layer, said drain and source electrodes contacting said
respective source and drain regions through vias formed
in said passivation layer.

9. The method of claim 6 wherein a layer of SiO_2 is
25 formed on said channel layer interposed between said
channel layer and said shield.

10. The method of claim 6 wherein said
30 semiconductor material is formed of one of CdSe, CdTe,
CdS, InP and GaP.

11. The method of claim 6 wherein said reagent is
in the form of one of a gas, plasma and liquid chemical
35 reagent.

12. A self-aligned thin film transistor fabrication method wherein a gate electrode is deposited on a substrate, said substrate and gate electrode are covered by a gate insulating layer, a channel and doped source and drain regions on opposite sides of said channel are deposited on said gate insulating layer and source and drain electrodes are formed and contact the respective source and drain region, the improvement comprising:

depositing a channel layer formed of a compound semiconductor material on said gate insulating layer;

shielding a portion of said channel layer overlying and aligned with said gate electrode; and

doping portions of said channel layer not shielded by exposing the portions to a reagent selected to yield a chemical reaction with said compound semiconductor material causing removal of a component of said semiconductor material thereby to change its electrical properties and define said doped source and drain regions.

13. The method of claim 12 wherein said semiconductor material is formed of CdSe and said reagent is in the form of a hydrogen plasma.

14. The method of claim 12 wherein said semiconductor material is formed of one of CdSe, CdTe, CdS, InP and GaP.

15. The method of claim 12 wherein said reagent is in the form of one of a gas, plasma and liquid chemical reagent.

16. In a method of forming a self-aligned thin film transistor, wherein a gate insulating layer covers a gate electrode and a surface of a glass substrate, said method comprising the steps of:

depositing a channel layer formed of compound semiconductor material on said gate insulating layer, said channel layer being positioned over and extending beyond said gate electrode;

5 forming a shield over a portion of the channel layer aligned with and overlying said gate electrode;

 subjecting the structure to a reagent selected to react with said semiconductor material causing removal of a component thereof, said reagent reacting with the
10 portions of said channel layer not covered by said shield to form doped source and drain regions extending to the edges of said gate electrode and positioned on opposite sides of a channel; and

 forming source and drain electrodes in contact
15 with said respective source and drain regions.

17. The method of claim 16 wherein said semiconductor material is formed of CdSe and said reagent is in the form of a hydrogen plasma.

20

18. The method of claim 16 wherein said semiconductor material is formed of one of CdSe, CdTe, CdS, InP and GaP.

25 19. The method of claim 16 wherein said reagent is in the form of one of a gas, plasma and liquid chemical reagent.

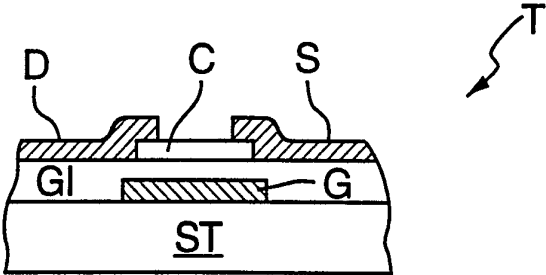


FIG.1a (Prior Art)

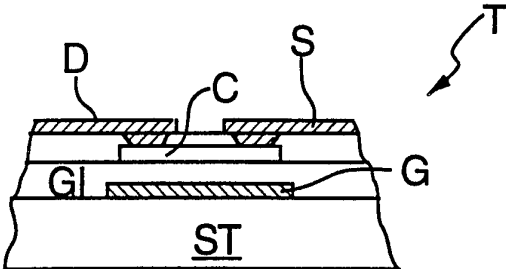


FIG.1b (Prior Art)

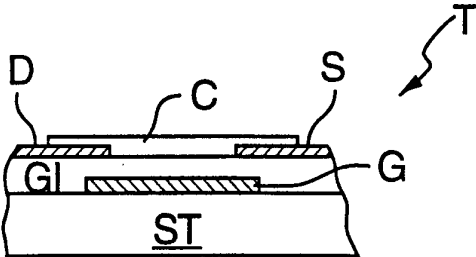


FIG.1c (Prior Art)

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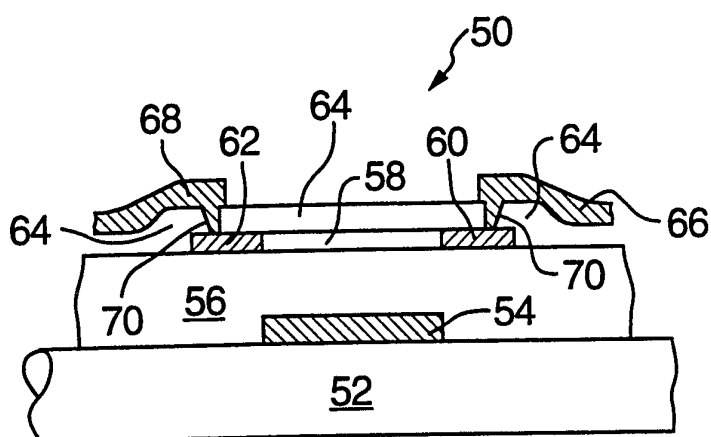


FIG.2

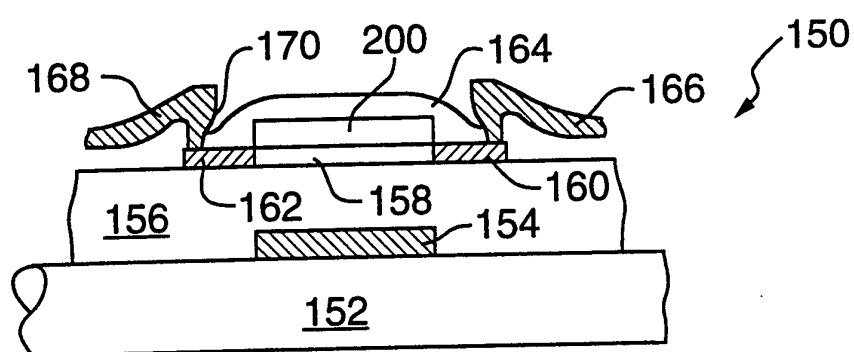


FIG.4

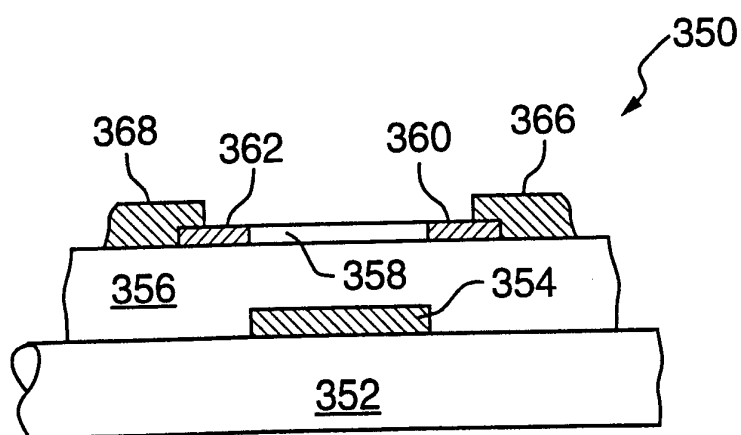


FIG.6

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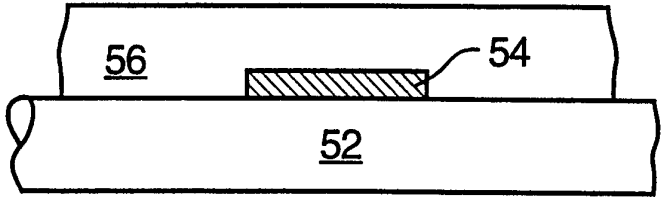
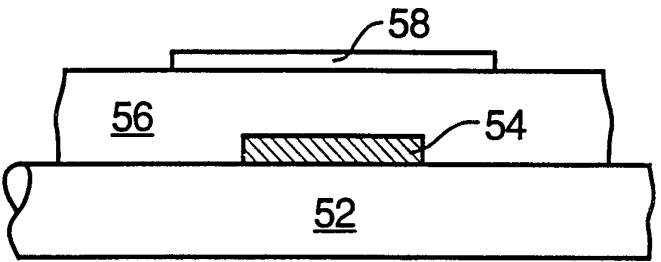
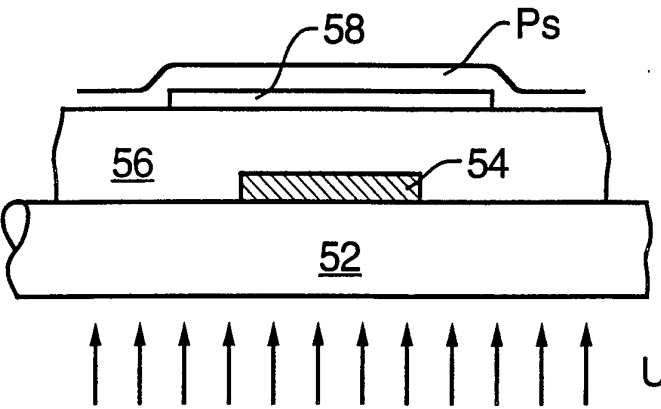


FIG.3a



Step (i)

FIG.3b



Step (ii)

FIG.3c

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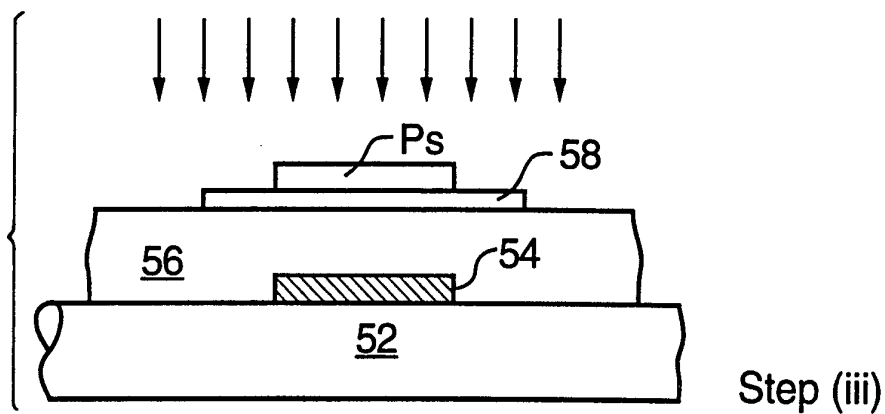


FIG.3d

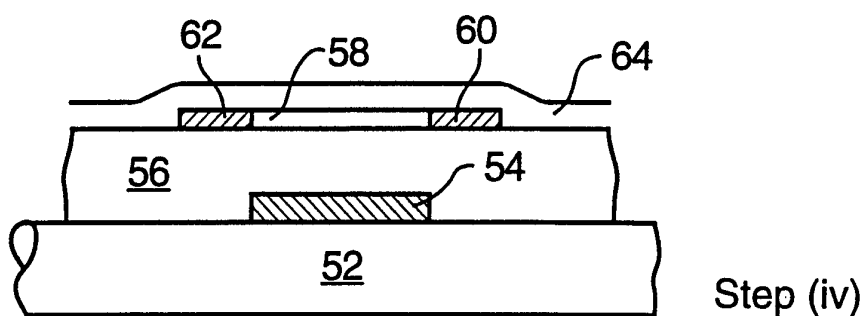


FIG.3e

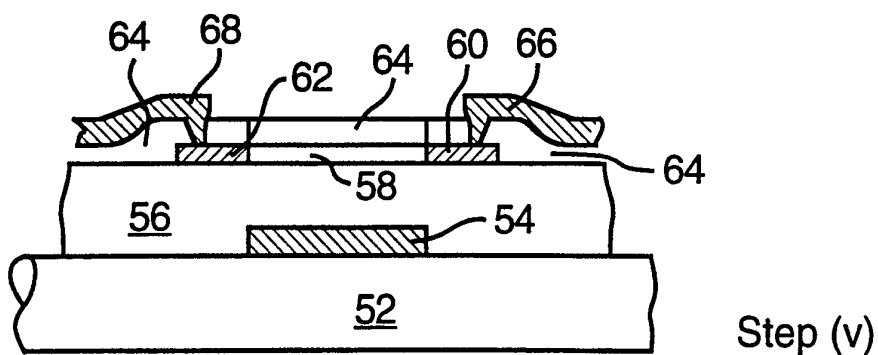


FIG.3f

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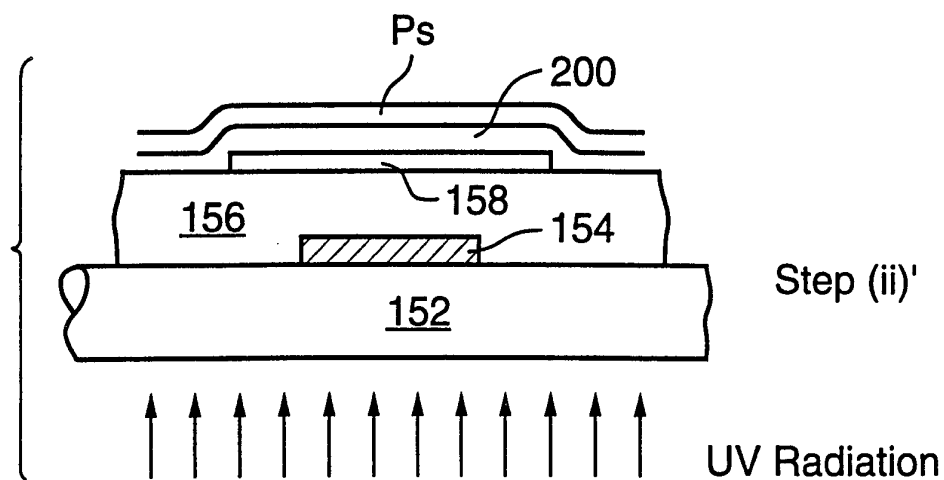


FIG.5a

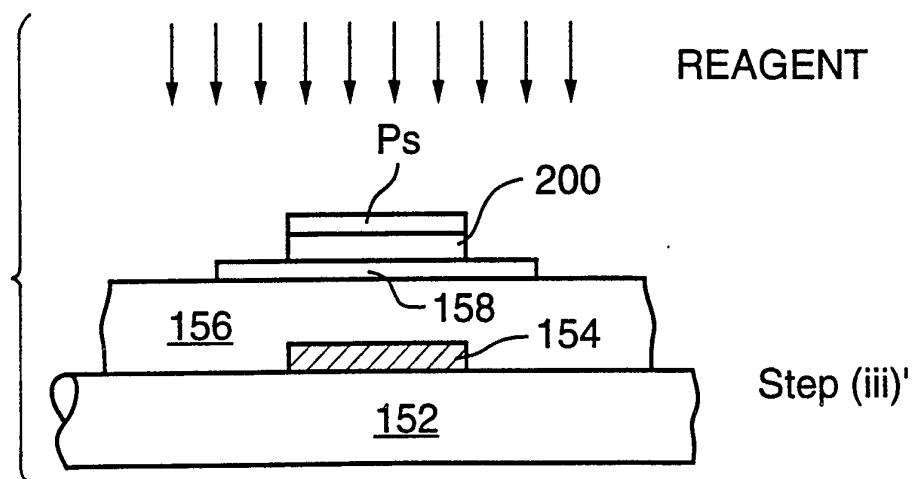


FIG.5b

INTERNATIONAL SEARCH REPORT

International Application No

PCT/CA 95/00455

A. CLASSIFICATION OF SUBJECT MATTER
 IPC 6 H01L21/22 H01L21/38 H01L21/34

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 6 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	JOURNAL OF VACUUM SCIENCE AND TECHNOLOGY: PART A, vol. 3, no. 1, January 1985 - February 1985, NEW YORK US, pages 203-205, XP002005475 G.D. DAVIS ET AL.: "Surface stoichiometry changes induced by the hydrogenation of Hg _{0.72} Cd _{0.28} Te" see the whole document ---	1,5
X	APPLIED PHYSICS LETTERS, vol. 42, no. 1, 1 January 1983, NEW YORK US, pages 50-52, XP002005476 R.R. DANIELS ET AL.: "Changes in the local chemical composition during the Hg _{1-x} CdTe-Al interface formation" see the whole document --- -/--	1,5

☒ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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Date of the actual completion of the international search

12 June 1996

Date of mailing of the international search report

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Name and mailing address of the ISA

European Patent Office, P.B. 5818 Patentlaan 2
 NL - 2280 HV Rijswijk
 Tel. (+31-70) 340-2040, Tx. 31 651 epo nl,
 Fax: (+31-70) 340-3016

Authorized officer

Visentin, A

INTERNATIONAL SEARCH REPORT

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	APPLIED SURFACE SCIENCE, vol. 84, no. 2, February 1995, AMSTERDAM, pages 187-192, XP000566688 D. BALLUTAUD ET AL.: "Reactivity of III-V and II-VI semiconductors toward hydrogen: surface modification and evolution in air" see the whole document ---	1,3-5
X	APPLIED PHYSICS LETTERS, vol. 62, no. 18, 3 May 1993, NEW YORK US, pages 2254-2255, XP000565185 C.DEBIEMME-CHOUVY ET AL.: "X-ray photoelectron spectroscopy study of GaAs surface exposed to a rf hydrogen plasma" see the whole document ---	1,3,5
A	GB,A,2 044 994 (PHILIPS ELECTRONIC AND ASSOCIATED INDUSTRIES LIMITED) 22 October 1980 see the whole document ---	6,10,12, 14,16,18
A	WO,A,94 13019 (LITTON SYSTEMS CANADA LIMITED) 9 June 1994 see page 7, line 36 - page 9, line 2; figure 4 ---	6,8,10, 12,14, 16,18
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A	EP,A,0 308 128 (NATIONAL RESEARCH DEVELOPMENT CORPORATION) 22 March 1989 ---	
A	US,A,4 040 073 (FANG-CHEN LUO) 2 August 1977 -----	

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International application No.

PCT/CA95/00455

Box I Observations where certain claims were found unsearchable (Continuation of item 1 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box II Observations where unity of invention is lacking (Continuation of item 2 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

SEE ANNEXED SHEET

1. ☒ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2. ☐ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:
4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

- ☐ The additional search fees were accompanied by the applicant's protest.
- ☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No

PCT/CA 95/00455

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
GB-A-2044994	22-10-80	NONE	
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