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INTEGRATING CIRCUIT

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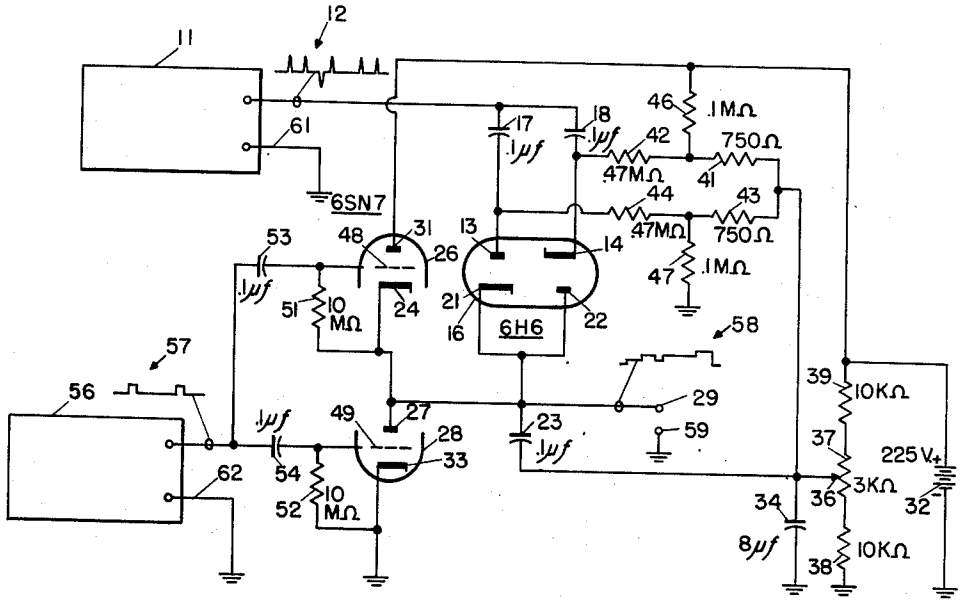


Fig. 1

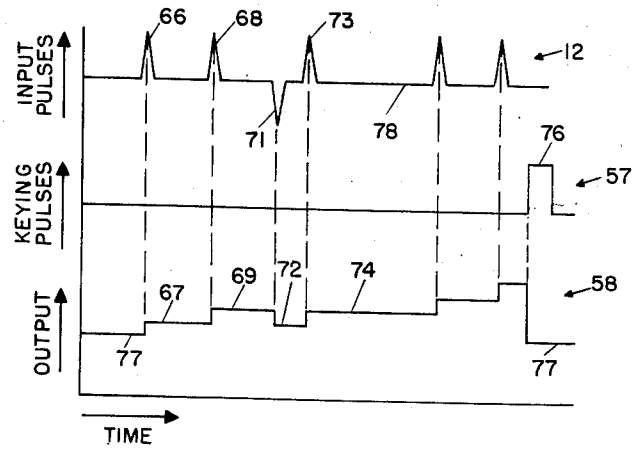


Fig. 2

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INTEGRATING CIRCUIT

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This invention relates to electric integrating circuits which function to produce an output signal, the magnitude of which is periodically controlled by a series of input pulses.

A use for integrating circuits is described in U. S. Patent No. 2,530,431, entitled "Color Device for Utilizing Control Signals." In that patent, pulses derived from a television picture tube at the end of horizontal sweep lines of the electron beam are fed into the integrating circuit. The output of the integrating circuit provides a responsive signal of longer duration than that of the input pulse, said duration corresponding to the time required for the next succeeding one or more horizontal sweep lines. Said output signal is utilized to affect the vertical deflection of the electron beam in order to secure accurate registration of the horizontal lines.

Objects of the present invention are to provide an integrating circuit which will accommodate both positively and negatively polarized input pulses, which will accurately maintain a constant level of output voltage after each input pulse and until the next input pulse occurs, which will quickly reset when desired, which has improved linearity of response, and which has improved response to signals of small magnitude.

Figure 1 is a partial block-and-schematic diagram of a circuit embodying the invention.

Figure 2 is a graph showing the time correlation of signals appearing in various portions of the circuit.

In Figure 1, a source 11 of input pulses 12 is connected to an anode 13 and a cathode 14 of a dual diode tube 16 through capacitors 17 and 18. The remaining cathode 21 and anode 22 of the tube 16 are connected together, to an integrating capacitor 23, to a cathode 24 of a first triode tube 26, to an anode 27 of a second triode tube 28, and to an output terminal 29. An anode 31 of the first triode 26 is connected to a source 32 of positive potential, of which the remaining terminal is grounded. A cathode 33 of the second triode 28 is grounded. The remaining terminal of the integrating capacitor 23 is connected to a filter capacitor 34 and to an adjustable contact 36 of a resistor 37. One end of the resistor 37 is connected through a resistor 38 to ground. The remaining end of the resistor 37 is connected through a resistor 39 to the source 32 of positive potential. The adjustable contact 36 is connected to the cathode 14 of the diode 16 through series resistors 41 and 42 and also to the anode 13 of diode 16 through series resistors 43 and 44. A resistor 46 is connected between the junction of

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said resistors 41 and 42 and the source 32. A resistor 47 is connected between the junction of said resistors 43 and 44 and ground. The control electrodes 48 and 49, of the triode tubes, 26 and 28, are connected respectively through resistors 51 and 52 to the cathodes 24 and 33, of said tubes and through capacitors 53 and 54 to a source 56 of keying signals 57. An output signal 58 occurs at the output terminal 29. The return path of the output signal 58 is provided through a grounded terminal 59. Return paths for the signal sources 11 and 56 are provided by grounded terminals 61 and 62.

In Figure 2 the input signal 12, the keying signal 57 and the output signal 58 are represented together on a time axis. When the circuit is operated, a first input pulse 66 causes an output signal 67 to occur. A second input pulse 68 causes an incremental increase 69 in the output signal. A third input pulse 71 of opposite polarity from the first two input pulses causes an incremental decrease 72 in the output signal. A further input pulse 73, having the same polarity as the first two pulses again causes an incremental increase 74 in the output signal 58, etc. When a keying pulse 76 occurs in the keying signal 57, the output signal is restored to its original steady magnitude 77. It is to be noted that the input pulses do not necessarily occur at regular intervals, as is indicated by the absence of a pulse at the time indicated by numeral 78 in the input signal 12. Furthermore, said input pulses need not be of equal magnitudes.

The circuit operates as follows: The movable connection 36 of the resistor 37 is adjusted to obtain a desired value of bias voltage. The network, comprising resistors 46, 41, 43 and 47, provides operating voltages in conjunction with resistors 42 and 44 for the input cathode 14 and anode 13 of the dual diode tube 16. Said resistors, comprising the bias voltage-producing network, have values to provide a bias on the anode 13 which is negative with respect to the bias on the cathode 14. The purpose of these bias voltages is to compensate for a "contact potential" voltage inherent in the diode tube 16, so that the integrating capacitor 23 will be equally affected by positive or negative input pulses. The compensation also improves linearity at low signal levels. The bottom terminus of the integrating capacitor 23, being connected to the junction of resistors 41 and 43, biases said terminus at a potential intermediate that of the anode 13 and cathode 14 of the dual diode tube 16. The exact value of this bias may be controlled by adjusting the connec-

tion 36 of the resistor 37. In the particular circuit shown the ohmic values of resistors 46 and 47, 41 and 43, 39 and 38, and 42 and 44, are respectively equal, thus providing a steady bias voltage on the two terminals of the integrating condenser 23 that is approximately one-half of the voltage of the potential source 32.

The pulses of the input signal 12, either positive or negative polarity, are passed through and rectified by the dual diode tube 16 and place increments of charge on the integrating capacitor 23. The capacitance of said condenser 23 is relatively large so that individual pulses of said signal 12 do not fully charge said condenser, but merely add or subtract increments of charge; i. e., if the integrator capacitor 23 is positively charged, then a positive pulse from the signal 12 will increase the positive charge by an incremental amount, and a negative pulse from the signal 12 will reduce said positive charge by an incremental amount. If the majority of said pulses have negative polarities, the charge on the capacitor 23 will be of negative polarity.

The triode tubes 26 and 28 function as discharge paths for the integrating capacitor 23. Said discharge devices 26 and 28 are normally non-conductive and the leakage path across the terminals of the integrating capacitor 23 is of a relatively high resistance so that the voltage charges on said capacitor will not leak off and will be affected only by incoming pulses from the input signal 12. When it is desired to completely discharge capacitor 23, a keying signal 57 is applied to the discharge devices 26 and 28. Each of said keyed discharge devices 26 and 28 then becomes effectively a short-circuit path connected in parallel with the integrating capacitor 23, but with opposite polarities. Therefore, if said capacitor 23 is positively charged, when the discharge tubes are keyed said charge will discharge through the tube 28; if the charge on said capacitor 23 is negative, said charge will discharge through the tube 26. The discharge paths include the resistors 39, 37, and 38. These resistors have relatively small values of resistance and do not materially affect or impede the discharge of said capacitor 23 through said discharge devices.

As referred to in the above-mentioned issued patent, when the integrating circuit is used in connection with registration of electron beam scanning lines in a television picture tube the keying pulses 57 may conveniently comprise vertical blanking or synchronizing pulses from a television signal, so that, at the end of each picture scanning field, the output signal 58 is reduced to zero value. Thus, each new picture field is commenced with a zero value of output corrective voltage 58; as each successive horizontal scanning line occurs, any deviation from the desired scanning path causes signal pulses 12 to be generated, from which the integrator circuit of the present invention derives a corrective output signal 58, the value of which changes incrementally with further deviations from required registry until the end of that particular field, whereupon said corrective signal 58 is restored to its initial zero value by the action of the discharge tubes 26 and 28.

Although the invention has been described particularly in connection with television apparatus, it may also be used for any application where its characteristics are desired.

What is claimed is:

1. An integrator circuit comprising a source of recurrent pulse signals, a first rectifier having an anode and a cathode, said anode being connected to said signal source, a first source of bias voltage connected to said anode, a second rectifier having an anode and a cathode, said cathode being connected to said signal source, a second source of bias voltage connected to said cathode of said second rectifier, a common connection between said cathode of said first rectifier and said anode of said second rectifier, a third source of bias voltage, a capacitor connected between said third source of bias voltage and said common connection, an output terminal connected to said common connection, a first and a second electron discharge device each having an anode, a cathode and a control electrode, a connection between said anode of said first electron discharge device and said output terminal, a connection between said cathode of said second discharge device and said output terminal, a connection between said cathode of said first electron discharge device and the terminal of said capacitor connected to said third source of bias voltage, a connection between said anode of said second electron discharge device and said terminal of said capacitor connected to said third source of bias voltage, and a source of keying signals connected to said control electrodes.

2. The apparatus of claim 1, in which said third source of bias voltage is variable.

3. The apparatus of claim 1, in which said third source of bias voltage has a value intermediate the values of said first and second sources of bias voltage.

4. The apparatus of claim 1, in which said source of pulse signals comprise pulses having differing polarities.

5. The apparatus of claim 1, in which said first source of bias voltage is negative with respect to said second source of bias voltage.

6. The apparatus of claim 1, in which said connections between said first source of bias voltage and said anode and between said second source of bias voltage and said cathode comprise impedances having values to provide time constants in conjunction with said capacitor that are greater than the time of recurrence of said pulse signals.

7. An integrator circuit comprising a source of pulses, a bi-directional conductive rectifier, and a capacitor connected in series, output terminals connected across said capacitor, a keyed bi-directional conductive discharge device connected across said capacitor, and a source of keying signals connected to said discharge device.

8. An integrator comprising a duo-diode having two each of anode and cathode electrodes, means for applying biasing voltages to one of the anodes and one of the cathodes of said duo-diode, a source of recurrent pulse signals connected to said last-named anode and cathode, an output circuit connected to the remaining anode and cathode electrodes of said duo-diode, a biased capacitor also connected to said remaining anode and cathode electrodes, means providing a normally non-conductive discharge path for said capacitor and a source of keying pulses for causing said last means to be conductive at pre-determined intervals.

9. An integrator comprising a source of recurrent positive and negative pulse signals, an integrating capacitor, means for bi-directionally rectifying said pulses and charging said capacitor with said rectified positive and negative

pulses, normally non-conductive means for discharging said capacitor, a source of keying pulses for selectively rendering said discharging means conductive, and an output circuit connected across said capacitor.

10. In the combination of claim 9, means for applying a biasing potential to said rectifying means and means for applying a biasing potential to said capacitor.

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